University of British Columbia
Electrical and Computer Engineering
Digital Design and Microcomputers
CPEN312

Lab 1 - Logic Gates Pandemic Edition

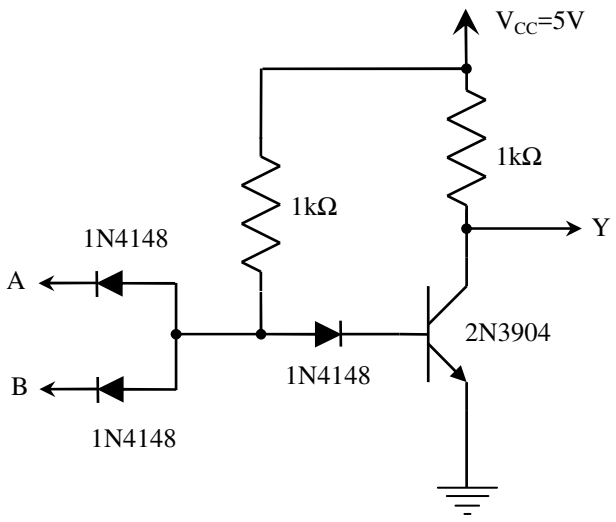
In this laboratory you will implement a simple digital system using logic gates built with discrete transistors.

Tools and Parts Needed

Due to the pandemic, this laboratory experiment will be completed using NI Multisim only. So we don't need any tools or parts.

Activities

1) The diagram below shows a basic DTL 2-input NAND gate. Test the gate using Multisim and verify that it operates as expected.



2) Add the last two digits of your student number. From the result pick the four digits from the table below.

Sum	Display
0	0523
1	2038
2	5261
3	4386
4	4826
5	1268
6	7480
7	3274
8	6321
9	1625

Sum	Display
10	3946
11	2386
12	7951
13	5379
14	2508
15	2159
16	3527
17	9630
18	8316

Design and simulate with Multisim a 2-bit decoder that displays the digits that correspond to your student number using a 7-segment common anode display as indicated in the table below. Remember that the LED segments are turned on with logic 0. Use ONLY DTL NAND logic gates (with any number of inputs; a 'NAND' gate with only one input is a valid option!).

Inputs		Digits (left to right)
B	**A**	
0	0	Digit 1
0	1	Digit 2
1	0	Digit 3
1	1	Digit 4

For example, if the last two digits of your student number add up to decimal 14, then you have to display "2508" with the 7-segment display. When the binary input is 00 display number 2, when the binary input is 01 display 5, when the binary input is 10 display 0, and when the binary input is 11 display 8.

To build your decoder you are limited to the following maximum number of components:

1. Up to 8 NPN transistors
2. Up to 24 diodes
3. Up to 16 resistors

The current limiting resistors for the 7-segment display are not included in the limitations above. Push buttons or switches used to control the inputs are also not included in the limitations above.

Upload to canvas you Multisim files (one for the DTL gate test, and one for the decoder) and a PDF with the complete design process of your decoder.