Computer Organization 2023 Lab 4

Finished part:

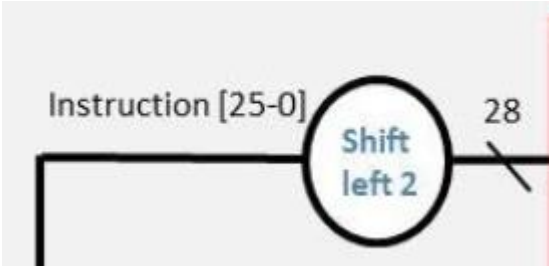
ALU.v / ALU_1bit.v / Full_adder.v: a set of module from Lab3 Template
Decoder.v / ALU_Ctrl.v
Shift_Left_Two_28.v: shift from 26 to 28
Shift_Left_Two_32.v: shift from 32 to 32
Simple_Single_CPU.v: summary all module together

Problems you met and solutions:

因為同時用了助教給的 template 和上次 Lab3 來做這次的作業，最常出現的問題就是變數一直打錯名字，debug 都要找好久，還有些會跟原本給的長度不一樣，還要找出來改。
設計圖比上次複雜很多，多拉了很多條線，打 Simple_Single_CPU 的時候更辛苦了，一堆 module 和線的名字很常搞混，很痛苦。

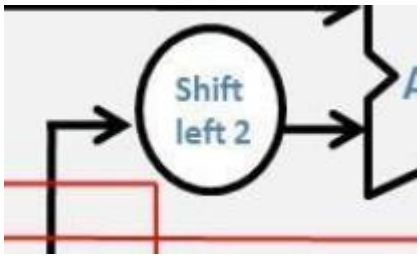
If you create additional module, please give a short explanation here:

Shift_Left_Two_28:



Input is instr. with 26 bits, so I shift 2 bits to left and add 2'b00 at the end.

Shift_Left_Two_32:



Input is address after sign extend, so it's 32 bits shift left to 32 bits.