Computer Organization

1. The input fields of each pipeline register:

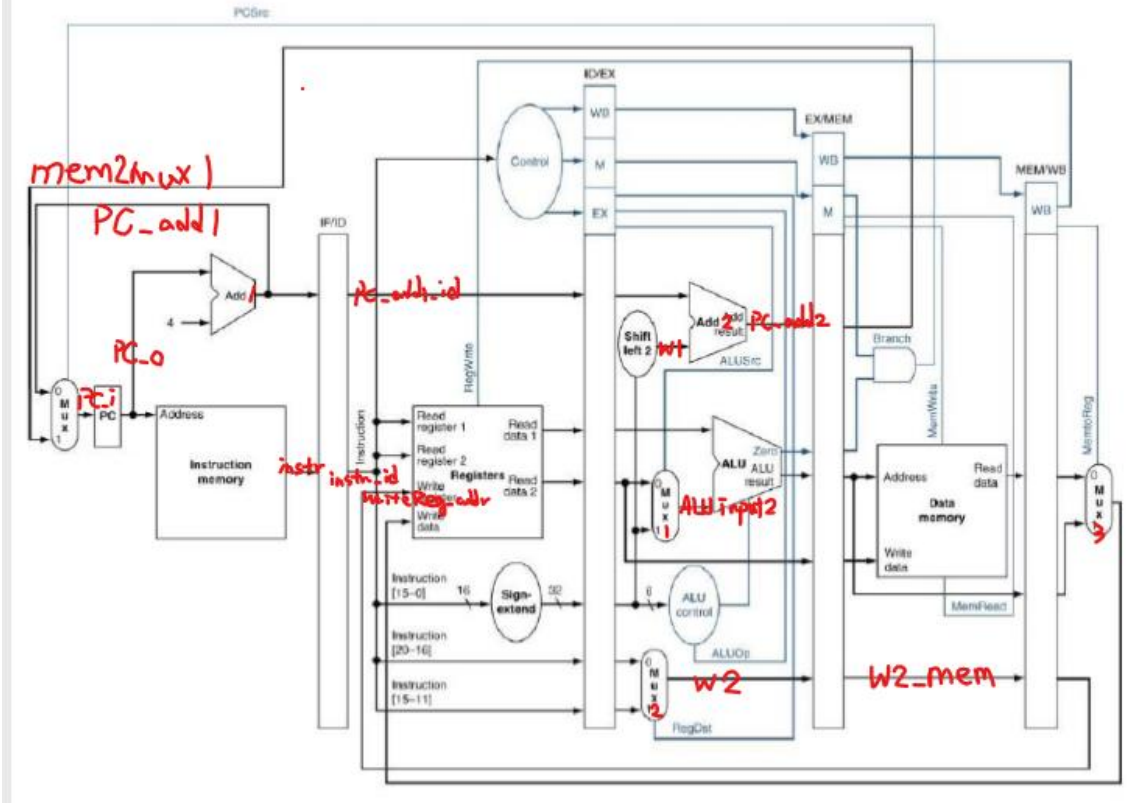
IF/ID: {instr, PC_add1}

ID/EX: {ReadData1, ReadData2, signextend, PC_add1_id, ALUOP, RegDst, MemtoReg, RegWrite, ALUSrc, Branch, MemWrite, MemRead, instr_id[20:0]}

EX/MEM: {PC_add2, ALUResult, ReadData2_ex, zero, w2, MemtoReg_ex, RegWrite_ex, Branch_ex, MemRead_ex, MemWrite_ex}

MEM/WB: {ALUResult_mem, DM_ReadData, w2_mem, MemtoReg_mem, RegWrite_mem}

A. Architecture Diagram



2. Compared with lab4, the extra modules:

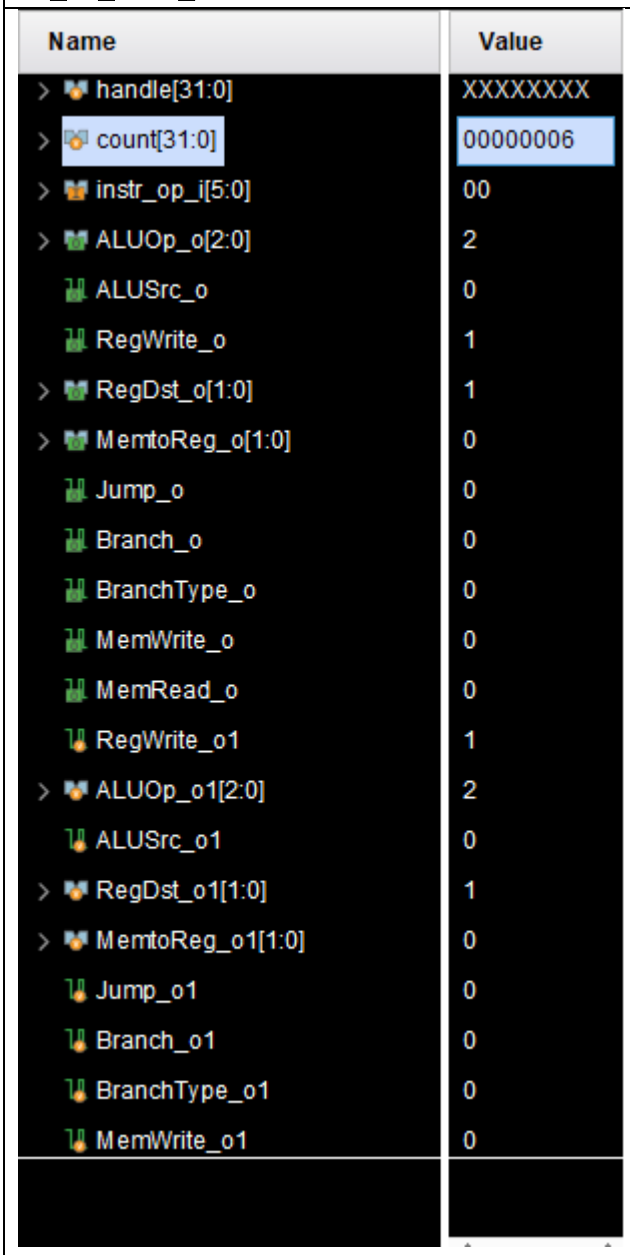
Pipe_Reg: the register for storing each stage

Pipe_CPU: combine all modules together

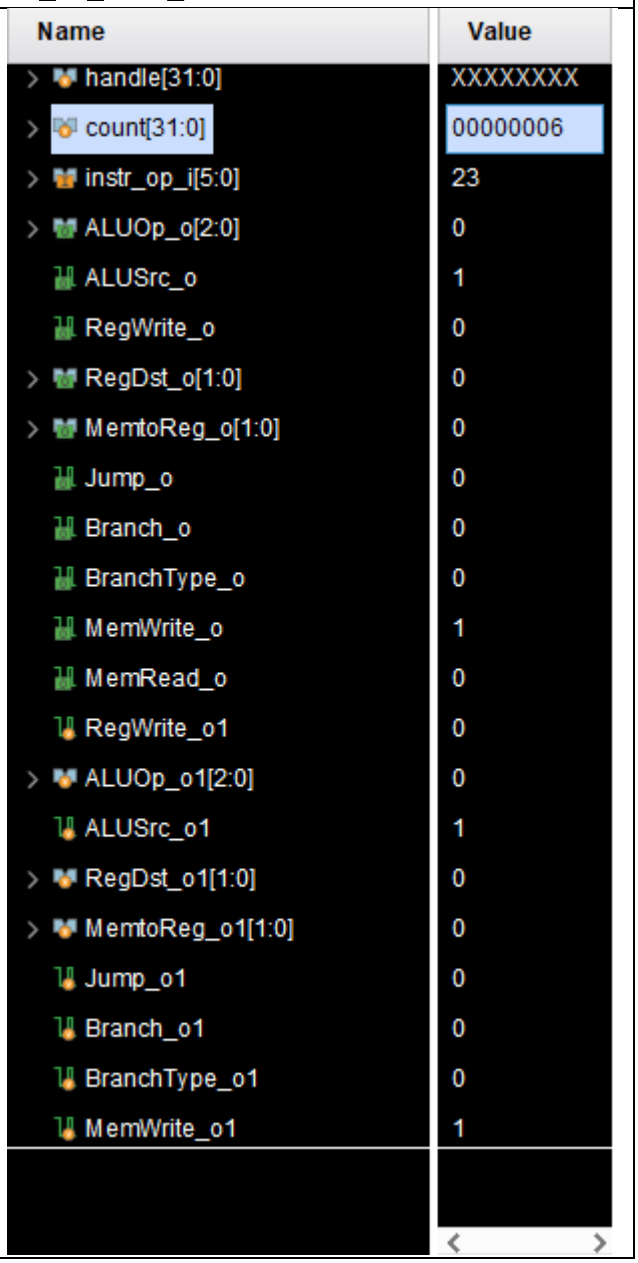
3. Explain your control signals in sixth cycle (both test patterns C0_P5_test_data1 and C0_P5_test_data2 are needed):

Picture:

CO_P5_test_data1



CO_P5_test_data2



4. Problems you met and solutions:

I should remember the wire name that I created. I have debugged for the names for several hours and Vivado is a terrible tool that it won't tell me where I made a mistake on a wrong name. Next time, I should write on VScode and simulate on Vivado.

5. Summary:

This lab is a nightmare for me. Although this is the last homework for this class, I feel that I ‘m unfamiliar with Vivado. But in the better part, the coding homeworks let me learn more about how a computer works and be more organized.