Chapter 6

Registers and Counters

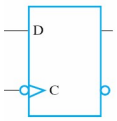
J.J. Shann

1

§6-2

1. Given the function table of a 2-bit shift register, derive the input equation for each D flip-flop of the register and draw the logic diagram of the register.

CLK	S_1	S_0	A_1^+	A_0^+	Register Operation
↓	0	0	A_1	A_0	**No Change**
↓	0	1	I_1	I_0	**Parallel load**
↓	1	0	A_0	SI	**Shift left**



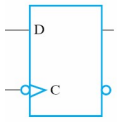
EX-2

2

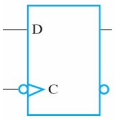
§6-3

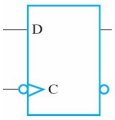
2. Given the counting sequence of a 2-bit binary counter, design a **ripple** counter using negative-edge triggered D flip-flops. Derive and draw your logic circuit.

Q_1	Q_0
1	1
1	0
0	1
0	0



<Ans>





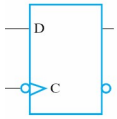
EX-3

3

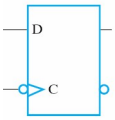
§6-4

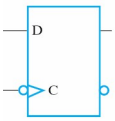
3. Given the counting sequence of a 2-bit binary counter, design a **synchronous** counter using D flip-flops. Derive the flip-flop input equations and draw the logic diagram of the circuit.

Q_1	Q_0
1	1
1	0
0	1
0	0



<Ans>





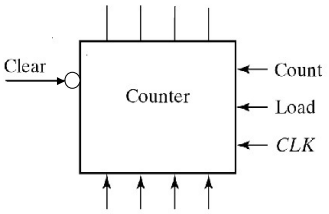
EX-4

4

§6-4

4. Given the function table and the block diagram of a 4-bit binary up-counter, implement a counter that follows the sequence 0101 through 1011 and then repeats using the *load* input.

Clear	CLK	Load	Count	Function
0	×	×	×	**Clear to 0**
1	↑	**1**	×	**Load inputs**
1	↑	**0**	**1**	**Count next binary state**
1	↑	**0**	**0**	**No change**



EX-5

5

Brief Answers of the Exercises

1. $D_1 = S_1'S_0'A_1 + S_1'S_0I_1 + S_1S_0'A_0$, $D_0 = S_1'S_0'A_0 + S_1'S_0I_0 + S_1S_0'SI$

2. FF_0 : C_0 : CLOCK, $D_0 = Q_0'$
   FF_1 : $C_1 : Q_0 \uparrow \Rightarrow Q_0' \downarrow$, $D_1 = Q_1'$

3. $D_1 = Q_1^+ = Q_1 \oplus Q_0'$, $D_0 = Q_0^+ = Q_0'$

EX-6

6