Chapter 5

Synchronous Sequential Logic

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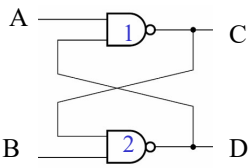
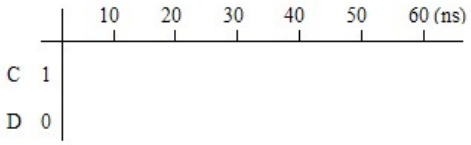
1

§5-3

1. Given two cross-couple NAND gates, assume that the propagation delay (*PD*) of each gate is 10 ns. Draw the timing waveform for outputs C and D, and estimate the time required for the outputs to become stable in the following conditions:





(a) A = 1, B = 0, C = 1, and D = 0

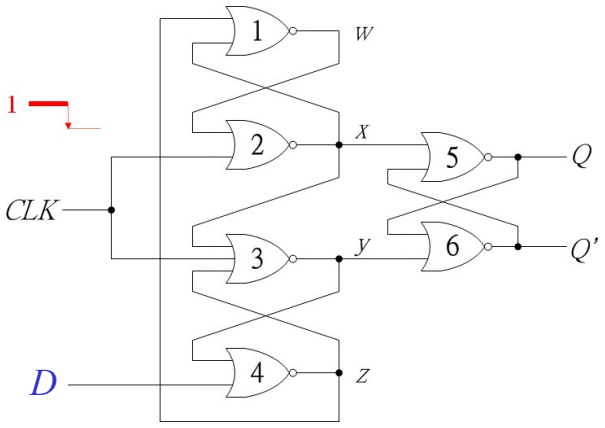
(b) i. A = 0, B = 1, C = 0, and D = 1
ii. A = 0, B = 0, C = 0, and D = 1
iii. A = 1, B = 1, C = 1, and D = 1

EX-2

2

§5-4

2. Given the following logic diagram, explain why it is a negative-edge-triggered D flip-flop.

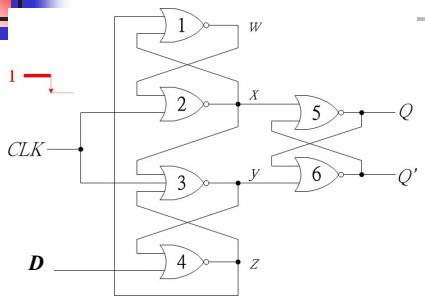


EX-3

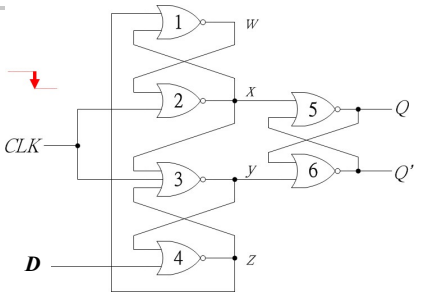
3

<Ans>

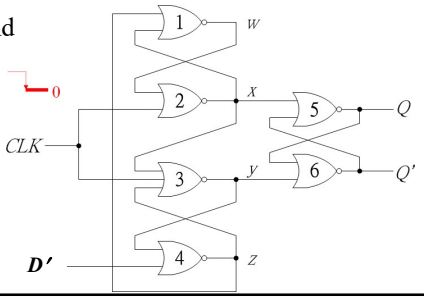
i. When clock is HIGH:



ii. When clock goes HIGH-to-LOW:



iii. When clock is LOW and D is changed to D' :



EX-4

4

§5-5

3. A synchronous sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following equations:

$$D_A = \overline{X}A + XY$$
$$D_B = \overline{X}A + XB$$
$$Z = A\overline{B}$$

(a) Draw the logic diagram of the circuit.
(b) Derive the next state equations.
(c) Complete the transition/state table of the circuit.
(d) Draw the state diagram.
(e) Starting from state 00 in the state diagram, determine the state transitions and output sequence that will be generated when an input sequence of XY = 01, 11, 11, 00, 10, 01, 11, 10 is applied.

EX-5

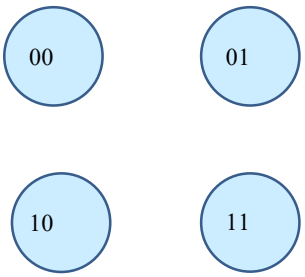
5

<Ans>

Transition/state table:

Present state		Input		Next state		Output
A	B	X	Y	A+	B+	Z
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

State diagram:



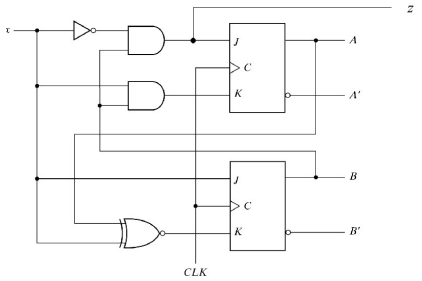
Cycle	0	1	2	3	4	5	6	7	8
xy	01	11	11	00	10	01	11	10	
AB	00								
Z									

EX-6

6

§5-5

4. Analyze the following synchronous sequential circuit, which has one input x and one output z, step by step:



(a) Derive the memory input equations and the output equation.
(b) Derive the next state equations.
(c) Complete the transition/state table of the circuit.
(d) Draw the state diagram.

EX-7

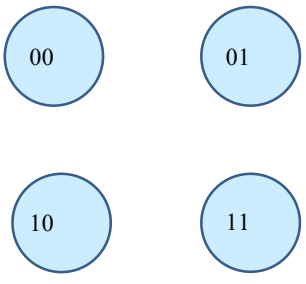
7

<Ans>

Transition/state table:

Present state		Input	Next state		Output
A	B	X	A+	B+	Z
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

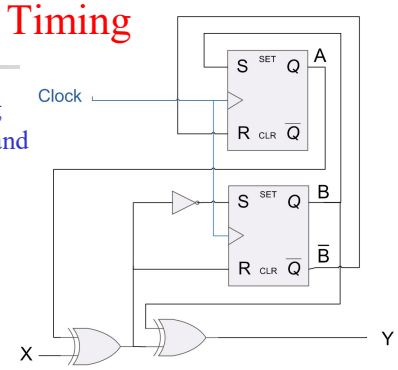
State diagram:



EX-8

8

補充資料：Sync Seq Ckt Timing



5. A sequential circuit is given in the following figure. The timing parameters for the gates and flip-flops are as follows:

   Inverter: $t_{pd} = 0.5$ ns

   XOR Gate: $t_{pd} = 2.0$ ns

   Flip-flop: $t_{pd} = 2.0$ ns,

   $t_s = 1.0$ ns, and

   $t_h = 0.25$ ns

   (a) Find the longest path delay from an external circuit input passing through gates only to an external circuit output.

   (b) Find the longest path delay in the circuit from an external input to positive clock edge.

   (c) Find the longest path delay from positive clock edge to output.

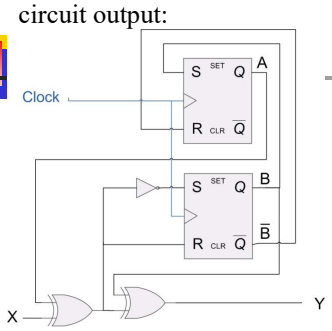
   (d) Find the longest path delay from positive clock edge to positive clock edge.

   (e) Determine the maximum frequency of operation of the circuit in megahertz (MHz).

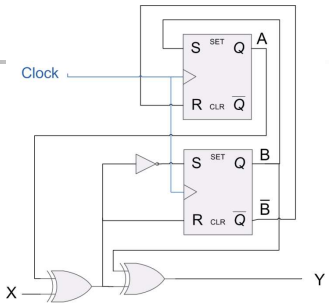
EX-9

9

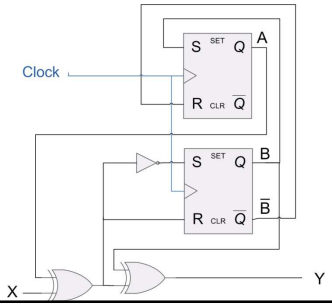
(a) external circuit input → external circuit output:



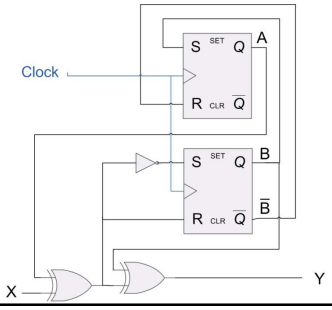
(b) external input → positive clock edge:



(c) positive clock edge → output:



(d) positive clock edge → positive clock edge:



EX-10

10

§5-7 & 5-8

6. Design a Moore-type recognizer which has one input (X) and one output (Z). The output is asserted (= 1) whenever the input sequence …010… has been observed, as long as the sequence …100… has not been seen since the last reset.

   (a) Draw the state diagram of the recognizer.

   (b) Starting from the initial state of your design, determine the state transitions and output sequence that will be generated when an input sequence of 00111010100101 is applied.

<Ans>

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Input	0	0	1	1	1	0	1	0	1	0	0	1	0	1	
State	A														
Output															

11

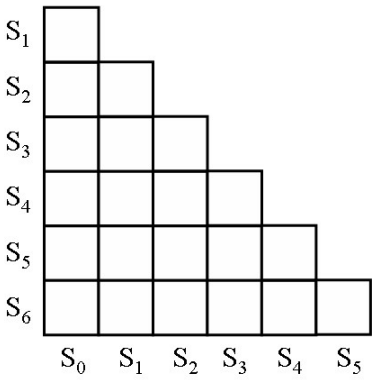
補充資料：State Reduction

7. Given the following state table,

   (a) Use the row matching method to find the equivalent states.

   (b) Use the implication chart method to find the equivalent states. Tabulate the reduced state table.

Present state	Next state		Output	
	x = 0	x = 1	x = 0	x = 1
S_0	S_1	S_4	0	0
S_1	S_1	S_2	0	0
S_2	S_1	S_6	0	0
S_3	S_1	S_3	0	0
S_4	S_5	S_4	0	0
S_5	S_5	S_2	0	0
S_6	S_5	S_3	0	1



EX-12

12

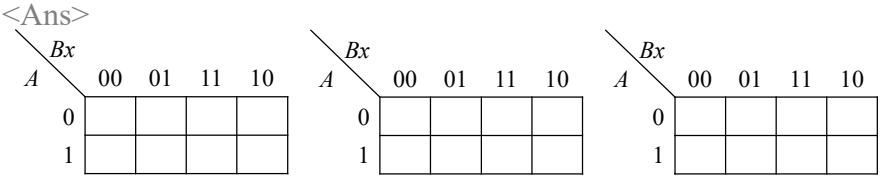
§5-7 & 5-8

9. Given the following state (transition) table, treat the unused state as don't-care conditions.

   Implement the circuit with **D** flip-flops. Derive the minimized Boolean equations in sum-of-products form for the flip-flop inputs and the output Z .

Present state		Input	Next state		Output
Q_A	Q_B	X	Q_A+	Q_B+	Z
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	0	1	1
1	0	1	0	1	0

<Ans>



EX-14

14

§5-7 & 5-8

10. Given the following state (transition) table, treat the unused state as don't-care conditions. .

    Implement the circuit with **JK** flip-flops. Complete the excitation table shown above and derive the minimized Boolean equations in sum-of-products form for the flip-flop inputs .

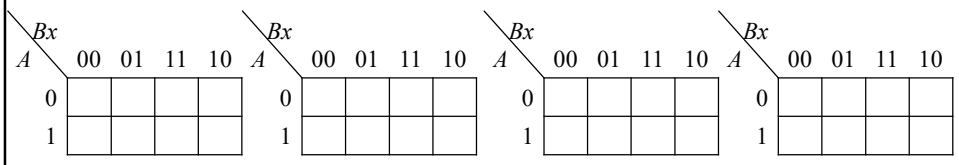
Present state		Input	Next state		Output	Excitation Table Flip-Flop Inputs			
Q_A	Q_B	X	Q_A+	Q_B+	Z	J_A	K_A	J_B	K_B
0	0	0	0	0	0				
0	0	1	0	1	0				
0	1	0	1	0	0				
0	1	1	1	0	1				
1	0	0	0	1	1				
1	0	1	0	1	0				

EX-15

15

<Ans>

Present state		Input	Next state		Output	Excitation Table Flip-Flop Inputs			
Q_A	Q_B	X	Q_A+	Q_B+	Z	J_A	K_A	J_B	K_B
0	0	0	0	0	0				
0	0	1	0	1	0				
0	1	0	1	0	0				
0	1	1	1	0	1				
1	0	0	0	1	1				
1	0	1	0	1	0				



EX-16

16

補充資料：Word Problems

* Give an example of synchronous sequential circuits by yourself. Describe the problem, define the input variables, output variables, and states, and draw the state diagram of the problem.

EX-17

17

Brief Answers of the Exercises

1. (a) C: 1→1→0→0→… , D: 0→1→1→1→… ; 20 ns
   (b) i. C: 0→1→1→1→… , D: 1→1→0→0→… ; 20 ns
   ii. C: 0→1→1→… , D: 1→1→1→… ; 10 ns
   iii. C: 1→0→1→0→… , D: 1→0→1→0→… ; isolated

3. (b) $A(t+1) = x'A + xy$, $B(t+1) = x'A + xB$
   (e) AB: 00 00 10 10 11 01 00 10 00
   Z: 0 0 1 1 0 0 0 1 0

4. (a) $J_A = Bx'$, $K_A = Bx$, $J_B = x$, $K_B = Ax + A'x'$, $Z = Bx'$
   (b) $A^+ = Bx' + AB'$, $B^+ = A'x + B'x + ABx'$

5. (a) 4 ns (b) 3.5 ns (c) 6 ns (d) 5.5 ns (e) 167 MHz

6. (a) 7 states

7. (a) None.
   (b) (0, 3, 4); (1, 5)

9. $D_A = B$, $D_B = A + B'x$, $Z = Bx + Ax'$

10. $J_A = B$, $K_A = 1$, $J_B = A + x$, $K_B = 1$

EX-18