Lab 1：簡易組合電路之 HDL 模組撰寫與測試

(Writing and Testing HDL Modules of Simple Combinational Circuits)

1. 目標 (Goal)

在這次 Lab 中，我們希望同學們可以熟悉 Verilog 程式碼的撰寫與模擬。同學需模擬提供之附檔 *Simple_Circuit.v*、*Simple_Circuit_prop_delay.v*、及 *t_Simple_Circuit.v*，並依指示修改電路模組、觀察結果波形圖。
此外，將提供同學一份組合電路的邏輯電路圖，請以 gate-level modeling、dataflow modeling、以及訂定 user-defined primitive 等不同方式撰寫其 HDL 電路模組，並撰寫其測試模組。分別模擬後，繳交模組檔案及波形圖。

The main purpose of this Lab Unit is familiar with Verilog coding and simulation. Students need to simulate the attached file *Simple_Circuit.v*, *Simple_Circuit_prop_delay.v*, and *t_Simple_Circuit.v*, and modify the circuit module according to the experiment description and observe the waveform of simulation result.
Moreover, we will provide a combinational circuit diagram. Please writes its HDL circuit modules by *gate-level modeling*, *dataflow modeling*, and *user-defined primitive*, and write the test benches for these circuit modules. After simulation, upload the files of the modules and the waveforms of the simulation results.

2. 撰寫 HDL 電路模組與測試模組（Design of the HDL Circuit Modules and Testbench)

A. 模擬並修改附檔 *Simple_Circuit_prop_delay.v*
(Simulating and modifying the attached file ***Simple_Circuit_prop_delay.v***)

(a) 模擬附檔 *Simple_Circuit.v*、*Simple_Circuit_prop_delay.v*、及 *t_Simple_Circuit.v*，觀察兩個電路模組之結果波形圖的差異。
Simulate the attached files *Simple_Circuit.v*, *Simple_Circuit_prop_delay.v*, and *t_Simple_Circuit.v*, and observe the difference of waveform of these two circuit modules.

(b) 請將 *Simple_Circuit_prop_delay.v* 中，**and** 與 **or** 兩行敘述(statements)互換，存檔並重新編譯後，模擬之，觀察結果波形圖。
Please swap the two statements of **and** and **or** in *Simple_Circuit_prop_delay.v,* save and compile the module again, and observe the waveform of its simulation result.

B. 撰寫組合電路之 HDL 電路設計模組(design module)與測試模組(testbench) (Writing the HDL design module and testbench of a combinational circuit)

下圖為一組合電路之邏輯電路圖，請以不同方式撰寫其 Verilog 模組，無需考慮 propagation delay，其 **Verilog module 的 port list 順序請務必訂為 F, A, B, C, D**。

The logic diagram of a combinational circuit is shown in the following figure. Please write the Verilog module in different way without considering the propagation delay. The order of the port list of this Verilog module must be F, A, B, C, D.

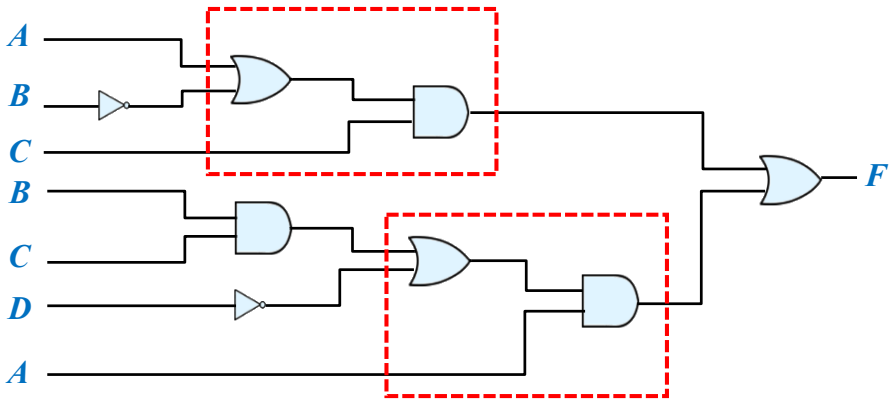

圖 1：一組合電路之邏輯電路圖

Figure 1: The logic diagram of a combinational circuit.

(a) 請以 **gate-level modeling** 方式撰寫其 Verilog 電路模組(模組命名為 *Lab1_gatelevel*，檔案命名為 *Lab1_gatelevel.v*)。

Please write the Verilog circuit module in gate-level modeling. The circuit module should be named as *Lab1_gatelevel*, and its file should be named as *Lab1_gatelevel.v*.

(b) 請以 **dataflow modeling** 方式(**assign** statements)撰寫其 HDL 電路模組(模組命名為 *Lab1_ dataflow*，檔案命名為 *Lab1_dataflow.v*)。

Please write the Verilog circuit module in dataflow modeling. The circuit module should be named as *Lab1_ dataflow*, and its file should be named as *Lab1_dataflow.v*.

(c) 請將圖 1 中虛線框內之電路撰寫成 **user-defined primitive (UDP)** (模組命名為 *Lab1_UDP*，檔案命名為 *Lab1_UDP.v*)，而後利用此 UDP 設計此電路之 HDL 模組(模組命名為 *Lab1_gatelevel_UDP*，檔案命名為 *Lab1_gatelevel_UDP.v*)。

Please design the circuit of the dashed box in Figure 1 as a user-defined primitive (UDP). Name the UDP as *Lab1_UDP* and its file as *Lab1_UDP.v* . And then, use this UDP to design the Verilog circuit module. The circuit module should be named as *Lab1_gatelevel_UDP*, and its file should be named as *Lab1_gatelevel_UDP.v*.

(d) 請撰寫一個測試模組(模組命名為 t_Lab1，檔案命名為 t_Lab1.v)來測試上述三個電路模組的所有輸入組合。存檔、編譯後，模擬之，並觀察其結果波形圖。

Write the testbench for the above three circuit modules to test all the input combinations. The testbench should be named as *t_Lab1,* and its file should be named as *t_Lab1.v* . After saving the modules, compile and simulate the modules and observe the waveforms of the simulation results.

3. 注意事項（Notes）

A. **請用 Icarus Verilog 做為編譯器，以 vvp 執行，並以 GTKWave 觀察波形圖。**
Please compile your Verilog code by **Icarus Verilog**, execute the compiled code by vvp, and then observe the waveform by GTKWave.

B. **請務必使用附件提供的檔案來完成作業 2.A** (Please use the attached file listed below for 2.A)：
Simple_Circuit.v 、*Simple_Circuit_prop_delay.v* 、*t_Simple_Circuit.v*

C. **請務必依照 2.B (a)~(d) 中之規定命名模組及檔案。**
Be sure to name the modules and files as described in 2. B (a)~(d).

4. 作業及 HDL 模組繳交（Hand in）

A. **作業繳交: pdf 檔，命名為 Lab1_學號**

(1) 2A(a)之模擬結果波形圖(包含輸出 D 與 E，以及 $w1$)，並說明 *Simple_Circuit.v* 與 *Simple_Circuit_prop_delay.v* 之波形圖間的差異。(10%)

(2) 2A(b)之模擬結果波形圖，並說明與 2A(a)之波形圖是否有差異及原因。(10%)

(3) 2B(d)之電路模擬結果波形圖，並說明三個電路模組是否正確。(60%)

(4) 請判斷圖 1 之電路是否為該函式 gate input counts 最少之實作? 若是，請說明之；若否，則請推導出此函式 gate input count 最少的布林代數式，寫出 gate input count 數值，並以 AND、OR、NOT 邏輯閘畫出其電路圖。(10%)

(5) 心得與感想、及遭遇到的問題或困難。(10%)

Hand in a pdf file, named Lab1_StudentID , including the following items:

(1) Give the waveform of the simulation result of 2A(a), including outputs *D* and *E* and internal connection *w*1, and explain the difference between the waveform of *Simple_Circuit.v* and that of *Simple_Circuit_prop_delay.v.* (10%)

(2) Give the waveform of the simulation result of 2A(b), and explain whether there is any difference between the waveforms of 2A(a) and 2A(b). (10%)

(3) Give the waveform of the simulation result in 2B(d), and explain whether the three modules are correct. (60%)

(4) Does the design of Figure 1 have the least gate input count for the function of the circuit? If yes, explain your reason; if not, derive the Boolean expression with least gate input count for the function, write the gate input count, and draw the logic diagram of the circuit by using AND, OR, and NOT gates. (10%)

(5) Describe what you have learned from this lab unit and discuss the problems or difficulties encountered in this lab. (10%)

B. Verilog modules 檔案繳交(Hand in the following Verilog modules)：

Lab1_gatelevel.v、Lab1_dataflow.v、Lab1_UDP.v、Lab1_gatelevel_UDP.v、t_Lab1.v

C. 助教會使用不同的測試模組來驗證同學的電路模組正確性。

After you hand in your code, TA will use similar TestBench modules with different test data to verify the correctness of your design of the Verilog circuit modules.

5. DEADLINE

A. 本實驗單元為一人一組，請將實驗報告及相關 Verilog 檔案上傳至 e3 平台。

This lab unit is one student per group. Please upload your Lab Report (pdf file) and the corresponding HDL code (.v files) onto e-Campus platform.

B. 請請將上述作業報告及 Verilog 電路模組與測試模組檔案(.v)全部壓縮成一個 zip 檔 (禁止上傳 rar 檔或是其他檔案格式)，並以「Lab1_學號」的方式命名，如 ： 「Lab1_0816000」。壓縮檔案時，請選取好要求繳交的檔案執行壓縮，不要對整個資料夾壓縮。

Please compress the pdf file of lab report and the Verilog circuit modules and testbench described above all into one zip file (rar file or other format is not accepted), and name the zip file as "Lab1_StudentID" , for example, "Lab3_0816000". When compressing files, please select the requested files for compression, and do not compress the entire directory."

C. 繳交截止日期為 2022/4/21 (四) 23:59。不接受逾期繳交。

The deadline is **2022/4/21 (Thursday) 23:59. No late hand-in is allowed.**

D. **禁止抄襲，違者(抄襲者與被抄襲者)以 0 分計算。**

Any assignment work by fraud will get a zero point.