DIGITAL DESIGN

ASSIGNMENT 2

Deadline: *12 noon,* Wednesday *31 October 2018*

Lab sessions&Location:

Lychee Garden 6,Room 408 (Wednesday 10:20am-12:10 pm)

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PART 1: DIGITAL DESIGN THEORY

Provide answers to the following questions:

1. Convert the following binary numbers to hexadecimal and to decimal: (a) 1.10010, (b) 1100.010. Explain why the decimal answer in (b) is 8 times that in (a).
2. Do the following conversion problems: (a) Convert decimal 35.125 to binary. (b) Calculate the binary equivalent of 1/3 out to eight places. Then convert from binary to decimal. How close is the result to 1/3? (c) Convert the binary result in (b) into hexadecimal. Then convert the result to decimal. Is the answer the same?
3. Obtain the 1's and 2's complements of the following binary numbers: (a) 11110000 (b) 00000000 (c) 11011000 (d) 01010101 (e) 10000000 (f) 11111111.
4. Represent the decimal number 6,514 in (a) BCD, (b) excess-3 code, (c) 2421 code, and (d) a 6311 code.
5. We can perform logical operations on strings of bits by considering each pair of corresponding bits separately (called bitwise operation). Given two eight-bit strings A = 10110001 and B = 00001110, evaluate the eight-bit result after the following logical operations: (a) AND (b) OR (c)* XOR (d)* NOT A (e) NOT B (f) NAND (g) NOR
6. Simplify the following Boolean expressions to a minimum or the indicated number of literals:
    a. (a + b + c')(a'b'+ c)
    b. a'b'c + ab'c + abc + a'bc
    c. (a + c)(a'+ b + c)(a'+ b'+ c)
    d. A'BD' + ABC'D'+ ABCD' to two literals
7. Given the Boolean functions F1 and F2 , show that
    a. The Boolean function E = F1 + F2 contains the sum of the miniterms of F1 and F2

b. The Boolean function G = F1 · F2 contains only the minterms that are common to F1 and F2 .

8. Convert each of the following to the other canonical form:
   a. F(x, y, z) = ∑(1, 3, 5, 7)
   b. F(A, B, C, D) = ∏(3, 5, 8, 11, 13, 15)
9. Write the following Boolean expressions in:
   a. (b + d)(a'+ b'+ c)(a + c) sum of products form
   b. a'b + a'c'+ bc product of sums form
10. Determine whether the following Boolean equation is true or false.
   a. y'z' + yz' + x'z = x'+ xz
   b. x'y'+ xz'+ yz = y'z' + xy + x'z
11. Simplify the following Boolean functions, using Karnaugh maps:
   a. F (w, x, y, z) = ∑(11, 12, 13, 14, 15)
   b. F (w, x, y, z) = ∑(8, 10, 12, 13, 14)
12. Simplify the following Boolean functions and expressions, using four-variable maps:
   a. F (A, B, C, D) = ∑ (2, 3, 6, 7, 12, 13, 14)
   b. F (w, x, y, z) = ∑ (1, 3, 4, 5, 6, 7, 9, 11, 13, 15)
   c. A'BCD + ABC + CD + B'D
   d. A'B'C'D' + BC'D + A'C'D + A'BCD + ACD
13. Simplify the following functions, and implement them with two-level NAND gate circuits:
   a. F(A, B, C, D) = AD + BC'D+ ABC + A'BC'D
   b. F(A, B, C, D) = A'B'C'D + CD' + AC'D
   c. F(A, B, C, D)= (A'+ C'+ D')(A'+ C')(C'+ D')
   d. F(A, B, C, D) = A'+ AB + B'C + ACD

PART 2: DIGITAL DESIGN LAB

INTRODUCTION

In the previous lab, you have learned how to use the practice suit (vivado and minisystem development board) to do the design, do the function simulation, generate

bitstream, program FPGA chip and test. You have practiced in 3 different ways (dataflow, block design and structured design) on Demorgan Theorem proving.

In this lab, you are required to create an IP and doing the design using primitive and UDP respectively, simplify the testbench using loop of Verilog, observe the state of variable using system task of Verilog. Please use the vivado and minisys development board to do the design, simulation and test.

PREAMBLE

Before working on the coursework itself, you should master the following material.

- 'Ch2-Boolean Algrebra-ICs-SUSTC.ppt' and CH3-Minimisation-SUSTC ' in Sakai site.
- 'Digital design lab3' and 'Digital design lab4' in Sakai site.
- Verilog :
  - http://www.verilog.com/

EXERCISE SPECIFICATION

Task 1:

Design a NAND gate using data flow style, make it customizable. Package it to an IP Core named as SUSUC_CSE_nandgate.

1. Do the design using data flow style, this NAND gate has two parameters: the 1st one indicates the size of input port (range from 2 to 4, default value is 2); the 2nd one indicates the width of the input ports and output ports (range from 1 to 8 bits, default value is 1).

2. Make the testbench of an instance (with 2bits width and 3 input ports available) on this NAND gate, do the simulation to verify its function.

3. package it as an IP Core. While packaging, make it a customizable IP core.

Task 2:

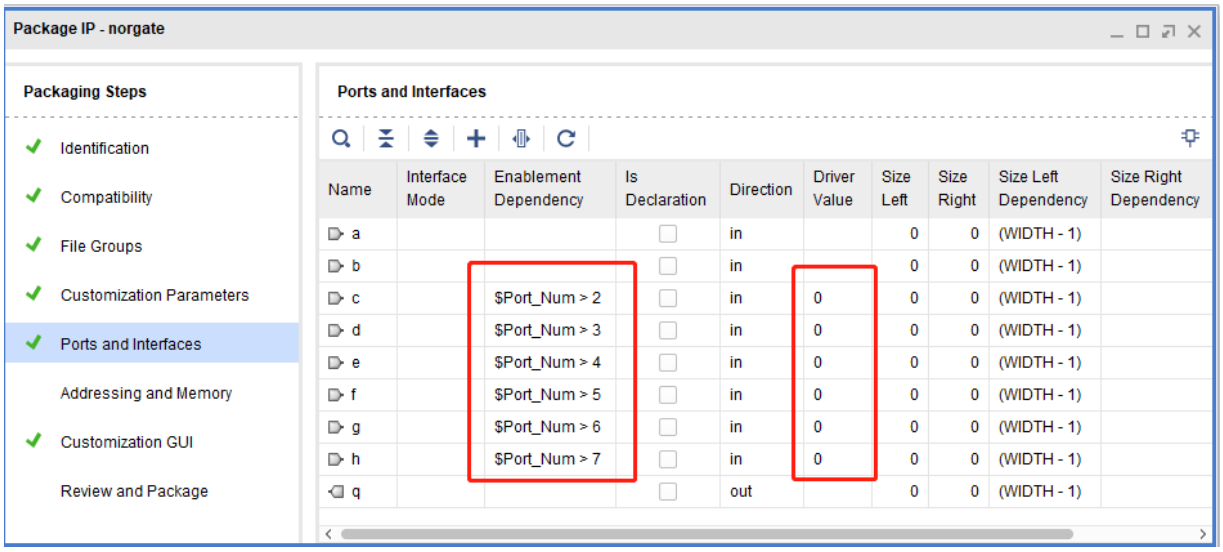
Do the design on the following logic function: F(x,y,p) = x⊕y⊕p (⊕ is an XOR operator), using UDP and primitive gate respectively. Observe its Schematic in different views. Verify its function and test on the minisys development board

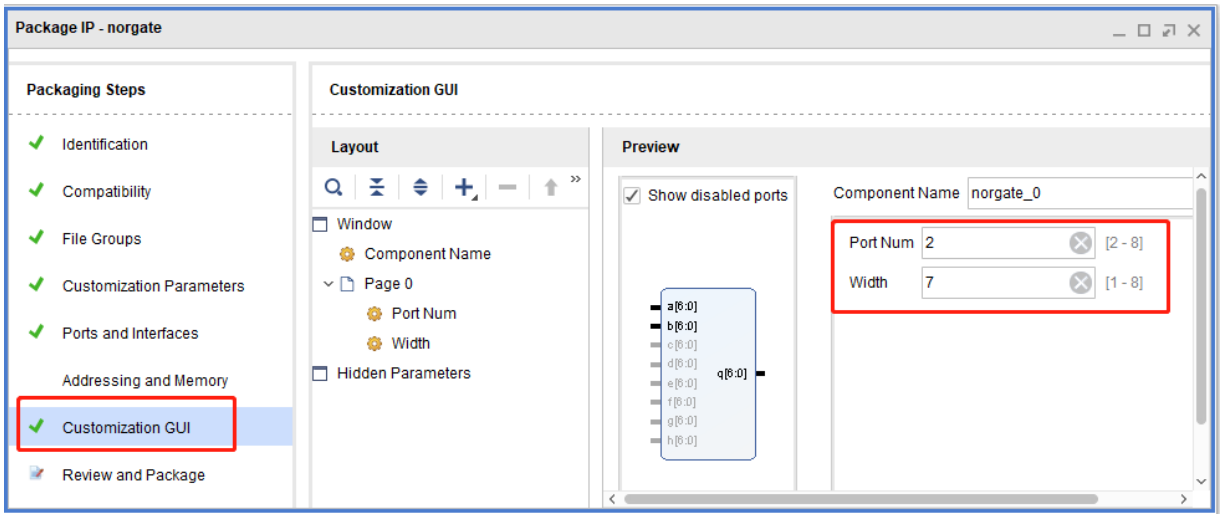
1. Using the UDP to realize circuit design
2. Using data flow to realize circuit design in sop and pos style respectively
3. Write the testbench in Verilog to verify the function of design (using any style of loop is ok)
4. Do the synthesis to check if the UDP or module can be synthesized or not
5. Check the schematic of the synthesis and the RTL analysis respectively to see the difference
6. Generate the bitstream and program the device to test the function

TIPS:

1. screenshot on every sub-task result which is requested, record it in your report.

Sample screenshot





2. ***Regarding the testing scenes, please give a description for the input and output respectively, such as which part is the MSB. Otherwise you might suffer the deduction on marks***
3. ***Please transform your report from word to PDF, and upload the PDF file to sakai.***

ASSESSEMENT

The full mark for this this exercise is 200, distributed as follows:

Theory: 30%

Question 1	4
Question 2	4
Question 3	4
Question 4	4
Question 5	4
Question 5	4
Question 6	6
Question 7	5
Question 8	5
Question 9	6

Question 10	6
Question 11	4
Question 12	4
Total	60 marks

Lab: 70%

Task 1: design with parameter	10
Task 1: instantiate the module in testbench with desired parameter	5
Task 1: using loop to set the states of variable binding with input ports of module in testbench	5
Task 1: set identification while do the IP packaging	5
Task 1: set ports and interface while do the IP packaging	10
Task 1: customization the IP while do the IP packaging	5
Task 2: using UDP to realization the design on logic function	10
Task 2: using primitive gate to realize the sop of the logic function	10
Task 2: using primitive gate to realize the pos of the logic function	10
Task 2: open elaborated design to check the schematic view of the design, open synthesized design to check the schematic view of the design tell the difference between them.	5+5+10
Task 2: instantiate the design in the testbench, binding its ports with variables, using loop to	5+5

set the states of the variables Using system task such as display to observe the inputs and outputs	
Task 2: set the constraints file	10
Task 2: generate the bitstream file, program the device and test the design on the minisys develop board, at least 3 testing scenes	10+10
Problem and solutions	10
Total	140marks

Please use the same template of Digital design assignment 1.