DIGITAL DESIGN

ASSIGNMENT 3

Deadline: *12 noon, Saturday 17 November 2018*

Lab sessions & Location:

1. Lychee Garden 6, Room 402 (Tuesday 19:00-20:50 pm)

2. Lychee Garden 6, Room 402 (Wednesday 8:00-9:50 am)

3. Lychee Garden 6, Room 408 (Wednesday 10:10~12:10 am)

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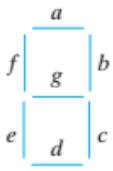
PART 1: DIGITAL DESIGN THEORY

Provide answers to the following questions:

1. Draw the multiple-level NOR circuit for the following expression:
   F = BC(D + C)A + (BC' + DE') + BD'
2. Implement the following Boolean function F , using the two-level forms of logic (a) AND-OR, (b) OR-NAND, (c) NOR-OR, (d) NAND-NAND, (e) OR-AND, (f) NOR-NOR, and (g) NAND-AND: F(A, B, C, D) = ∑ (1, 5, 8, 9, 10, 11, 12, 13, 15)
3. Derive the circuits for a four-bit parity generator and three-bit parity checker using an odd parity bit.
4. Design a combinational circuit with three inputs, x , y , and z , and three outputs, A, B , and C. When the binary input is 3, 4, 5, 6, or 7, the binary output is one less than the input. When the binary input is 0, 1, or 2, the binary output is two greater than the input.
5. An ABCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, g) select the corresponding segments in the display, as shown in figure (a). The numeric display chosen to represent the decimal digit is shown in (b). Using a truth table and Karnaugh maps, design the BCD-to-seven-segment decoder using a minimum number of gates.



(a) Segment designation

(b) Numerical designation for display

6. For a binary multiplier that multiplies two unsigned four-bit numbers
   a. Using AND gates and binary adders, design the circuit.
   b. Write and verify a Verilog dataflow model of the circuit.
7. Specify the truth table of an octal-to-binary priority encoder. Provide an output V to indicate that at least one of the inputs is present. The input with the

highest subscript number has the highest priority. What will be the value of the four outputs if inputs D2 and D6 are 1 at the same time?

8. Implement the following Boolean function with a multiplexer
    a. (a) F(A, B, C, D) =∑ (0, 2, 5, 8, 10, 14)
    b. F(A, B, C, D) = Π(2, 6, 11)
9. Implement a full subtractor with two 4 x1 multiplexers.
10. An 8 x1 multiplexer has inputs A , B , and C connected to the selection inputs S0 , S1 , and S2 , respectively. The data inputs I0 through I7 are as follows: I1 =I2 =1; I3 =I7 =0; I4 =I5 =D'; and I0 =I6= D .Determine the Boolean function that the multiplexer implements

PART 2: DIGITAL DESIGN LAB

INTRODUCTION

A combinational circuit has logic gates with no feedback paths or memory elements.

The design of combinational logic circuits includes the following steps:

1、 analyzing the requirements of the circuits and determining the number of inputs and outputs

2、 Do the design:

   a) If you do the design using data flow, you should derive the truth table that defines the required relationship between inputs and outputs. Obtain the simplified Boolean functions for each output as a function of the input variables

   b) If you do the design using behavioral modeling, you should describe the corresponding relationship between output and input from the perspective of algorithm.

3、 Write testbench to verify your design.

In this lab, you are required to design a combinational circuit with the specified requirements, write testbench to verify your design and generate bitstream. Please use the vivado and minisys development board to do the design, simulation and test.

You are also expected to practice how to use multiplexer to implement a Boolean function. A demo could be found in the multiplexer part of ‘Digital design lab8’.

PREAMBLE

Before working on the coursework itself, you should master the following material.

- ‘CH4-COMBINATIONAL LOGIC.pdf’ in Sakai site.
- ‘Digital design lab7’ and ‘Digital design lab8’ in Sakai site.
- Verilog :
  - http://www.verilog.com/

EXERCISE SPECIFICATION

Task1:

- There are **sixteen wards**, which are numbered from 0 to F respectively, among which the #0 ward has the highest priority, and the #F has the lowest priority (Priority decreases as the number increases). **Each room has a call bell, it can be turn on and turn off**. In the main control room there is a display screen which shows the ID of the room whose bell is on with the highest priority.
- Please write a circuit to realize this function and test.
  - Do the design.
  - Write testbench to verify the function of your design.
  - Create the constraint file.
  - Do the synthetic and implementation, generate the bitstream file and program the device, then test on the minisys develop board.

Task 2:

1. Use one piece of 74151(8-to-1-line multiplexer) realize the following logic function

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C} + A\bar{B}C\bar{D} + ABD + \bar{A}\bar{B}C\bar{D} + B\bar{C}D + \bar{A}$$

   - Get the SOP of the function

- Do the design.
- Write testbench to verify the function of your design.
- Create the constraint file.
- Do the synthetic and implementation, and generate the bitstream file and program the device, then test on the minisys develop board.

SUBMISSION

TIPS:

1. ***screenshot on every sub-task result which is requested, record it in your report.***
2. ***Regarding the testing scenes, please give a description for the input and output respectively, such as which part is the MSB. Otherwise you might suffer the deduction on marks***
3. ***Please transform your report from word to PDF, and upload the PDF file to sakai.***
4. ***Submit your assignment to the Sakai by the deadline.***

ASSESSEMENT

The full mark for this this exercise is 200, distributed as follows:

Theory: 58%

Question 1	10
Question 2	10
Question 3	10
Question 4	10

Question 5	18
Question 6	10
Question 7	12
Question 8	12
Question 9	12
Question 10	12
Total	116 marks

Lab: 42%

Task 1: the design in Verilog(**notes the input port number**)	12
Task 1: testbech (using verilog) and simulation result	5
Task 1: set the constraints file	5
Task 1: generate the bitstream file, program the device and test the design on the minisys develop board, at least 3 testing scenes	10
Task 2: get the SOP of the function	7
Task 2: the design in Verilog	15
Task 2: testbech (using verilog) and simulation result	5
Task 2: set the constraints file	5
Task 2: generate the bitstream file, program the device and test the design on the minisys develop board, at least 3 testing scenes	10
Problem and solutions	10
Total	84marks

Please use the same template of Digital design assignment 1.