DIGITAL DESIGN

ASSIGNMENT 4

Deadline: *11：55 PM Friday 30 November 2018*

Lab sessions & Location:

1. Lychee Garden 6, Room 402 (Tuesday 19:00-20:50 pm)

2. Lychee Garden 6, Room 402 (Wednesday 8:00-9:50 am)

3. Lychee Garden 6, Room 408 (Wednesday 10:10~12:10 am)

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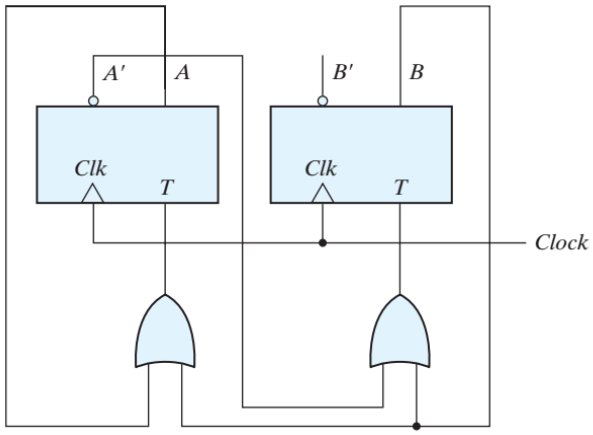
PART 1: DIGITAL DESIGN THEORY

Provide answers to the following questions:

1. Show that the characteristic equation for the complement output of a T flip-flop is Q'(t + 1) = T'Q'+ TQ
2. Derive the state table and the state diagram of the sequential circuit shown below. Explain the function that the circuit performs.



3. A sequential circuit has two JK flip-flops A and B and one input x . The circuit is described by the following flip-flop input equations:

   $J_A = x$ $K_A = B$

   $J_B = x'$ $K_B = A'$

   (a) Derive the state equations A (t + 1) and B (t + 1) by substituting the input equations for the J and K variables.

   (b) Draw the state diagram of the circuit.

PART 2: DIGITAL DESIGN LAB

INTRODUCTION

A sequential circuit is specified by a time sequence of inputs, outputs, and internal states, while the outputs of combinational logic depend only on the present values of the inputs. **A synchronous sequential circuit** is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time. Synchronization is achieved by a timing device called **a clock generator**, which provides a clock signal having the form of a periodic train of clock pulses. **Storage elements** that operate with signal levels (rather than signal transitions) are referred to as **latches**; those controlled by a clock transition are **flip-flops**. There are two ways with regard to the generation of outputs: in the **mealy** model, the output is a function of both the present state and the input, while in the **moore** model, the output is a function of only the present state.

The design of a clocked sequential circuit starts from a set of specifications and culminates in a logic diagram or a list of boolean functions from which the logic diagram can be obtained. The procedure of designing synchronous sequential circuits can be summarized by a list of recommended **steps**:

1. from the textual description and specifications of the desired operation, derive a state diagram for the circuit.
2. reduce the number of states if necessary
3. assign binary values to the states
4. obtain the binary-coded state table
5. choose the type of flip-flop to be used
6. derive the simplified flip-flop input equations and output equations
7. draw the logic diagram.

In this lab, you should learn the difference between latches and flip-flops, the relationship between 3 types of classic flip-flops, practice the state reduction and assignment and use behavior modeling in verilog to realise a synchronous sequential circuit.

PREAMBLE

Before working on the coursework itself, you should master the following material.

- 'CH5-Synchronous Sequential Logic-SUSTC.ppt' in Sakai site.
- 'Digital design lab9'，'Digital design lab10'，'Digital design lab11' in Sakai site.
- Verilog :
  - http://www.verilog.com/

EXERCISE SPECIFICATION

Task1:

construct a T Flip Flop with a *D* flip-flop and an exclusive-OR gate.

- Do the design（by structured design style）
- Write testbench to verify the function of your design.

Task 2:

Construct a synchronous JK flipflop with set and reset control

- Do the design as UDP
- Write testbench to verify the function of your design.

Task 3:

Construct a sequential circuit with an input x_in(1 bit width) and ouput state(2 bits width).

The initial state of circuit is 00, if the inputs meet the condition, it change to 01, then from 01 to 11, then from 11 to 10,then from 10 to 00,and so on.

while x_in is 0, the state of the circuit remains unchanged;

while x_in is1, the state of the circuit changed on on every positive edge of clock.

- Do the design: make the state equations and flip flop input functions, using D filp-flop(with synchronous reset signal) A and B ,do the design by structured style in Verilog.
- Do the design by using behavior modeling with Moore mode in Verilog
- Write testbench to verify the function of your design

SUBMISSION

TIPS:

1. ***screenshot on every sub-task result which is requested, record it in your report.***
2. ***Regarding the testing scenes, please give a description for the input and output respectively. Otherwise you might suffer the deduction on marks.***
3. ***Please transform your report from word to PDF, and upload the PDF file to Sakai.***
4. ***Submit your assignment to the Sakai by the deadline.***

ASSESSEMENT

The full mark for this this exercise is 100, distributed as follows:

Theory: 55%

Question 1	15
Question 2	15
Question 3	25
Total	55 marks

Lab: 45%

Task 1: the design in Verilog	5
Task 1: testbech (using verilog) and simulation result	5
Task 2: the design in Verilog	5
Task 2: testbech (using verilog) and simulation result	5
Task 3: State Equations and Flip flop input functions (while using D filp-flops to do the design)	5
Task 3: the design of a synchronous reset D flip flop in Verilog	5
Task 3: the design in Verilog(structured style by using D filp-flop)	5
Task 3: the design in Verilog(by using moore mode in verilog)	5
Task 3: testbech (using verilog) and simulation result	5
Total	45 marks

Please use the same template of Digital design assignment 1.