6.301 Final Project

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1 Schematic and PCB Layout

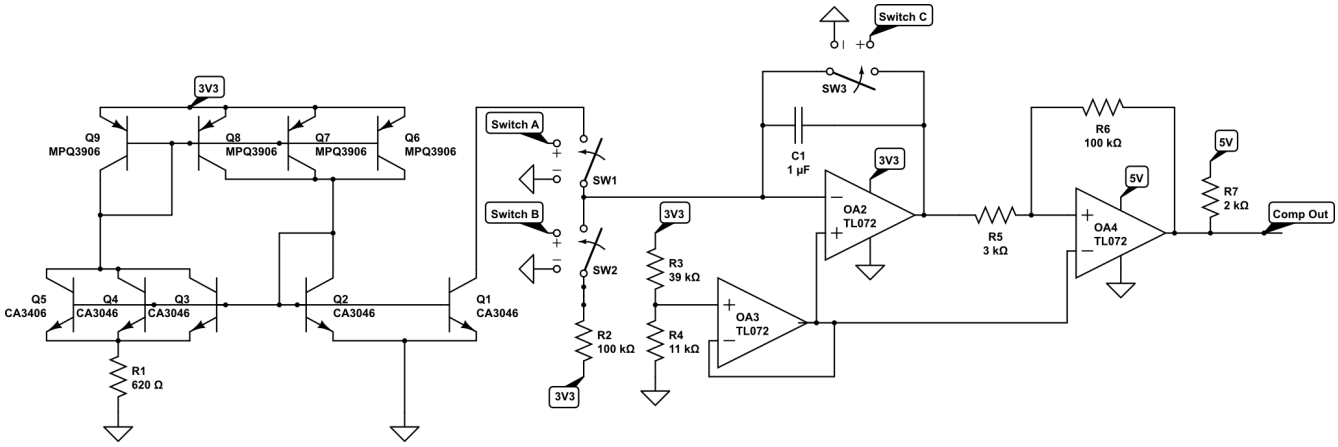

Figure 1: Thermometer schematic

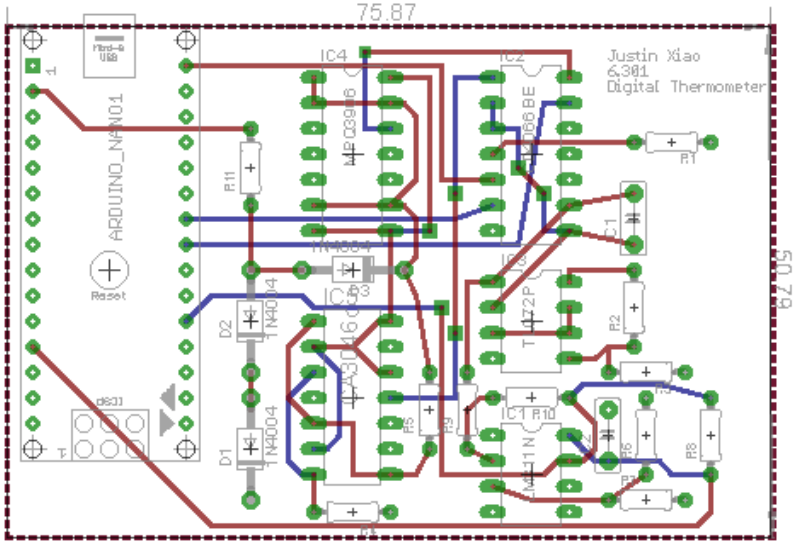

Figure 2: PCB Layout

2 PTAT Summary

In this section we discuss the PTAT circuit design. First, a derivation of the PTAT output current is presented. In reference to Fig. 1, treat Q3, Q4 and Q5 as a single transistor Q3 with three times the area as Q2. The output current is then given by the voltage at the base of Q3, V_{b3}, divided by R_1, where

$$V_{b3} = V_{BE2} - V_{BE3} = \frac{kT}{q} \ln\left(\frac{3I_C}{I_S}\right) - \frac{kT}{q} \ln\left(\frac{I_C}{3I_S}\right) = \frac{kT}{q} \ln(9)$$

where I_C is the current mirror output fed into Q3. Because of the triplet of Q6, Q7, and Q9, the current fed into Q2 is $3I_C$. Thus,

$$I_C = V_{b3}/R_1 = \frac{kT}{qR_1} \ln(9)$$

so the final output of the PTAT is

$$I_O = 3I_C = 3\frac{kT}{qR_1} \ln(9)$$

In my own design, the CA3046 was used to get as many matched transistors as possible to increase the area ratio and thus the output current. Likewise, the MPQ3906 was used for the PNP current mirror, with three of the PNPs in parallel to likewise increase output current. Initially planning to use a value of 100Ω for R_1, it was found found that this amount of current drew too much power for my Arduino so instead a value of 620Ω was used.

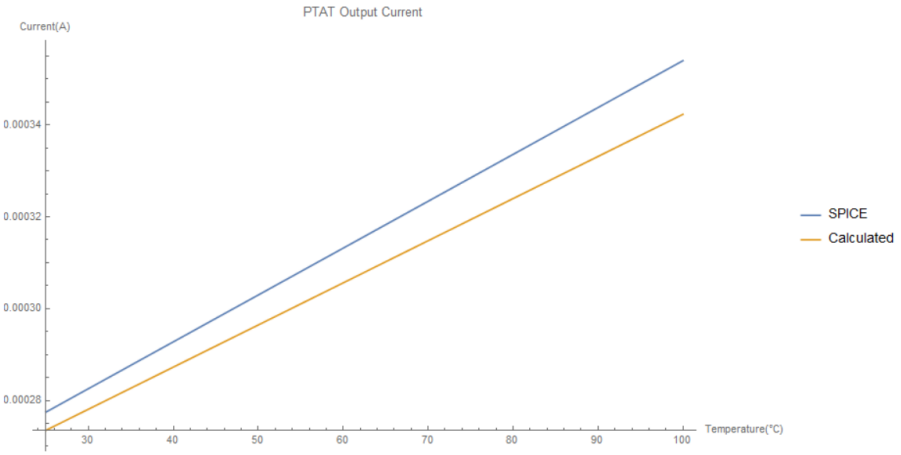

Figure 3: Comparison of theoretical to simulated PTAT currents

3 ADC Summary

The Dual-Slope Integrating ADC is designed as follows. In the ramp-up time, the input to the integrator is the PTAT output. This is integrated for a fixed amount of time, before it ramps down from integrating the reference voltage. The larger the input current, the larger time it takes for the output voltage to fall to the proper value in the ramp-down. Once the voltage falls to V_- of the comparator, we can digitally trigger Switch A closed and Switch B open to restart the integration process. In between cycles, Switch C is cycled closed then open to make sure each integration process is initialized at proper conditions. The output voltage of the integrator after the first step is given by $V_{out-up} = I_{in}/C_1 t_u$, where t_u is the fixed integration time. Then, $V_{out-down} = 0 = V_{out-up} - \frac{V_{ref}}{R_2 C_1} t_d$, where t_d is the time it takes the integrator to ramp down. We then see that

$$t_d = \frac{I_{in} R_2 t_u}{V_{ref}}$$

This design used a large value of $R_2 = 100k\Omega$ to increase the de-integration time and thus introduce less uncertainty in the time measurements. Having a decently large capacitance of $C_1 = 1\mu F$ also adds to this effect. The integrator and comparator were biased to have a virtual ground of around 0.7 V to avoid being directly at ground, which would cause the ADC to not work. To avoid improper biasing, this bias was buffered using a second op amp. A

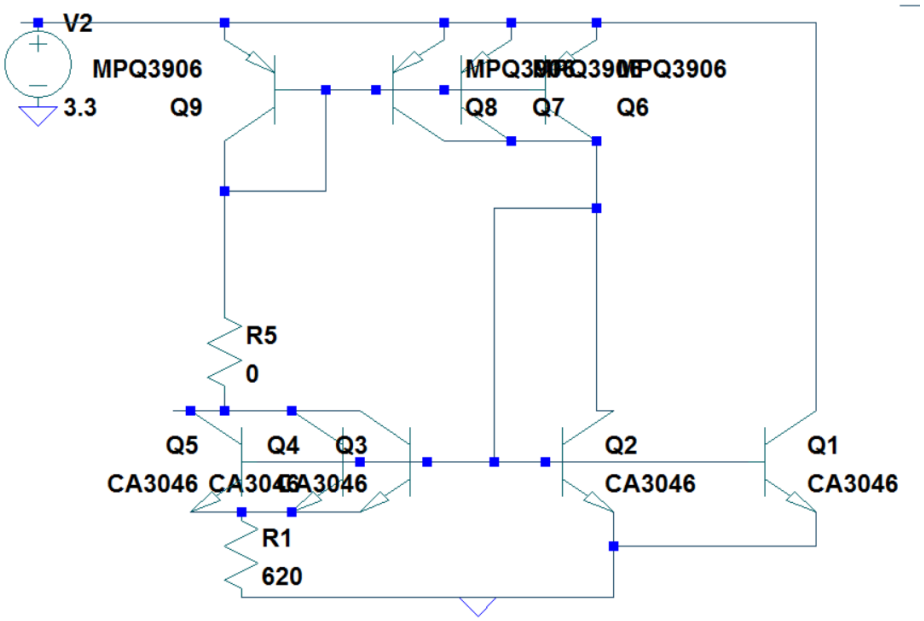

Figure 4: PTAT cell schematic

small amount of hysteresis was added to the comparator by setting $R_5 = 3k\Omega$ and $R_6 = 100k\Omega$ to reject noise without sacrificing accuracy.

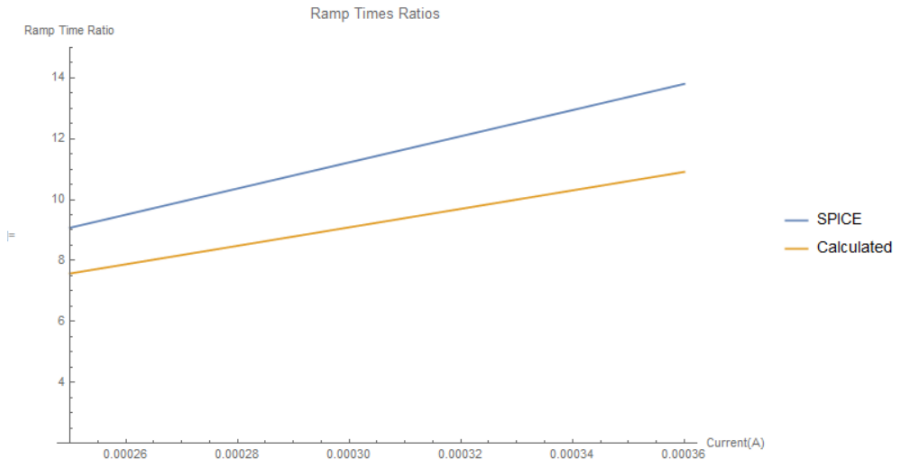

Figure 5: Comparison of theoretical to simulated ramp time ratios with respect to current

The one-shot circuit works by receiving a trigger pulse and outputting a logic one pulse once the triggering pulse is above some reference voltage, and remains on for some time determined by R and C in Fig. 6. The on-time of the one-shot circuit can be derived as follows: The output of the one-shot goes to zero once the CLR input hits the reference voltage. Now, the CLR voltage goes as $V_{cc}(1 - e^{-t/RC})$. Solving for t, we get

$$t = RC \ln(V_{cc}/(V_{cc} - V_{ref}))$$

In the firmware, we can set the ramp-up time equal to the one-shot output time by setting

```
const uint16_t ramp_up_delta_t_us = 3540;
...
// Start the integrator ramp-up
digitalWrite( pin_switch_en_a , HIGH );
```

```
// Integrate the known current for a known amount of time
delayMicroseconds( ramp_up_delta_t_us );

// Stop the integrator ramp-up
digitalWrite( pin_switch_en_a , LOW );
```

which integrates the input current for 3.54 ms. A ramp-up time of 3.54 ms was chosen to prevent any clipping. Another change made in the firmware is the implementation of the integrator reset, which is implemented by

```
digitalWrite(pin_switch_en_c , HIGH);
delayMicroseconds(10);
digitalWrite(pin_switch_en_c , LOW);
```

in between ramp cycles.

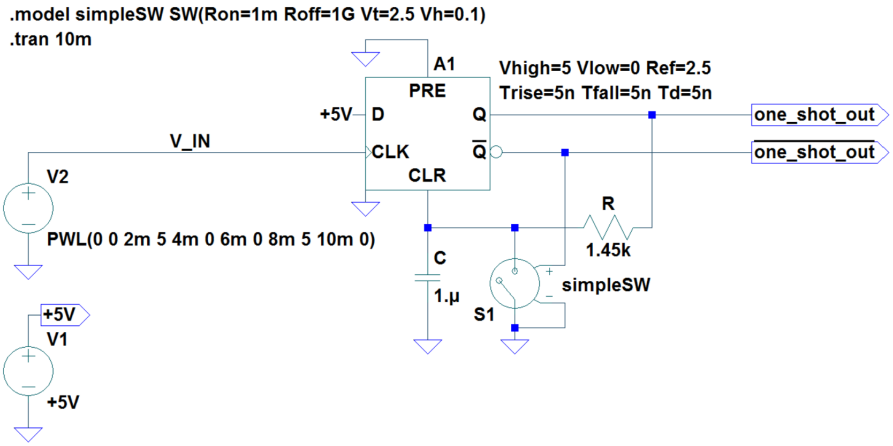

Figure 6: One-shot circuit

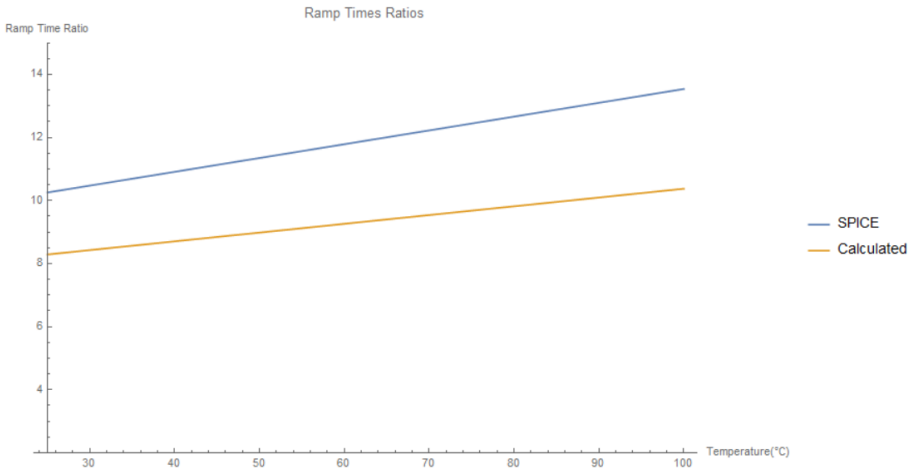

Figure 7: Comparison of theoretical to simulated ramp time ratios with respect to temperature

4 Characterization

The process of characterizing the temperature sensor is as follows. First, the CA3046 NPN array was separated from the rest of the circuit and soldered on its own protoboard, in order to isolate any heating to the NPN array alone. Thermal paste was applied to the top of the chip, and then a Peltier device was clamped securely onto the chip such that the entire chip was evenly heated. A heat sink was attached to the top of the Peltier device for more

efficient heating, and a thermocouple was taped on in order to measure real temperature. A variable power supply was used to change the voltage across the Peltier device and heat the NPN array at various temperatures.

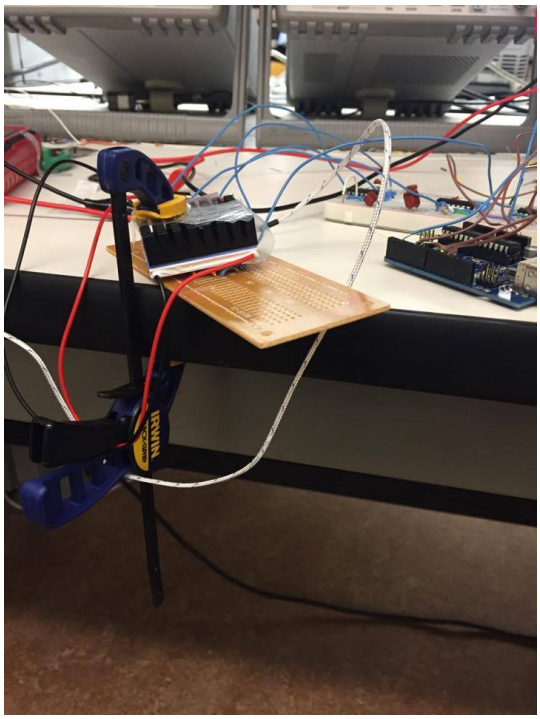

Figure 8: PTAT heating setup

Ten different ramp-down readings were taken every 5 °C. The data and linear fit is shown in Fig. 9.

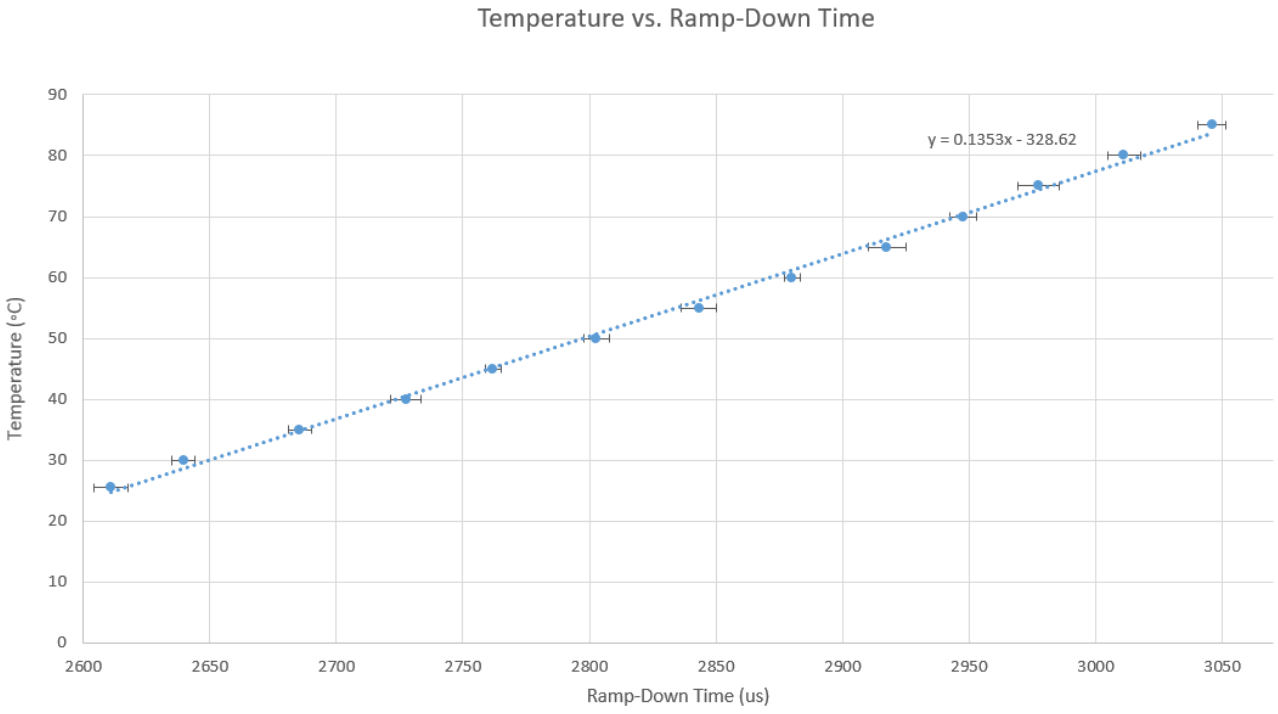

Figure 9: Data and linear fit

By plotting the residuals, we see that our temperature sensor is quite linear with temperature, with deviations usually within 3 °C and no greater than 5 °C at the extreme temperature values. The largest source of error arises from inaccuracy in measuring real temperature, which was difficult to control precisely in the Peltier device using the variable power supply. Often, in order to measure at some temperature I would frequently have to change the voltage across the Peltier device in order to prevent overshooting or undershooting the temperature.

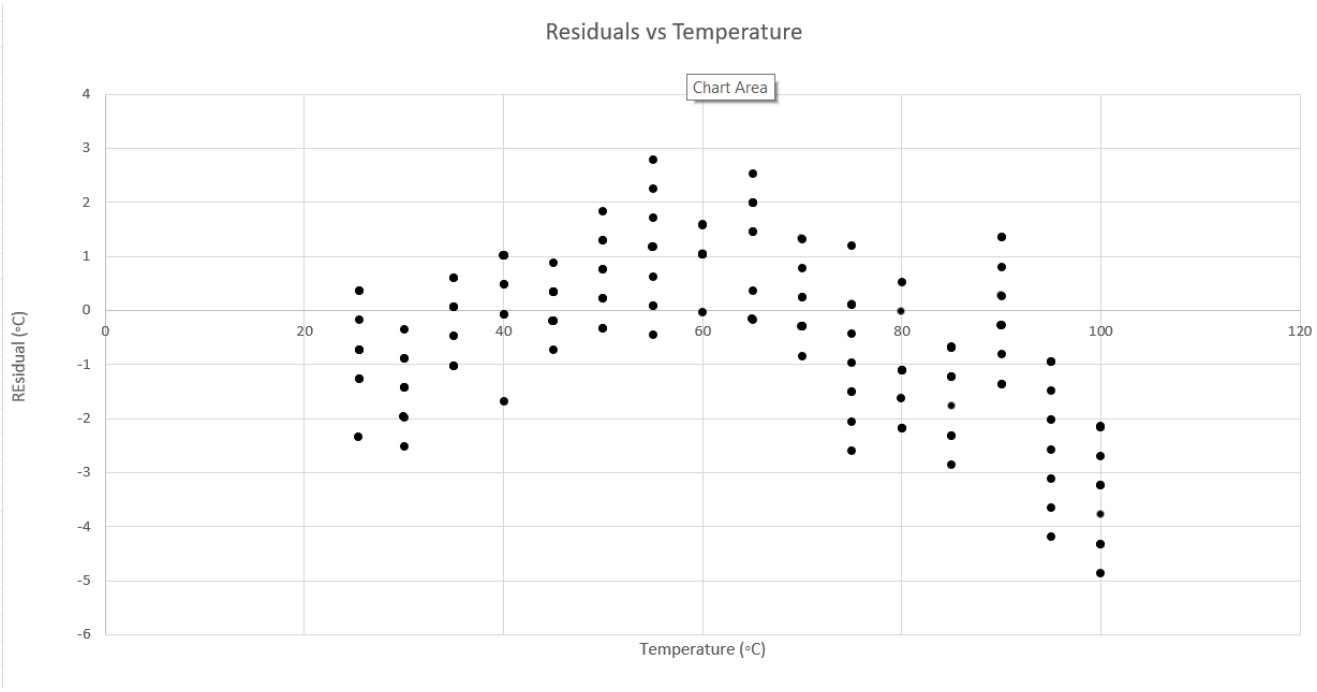

Figure 10: Plot of residuals

Now, discrepancies between the calculated and simulated ramp time ratios are relatively small, and can be explained by using different virtual grounds (changing the bias point to be 470 mV in SPICE brings the calculated and simulated ratios to be about the same). However, there is a very large discrepancy between these values and the measured ones, at about an order of magnitude difference. One explanation is that the biasing in the built configuration was not correct; for example, the Arduino's 3V3 output, when connected to my circuit, produced 3.9 V instead. However, since the output was still very linear, the design was kept as is. Despite being difficult to predict the results, they seemed very reproducible as using different chips gave the same measured results.

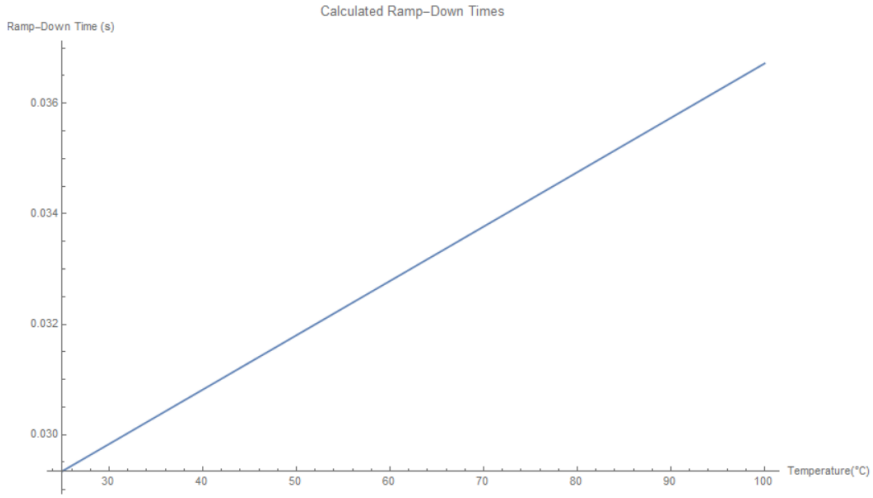

Figure 11: Calculated ramp-down times

5 PCB Design

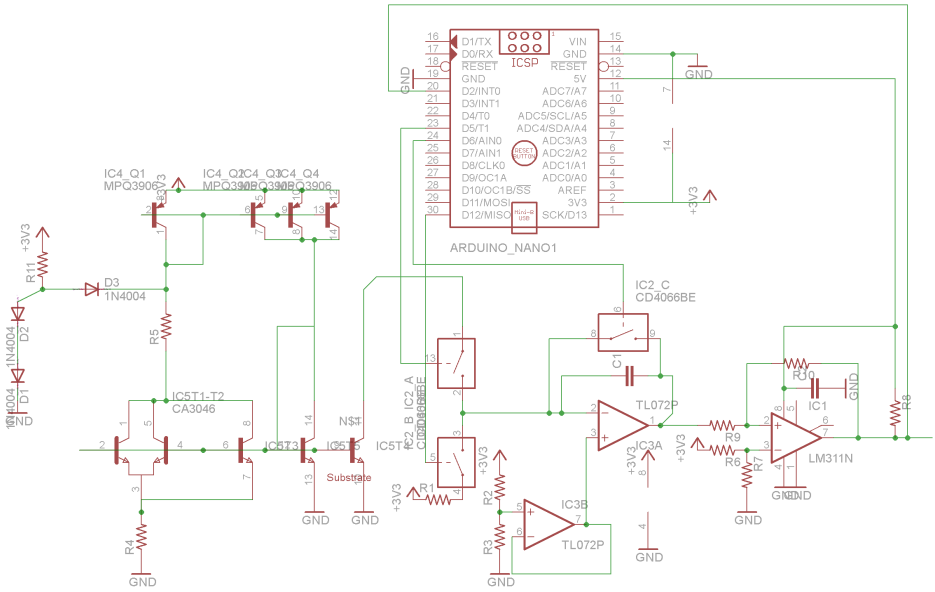

Figure 12: PCB Schematic

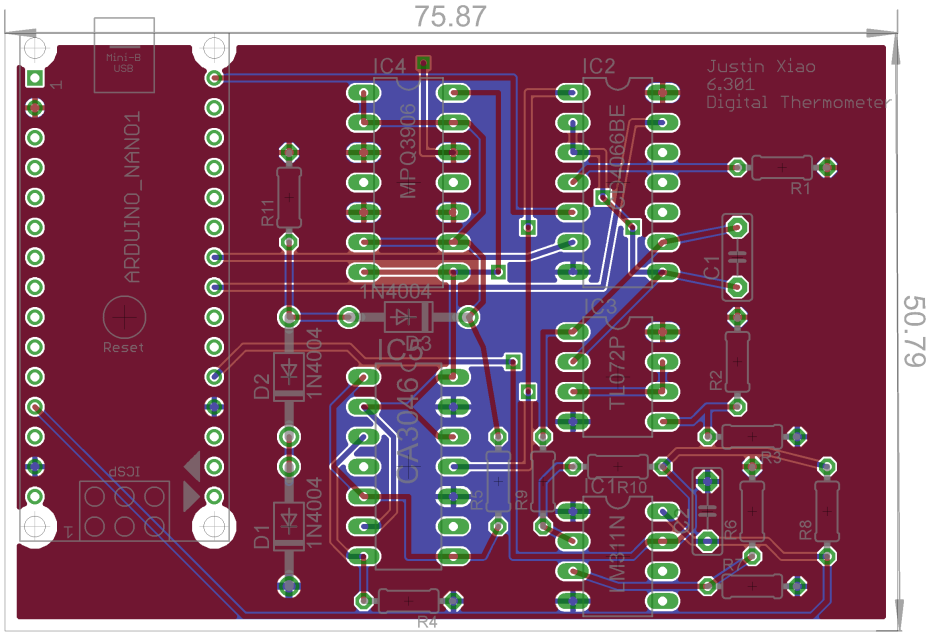

Figure 13: PCB Design

They layout was designed to be compact while reducing parasitics by using ground and power planes and avoiding parallel traces between layers. Github repository: https://github.com/jtxiao/6.301-Final-Project.