

Dokumentation von Tests und Verhalten

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Part I

Audio Signal: speaker output

The first major test that is implemented is to forward the incoming signal directly to the output. That enables the possibility to plugin a speaker so that it is possible to control the Audio signal by listening and comparing. However keep in mind that the human ear can detect differences in audio signals only to a certain degree.

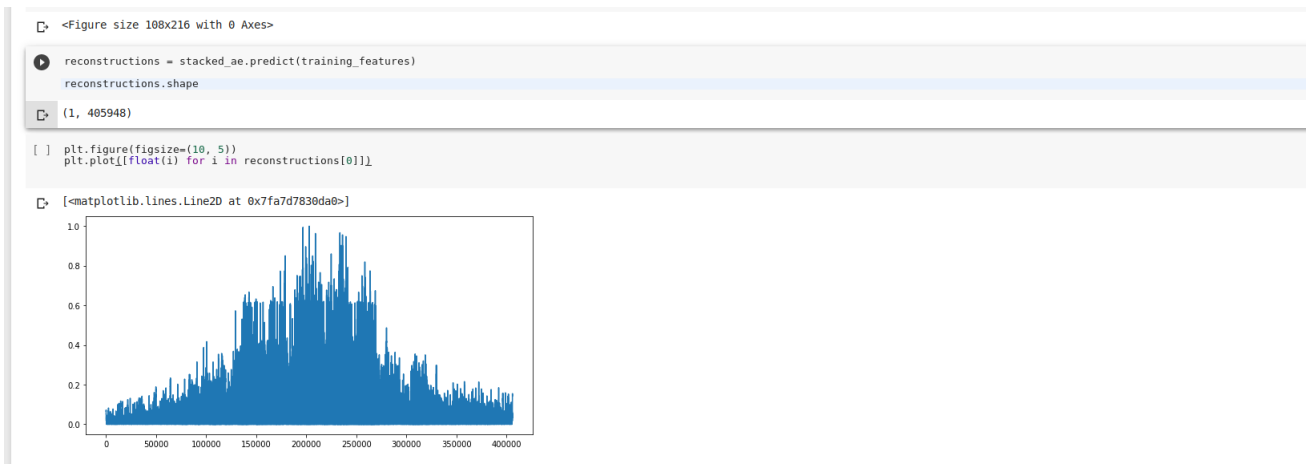
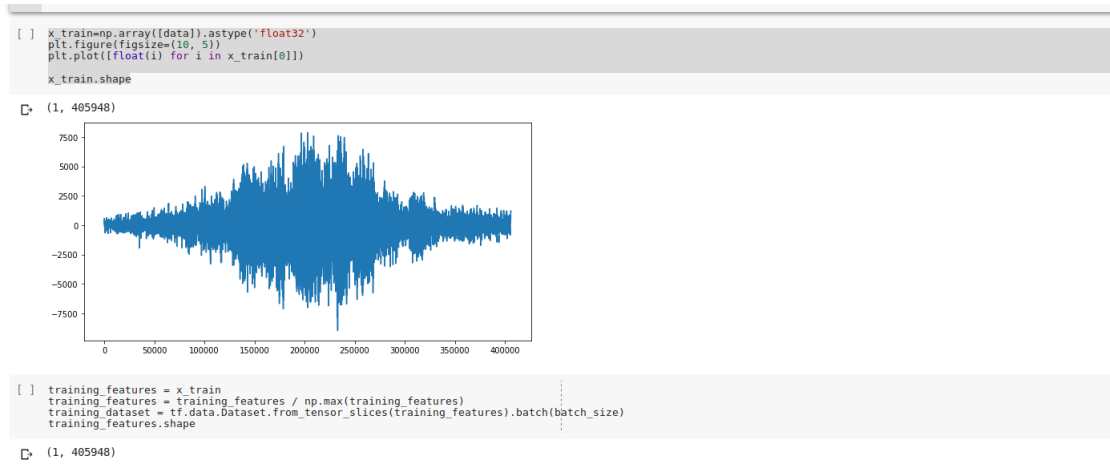
Part II

Test of the algorithm

Another step that is also part of the testing procedure was to evaluate the Neural Networks algorithm on a computer first. This leads to a proof whether the algorithm and architecture that was chosen - the AutoEncoder - is able to detect certain patterns and filter out random noise. For the evaluation Tensorflow 2.0. The whole python script can be found in the drive folder as a google colab document and under the code section.

The proof-of-concept shows that it is possible to create a more accurate representation, of the important parts of the signal, out of the input audio signal.

The next two figures are showing the original audio data (upper picture) and the latent pattern representation (bottom picture).

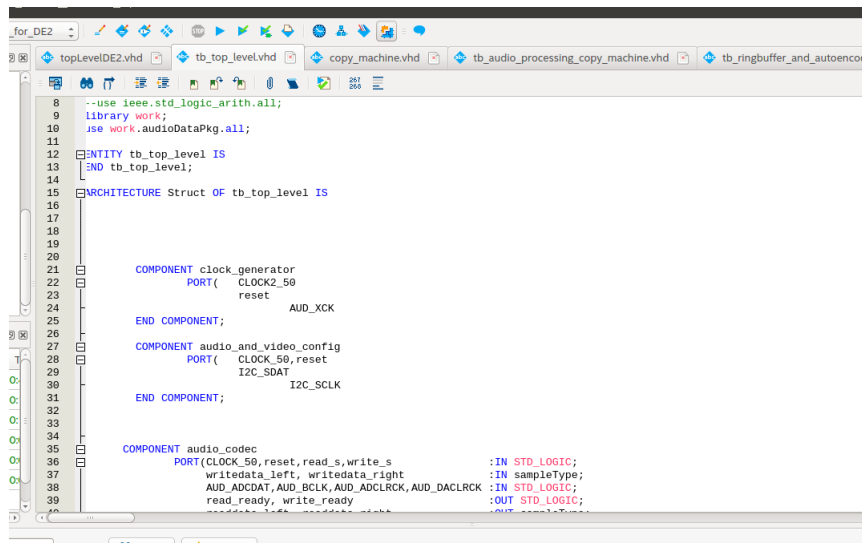


Part III

Testbenches

Testbenches are extremely important when creating high quality code with Quartus. Since Quartus is not easy to debug, Testbenches are one of the fastest and most straight-forward ways to test either specific components of your system or the architecture as a whole by running them in a simulation. In this section a description of the Testbenches that were used during the project is given as well as further explanations and ideas.

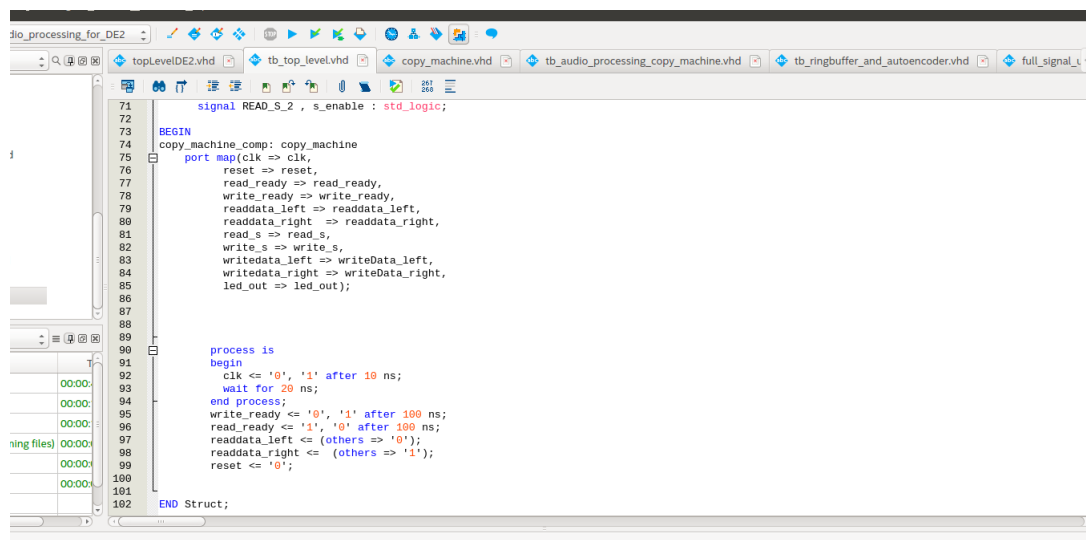
- Snippets of the top-level Testbench can be seen on the pictures bellow.



```

1  for DE2
2
3  topLevelDE2.vhd  tb_top_level.vhd  copy_machine.vhd  tb_audio_processing_copy_machine.vhd  tb_ringbuffer_and_autoencod
4
5  8  --use ieee.std_logic_arith.all;
6  9  library work;
7  10 use work.audioDataPkg.all;
8  11
9  12 ENTITY tb_top_level IS
10 13 END tb_top_level;
11 14
12 15 ARCHITECTURE Struct OF tb_top_level IS
13 16
14 17
15 18
16 19
17 20
18 21 COMPONENT clock_generator
19 22 PORT(
20 23     CLOCK2_50
21 24     reset
22 25     AUD_XCK
23 26
24 27 END COMPONENT;
25 28
26 29 COMPONENT audio_and_video_config
27 30 PORT(
28 31     CLOCK_50,reset
29 32     I2C_SDAT
30 33     I2C_SCLK
31 34
32 35 END COMPONENT;
33 36
34 37 COMPONENT audio_codec
35 38 PORT(CLOCK_50,reset,read_s,write_s      :IN STD_LOGIC;
36 39     writedata_left, writedata_right    :IN sampleType;
37 40     AUD_ADCCDAT,AUD_BCLK,AUD_ADCLRCK,AUD_DACLCK :IN STD_LOGIC;
38 41     read_ready, write_ready            :OUT STD_LOGIC;
39 42     readdata_left, readdata_right      :OUT sampleType;
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1  audio_processing_for_DE2
2
3  topLevelDE2.vhd  tb_top_level.vhd  copy_machine.vhd  tb_audio_processing_copy_machine.vhd  tb_ringbuffer_and_autoencoder.vhd  full_signal_u
4
5  71  signal READ_S_2 , s_enable : std_logic;
6  72
7  73 BEGIN
8  74 copy_machine_comp: copy_machine
9  75 port map(clk => clk,
10 76     reset => reset,
11 77     read_ready => read_ready,
12 78     write_ready => write_ready,
13 79     readdata_left => readdata_left,
14 80     readdata_right => readdata_right,
15 81     read_s => read_s,
16 82     write_s => write_s,
17 83     writedata_left => writedata_left,
18 84     writedata_right => writedata_right,
19 85     led_out => led_out);
20 86
21 87
22 88
23 89
24 90 process is
25 91 begin
26 92     clk <= '0', '1' after 10 ns;
27 93     wait for 20 ns;
28 94 end process;
29 95 write_ready <= '0', '1' after 100 ns;
30 96 read_ready <= '1', '0' after 100 ns;
31 97 readdata_left <= (others => '0');
32 98 readdata_right <= (others => '1');
33 99 reset <= '0';
34 100
35 101
36 102 END Struct;
37 103
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Testbench Top-Level Architecture

The top-level Testbench is the test of the system as a whole. It is the last instance before the system can be tested on a real FPGA. A clock signal is given that switches every 10 nanoseconds within the Testbench's process. Furthermore instances of all the top-level components are created and connected to Testbench signals so that it is also possible to read inner signals of the system within the simulation process. However the main aim of this Testbench is to look onto the whole system as a black box, give some well-defined and necessary signals to the inputs and check if the output matches the expectations.

For more unit level analysis the following described Testbenches are likely to be better candidates.

Testbench Copy-Machine

In this Testbench an the copy-machine is instantiated. Hence the other components are Altera IP they are expected to behave correctly per default. That is why this Testbench focuses on the functionality of the copy-machine. Again it is possible to look at the copy-machine as a black-box and observe the output signals while changing the input signals and see if the behaviour matches the expectation. However the most relevant signals of the copy-machines inner circles are again connected to Testbench signals so an observation during the simulation is possible.

Testbench Ringbuffer - Denoising AutoEncoder

The most complex part of the whole system is the processing of data between the component Ringbuffer and the component Denoising AutoEncoder. To ease the analysis of this key route another Testbench has been created. Within this system every single Signal between all those components is measured. This Testbench is crucial during development to get a quick understanding where certain error occuring. The picture below shows the relevant part that is tested with all its signals.

