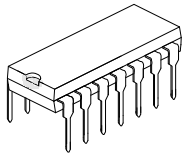
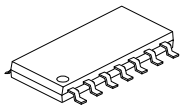
CD4069

CMOS IC

INVERTER CIRCUITS



DIP-14



SOP-14

■ DESCRIPTION

The UTC **CD4069** consists of six inverter circuits and is manufactured using complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity, and symmetric controlled rise and fall times.

All inputs are protected from damage due to static discharge by diode clamps to VDD and VSS.

■ FEATURES

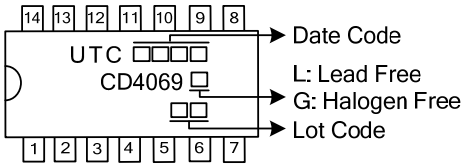
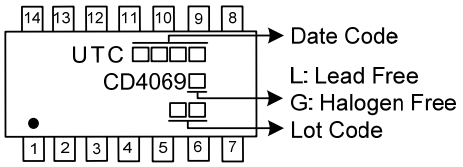
* Wide supply voltage range: 3.0V ~ 15V.
* High noise immunity: 0.45 V_{DD} typ.
* Low Power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS.

■ ORDERING INFORMATION

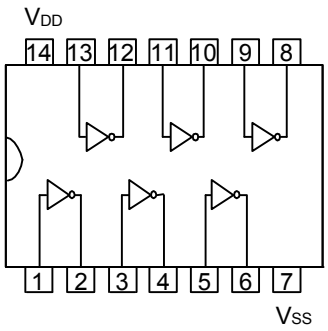
Ordering Number		Package	Packing
Lead Free	Halogen Free		
CD4069L-D14-T	CD4069G-D14-T	DIP-14	Tube
CD4069L-S14-R	CD4069G-S14-R	SOP-14	Tape Reel

CD4069G-D14-T (1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube, R: Tape Reel (2) D14: DIP-14, S14: SOP-14 (3) G: Halogen Free and Lead Free, L: Lead Free

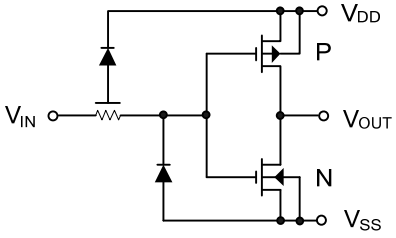
■ MARKING

DIP-14	SOP-14
	

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
DC Supply Voltage		V_{DD}	-0.5 ~ +18	V
Input Voltage		V_{IN}	-0.5 ~ V_{DD} +0.5	V
Storage Temperature Range		T_S	-65 ~ +150	°C
Power Dissipation	DIP-14	P_D	700	mW
	SOP-14		500	
Junction Temperature		T_J	125	°C
Operating Temperature		T_{OPR}	-20 ~ +85	°C
Storage Temperature		T_{STG}	-40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage	V_{DD}	3 ~ 15	V
Input Voltage	V_{IN}	0 ~ V_{DD}	V
Operating Temperature	T_A	-40 ~ 85	°C

■ DC ELECTRICAL CHARACTERISTICS (V_{SS}=0V, T_A=25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{DD} or V_{SS}				1.0	μA
		V_{DD}=10V, V_{IN}=V_{DD} or V_{SS}				2.0	μA
		V_{DD}=15V, V_{IN}=V_{DD} or V_{SS}				4.0	μA
Low Level Output Voltage	V_{OL}	$\|I_O\|$<1μA	V_{DD}=5V		0	0.05	V
			V_{DD}=10V		0	0.05	V
			V_{DD}=15V		0	0.05	V
High Level Output Voltage	V_{OH}	$\|I_O\|$<1μA	V_{DD}=5V	4.95			V
			V_{DD}=10V	9.95			V
			V_{DD}=15V	14.95			V
Low Level Input Voltage	V_{IL}	$\|I_O\|$<1μA	V_{DD}=5V, V_O=4.5V			1.0	V
			V_{DD}=10V, V_O=9V			2.0	V
			V_{DD}=15V, V_O=13.5V			3.0	V
High Level Input Voltage	V_{IH}	$\|I_O\|$<1μA	V_{DD}=5V, V_O=0.5V	4.0			V
			V_{DD}=10V, V_O=1V	8.0			V
			V_{DD}=15V, V_O=1.5V	12.0			V
Low Level Output Current (Note 2)	I_{OL}	V_{DD}=5V, Vo=0.4V		0.44	0.88		mA
		V_{DD}=10V, Vo=0.5V		1.1	2.25		mA
		V_{DD}=15V, Vo=1.5V		3.0	8.8		mA
High Level Output Current (Note 2)	I_{OH}	V_{DD}=5V, Vo=4.6V		-0.44	-0.88		mA
		V_{DD}=10V, Vo=9.5V		-1.1	-2.25		mA
		V_{DD}=15V, Vo=13.5V		-3.0	-8.8		mA
Input Current	I_{IN}	V_{DD}=15V, V_{IN}=0V			-10^{-5}	-0.30	μA
		V_{DD}=15V, V_{IN}=15V			10^{-5}	0.30	μA

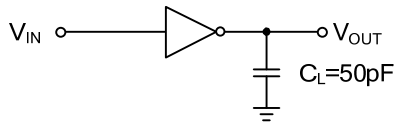
■ AC ELECTRICAL CHARACTERISTICS (Note 1)

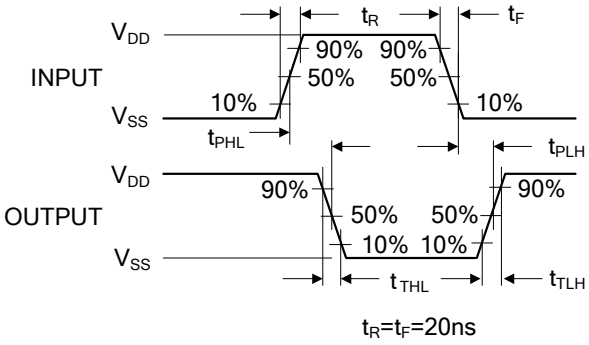
(T_A=25℃, C_L=50pF, R_L=200kΩ, t_R and t_F ≤ 20 ns, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time from Input to Output	t_{PHL} or t_{PLH}	V_{DD}=5V		50	90	ns
		V_{DD}=10V		30	60	ns
		V_{DD}=15V		25	50	ns
Transition Time	t_{THL} or t_{TLH}	V_{DD}=5V		80	150	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Average Input Capacitance	C_{IN}	Any Gate		6	15	pF
Power Dissipation Capacitance	C_{PD}	Any Gate (Note 3)		12		pF

Notes: 1. AC Parameters are guaranteed by DC correlated testing.
2. I_{OH} and I_{OL} are tested one output at a time.
3. C_{PD} determines the no load AC power consumption of any CMOS device.

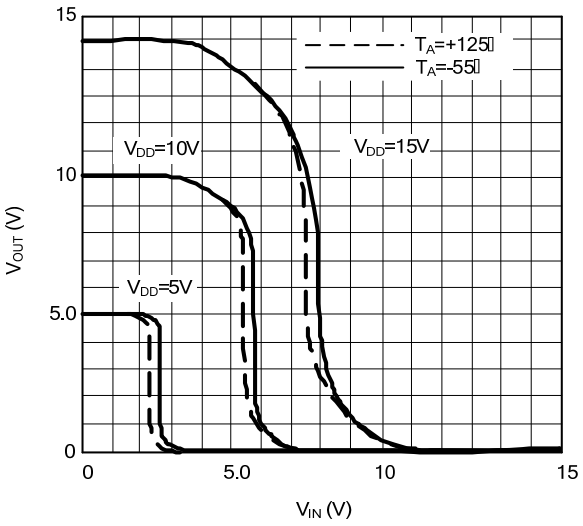
■ AC TEST CIRCUITS AND SWITCHING TIME WAVEFORMS



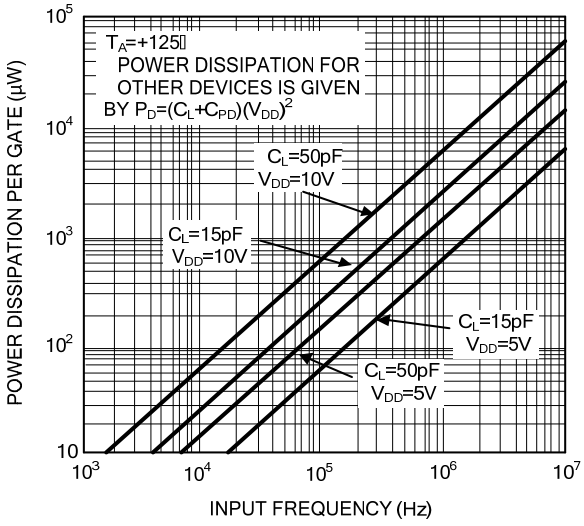


■ TYPICAL PERFORMANCE CHARACTERISTICS

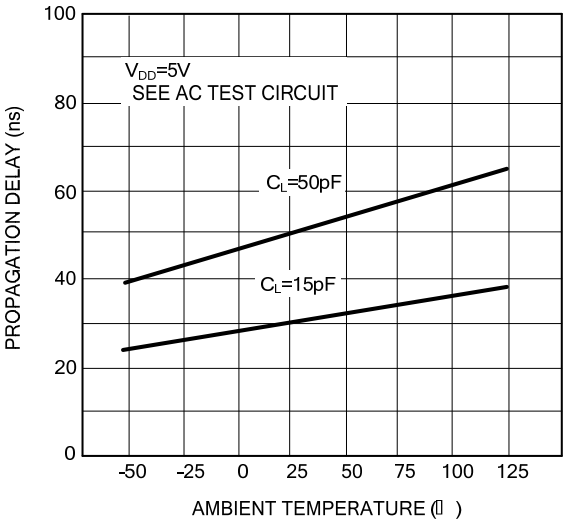
Gate Transter Characteristcis



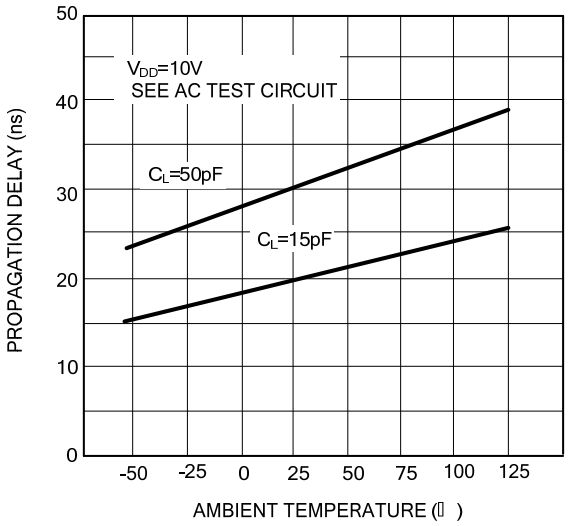
Power Dissipation vs Frequency



Propagation Delay vs Ambient Temperature



Propagation Delay vs Ambient Temperature



Propagation Delay Time vs Load Capacitance