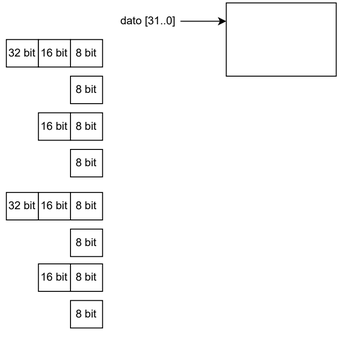
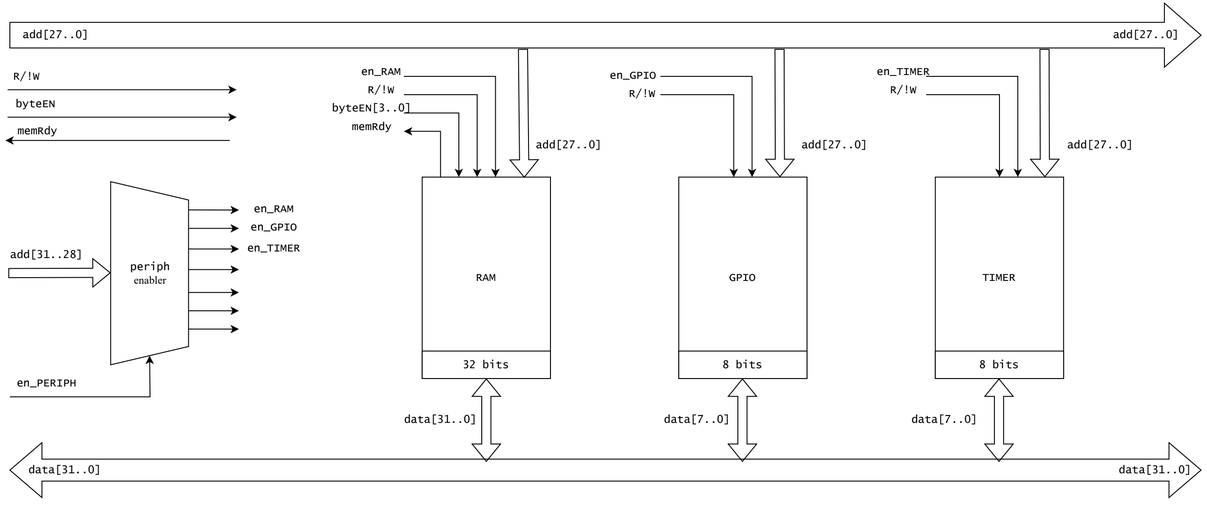
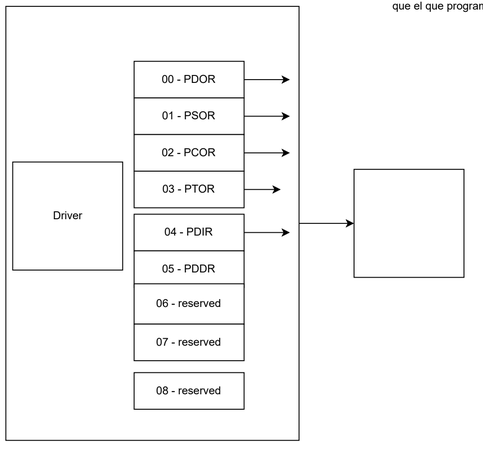
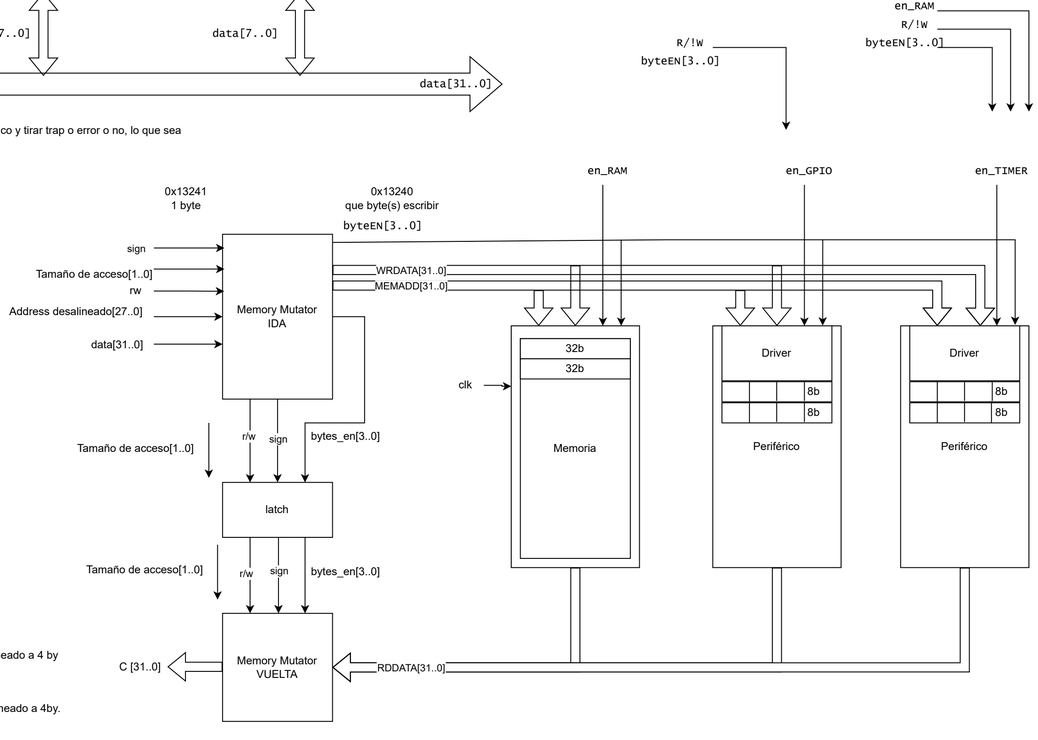
An EEI may guarantee that misaligned loads and stores are fully supported, and so the software running inside the execution environment will never experience a contained or fatal address-misaligned trap. In this case, the misaligned loads and stores can be handled in hardware, or via an invisible trap into the execution environment implementation, or possibly a combination of hardware and invisible trap depending on address.





- Memoria de 32 bits, periféricos de 8 bits, detectar cuando se le escriben los 24 bits MSB a un periférico y tirar trap o error o no, lo que sea
O
que el que programe no sea boludon





Lectura: llega address arbitrario, y byte o bytes a acceder. Se transforma en address alineado a 4 by una etapa posterior general decide con cuáles partes de la palabra se tiene que quedar. Periférico debe mapear eso a la lectura de ciertos registros.

Escritura: llega address arbitrario, y byte o bytes a escribir. Se transforma en address alineado a 4by. Lógica interna de cada