CMSI 284 CISC-RISC Project

Due date: April 28, 2017

Background

Historically, mainframe computer hardware (before laptops were invented) was becoming more and more complex with Instruction Set Architecture's (ISA's) growing considerably larger over time. This eventually became the basis for what is today called the Complex Instruction Set Computer (CISC) architecture. In contrast during the late 1970's and 1980's, a new philosophy emerged highly restricting the size of the ISA by significantly reducing the number of computer hardware instructions. Thus the Reduced Instruction Set Computer (RISC) architecture rose to become the major CISC challenger.

The purpose of this project is to give you an opportunity for an individual investigation into the two current predominate computer architecture styles by studying the major characteristics of each style and understand their advantages and disadvantages.

In particular, you are to focus on X86-64 as the CISC representative. And for RISC you are to focus on the very latest representative which has recently been released: RISC V (pronounced "risk 5"). RISC V reference information can be found in the appendix.

Assignment (*Choose <u>only one</u> of the following options*)

1. [*Single student project*] Write a double spaced, ten page (minimum) report describing and contrasting CISC vs. RISC. This is to include an overview of each describing organization and general function. The major thrust of your report is to be on what effects each has on object code size, basic instruction speed, instruction decode overhead, memory access requirements, advantages or disadvantages for compilers, etc. You are to use x86-64 and RISC V as prime examples to illustrate the different aspects of your report. Take advantage to search various available online resources for technical background understanding, major issues, and future growth.
2. [*Single student or 2 student team project*] Go to the RISC V website (refer to the appendix) and download the RISC V ISA simulator along with the complete tool chain (C compiler, assembler, linker, loader, debugger, etc.). Configure this software if necessary and get it running on your computer. If successful, you will have a tool chain for which you can compile C programs into RISC V binaries, an assembler for assembling RISC V assembly programs, a linker for linking a C main program with one or more assembly language programs, and a RISC V-ISA simulator which can run the compiled/assembled and linked generated binaries from select C and Assembly language programming

assignments. Finally, you are to submit a written report of your experience with this installation documenting all the hurdles and missteps you had to deal with to make this work. The document should include output screenshots of sample C and Assembly programs compiled with the toolchain and run in simulation. **NOTE**: The "**Angel**" RISC V simulator **is not** allowed for this option.

3. [*Single student project*] This is a hybrid of 1. and 2. above using x86-64 (this is a must) and your favorite RISC architecture (ARM, MIPS, etc.) . A shortened report of 1. together with toolchain and simulator installation of your RISC architecture of choice to be configured. The same report of the compilation and assembling, linking, and running activities are to be demonstrated as found in 2. **NOTE**: The "**Angel**" RISC V simulator **is** allowed for this option.

Appendix

As found on https://riscv.org/risc-v-foundation/:

The RISC-V Foundation

RISC-V (pronounced "risk-five") is a new instruction set architecture (ISA) that was originally designed to support computer architecture research and education and is now set to become a standard open architecture for industry implementations under the governance of the RISC-V Foundation. The RISC-V ISA was originally developed in the Computer Science Division of the EECS Department at the University of California, Berkeley.

The RISC-V Foundation, a non-profit corporation controlled by its members, directs the future development and drives the adoption of the RISC-V ISA. Members of the RISC-V Foundation have access to and participate in the development of the RISC-V ISA specifications and related HW / SW ecosystem.

Important links:

RISC V specification: https://riscv.org/specifications/

riscv-tools https://riscv.org/software-tools/

Spike (RISC V hardware) simulator https://riscv.org/software-tools/risc-v-isa-simulator/