A Novel thermal-shutdown Protection Circuit

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***Abstract* — A new type thermal-shutdown circuit has been designed in UMC 0.6um BiCMOS process. A feedback is used to solve the problem of thermal-oscillation and a shunt regulator circuit is used to solve the problem of the limit of the technology model. This thermal-shutdown circuit has simple structure, process insensitive and low power dissipation. It can be widely used for modularize in power management ICs. HSPICE simulation results shows that the circuit has excellent capability of power supply rejection and operated in power range from 2V to 12V. The error between Activation temperature and deactivation temperature remained basically unchanged for 29℃.**

Keywords — Themral-shutdown; BiCMOS; Feedback; Modularize;

I. INTRODUCTION

Modern electronic circuits contain thermal shutdown circuit for reducing power dissipation and overheating in electronic circuits. As a result of the power dissipation of an electronic circuit on a chip, the temperature of the chip increases. When the power dissipation increases, this may result in the breakdown of the circuit. To protect the chip, the power dissipation should be limited. The thermal shutdown circuit is arranged to provide a thermal shutdown signal in response to an over temperature condition. In this paper, the circuit is presented that can able to operate at supply voltages in the range of 2-12V. It can be widely used for modularize in power management ICs.

II. CONVENTIONAL CIRCUIT

In order to have sufficient temperature sensitivity, over-temperature protection circuit is often designed with a comparator, Fig.1 is a schematic of a conventional thermal-shutdown circuit [1].

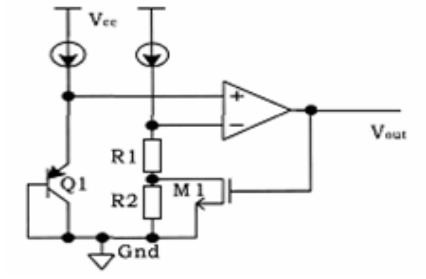

Fig.1. Conventional thermal-shutdown circuit

When V_{BE}<V_{R1}, the comparator output reversal occurred so that it can provide a low signal to cut off the main power circuit, make the system the heat lower. The thermal protection circuit base on the comparator can work with high temperature stability, but this circuit has a lot of disadvantage. It definitely adds the power dissipation. In addition, the PTAT current produced by the sub-threshold MOS accuracy is not high, threshold temperature is not stable enough under different supply voltage.

III. PROPOSED CIRCUIT

In this paper, the over-temperature protection circuit has three parts: the bias circuit, thermal shutdown circuit and shunt regulator circuit. The thermal shutdown circuit provides a first current in response to a change in temperature when a V_{BE} associated with a transistor decreases below a predetermined level. The first current is mirrored to provide a scaled current. A thermal shutdown signal is activated when the scaled current becomes greater than a reference current. The first current is increased in response to the activated thermal shutdown signal such that the thermal shutdown circuit is deactivated at a temperature that is lower than the temperature at which the circuit is activated. The thermal shutdown circuit is deactivated when the temperature of the die decreases.

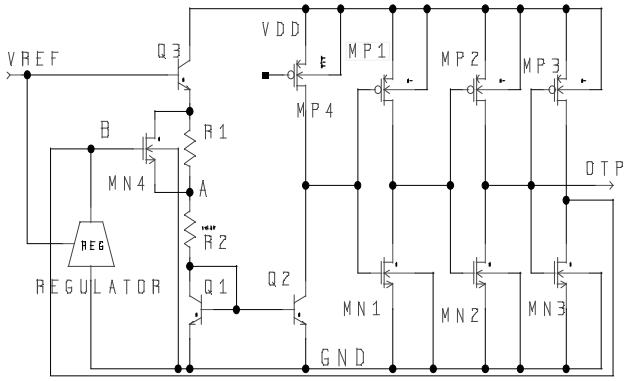

Fig.2. Thermal-shutdown circuit

The shunt regulator circuit is shown in Fig.3, This shut regulator circuit provides a desired regulated voltage at an output voltage (node B) and ensures the circuit works at higher voltages.

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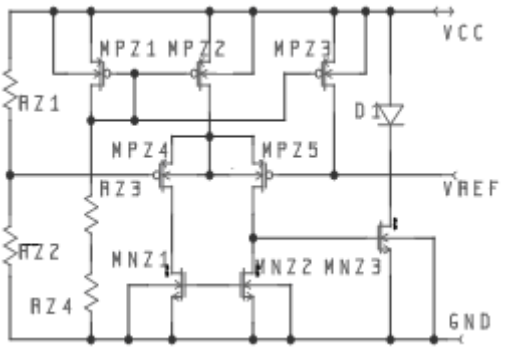

Fig.3. Shunt regulator circuit

The proposed current bias [2] is depicted in Fig .4. The PTAT current is produced by the transistors of M1-M4, R3, Q4, Q5. The MOSFET M5 has the same dimensions with M1 and M2, the current flowing into the emitter of Q1 is twice as large as that of Q2. The negative temperature-dependent current is produced by the transistor of M6 and the resistor of R4. Due to the resistor of R1 is connected to the source of M6, so they form a source follower. That is to say, the voltage across R1 varies linearly with voltage of the gate of M6.

In the power ICs chip, this bias can be replaced by current reference which is integrated in the chip.

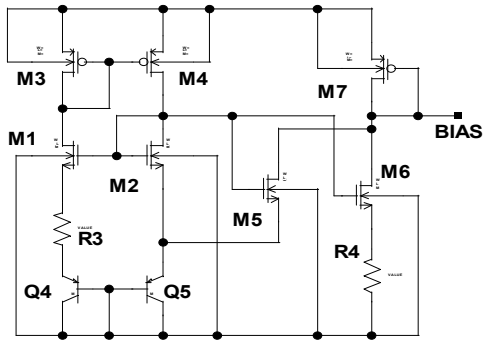

Fig.4. Bias circuit

Assuming V_{REF} is a bandgap reference voltage that is independent of temperature variations and the current flow MP4 is I_{REF}. From Fig.3 it is noticeable that the current across the resistance R1 is:

$$I_{R1} = I_{R2} = I_{Q1} = I_{Q2} = \frac{V_{REF} - 2V_{BE}}{R_1 + R_2} \quad (1)$$

At room temperature, the transistor turn-on voltage is 0.5V-0.7V, so when voltage $V_{REF} < V_{BE}$, transistor Q1, Q2 and Q3 are off, the current across R1 and R2 is zero. As the Q1 and Q2 constitute a current mirror, the drain voltage of MP4 is extremely high, after a inverter, the output voltage is high, the circuit is inactive.

When the temperature is rising, the V_{BE} of transistor Q1, Q2 further reduce. So from (1), I_{Q2} increased when the temperature rise to fever-off point threshold, output voltage (node OTP) is low, the current across Q2 increase to be equal to the current I_{REF}:

$$I_{REF} = I_{Q2} = \frac{V_{REF} - 2[V_{BE0} + \frac{\partial V_{BE}}{\partial T}(T_1 - T_0)]}{(R_1 + R_2)[1 + \frac{\partial R}{\partial T}(T_1 - T_0)]} \quad (2)$$

Where T_0 is the initial temperature of the circuit (room temperature), V_{BE0} is the VBE of transistors at the initial temperature, $\partial R/\partial T$ is the temperature coefficient of resistors and $\partial V_{BE}/\partial T$ is the temperature coefficient of the V_{BE} of transistors(for general -2.2mV/℃), The threshold temperature may be expressed as:

$$T_1 = T_0 + \frac{V_{REF} - 2V_{BE0} - (R_1 + R_2)I_{REF}}{(R_1 + R_2)\frac{\partial R}{\partial T}I_{REF} + 2\frac{\partial V_{BE}}{\partial T}} \quad (3)$$

When the circuit to achieve the threshold temperature, node OTP output low, so MN4 turns on, it effectively shorts resistor R1 to provide a deactivation temperature threshold that is different with the activation temperature threshold, the deactivation temperature threshold may be expressed as:

$$T_2 = T_0 + \frac{V_{REF} - 2V_{BE0} - R_2 I_{REF}}{R_2\frac{\partial R}{\partial T}I_{REF} + 2\frac{\partial V_{BE}}{\partial T}} \quad (4)$$

From (3) and (4), we can see that by adjusting the resistance R1 and R2, it can adjust the thermal shutdown temperature and the hysteresis temperature, when the R1 was shorted, $V_{REF} < V_{BE3}$ (node A).

Because of the limit of the technology model, the gate-source voltage of NMOS can not be higher than the 5V. When the voltage exceeds high, the parameters of NMOS have bad values, Fig. 5 is the simulation results gm of NMOS，we can see that when the V_{GS} of NMOS is changed, the value of gm changes evidently. In some case, NMOS works at linear region and it affects the function of circuit. This is not what we want to see. According to the design requirements of this article, it can be worked out that the highest voltage of node B can not be higher than 6V, so a shunt regulator circuit is increased to ensure the circuit works at higher voltages.

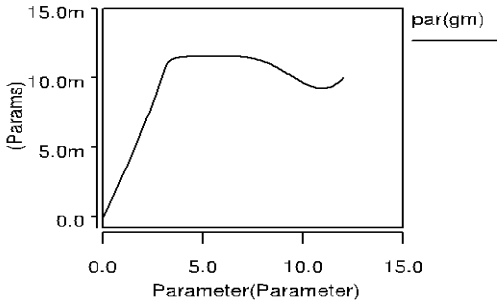

Fig.5. Simulation results gm of NMOS

IV. SIMULATION RESULTS

The proposed circuit has been designed and simulated in UMC 0.6um BiCMOS process.

Fig. 6 is the simulation results of shunt regulator circuit, we can see that the regulator circuit realization of the

functions of the circuit to ensure the thermal shutdown circuit at a higher supply voltage.

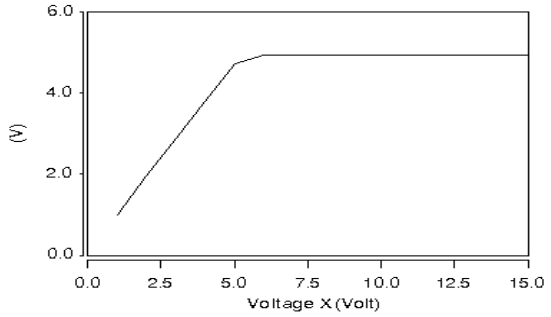

Fig.6. Simulation results of shunt regulator circuit

Fig. 7 is the simulation results of The PTAT and REF currents curve. It shows that when the temperature rises to 158℃,The PTAT current larger than the CTAT current and the thermal shutdown signal become down to zero.

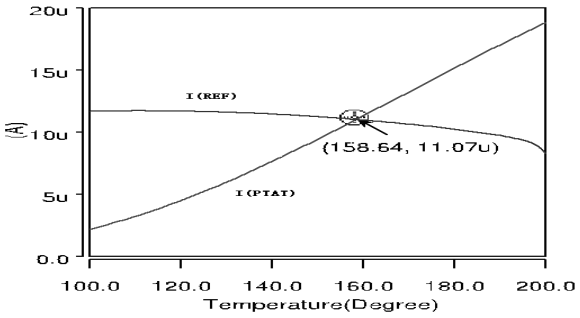

Fig.7. The PTAT and REF currents curve (V_{DD}=3.5*V*)

Fig. 8 shows when the circuit works at the 3.5V supply voltage, the temperature of the circuit for forward and reverse scan, node OTP output voltage changes, it can be seen in the temperature of 158℃, a vertical drop in output voltage, overheated after lag temperature of 29℃, the circuit began to work again and output high voltage. The circuit reflects a good on / off characteristic and has accurate turn-off and open the threshold and high temperature sensitivity.

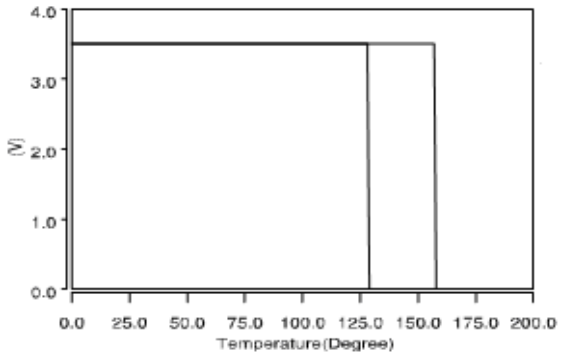

Fig.8. Temperature forward/reverse scan curve (V_{DD}=3.5*V*)

To simulate this circuit at a different process, the results as shown in table I, we can see the error between activation and deactivation temperature remained basically unchanged for 29℃ at different process corner.

TABLE I

SIMULATION RESULTS OF DIFFERENT PROCESS CORNER (V_{DD}=3.5*V*)

	TT	FF	SS
Activation temperature	158℃	159℃	158℃
Deactivation temperature	129℃	130℃	129℃

To simulate this circuit at a different power supply voltage, the results as shown in table II, when the power supply voltage from 2.5V to 12V, the error between activation and deactivation temperature remained basically unchanged for 29℃.Both in the low power supply voltage and high power supply voltage this circuit can work normally, it is very conducive to different power embedded chips and meet the needs of different design requirements. As the technology of simulation model restrictions, and taking into account the transistor and the bias of the normal work, the smallest power supply voltage should be 2V.

TABLE II
THE THERMAL SHUTDOWN TEMPERATURE AND THE TEMPERATURE LAG OPEN IN DIFFERENT SUPPLY VOLTAGES

V_{DD}	Activation temperature(℃)	Deactivation temperature(℃)	Error(℃)
2.5V	159	130	29
6V	157	128	29
8V	156	127	29
10V	156	127	29
12V	155	126	29

When the temperature does not meet the turn-off temperature, there is no current flow the core circuit, so power is very small. The simple structure of the circuit, which is ideal for integration in the internal power supply chips. Taking into account the supply voltage range of applications and accuracy, this circuit has a small area of layout, which is superior to [1]-[5].

V. CONCLUSION

In this paper, the over-temperature protection circuit is presented. This thermal-shutdown circuit has simple structure and low power dissipation. HSPICE simulation shows that the circuit has excellent capability of power supply rejection and can be operated in power supply range from 2V to 12V and as thermal shutdown module in the power management and the interface circuit chips.

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