LM200

T-41-38

- 240 dot (W) x 64 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see page 18).

MECHANICAL DATA (Nominal dimensions)

Module size	180W x 75H x 13.8T (max.) mm
Effective display area	132W x 39H mm
Number of dots	240W x 64H dot
Dot size	0.48W x 0.48H mm
Dot pitch	0.53W x 0.53H mm
Weight	about 150g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	13.5V
Input voltage (V_I)	V_{SS}	V_{DD}V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V±0.25V, V_{EE}=−5.0V±0.25V

Input "high" voltage (V_{IH})	0.7 x V_{DD}V min.
Input "low" voltage (V_{IL})	0.3 x V_{DD}Vmax.
Clock frequency (f_{CL2})	390 kHz min.
	460 kHz typ.
	520 kHz max.
Power supply current (I_{DD})	5mA typ.
(I_{EE})	3mA typ.
(D_1, D_2=GND, f_{CL2}=460 kHz)	
Power supply for LCD drive (Recommended) (V_O-V_{EE})	
	Duty = 1/32
Ta= 0°C	8.1 V typ.
Ta=25°C	7.4 V typ.
Ta=50°C	6.5 V typ.

OPTICAL DATA ..... See page 5

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data
2	FLM	H	The FLM signal indicates the beginning of each display cycle.
3	M	H/L	Control signal for a.c. driving
4	CL1	H→L	The CL1 latches the serial data in the shift registers.
5	CL2	H→L	Clock signal for shifting the serial data
6	D2	H/L	Serial row data
7	V_{DD}(+5V)	–	Power supply for logic circuit
8	V_{SS}(GND)	–	Ground
9	V_{EE}(−5V)	–	Power supply for LC driving
10	V_O	–	Operating voltage for LC driving

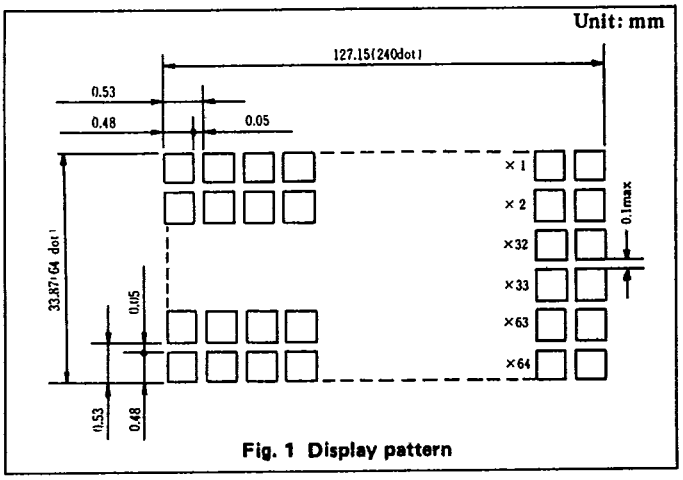


Fig. 1 Display pattern

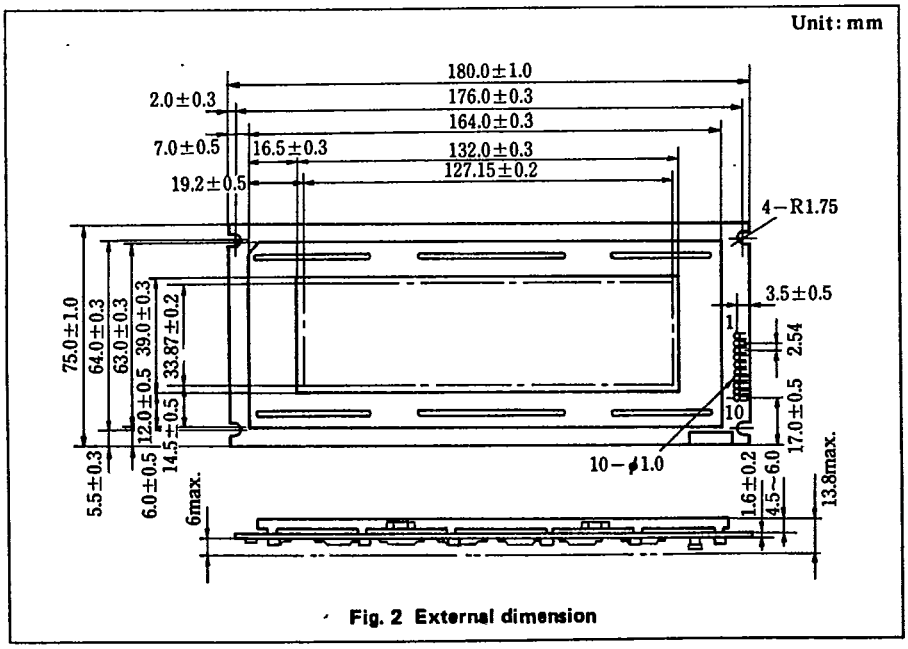


Fig. 2 External dimension

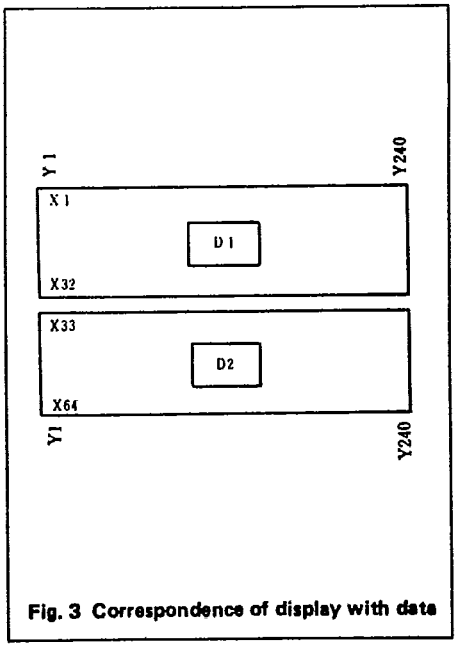


Fig. 3 Correspondence of display with data

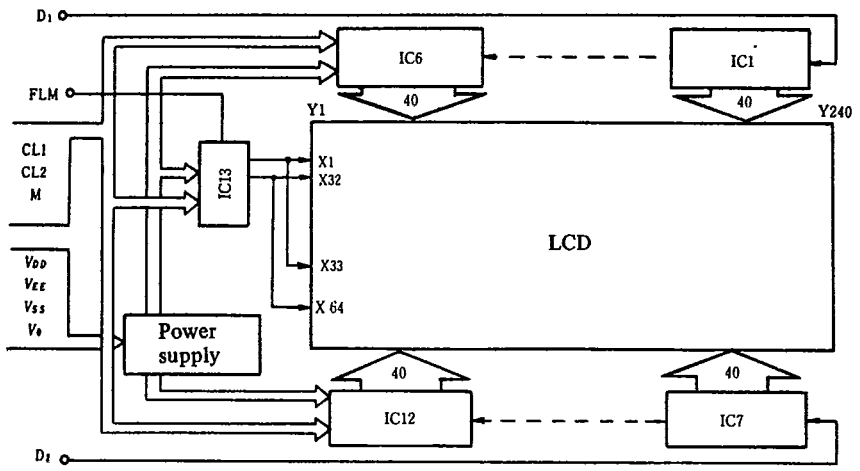
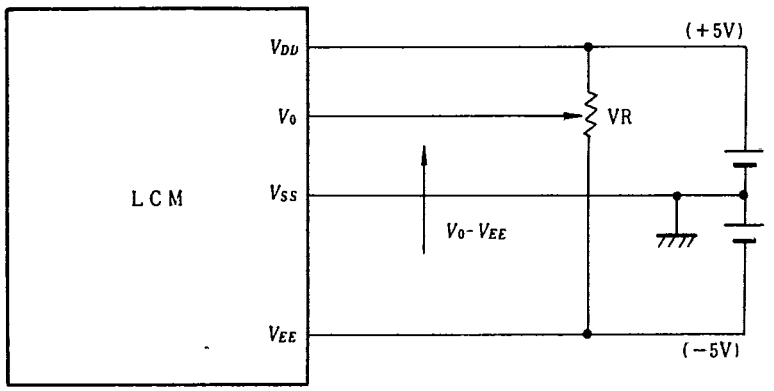


Fig. 4 Block diagram



V_O-V_{EE}: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 5 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CL2}	–	–	520	kHz (Note 1)
Clock pulse width (High level)	t_{CWH}	800	–	–	ns
Clock pulse width (Low level)	t_{CWL}	800	–	–	ns
Clock set up time	t_{CSU}	500	–	–	ns
Data set up time	t_{SU}	300	–	–	ns
FLM set up time	t_{FSU}	300	–	–	ns
M delay time	t_{DM}	−1000	0	+1000	ns (Note 2)
FLM hold time	t_{FH}	0	–	–	ns
Data hold time	t_{DH}	300	–	–	ns

Notes 1. Optimum frequency for the highest contrast depends on the type of module.
2. Timing of M signal to CL1 may be in the range of ±1000ns.
3. In adjusting FLM frequency, avoid setting it around the commercial frequency (50 Hz ±2 Hz or 60 Hz ±2 Hz) to prevent LCD flicker.

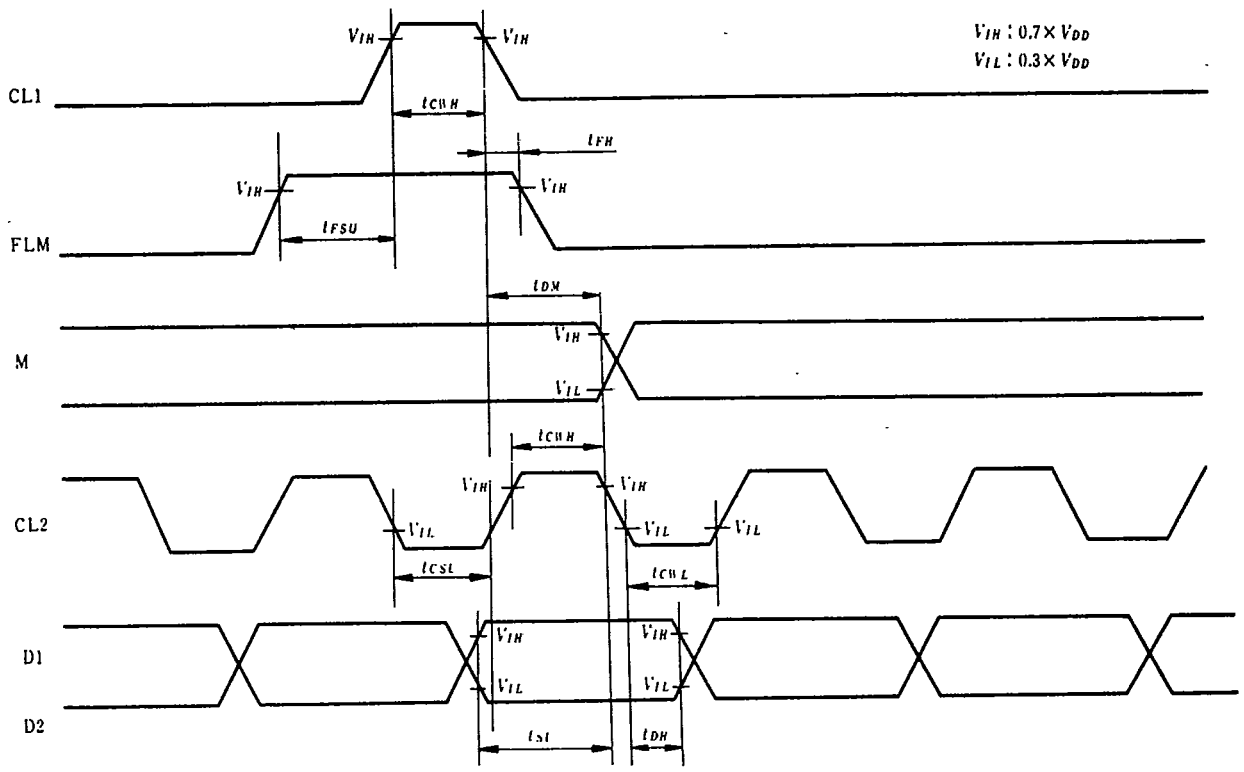


Fig. 6 Interface timing (data write)

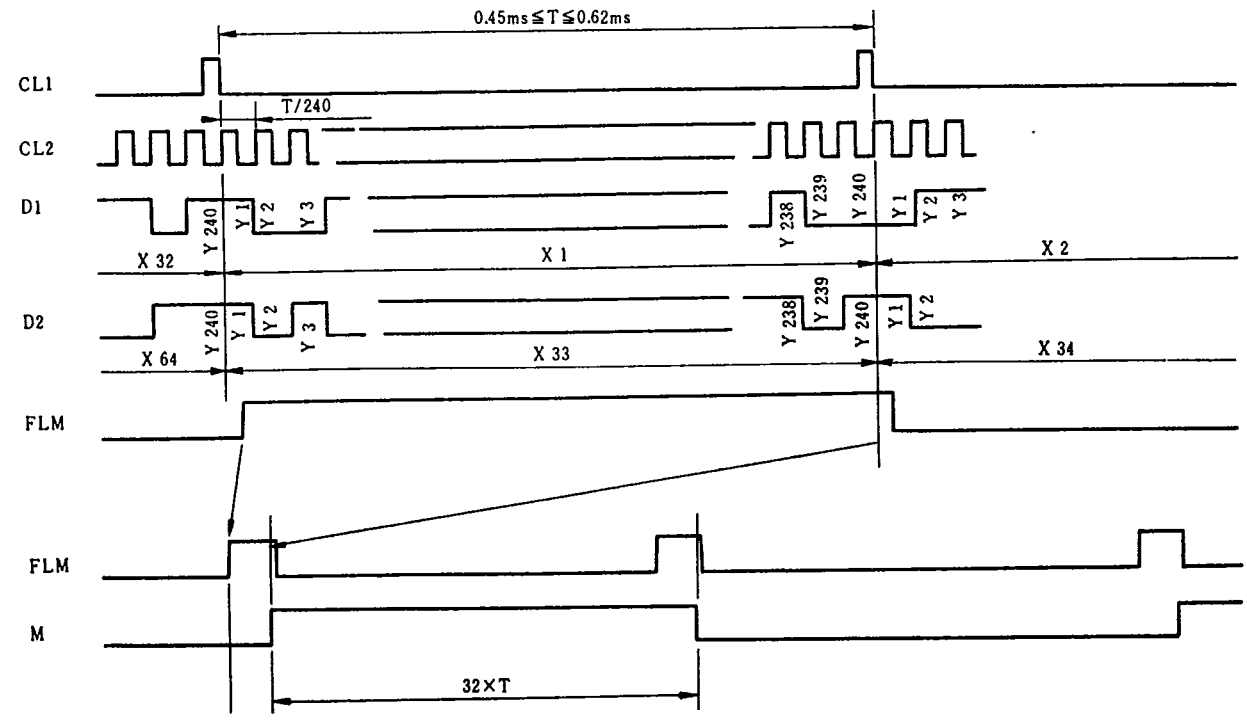


Fig. 7 Interface timing