UM9228-1

Floppy Data Separator

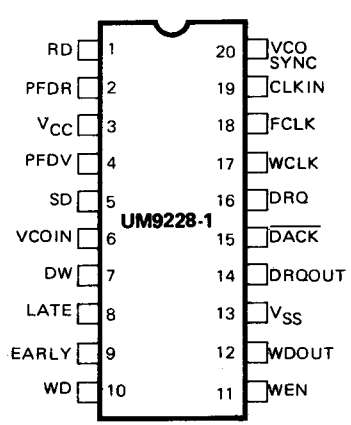
Features

- Complete data separation function with external circuit for floppy disk drives
- Separation of MFM encoded data
- 5¼" double density separation of compatible
- Early and late 250-ns write precompensation
- External 16-MHz clock required
- Compatible with FDC 765A (8272A) floppy disk controllers
- DMA interface logic
- CMOS technology
- Single + 5 Volt supply
- TTL-compatible
- Designed for IBM PC disk drives

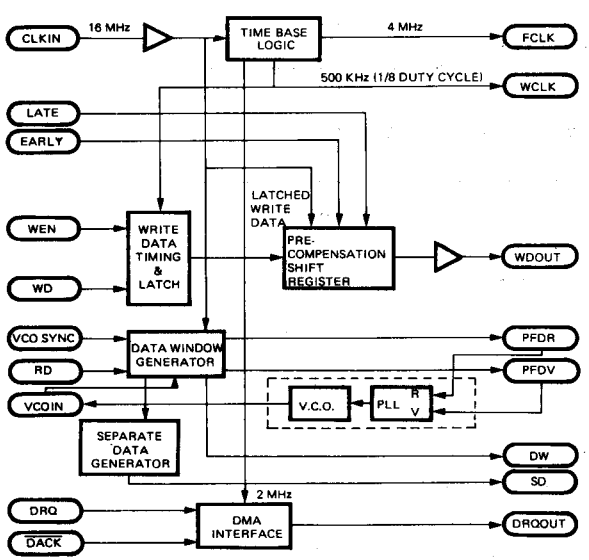
General Description

The UM9228-1 is a CMOS integrated circuit designed to complement the 765A (8272A) type of floppy disk controller chip, especially for the IBM PC. It incorporates a data separator, write precompensation logic, and DMA interface logic. A FDC 765A together with UM9228-1 and buffer drive and decoder can form a IBM PC diskette adapter. The UM9228-1 operates from a +5 Volt supply and simply requires a 16-MHz external clock input. All input and output are TTL-compatible. The UM9228-1 is available for 5¼" double density disk controller.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Ambient temperature under bias, T_A . . . . . 0 to + 70°C
Storage temperature, T_{STG} . . . . . –55 to + 125°C
Applied voltage on any pin with respect to ground
. . . . . –0.3 to + 8V
Power dissipation, P_D 0.5W

*Comments

Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

D.C. Electrical Characteristics

(T_A = 0 to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.)

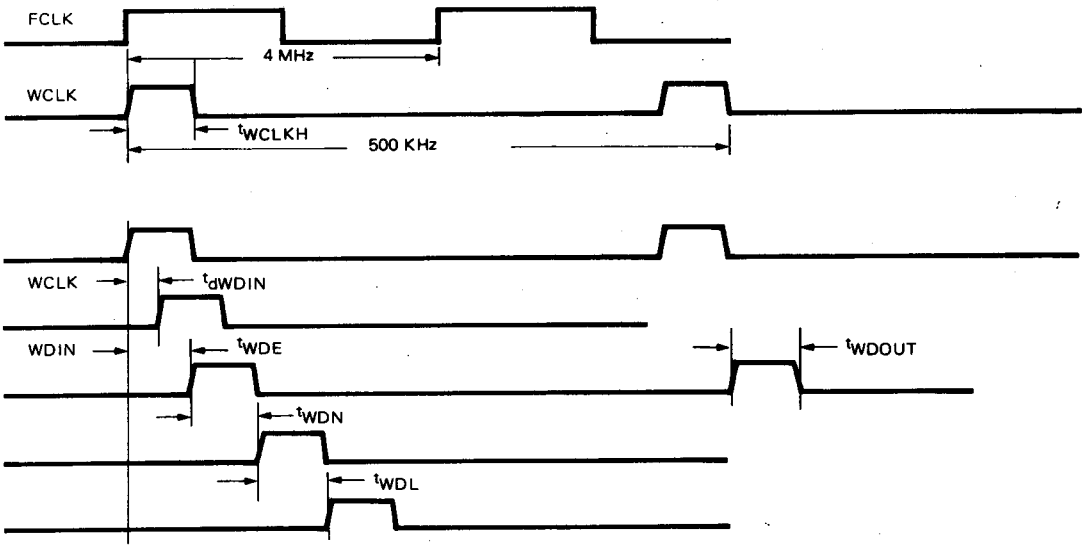
Parameter	Test Conditions	Limits			Units
		Min.	Typ.	Max.	
Input Voltage Low Level V_{IL} High Level V_{IH}		–0.3 2.0		0.8 V_{CC}	V V
Standby Current I_{ST}				10	μA
Input Current (for all input) Low Level I_{IL} High Level I_{IH}	 V_{IH} = 2.7V V_{IL} = 0.4V			 –200 20	 μA μA
Output Current (for all output) Low Level I_{OL} High Level I_{OH}	 V_{OL} = 0.4V V_{OH} = 4.5V	 4 –500			 mA μA
Power Supply Current I_{CC}	CLKIN = 16 MHz VCOIN = 4 MHz			10	mA
Input Leakage Current I_{IL}				10	μA
Input Capacitance C_{IN}				10	pF

A.C. Electrical Characteristics

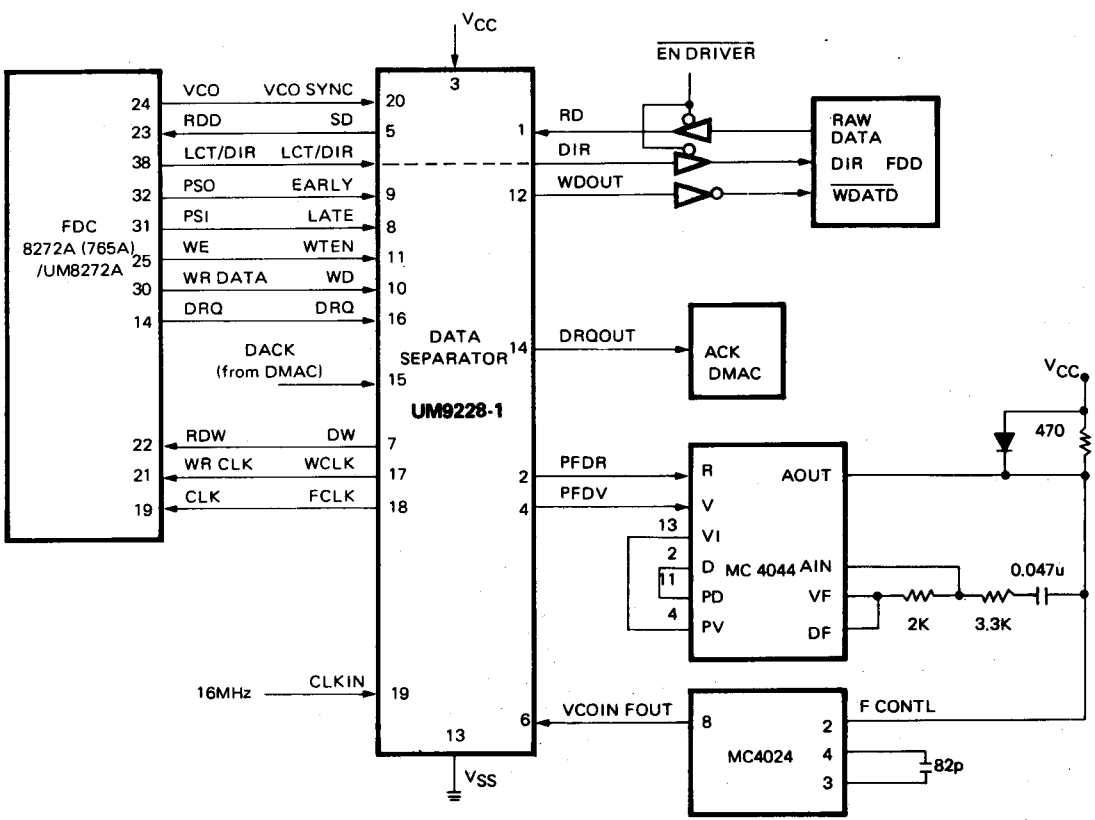
(T_A = 0 to 70°C, V_{CC} = 5V ± 5%, CLKIN = 16 MHz, VCOIN = 4 MHz)

Parameter	Limits			Units
	Min.	Typ.	Max.	
CLKIN frequency	1		16	MHz
VCOIN frequency	0		4	MHz
VCOIN DUTY CYCLE	30	50	70	%
DRQ to DRQOUT Delay t_{dDRQ}			2.0	μs
t_{WCLKH}		250		ns
t_{WDOUT}		250		ns
t_{dWDIN}	0		200	ns
t_{WDE}		250		ns
t_{WDN}		250		ns
t_{WDL}		250		ns

Precompensation



Application Circuits



Pin Description

Pin No.	Symbol	I/O	Descriptions
1	RD	I	Read Data from FDD.
2	PFDR	O	Reference Data Sample Pulse. This signal is applied to the reference input of a PLL circuit. See block diagram.
3	V_{CC}	I	+5 Volt power supply
4	PFDV	O	This output is connected to an input of a PLL circuit. See block diagram.
5	SD	O	Separate Data: This output is the generated data pulse derived from the RD input.
6	VCOIN	I	This signal is the V.C.O. output of a PLL circuit used to generate data window.
7	DW	O	Data Window: This is derived from RD input to be applied to FDC.
8	LATE	I	See Fig. 3.
9	EARLY	I	See Fig. 3.
10	WD	I	Write Data: The write data stream from the floppy disk controller.
11	WEN	I	Write Enable: This input is from FDC starting the write operation.
12	WDOUT	O	Write Data Output: The precompensated write data stream to the drive.
13	V_{SS}	I	Ground
14	DRQOUT	O	Data Request Output: Delayed DRQ signal from FDC.
15	$\overline{DACK}$	I	DMA Acknowledge: Direct memory access acknowledge from DMA controller.
16	DRQ	I	DMA Request: This is high when FDC make a DMA request.
17	WCLK	O	Write Clock: This signal is the write clock to the floppy disk controller.
18	FCLK	O	FDC Clock: This output is the master clock to the floppy disk controller.
19	CLKIN	O	Clock Input: This input is connected to a external 16-MHz clock input.
20	VCC SYNC	I	This is connected to VCO output pin of FDC 765.

Operational Description

DATA SEPARATOR

UM9228-1 is used with a external PLL circuit (see Fig. 1) to detect the leading edges of the disk data pulse and adjust the phase of the internal clock to provide the data window (DW) clock.

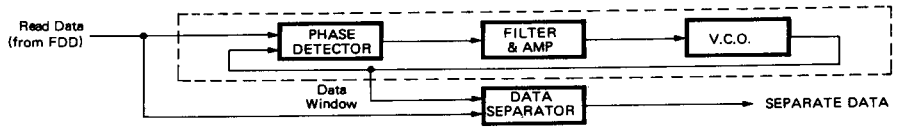


Figure 1. Data Windown Generator

The data window clock frequency is normally 250 KHz. See Fig. 2.

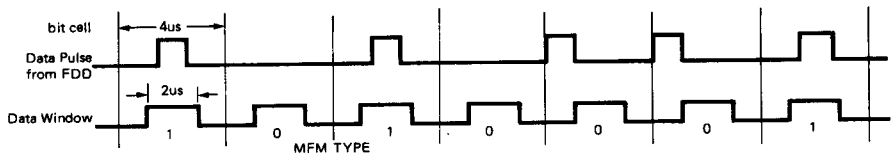
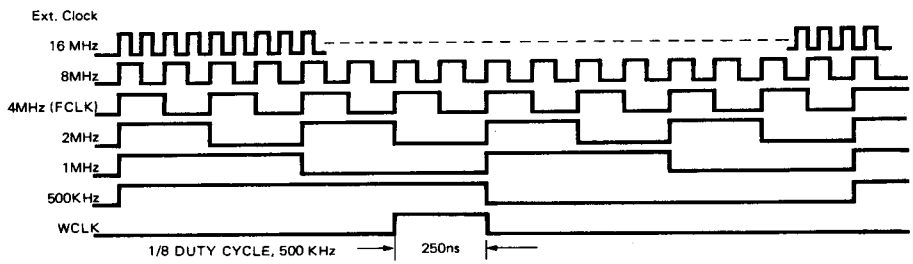


Figure 2. Data Window

TIME BASE LOGIC

This comprises 5 stages of ripple counter and a duty cycle clamping circuit. The write clock (WCLK) duty cycle is 1/8.



WRITE PRECOMPENSATION

The desired precompensation delay (250 ns) is determined by the state of EARLY and LATE inputs of UM9228-1.

	Early	Late
Nominal	0	0
Late	0	1
Early	1	0
Invalid	1	1

Figure 3. Write Precompensation State

DMA INTERFACE

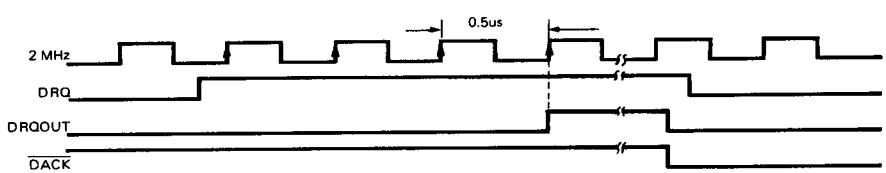


Figure 4. DMA Interface Timing

When requiring data read/write, FDC will check $\overline{\text{DACK}}$ from DMAC and will set DRQ (low to high) if $\overline{\text{DACK}}$ is high. The timing of the DMA Interface delay DRQ from FDC by 4-stage shift register is as shown above. This delay will prevent cpu from doing DMA without adequate system operation.