TOSHIBA MOS MEMORY PRODUCTS

65,536 WORD×4 BIT DYNAMIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM41464AP/AT/AZ-10, TMM41464AP/AT/AZ-12
TMM41464AP/AT/AZ-15

DESCRIPTION

The TMM41464AP/AT/AZ is N-channel dynamic RAM organized 65,536 words by 4 bit. The TMM41464 AP/AT/AZ utilizes TOSHIBA's N-channel/Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TMM41464AP/AT/AZ to be package in a standard 18 pin plastic DIP, 18 pin PLCC and 20 pin ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic familes such as schottky TTL.

FEATURES

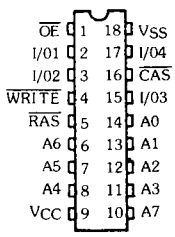
- 65,536 words by 4 bit organization
- Fast access time and cycle time

DEVICE	tRAC	tCAC	tRC
TMM41464AP/AT/AZ-10	100ns	50ns	190ns
TMM41464AP/AT/AZ-12	120ns	60ns	220ns
TMM41464AP/AT/AZ-15	150ns	75ns	260ns

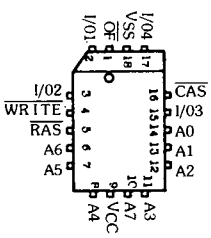
- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Lower Power:
  440mW MAX. Operating (TMM41464AP/AT/AZ-10)
  396mW MAX. Operating (TMM41464AP/AT/AZ-12)
  358mW MAX. Operating (TMM41464AP/AT/AZ-15)
  28mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{RAS}$ only refresh, Hidden refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, and Page Mode capability
- All inputs and outputs TTL compatible
- 256 refresh cycles/4ms
- Package
  Plastic DIP : TMM41464AP
  Plastic Leaded Chip Carrier : TMM41464AT
  Plastic ZIP : TMM41464AZ

PIN CONNECTION

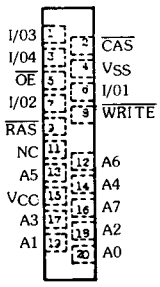
TMM41464AP



TMM41464AT



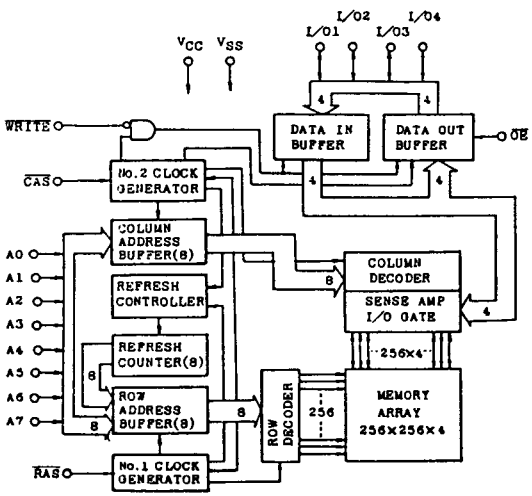
TMM41464AZ



PIN NAMES

A0 ~ A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
I/01 ~ I/04	Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	
Operating Temperature	T_{OPR}	0 ~ 70	°C	
Storage Temperature	T_{STG}	−55 ~ 150	°C	
Soldering Temperature•Time	T_{SOLDER}	260•10	°C•sec	
Power Dissipation	P_D	1	W	
Short Circuit Output Current	I_{OUT}	50	mA	

RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TMM41464AP/AT/AZ-10	–	80	mA	3, 4
		TMM41464AP/AT/AZ-12	–	72		
		TMM41464AP/AT/AZ-15	–	65		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	5	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} MIN.)	TMM41464AP/AT/AZ-10	–	70	mA	3
		TMM41464AP/AT/AZ-12	–	62		
		TMM41464AP/AT/AZ-15	–	55		
I_{CC4}	PAGE MODE CURRENT Average Power Supply Current, Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling: t_{PC} = t_{PC} MIN.)	TMM41464AP/AT/AZ-10	–	60	mA	3, 4
		TMM41464AP/AT/AZ-12	–	55		
		TMM41464AP/AT/AZ-15	–	50		
I_{CC5}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$: t_{RC} = t_{RC} MIN.)	TMM41464AP/AT/AZ-10	–	70	mA	3
		TMM41464AP/AT/AZ-12	–	62		
		TMM41464AP/AT/AZ-15	–	55		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Unter Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ + 5.5V)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41464AP/AT/AZ-10		TMM41464AP/AT/AZ-12		TMM41464AP/AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190	–	220	–	260	–	ns	
t_{RMW}	Read-Modify Write Cycle Time	260	–	300	–	355	–	ns	
t_{PC}	Page Mode Cycle Time	100	–	120	–	145	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	100	–	120	–	150	ns	8, 10
t_{CAC}	Access Time from $\overline{CAS}$	–	50	–	60	–	75	ns	9, 10
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	35	0	40	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	80	–	90	–	100	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	50	–	60	–	75	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	100	–	120	–	150	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	50	10,000	60	10,000	75	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	60	25	75	ns	13
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	20	–	20	–	25	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	40	–	50	–	60	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	15	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	20	–	25	–	35	–	ns	
t_{AR}	Column Address Hold Time Reference to $\overline{RAS}$	70	–	85	–	110	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$	0	–	0	–	0	–	ns	12
t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	10	–	15	–	20	–	ns	12
t_{WCH}	Write Command Hold Time	30	–	35	–	45	–	ns	
t_{WCR}	Write Command Hold Time Reference to $\overline{RAS}$	80	–	95	–	120	–	ns	
t_{WP}	Write Command Pulse Width	30	–	35	–	45	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30	–	35	–	45	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30	–	35	–	45	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	14
t_{DH}	Data-In Hold Time	30	–	35	–	45	–	ns	14
t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	80	–	95	–	120	–	ns	
t_{REF}	Refresh Period	–	4	–	4	–	4	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	ns	15
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	85	–	100	–	120	–	ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	135	–	160	–	195	–	ns	15
t_{OEA}	$\overline{OE}$ Access Time	–	25	–	30	–	40	ns	9, 10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TMM41464AP/AT/AZ-10		TMM41464AP/AT/AZ-12		TMM41464AP/AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{OED}	$\overline{OE}$ to Data Delay	25	–	30	–	40	–	ns	
t_{OEZ}	Output Buffer Turn-Off Delay Time from $\overline{OE}$	0	25	0	30	0	40	ns	
t_{OEH}	$\overline{OE}$ command Hold Time	25	–	30	–	40	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	30	–	30	–	30	–	ns	
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	10	–	10	–	10	–	ns	
t_{RPC}	$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	20	–	25	–	35	–	ns	
t_{ROH}	$\overline{OE}$ Command Hold Time	10	–	10	–	10	–	ns	

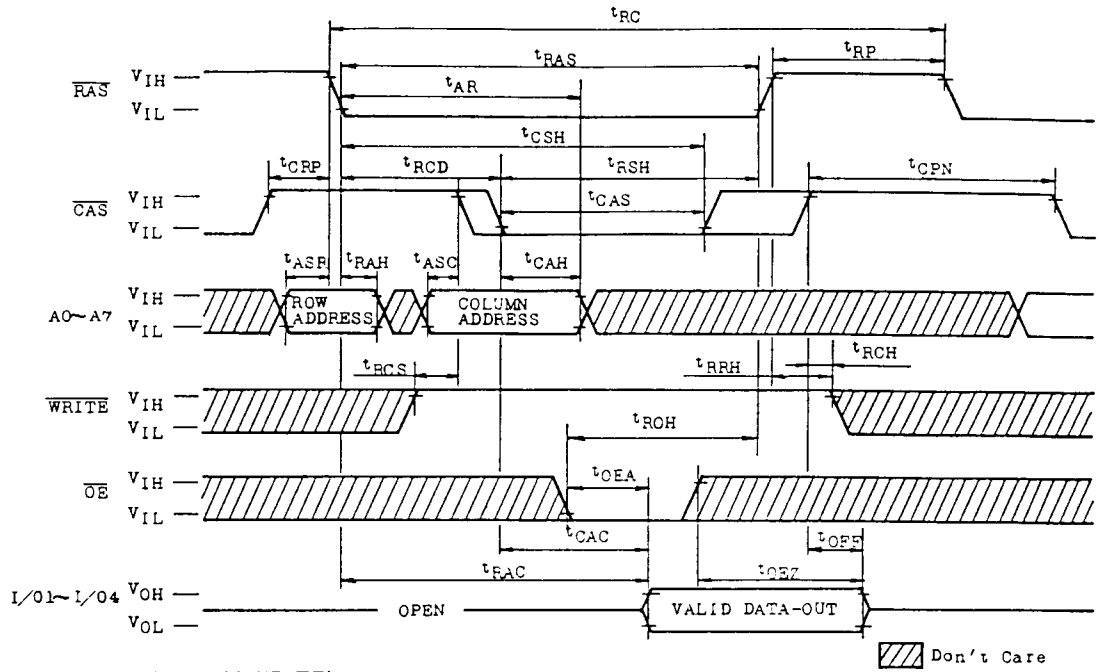
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
CI1	Input Capacitance (A0 ~ A7)	—	5	pF
CI2	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	—	7	
C_O	Input/Output Capacitance (I/01 ~ I/04)	—	7	

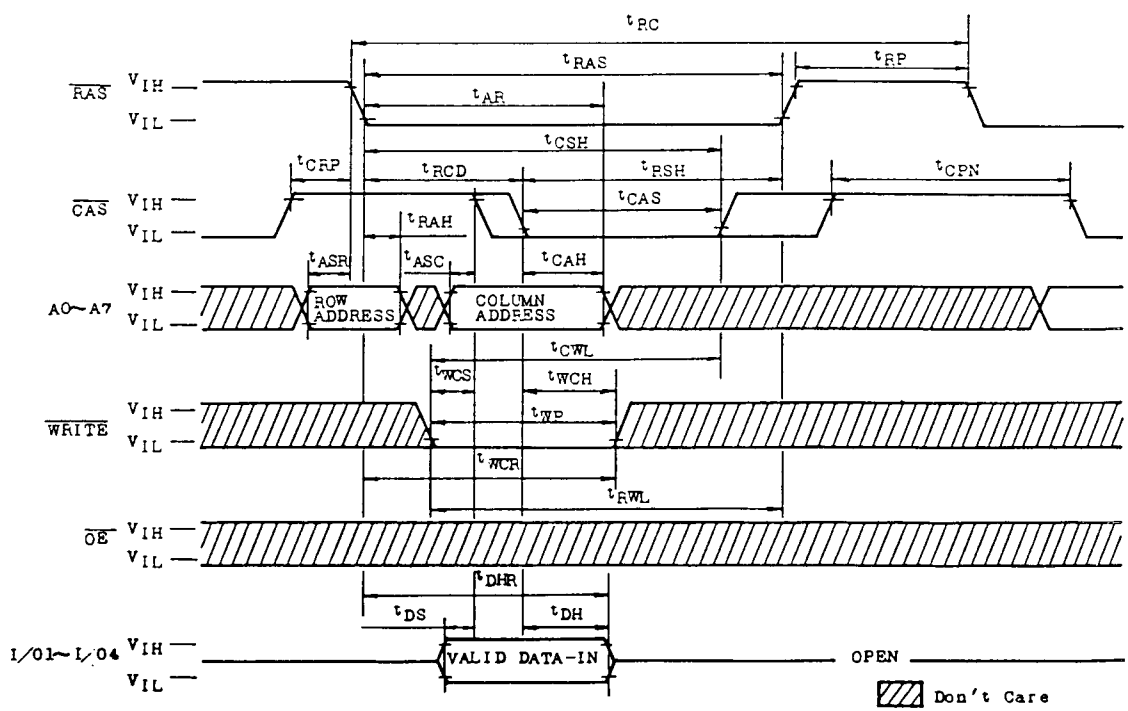
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T = 5 ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max.).
10. Measured with a load equivalent to 2 TTL loads and 100 pF.
11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the input/output pin will remain open circuits (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

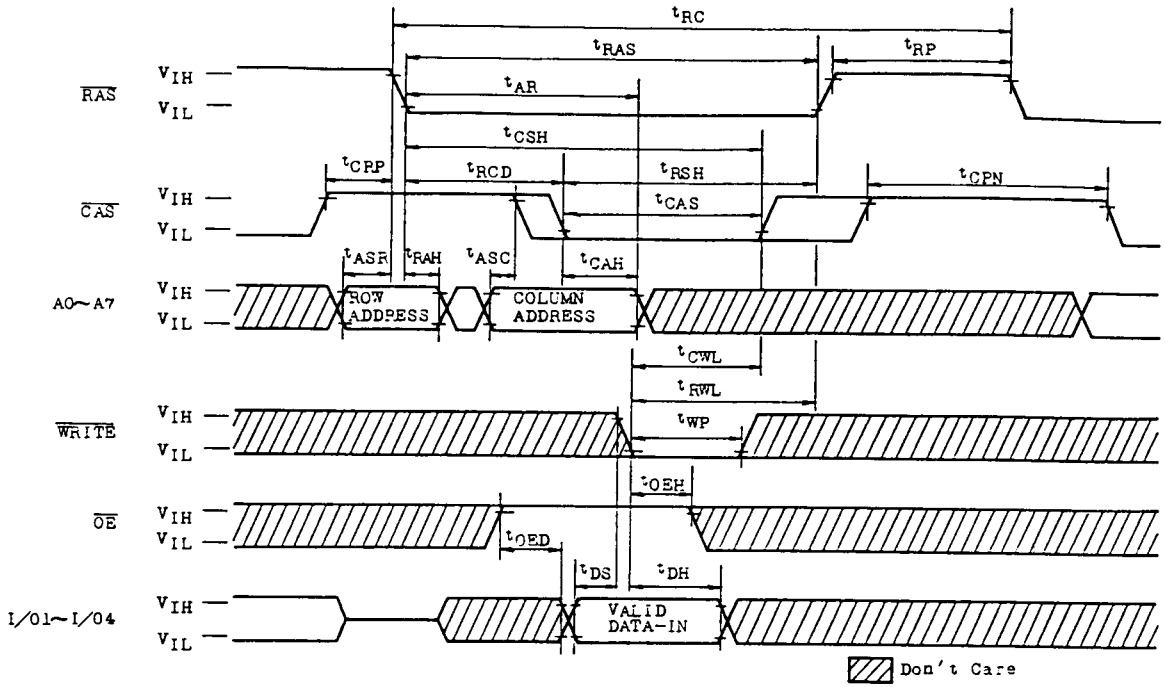
- READ CYCLE



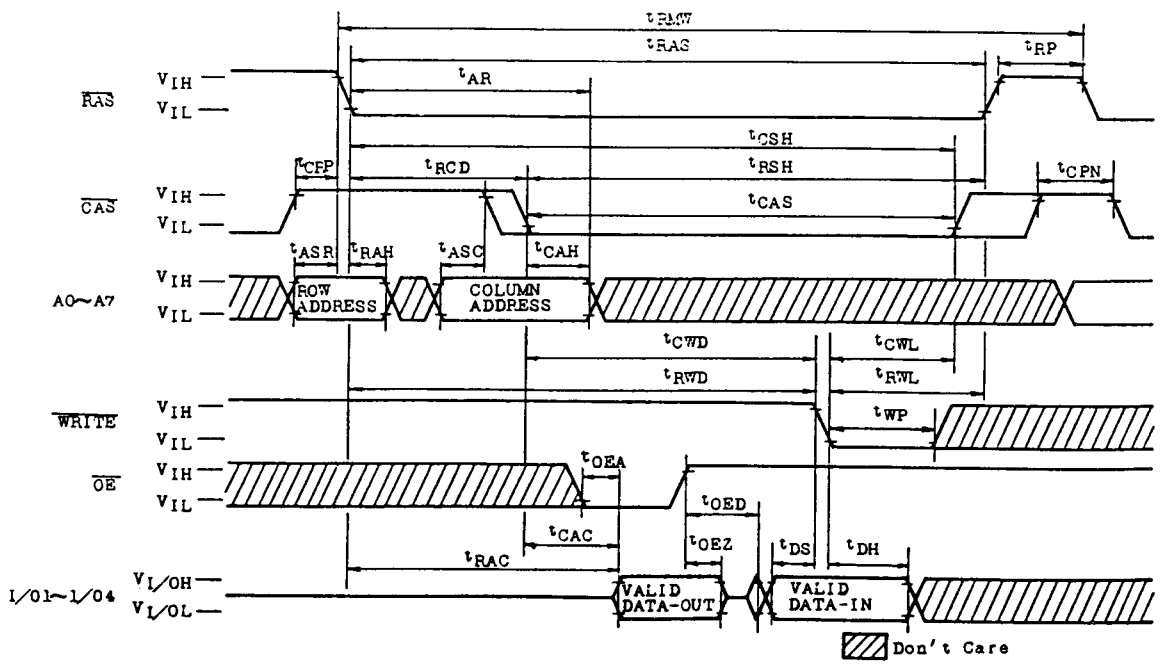
- WRITE CYCLE (EARLY WRITE)



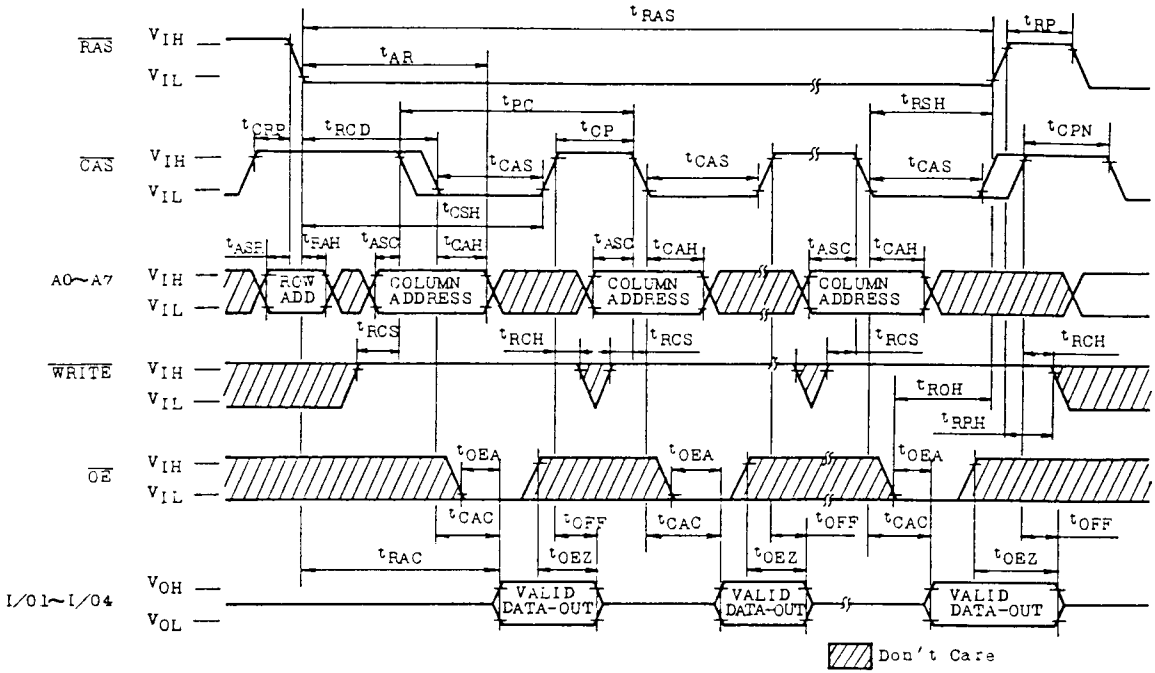
- WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



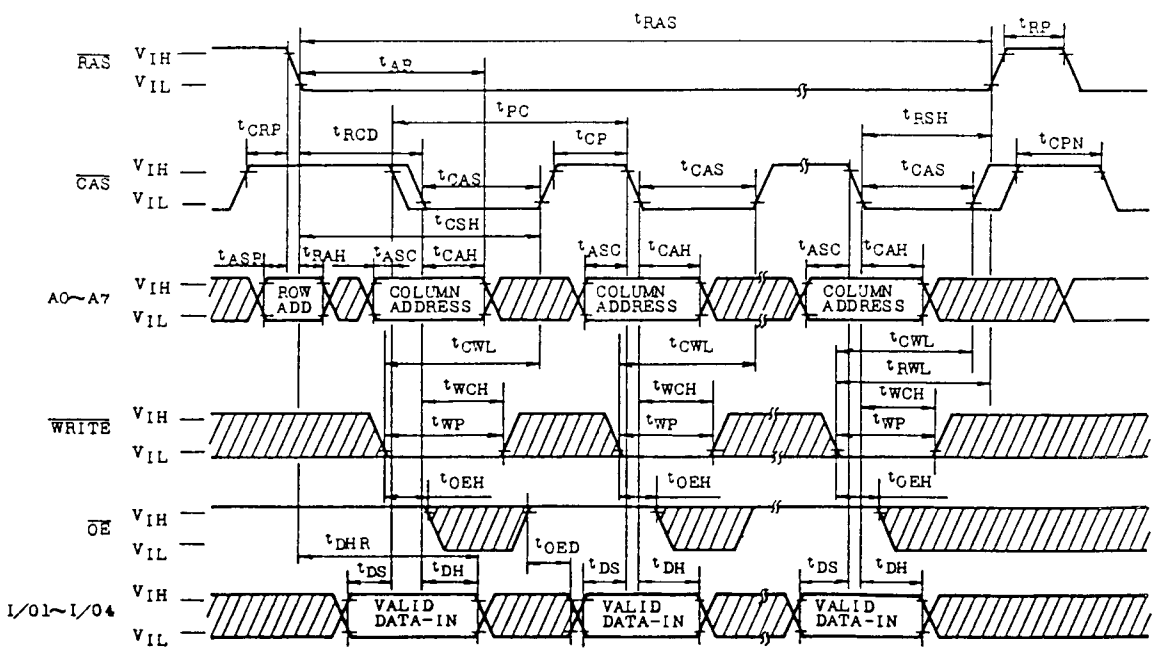
- READ-WRITE/READ-MODIFY-WRITE CYCLE



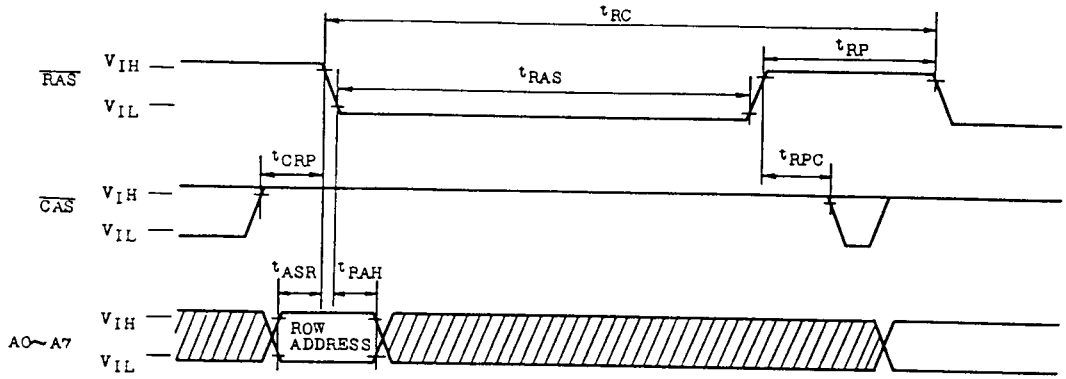
- PAGE MODE READ CYCLE



- PAGE MODE WRITE CYCLE

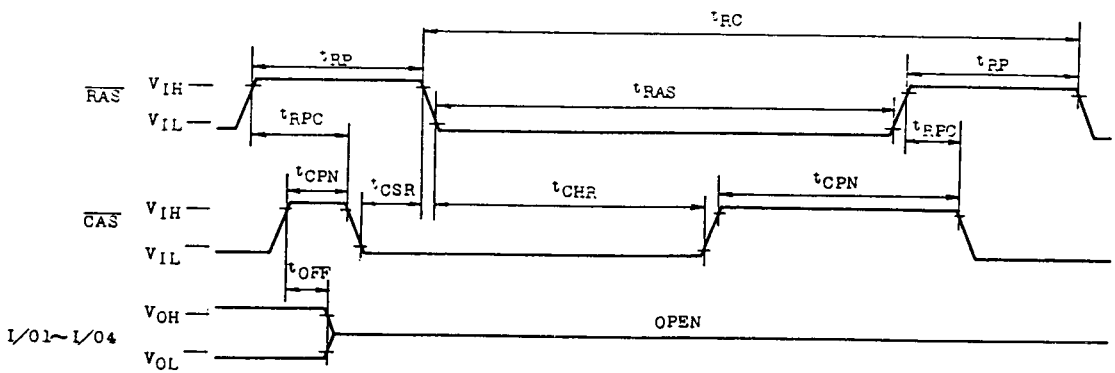


- $\overline{RAS}$ ONLY REFRESH CYCLE



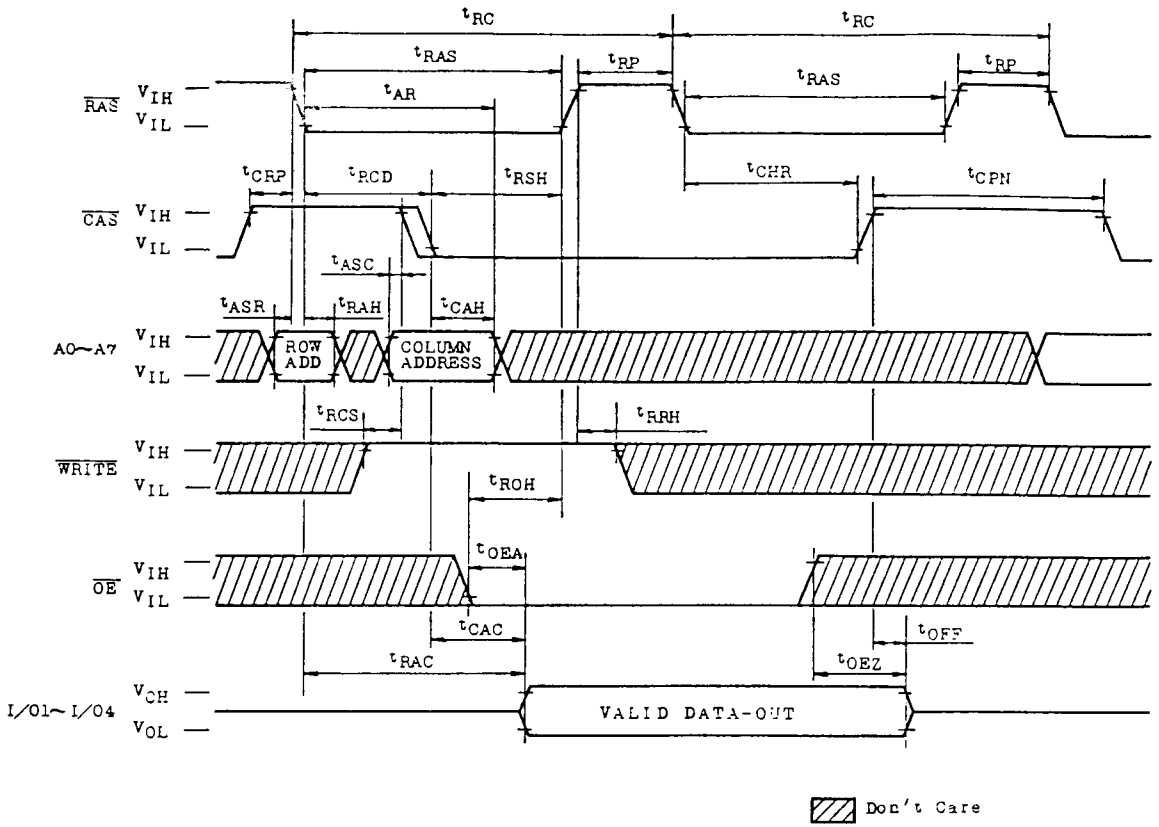
Notes: $\overline{WRITE}$, $\overline{OE}$=Don't Care Don't Care

- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

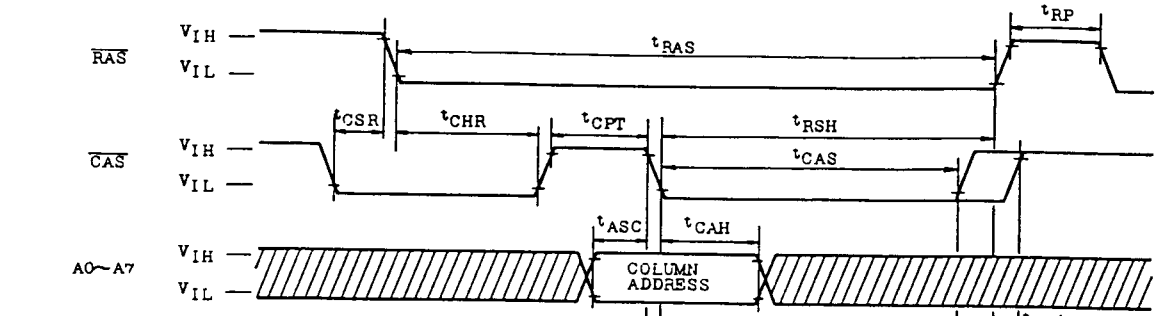


Note: $\overline{WRITE}$, $\overline{OE}$, A0 ∿ A7=Don't Care

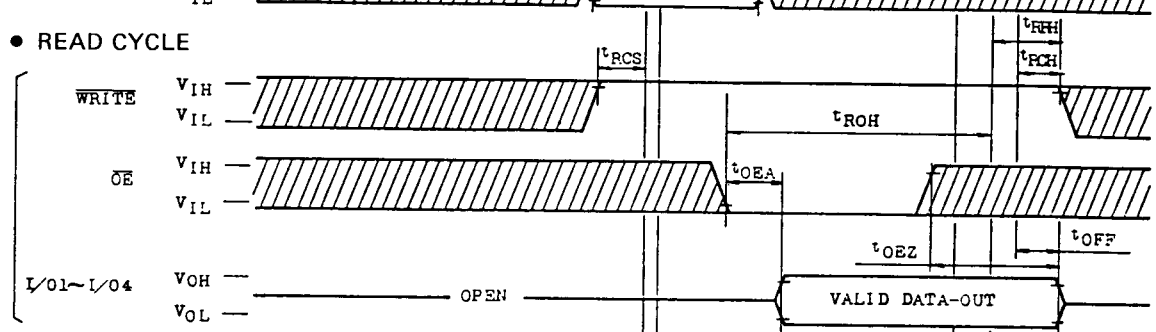
- HIDDEN REFRESH CYCLE



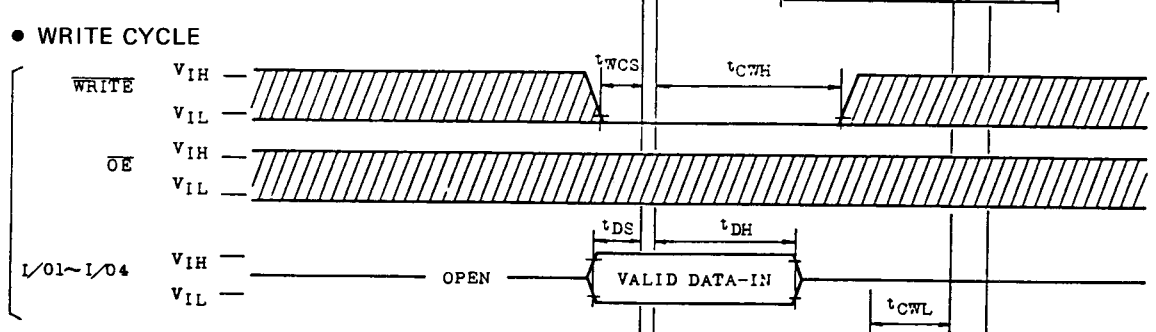
- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



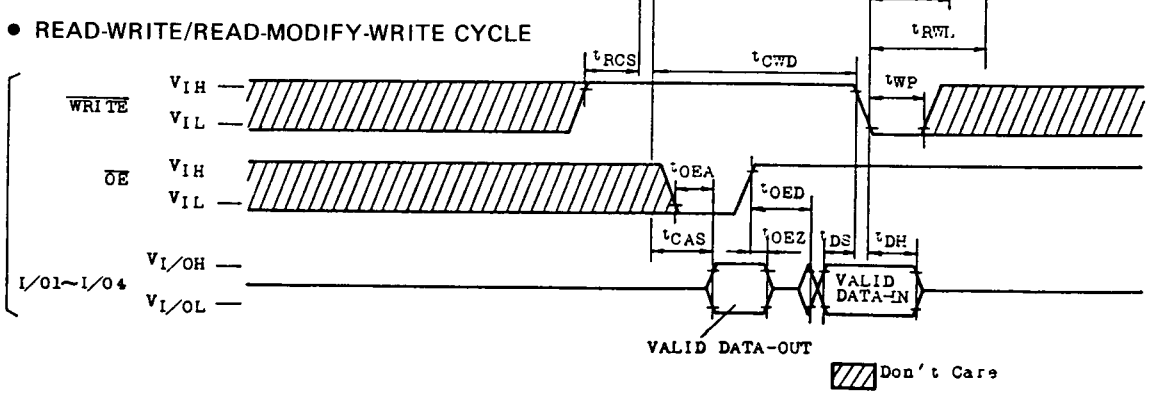
- READ CYCLE



- WRITE CYCLE



- READ-WRITE/READ-MODIFY-WRITE CYCLE



APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TMM41464AP/AT/AZ are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

Data is written during a write or read-modify-write cycle.

The falling edge of $\overline{CAS}$ or $\overline{WRITE}$ strobes data into the on-chip data latches. In an early-write cycle, $\overline{WRITE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WRITE}$ with setup and hold times referenced to this signal.

In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffer to high impedance prior to impressing data on the I/O lines.

Data Outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid which $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logic low level, the output buffer are enabled. Both $\overline{CAS}$ and OE can control the output. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address ($A_0 \sim A_7$) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TMM41464AP/AT/AZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

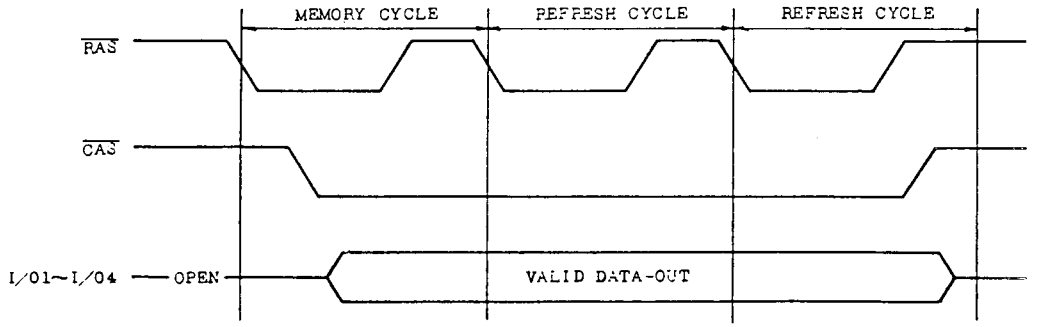
PAGE MODE

The "Page-Mode" feature of the TMM41464AP/AT/AZ allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the

chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TMM41464AP/AT/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of TMM41464AP/AT/AZ can be tested by $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 256 times.

③ Check "1" out of 256 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. Repeat this operation 256 times.

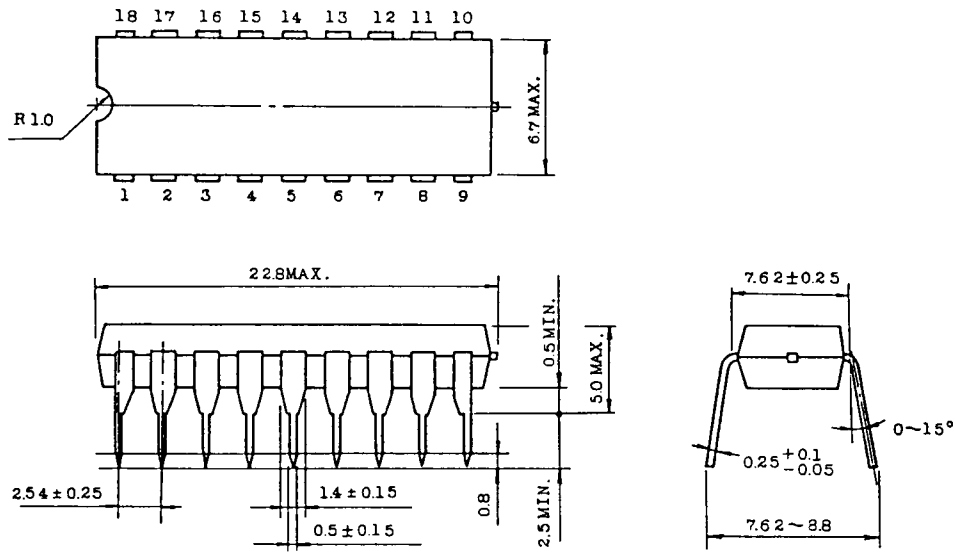
⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ to the complement data.

OUTLINE DRAWINGS

- Plastic DIP

Unit in mm

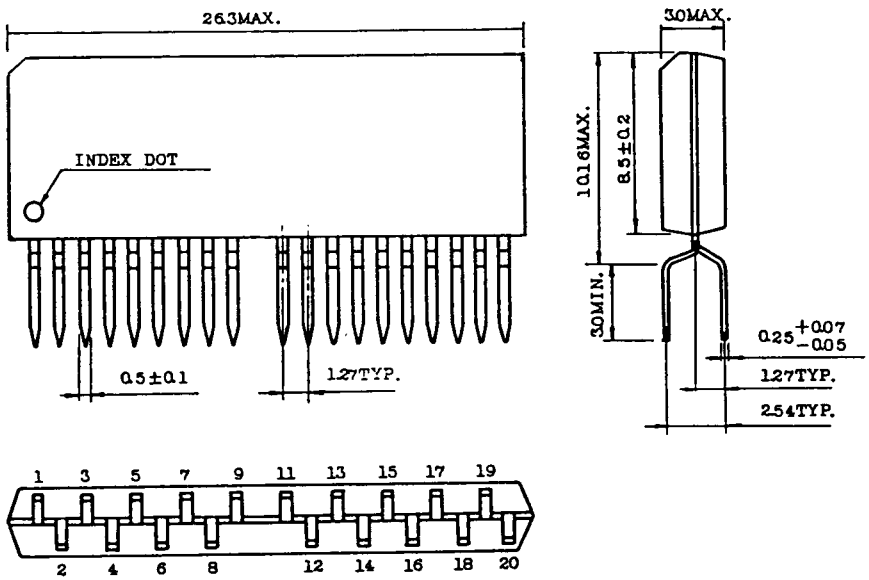


Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

- Plastic ZIP

Unit in mm



- Plastic LCC

Unit in mm