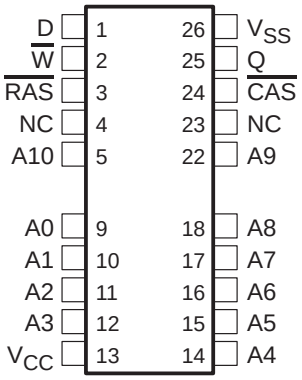
- **Organization . . . 4194304 × 1**
- **Single 5 V Power Supply, for TMS44100/P (±10% Tolerance)**
- **Single 3.3 V Power Supply, for TMS46100/P (±10% Tolerance)**
- **Low Power Dissipation (TMS46100P only)**
  - **200-μA CMOS Standby**
  - **200-μA Self Refresh**
  - **300-μA Extended-Refresh Battery Backup**
- **Performance Ranges:**

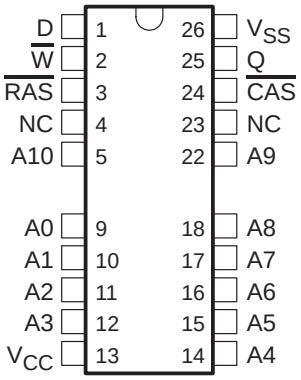
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
'4x100/P-60	60 ns	15 ns	30 ns	110 ns
'4x100/P-70	70 ns	18 ns	35 ns	130 ns
'4x100/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page-Mode Operation for Faster Memory Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  - **1024-Cycle Refresh in 16 ms**
  - **128 ms (Max) for Low-Power, Self-Refresh Version (TMS4x100P)**
- **3-State Unlatched Output**
- **Texas Instruments EPIC™ CMOS Process**
- **Operating Free-Air Temperature Range 0°C to 70°C**

DGA PACKAGE (TOP VIEW)



DJ PACKAGE (TOP VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V or 3.3-V Supply
V_{SS}	Ground

ADVANCE INFORMATION

description

The TMS4x100 series are high-speed, 4194304-bit dynamic random-access memories, organized as 4194304 words of one bit each. The TMS4x100P series are high-speed, low-power, self-refresh with extended-refresh, 4194304-bit dynamic random-access memories, organized as 4194304 words of one bit each. Both series employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low voltage.

DEVICE	POWER SUPPLY	SELF-REFRESH BATTERY BACKUP	REFRESH CYCLES
TMS44100	5 V	—	1024 in 16 ms
TMS44100P	5 V	YES	1024 in 128 ms
TMS46100	3.3 V	—	1024 in 16 ms
TMS46100P	3.3 V	YES	1024 in 128 ms

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4x100 and TMS4x100P are offered in a 20-/26-lead plastic surface-mount small-outline (TSOP) package (DGA suffix) and a 300-mil 20-/26-lead plastic surface-mount SOJ package (DJ suffix). Both packages are characterized for operation from 0°C to 70°C.

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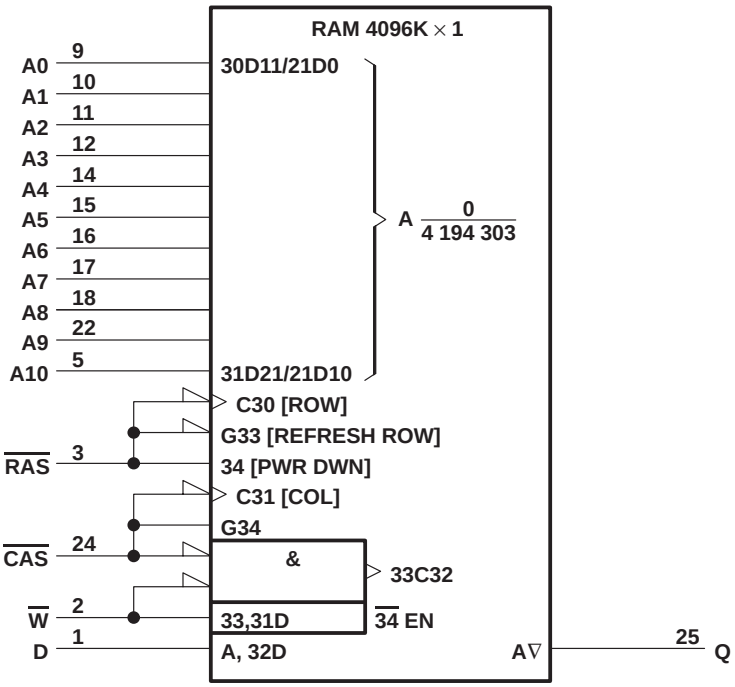
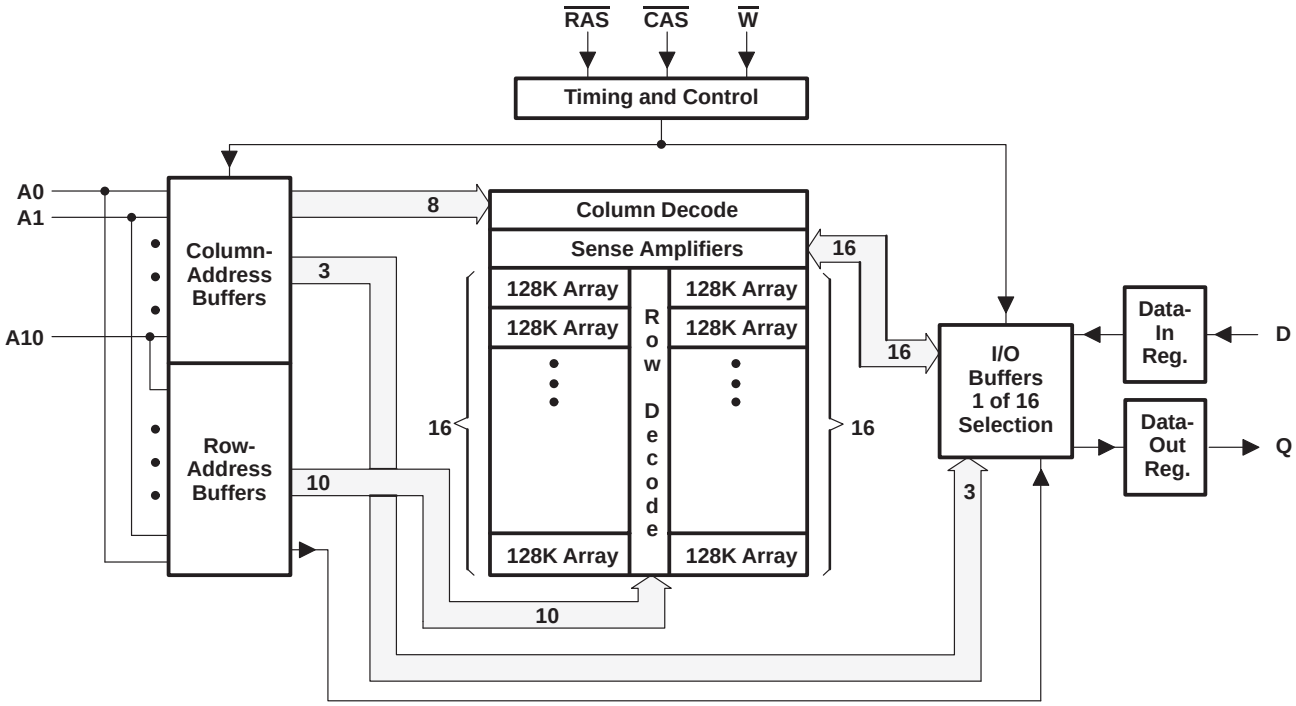
ADVANCE INFORMATION

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS4x100 to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. If column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0 – A10)

Twenty-two address bits are required to decode 1 of 4194304 storage cell locations. Eleven row-address bits are set up on inputs A0 through A10 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The eleven column-address bits are set up on A0 through A10 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. $\overline{W}$ can be driven from standard TTL circuits (TMS44100/P) or low-voltage TTL circuits (TMS46100/P) without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-write cycle, $\overline{CAS}$ is already low and the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{CAS}$) as long as t_{RAC} and t_{AA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to the high-impedance state. In a delayed-write or read-write cycle, the output follows the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every 16 ms (128 ms for TMS4x100P) to retain data. This can be achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh can be performed while maintaining valid data at the output. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden-refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh

CBR refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 300-µA (TMS46100P) or 500-µA (TMS44100P) refresh current is available on the low-power devices. Data integrity is maintained using CBR refresh with a period of 125 µs while holding $\overline{RAS}$ low for less than 1 µs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

self refresh

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 µs. The chip is then refreshed by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This ensures the DRAM is fully refreshed.

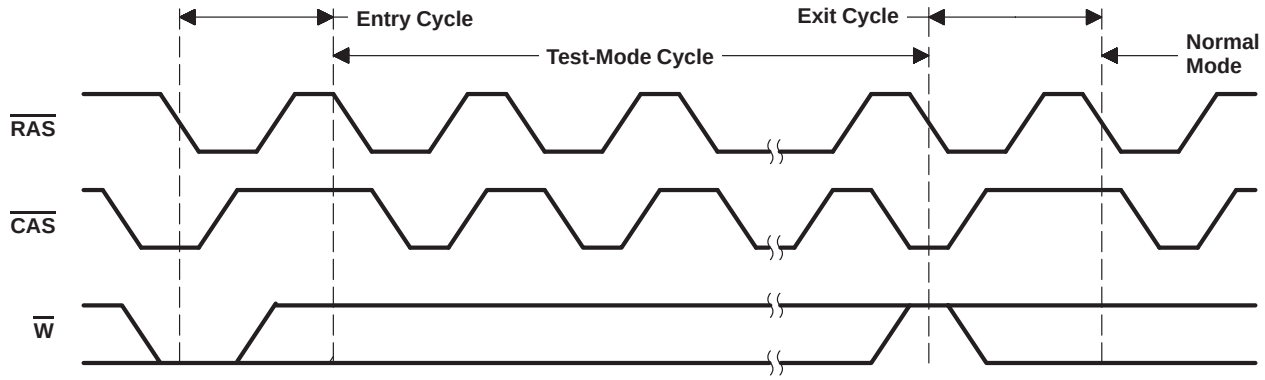
power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or CBR) cycle.

test mode

An industry-standard design-for-test (DFT) mode is incorporated in the TMS4x100 and TMS4x100P. A CBR cycle with $\overline{W}$ low (WCBR) cycle is used to enter the test mode. In the test mode, data is written into and read from eight sections of the array in parallel. Data is compared upon reading and if all bits are equal, the data-out terminal goes high. If any one bit is different, the data-out terminal goes low. Any combination of read, write, read-write, or page-mode cycles can be used in the test mode. The test-mode function reduces test times by enabling the 4-Mbit DRAM to be tested as if it were a 512K DRAM, where row address 10, column address 10, and column address 0 are not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

test mode (continued)



† The states of $\overline{W}$, data in, and address are defined by the type of cycle used during test mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}: TMS44100, TMS44100P . . . . . – 1 V to 7 V
TMS46100, TMS46100P . . . . . – 0.5 V to 4.6 V
Voltage range on any pin (see Note 1): TMS44100, TMS44100P . . . . . – 1 V to 7 V
TMS46100, TMS46100P . . . . . – 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		TMS44100/P			TMS46100/P			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	3	3.3	3.6	V
V_{IH}	High-level input voltage	2.4		6.5	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'44100-60 '44100P-60		'44100-70 '44100P-70		'44100-80 '44100P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle			105		90		80	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)			2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)	'44100		1		1		1	mA
			'44100P		500		500		500	µA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 4)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			105		90		80	mA
I_{CC4}	Average page current (see Notes 3 and 5)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling			90		80		70	mA
I_{CC6}†	Self-refresh current (see Note 3)	$\overline{CAS}$ ≤ 0.2 V, $\overline{RAS}$ < 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			500		500		500	µA
I_{CC7}	Standby current, outputs enabled (see Note 3)	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled			5		5		5	mA
I_{CC10}†	Battery-backup current (with CBR)	t_{RC} = 125 µs, t_{RAS} ≤ 1 ms, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			500		500		500	µA

† For TMS44100P only

NOTES: 3. I_{CC} max is specified with no load connected.
4. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
5. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'46100-60 '46100P-60		'46100-70 '46100P-70		'46100-80 '46100P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA (LVTTL)		2.4		2.4		2.4		V
		I_{OH} = – 100 µA (LVCMOS)		V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA (LVTTL)			0.4		0.4		0.4	V
		I_{OL} = 100 µA (LVCMOS)			0.2		0.2		0.2	
I_I	Input current (leakage)	V_I = 0 V to 3.9 V, V_{CC} = 3.6 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 3.6 V, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	Minimum cycle, V_{CC} = 3.6 V			70		60		50	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.0 V (LVTTL)			2		2		2	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (LVCMOS)	'46100		300		300		300	µA
			'46100P		200		200		200	µA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 4)	Minimum cycle, V_{CC} = 3.6 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			70		60		50	mA
I_{CC4}	Average page current (see Notes 3 and 5)	t_{PC} = minimum, $\overline{RAS}$ low, V_{CC} = 3.6 V, $\overline{CAS}$ cycling			60		50		40	mA
I_{CC6}†	Self-refresh current (see Note 3)	$\overline{CAS}$ ≤ 0.2 V, $\overline{RAS}$ < 0.2 V, t_{RAS} and t_{CAS} > 1000 ms			200		200		200	µA
I_{CC7}	Standby current, outputs enabled (see Note 3)	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Data out = enabled			5		5		5	mA
I_{CC10}†	Battery-backup current (with CBR)	t_{RC} = 125 µs, t_{RAS} ≤ 1 ms, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			300		300		300	µA

† For TMS46100P only

NOTES: 3. I_{CC} max is specified with no load connected.
4. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
5. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

ADVANCE INFORMATION

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0 – A10		5	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_o	Output capacitance		7	pF

NOTE 6: V_{CC} = 5 V ± .5 V for the TMS44100 devices, V_{CC} = 3.3 V ± 0.3 V for the TMS46100 devices, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'4x100-60 '4x100P-60		'4x100-70 '4x100P-70		'4x100-80 '4x100P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low impedance	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 7)	0	15	0	18	0	20	ns

NOTE 7: t_{OFF} is specified when the output is no longer driven.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4x100-60 '4x100P-60		'4x100-70 '4x100P-70		'4x100-80 '4x100P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 8)	110		130		150		ns
t_{RWC}	Cycle time, read-write (see Note 8)	130		153		175		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 8 and 9)	40		45		50		ns
t_{PRWC}	Cycle time, page-mode read-write (see Note 8)	60		68		75		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ low, page mode (see Note 10)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low, nonpage mode (see Note 10)	60	10 000	70	10 000	80	10 000	ns
t_{RASS}	Pulse duration, $\overline{RAS}$ low, self refresh	100		100		100		µs
t_{CAS}	Pulse duration, $\overline{CAS}$ low, (see Note 11)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{RPS}	Precharge time after self refresh using $\overline{RAS}$	140		130		150		ns
t_{WP}	Pulse duration, write	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 12)	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{WTS}	Setup time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{DH}	Hold time, data (see Note 12)	10		15		15		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 14)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 14)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low (early-write operation only)	10		15		15		ns
t_{WCR}	Hold time, $\overline{W}$ low after $\overline{RAS}$ low (see Note 13)	50		55		60		ns
t_{WHR}	Hold time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{WTH}	Hold time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (read-write operation only)	30		35		40		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns

NOTES: 8. All cycle times assume t_T = 5 ns.
9. To assure t_{PC} min, t_{ASC} should be ≥ 5 ns.
10. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
11. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
12. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

			'4x100-60 '4x100P-60		'4x100-70 '4x100P-70		'4x100-80 '4x100P-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)		5		5		5		ns
t_{CHS}	Hold time, $\overline{CAS}$ low after $\overline{RAS}$ high, self refresh		–50		–50		–50		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-write operation only)		15		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 15)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 15)		20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high		15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)		60		70		80		ns
t_{TAA}	Access time from address (test mode)		35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)		40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)		65		75		85		ns
t_{REF}	Refresh time interval	'4x100		16		16		16	ms
		'4x100P		128		128		128	ms
t_T	Transition time		2	50	2	50	2	50	ns

NOTE 15: The maximum value is specified only to assure access time.

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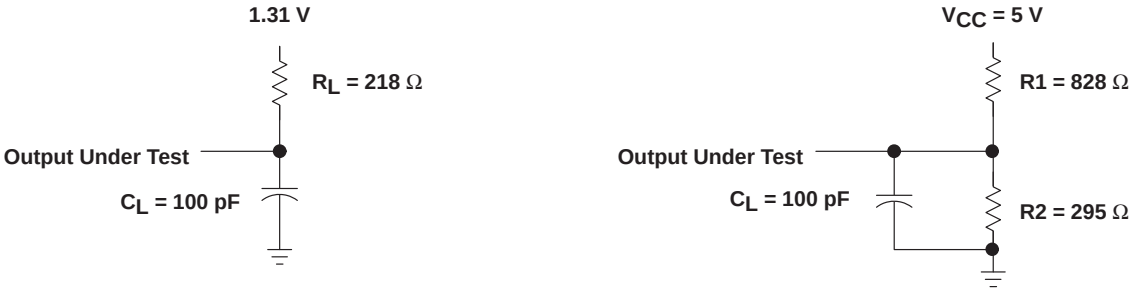
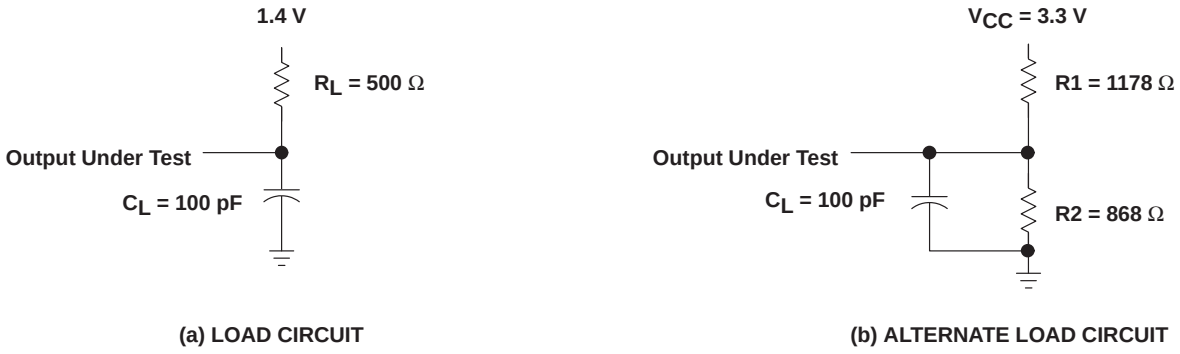


(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

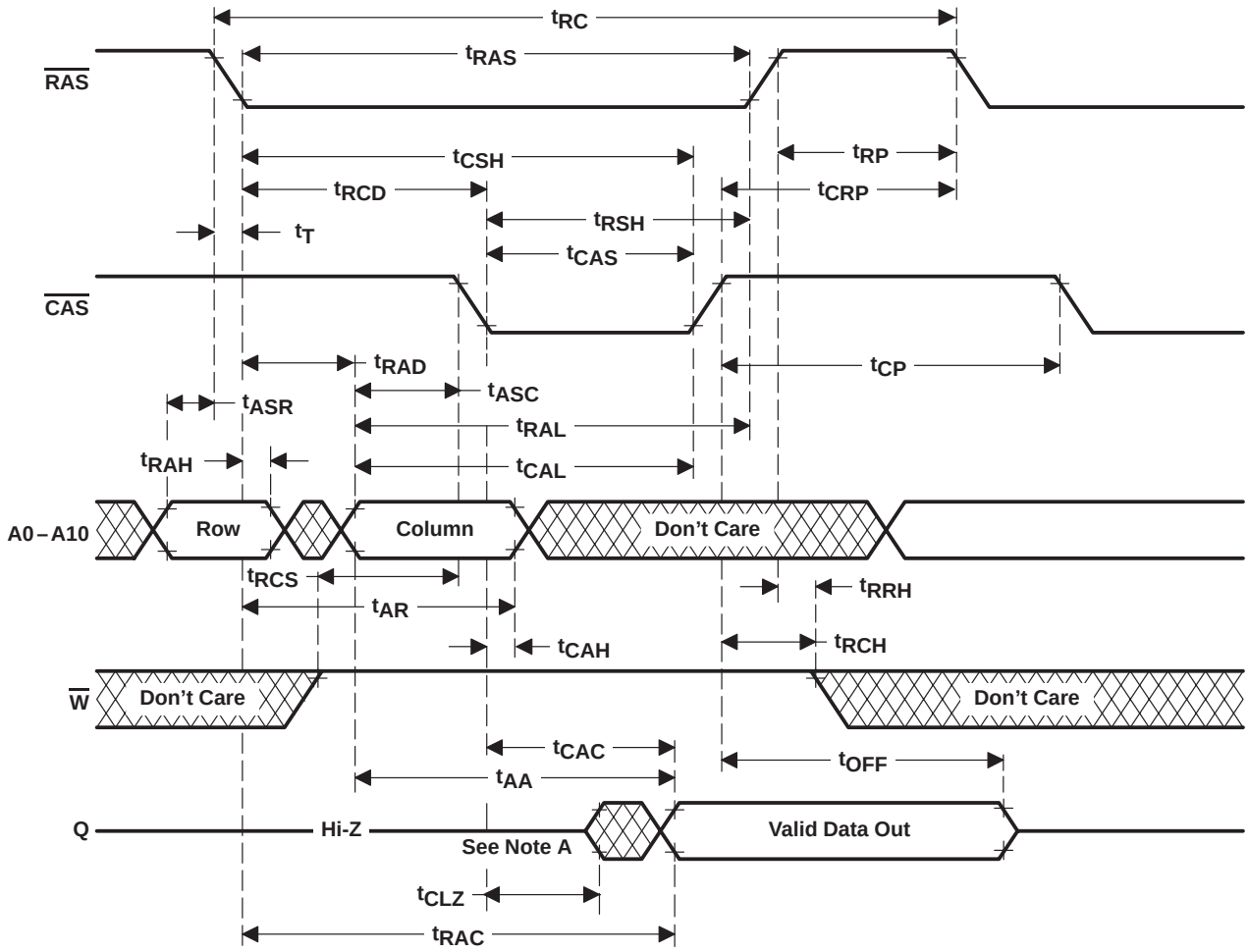
Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT (b) ALTERNATE LOAD CIRCUIT

Figure 2. Low-Voltage Load Circuits for Timing Parameters



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 3. Read-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

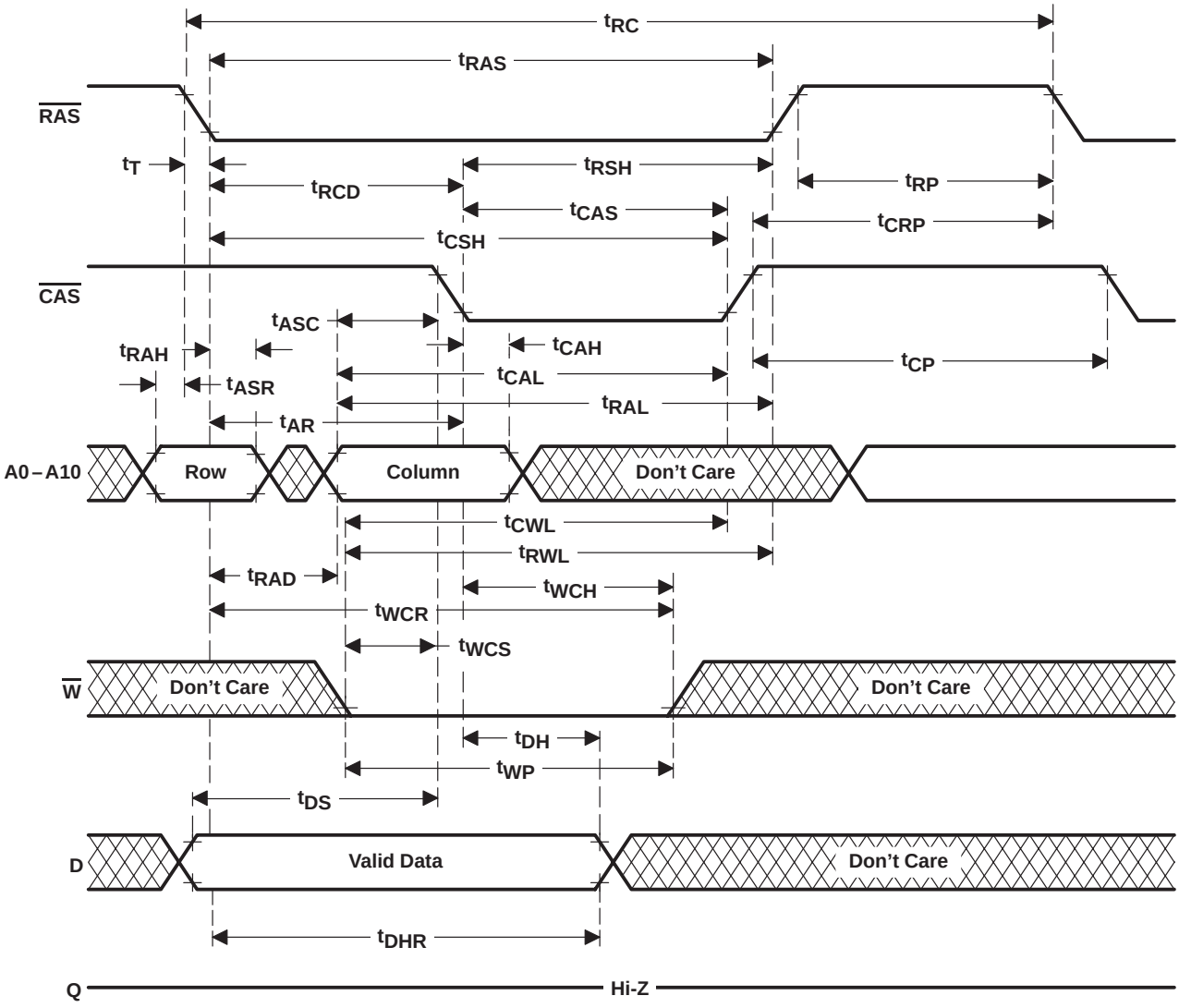


Figure 4. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

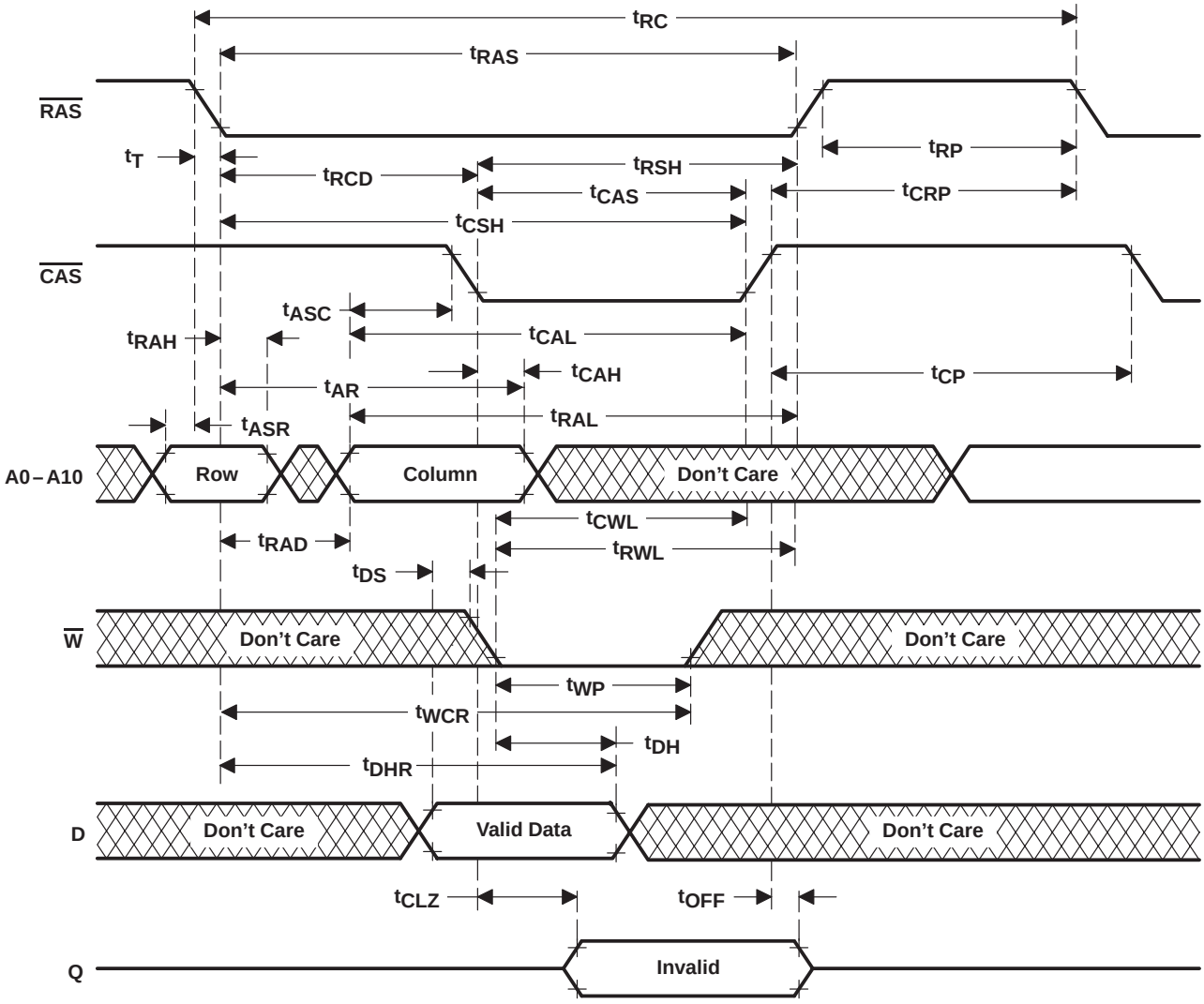
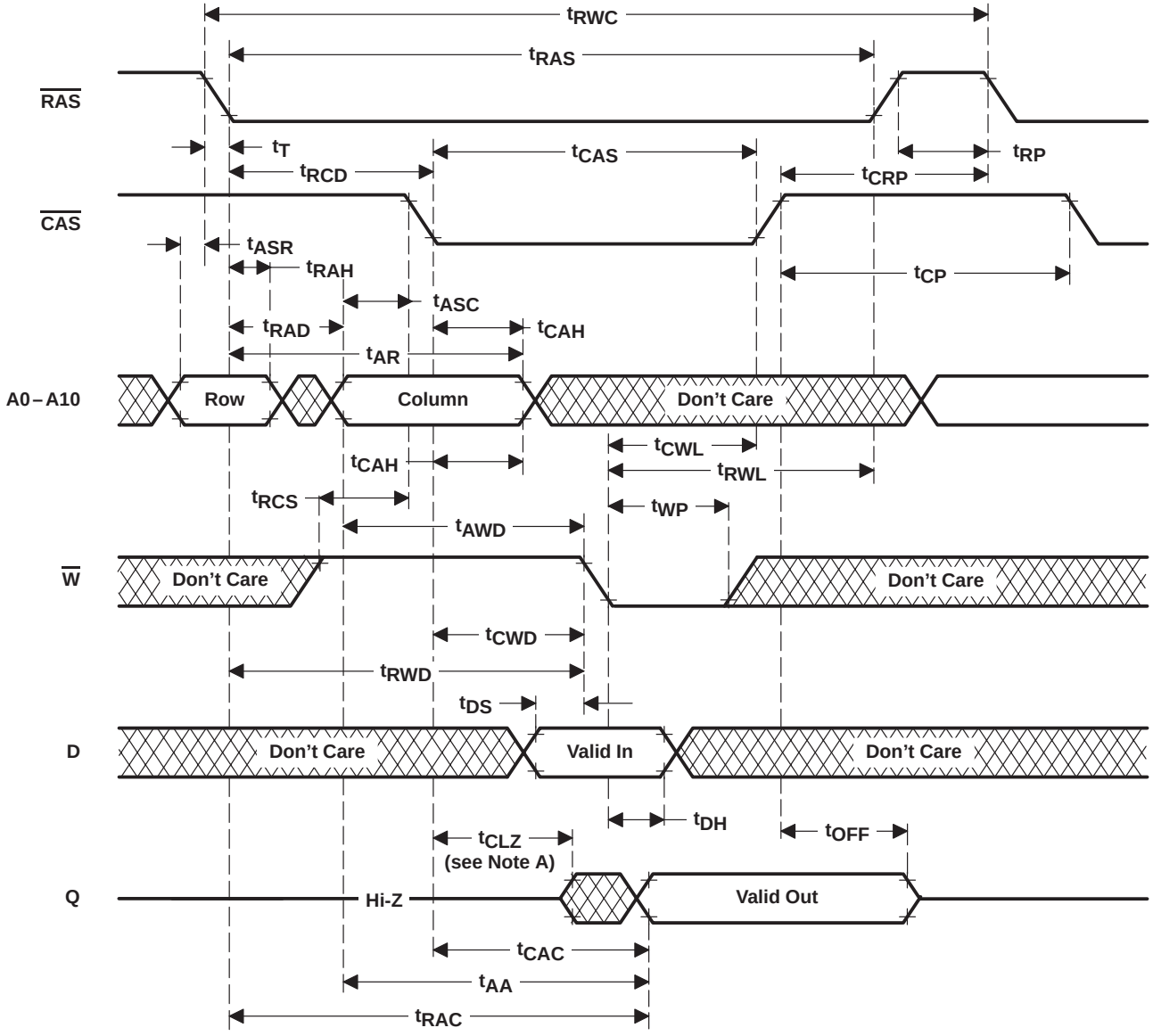


Figure 5. Write-Cycle Timing

ADVANCE INFORMATION

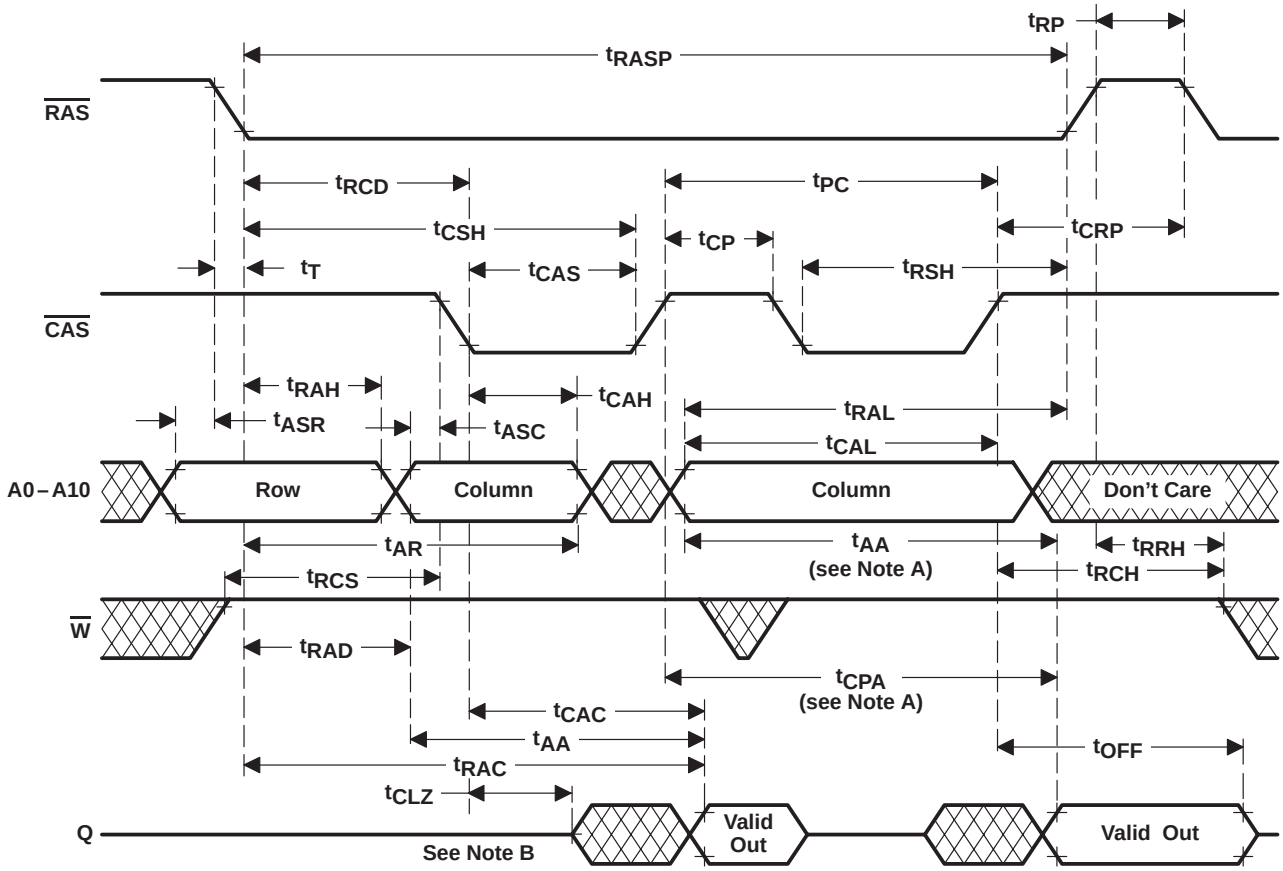
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

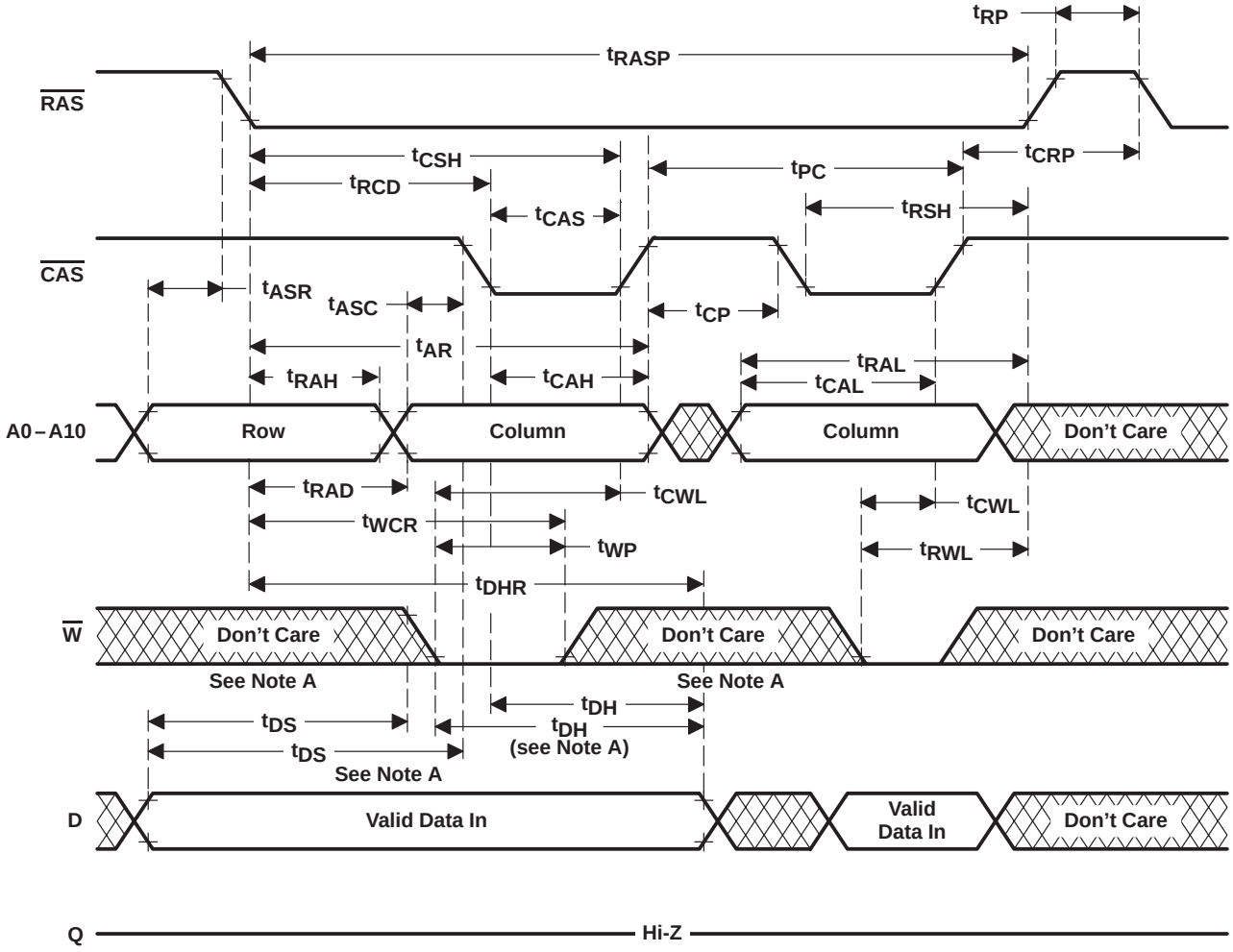


NOTES: A. Access time is t_{CPA} or t_{AA} dependent.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 7. Enhanced-Page-Mode Read-Cycle Timing

ADVANCE INFORMATION

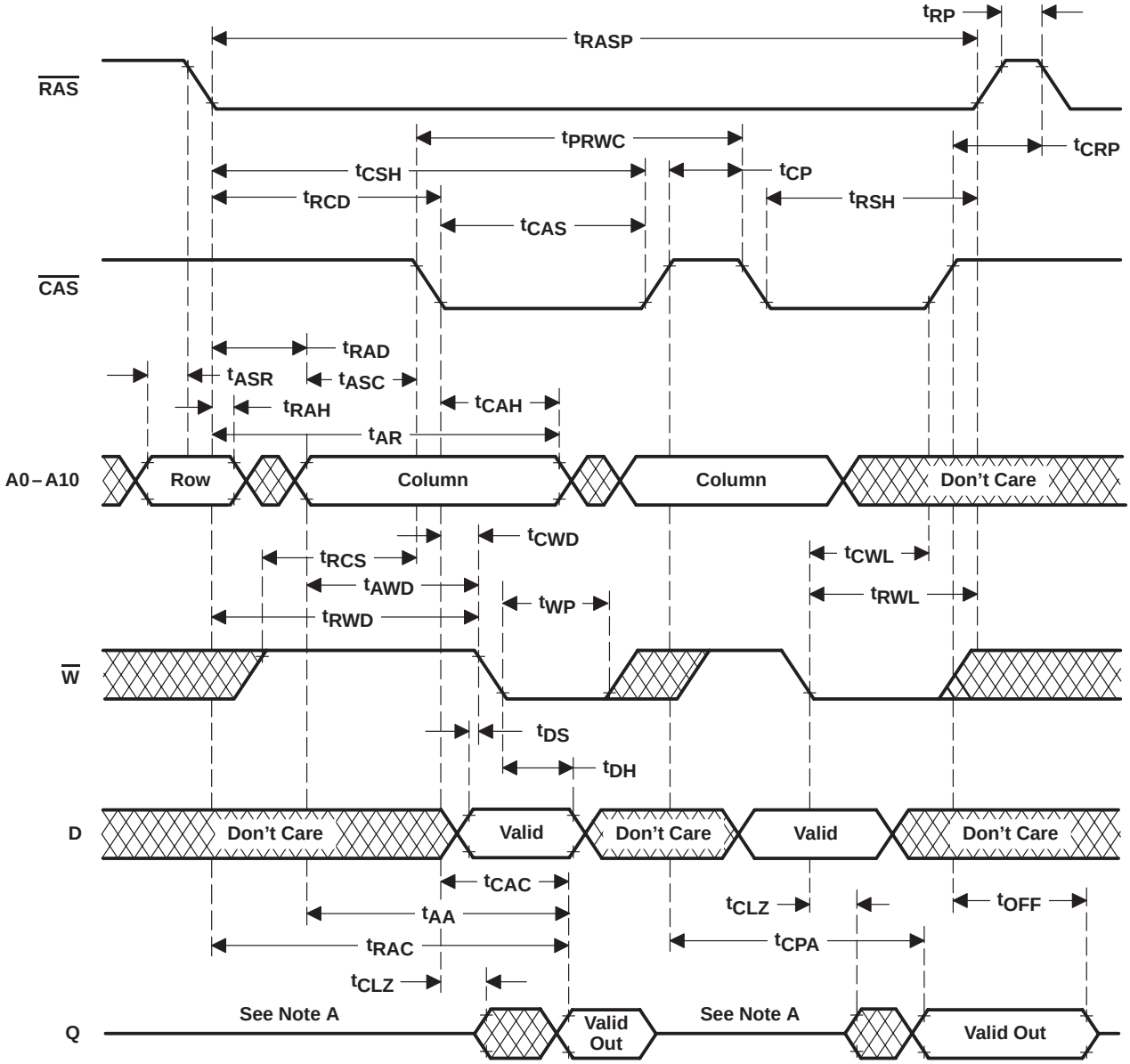
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

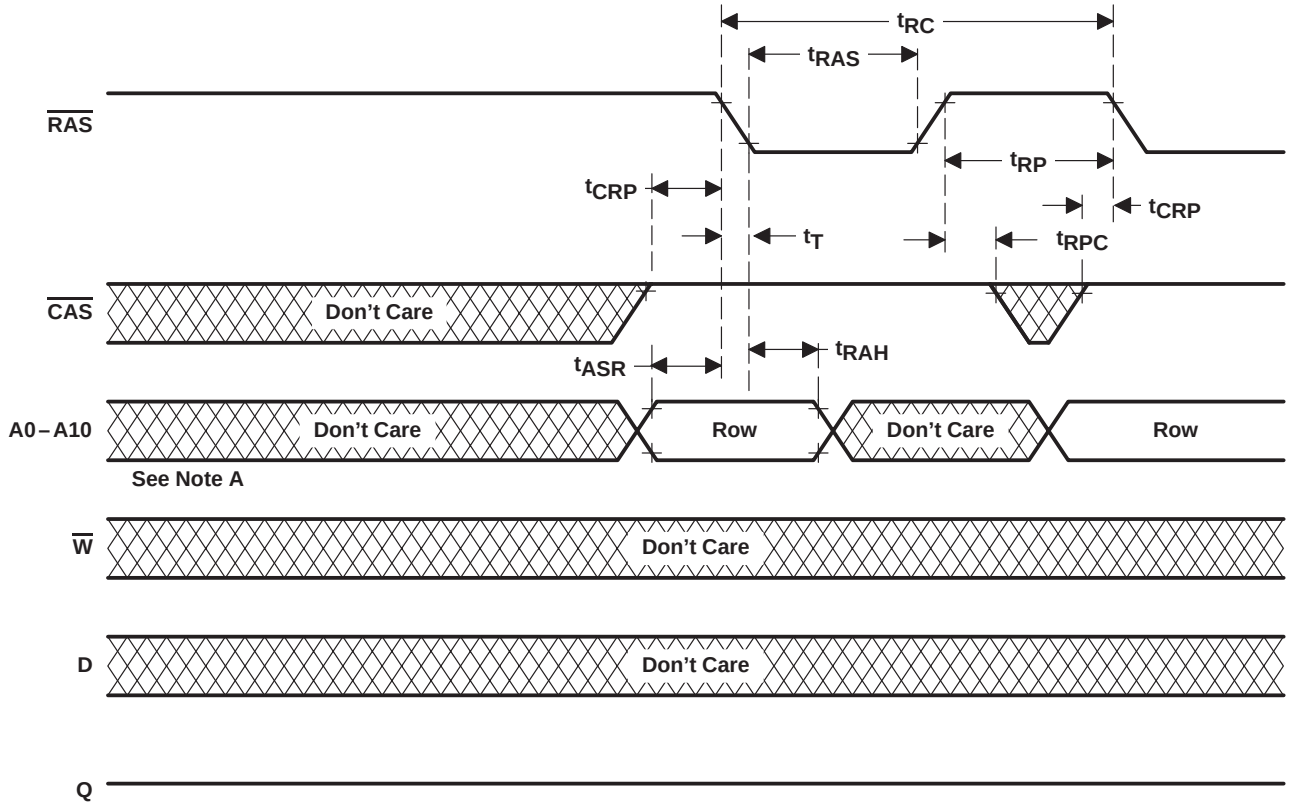


NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced-Page-Mode Read-Write-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTE A: A10 is a don't care.

Figure 10. $\overline{\text{RAS}}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

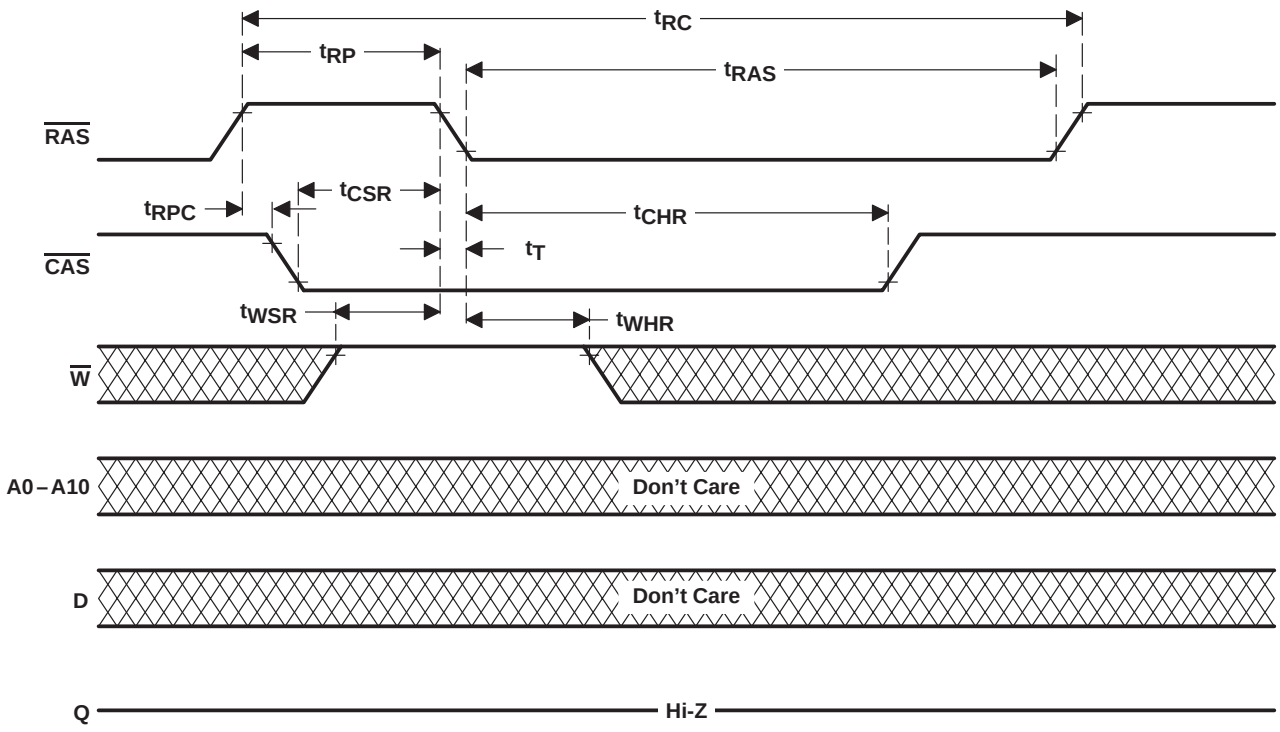


Figure 11. Automatic CBR-Refresh-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

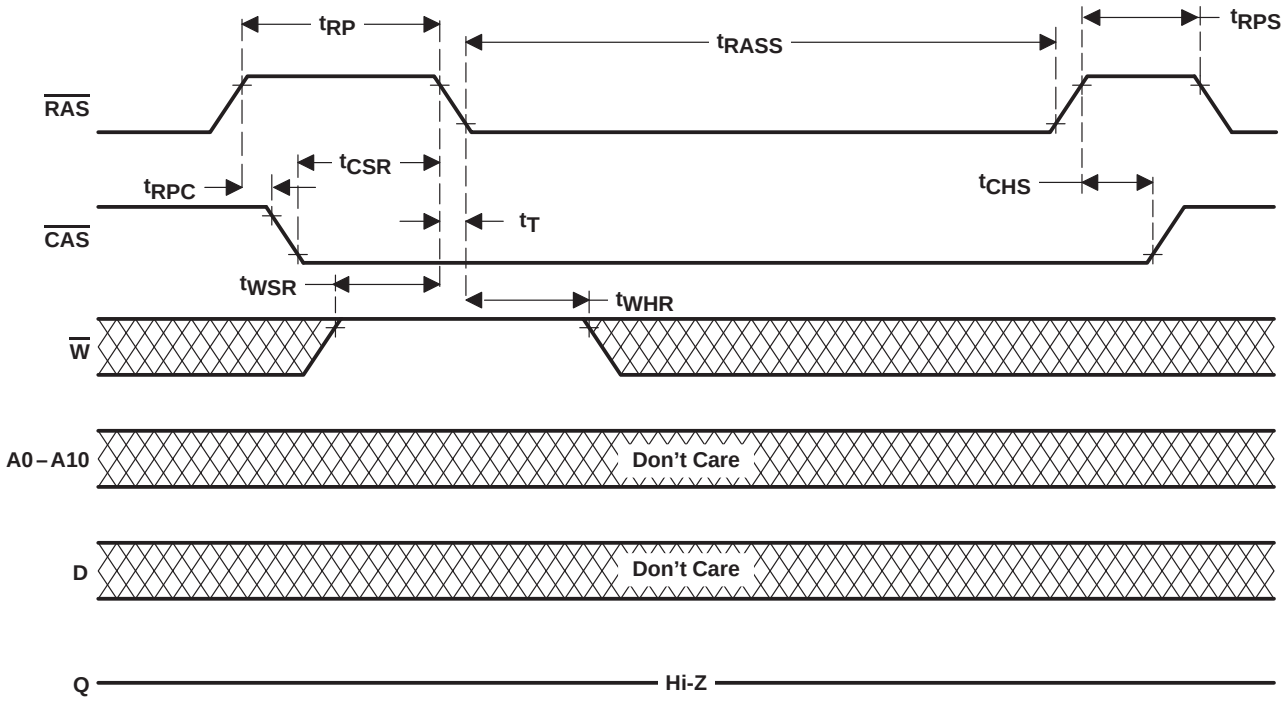

Figure 12. Self-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

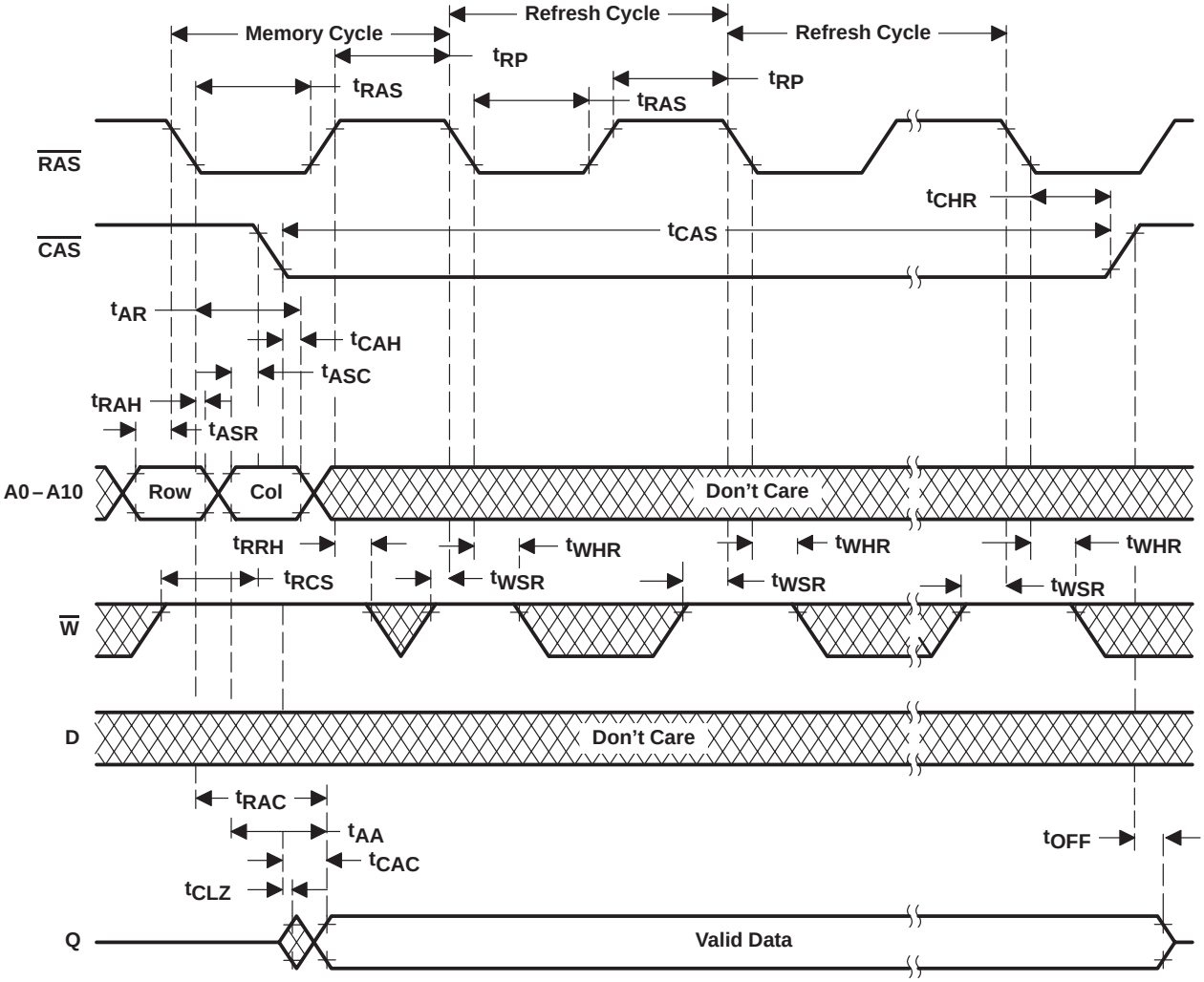

Figure 13. Hidden-Refresh-Cycle (Read) Timing

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PARAMETER MEASUREMENT INFORMATION

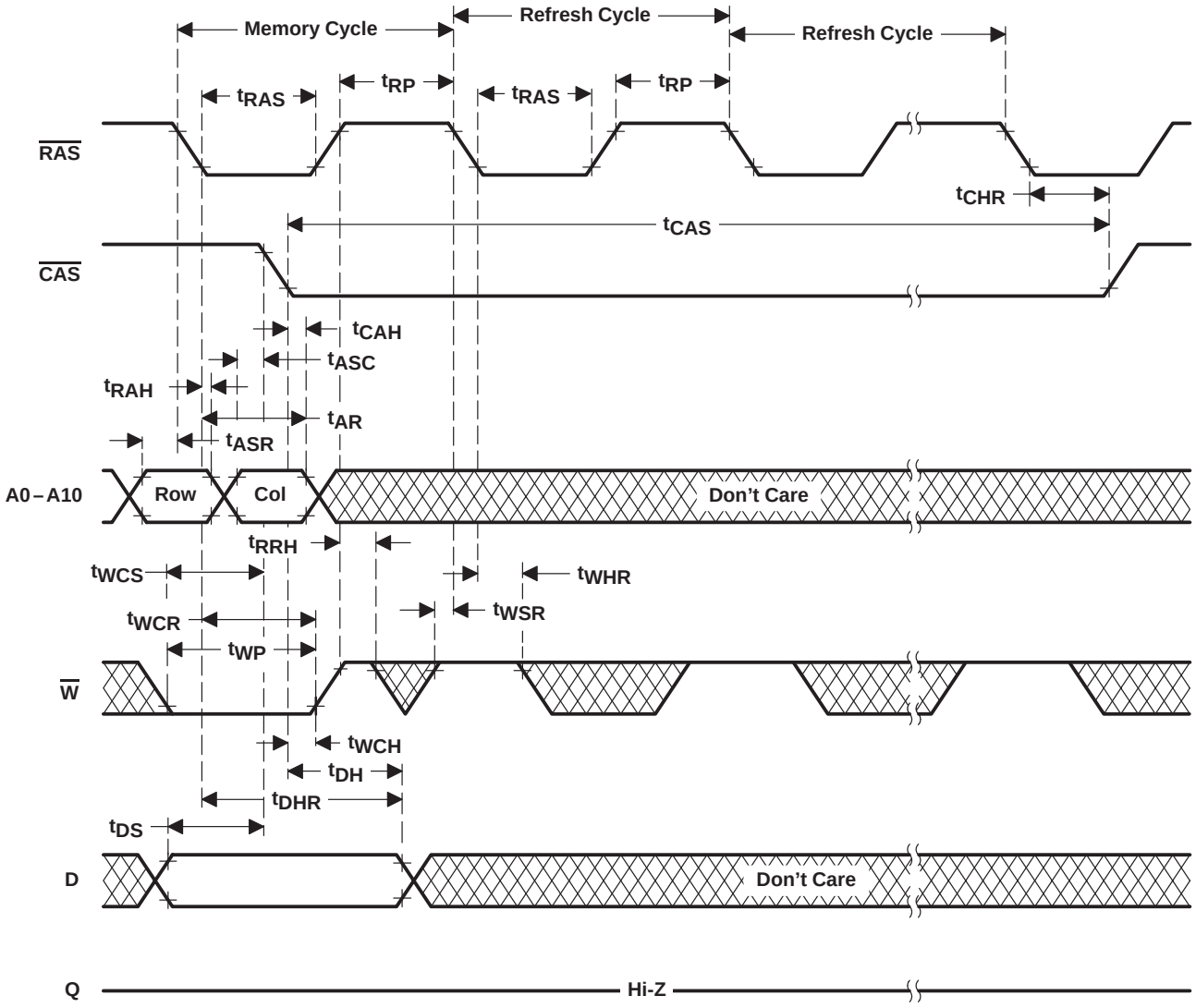

Figure 14. Hidden-Refresh-Cycle (Write) Timing

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PARAMETER MEASUREMENT INFORMATION

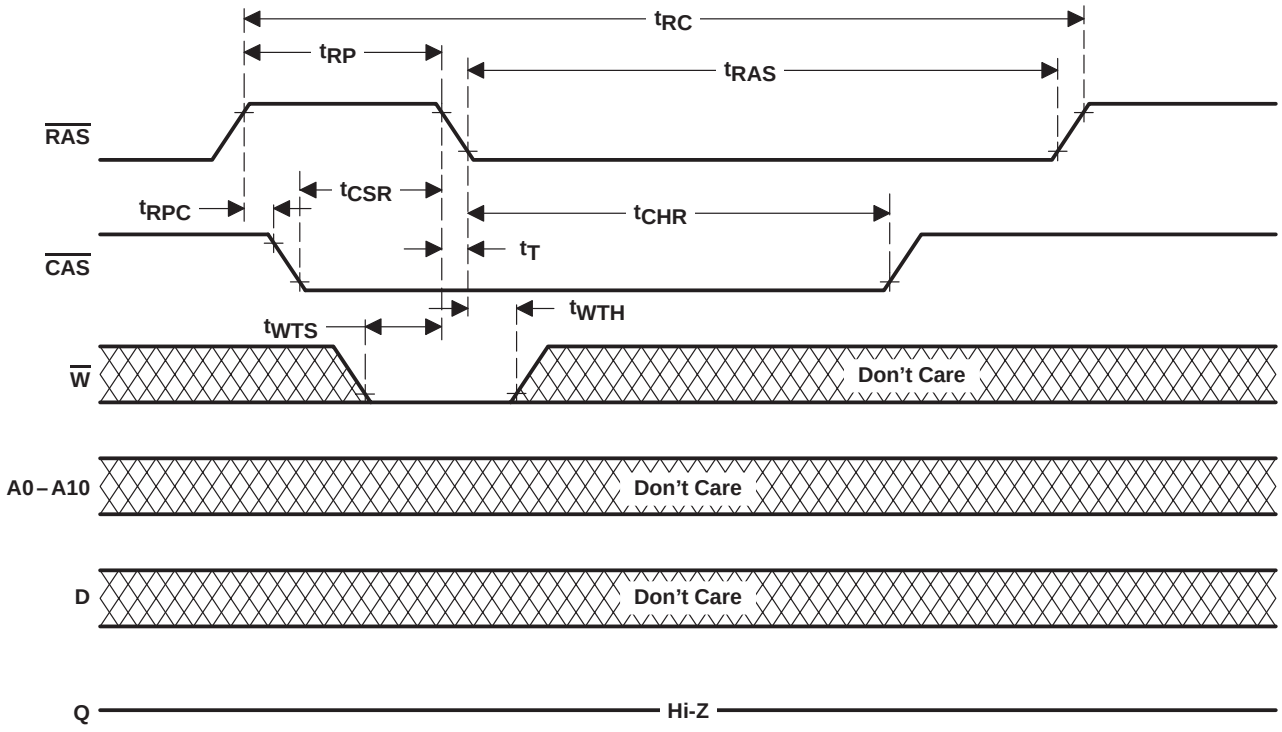
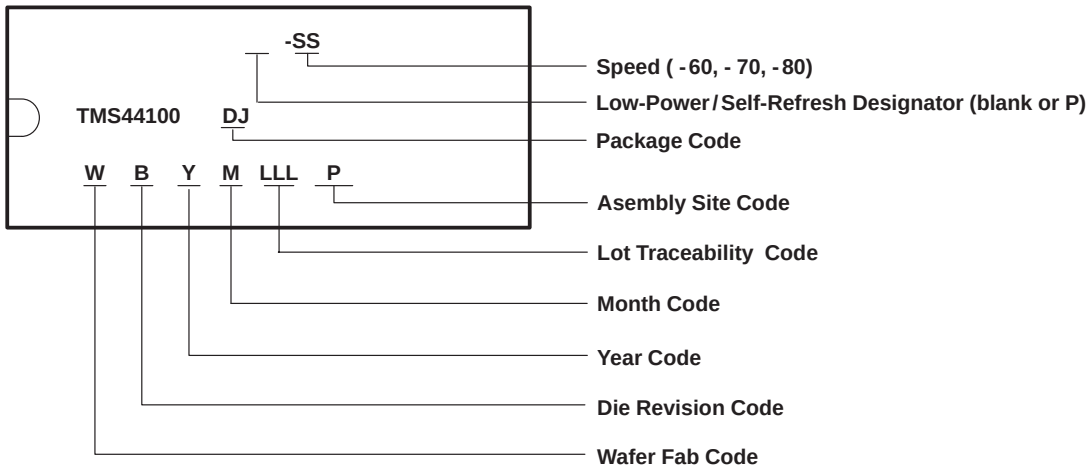


Figure 15. Test-Mode Entry Cycle

device symbolization (TMS44100 illustrated)



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