NEC

DATA SHEET

MOS INTEGRATED CIRCUIT

μPD70236A

V53A™
16-BIT MICROPROCESSOR

DESCRIPTION

The μPD70236A (V53A) is a 16-bit CMOS microprocessor that is software-compatible with the μPD70136A (V33A™).

The μPD70236A is based on the μPD70236 (V53™) with the only difference being its CPU, which is equivalent to that of the μPD70136A, instead of that of the μPD70136 (V33™).

The μPD70236A has a variety of on-chip peripheral LSI functions, enabling the creation of high-performance, very compact, low-power consumption, and high-reliability application systems.

Functions are described in detail in the following User's Manuals, which should be read before starting design work.

- **V53A User's Manual: U10108E**
- **16-Bit V Series™ User's Manual – Instructions: IEU-804***

(*: Document No. of Japanese version)

FEATURES

- High-performance 16-bit CPU (software-compatible with V33A)
  - 16M-byte memory space and 64K-byte I/O space
  - Software-compatible with V20™, V30™, V40™, and V50™ native modes
  - Dynamic bus sizing function
- On-chip standard peripheral LSI functions. . . TCU, SCU, DMAU, CG, WCU, REFU, BAU, ICU
- Allows connection of μPD72291 floating-point operation coprocessor.
- Standby functions. . . HALT mode
  STOP mode
- Maximum operating frequency: 20 MHz (with 40 MHz supplied externally)
- Operating temperature range: –40 to +85 °C
- Low voltage: V_{DD} = 2.7 V to 3.6 V (Max. 10 MHz)
- Small package versions available (20 x 20 mm fine-pitch QFP, 14 x 14 mm fine-pitch TQFP)
- Low current consumption

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The information in this document is subject to change without notice.

Document No. U10120EJ2V0DS00 (2nd edition)
Date Published October 1995 P
Printed in Japan

The mark ★ shows revised points.

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APPLICATIONS

- OA equipment (personal computers, word processors, etc.)
- Various control equipment (robot control, communications control, etc.)

ORDERING INFORMATION

	Part Number	Package	Max. Operating Frequency (MHz)
	μPD70236AGD-10-5BB	120-pin plastic QFP (28 x 28 mm)	10
	μPD70236AGD-12-5BB	120-pin plastic QFP (28 x 28 mm)	12.5
	μPD70236AGD-16-5BB	120-pin plastic QFP (28 x 28 mm)	16
	μPD70236AGD-20-5BB	120-pin plastic QFP (28 x 28 mm)	20
	μPD70236AGJ-10-3EB	120-pin plastic QFP (Fine pitch)(20 x 20 mm)	10
	μPD70236AGJ-12-3EB	120-pin plastic QFP (Fine pitch)(20 x 20 mm)	12.5
	μPD70236AGJ-16-3EB	120-pin plastic QFP (Fine pitch)(20 x 20 mm)	16
	μPD70236AGJ-20-3EB	120-pin plastic QFP (Fine pitch)(20 x 20 mm)	20
*	μPD70236AGC-10-9EV	120-pin plastic TQFP (Fine pitch) (14 x 14 mm)	10
*	μPD70236AGC-12-9EV	120-pin plastic TQFP (Fine pitch) (14 x 14 mm)	12.5
*	μPD70236AGC-16-9EV	120-pin plastic TQFP (Fine pitch) (14 x 14 mm)	16
*	μPD70236AGC-20-9EV	120-pin plastic TQFP (Fine pitch) (14 x 14 mm)	20
	μPD70236ARB-10	132-pin ceramic PGA	10
	μPD70236ARB-12	132-pin ceramic PGA	12.5
	μPD70236ARB-16	132-pin ceramic PGA	16
	μPD70236ARB-20	132-pin ceramic PGA	20

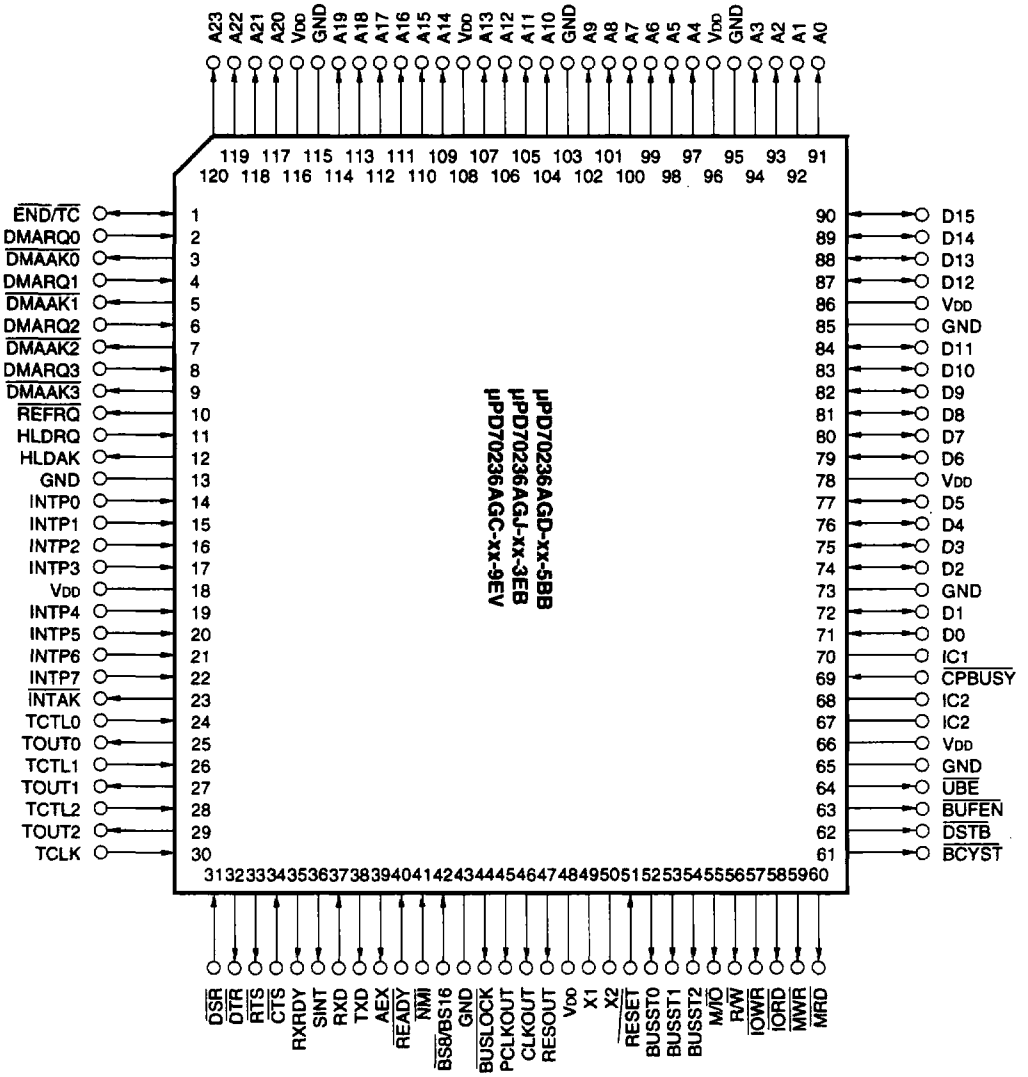
DIFFERENCES BETWEEN μPD70236A AND μPD70236

Parameter \ Part Number			V53A						V53				
			μPD70236A						μPD70236(A)		μPD70236		
			-10	-12	-16		-20		-10	-12	-10	-12	-16
Supply voltage: V_{DD} = 5 V ±10%	Operating temperature range: T_A [°C]		−40 to +85		−10 to +70	−40 to +85	−10 to +70		−40 to +85		−10 to +70		
	Operating frequency: f_x [MHz] Note 1		10	12.5	16	20			10	12.5	10	12.5	16
	Delay time (example): t_{DKA} [ns]	MAX.	35	30	20	30	20		45				40
		MIN.	2		3	2	3		5				
	Supply current: I_{DD} [mA] Note 2	Operating	f_x x 3.9 + 3						f_x x 10 + 20				
		HALT	1.0						20				
		STOP	0.005						1.0				
Supply voltage: V_{DD} = 3.6 to 4.5 V	Operating temperature range: T_A [°C]		−40 to +85										
	Operating frequency: f_x [MHz] Note 1		12.5	16									
	Delay time (example): t_{DKA} [ns] Note 1		35										
	Supply current: I_{DD} [mA] Note 2	Operating	f_x x 2.9 + 2										
		HALT	0.8										
		STOP	0.004										
Supply voltage : V_{DD} = 2.7 to 3.6 V	Operating temperature range: T_A [°C]		−40 to +85										
	Operating frequency: f_x [MHz] Note 1		8	10									
	Delay time (example): t_{DKA} [ns] Note 1		45										
	Supply current: I_{DD} [mA] Note 2	Operating	f_x x 2.2 + 2										
		HALT	0.6										
		STOP	0.003										
I/O recovery cycle			2 clocks						6 clocks				
Standby control register oscillation stabilization time			$2^{15}/f_{XX}$ to $2^{18}/f_{XX}$						$2^{18}/f_{XX}$ to $2^{21}/f_{XX}$				
External clock X1 input with X2 open			Possible						Not possible				
SCU transmission control by $\overline{CTS}$			External circuit unnecessary						External circuit necessary				
120-pin plastic QFP (fine-pitch) (20 x 20 mm)			Provided						Not provided					*
120-pin plastic TQFP (fine-pitch) (14 x 14 mm)			Provided						Not provided					*

Notes 1. MAX value
2. TYP value

PIN CONFIGURATION

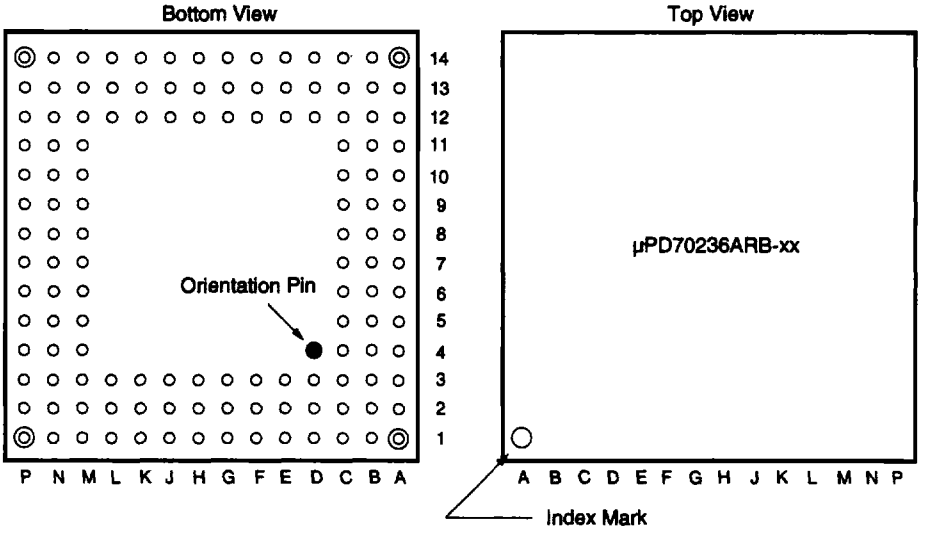
120-pin plastic QFP (28 x 28 mm) (Top View)
120-pin plastic QFP (Fine Pitch) (20 x 20 mm) (Top View)
120-pin plastic TQFP (Fine Pitch) (14 x 14 mm) (Top View)



IC: Internally Connected

Cautions 1. IC1: Leave open.
2. IC2: Connect to the ground.

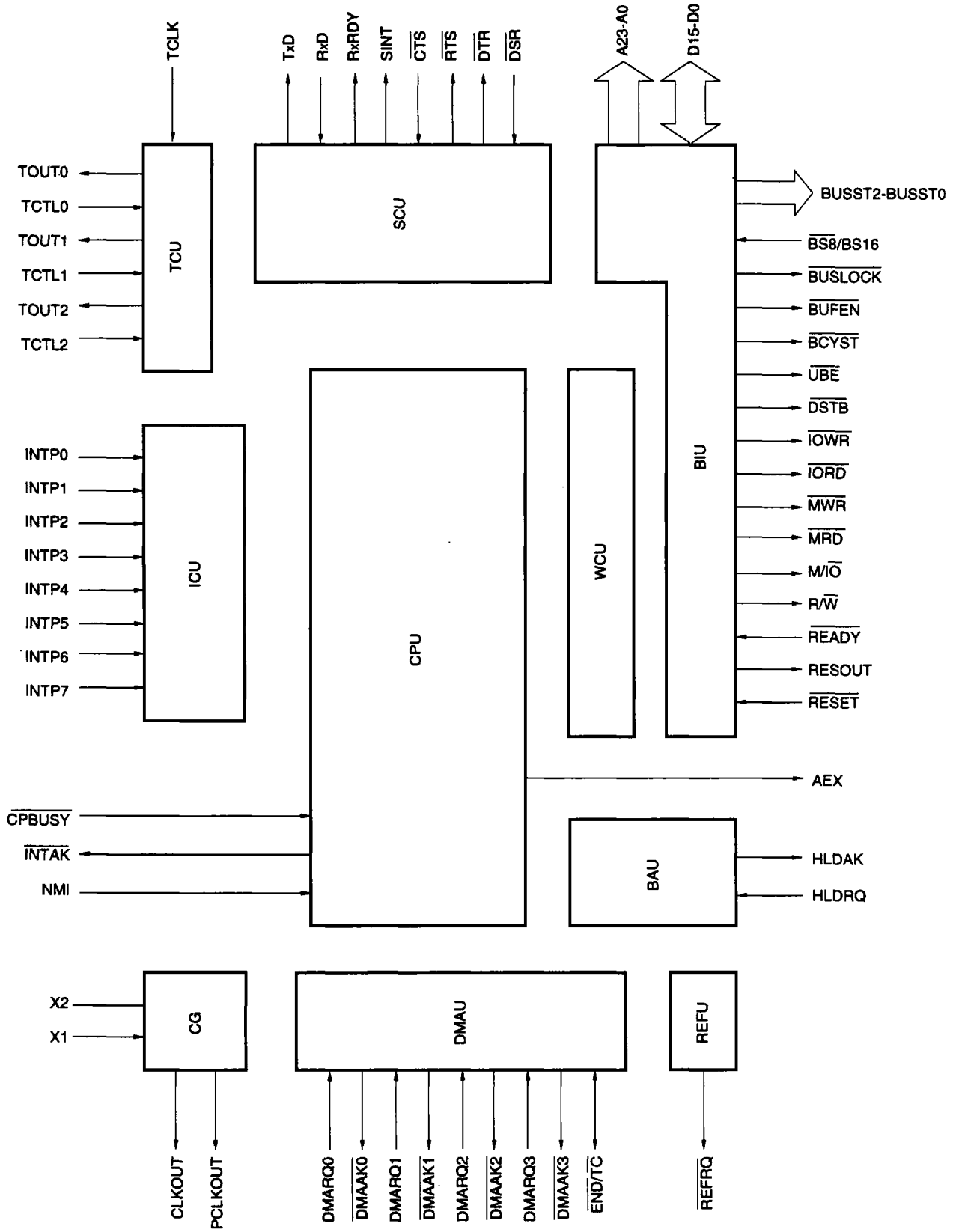
132-pin ceramic PGA



Remark The orientation pin is not included in the pin count.

No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name
A1	A22	B9	A9	D3	DMARQ0	H1	INTP2	L13	GND	N7	$\overline{\text{BUSLOCK}}$
A2	A20	B10	A5	D12	D14	H2	INTP3	L14	IC2	N8	RESOUT
A3	GND	B11	GND	D13	IC1	H3	V_{DD}	M1	TOUT0	N9	X2
A4	A19	B12	A2	D14	D11	H12	GND	M2	TCTL2	N10	BUSST0
A5	A16	B13	IC1	E1	HLDRQ	H13	D2	M3	TCLK	N11	R/$\overline{\text{W}}$
A6	A14	B14	D12	E2	$\overline{\text{DMAAK3}}$	H14	D3	M4	$\overline{\text{DTR}}$	N12	$\overline{\text{IORD}}$
A7	A12	C1	$\overline{\text{DMAAK2}}$	E3	$\overline{\text{DMARQ2}}$	J1	INTP4	M5	RxRDY	N13	$\overline{\text{BCYST}}$
A8	A11	C2	$\overline{\text{DMAAK0}}$	E12	V_{DD}	J2	INTP5	M6	AEX	N14	$\overline{\text{UBE}}$
A9	NC	C3	IC1	E13	D10	J3	INTP7	M7	GND	P1	$\overline{\text{DSR}}$
A10	A8	C4	A23	E14	D8	J12	IC1	M8	V_{DD}	P2	$\overline{\text{CTS}}$
A11	A6	C5	IC1	F1	NC	J13	D1	M9	BUSST1	P3	SINT
A12	A4	C6	A18	F2	HLDAK	J14	NC	M10	IC1	P4	TxD
A13	A3	C7	V_{DD}	F3	$\overline{\text{REFRQ}}$	K1	INTP6	M11	$\overline{\text{MRD}}$	P5	$\overline{\text{READY}}$
A14	A0	C8	GND	F12	D9	K2	$\overline{\text{INTAK}}$	M12	IC1	P6	$\overline{\text{BS8}}$/BS16
B1	DMARQ1	C9	A7	F13	D7	K3	TCTL1	M13	$\overline{\text{BUFEN}}$	P7	PCLKOUT
B2	$\overline{\text{END}}$/$\overline{\text{TC}}$	C10	V_{DD}	F14	D6	K12	V_{DD}	M14	IC2	P8	CLKOUT
B3	A21	C11	A1	G1	INTP1	K13	$\overline{\text{CPBUSY}}$	N1	TOUT1	P9	X1
B4	V_{DD}	C12	D15	G2	INTP0	K14	D0	N2	IC1	P10	$\overline{\text{RESET}}$
B5	A17	C13	D13	G3	GND	L1	TCTL0	N3	$\overline{\text{RTS}}$	P11	BUSST2
B6	A15	C14	GND	G12	V_{DD}	L2	IC1	N4	IC1	P12	M/$\overline{\text{IO}}$
B7	A13	D1	DMARQ3	G13	D5	L3	TOUT2	N5	RxD	P13	$\overline{\text{IOWR}}$
B8	A10	D2	$\overline{\text{DMAAK1}}$	G14	D4	L12	$\overline{\text{DSTB}}$	N6	$\overline{\text{NMI}}$	P14	$\overline{\text{MWR}}$

Cautions 1. IC1: Leave open.

2. IC2: Connect to the ground.

INTERNAL BLOCK DIAGRAM