64K x 4 Bit Dynamic RAM with Page Mode

FEATURES

- **Performance range**

	t_{RAC}	t_{CAC}	t_{RC}
KM41464A-12	120ns	60ns	220ns
KM41464A-15	150ns	75ns	260ns

- **Page Mode capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or Output Enable Controlled Write**
- **Single +5V±10% power supply**
- **256 cycle/4ms refresh**
- **JEDEC standard pinout in 18-pin DIP, 18-lead PLCC and 20-pin ZIP.**

GENERAL DESCRIPTION

The KM41464A is a fully decoded 65,536 x 4 NMOS Dynamic Random Access Memory. The design is optimized for high speed, high performance applications such as computer memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The KM41464A features page mode which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. Multiplexed row and column address inputs permit the KM41464A to be housed in a standard 18-pin DIP.

The KM41464A is fabricated using Samsung's advanced silicon gate NMOS process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and outputs are TTL complible.

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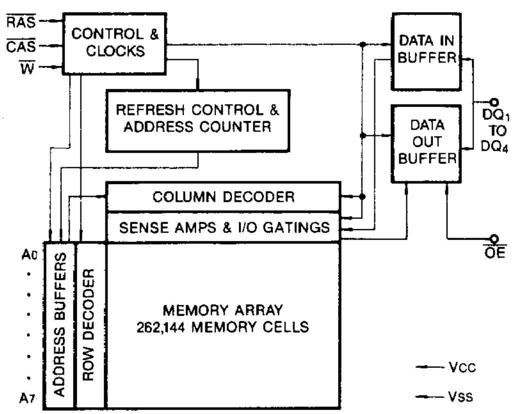
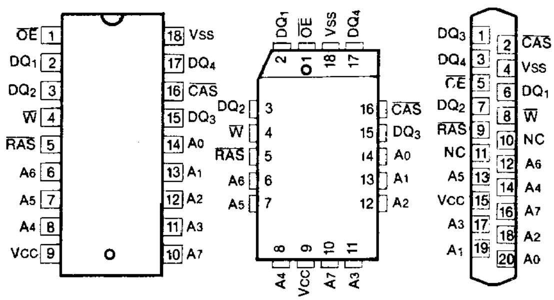
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

- **KM41464AP**
- **KM41464AJ**
- **KM41464AZ**



Pin Name	Pin Function
A_0-A_7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Output Enable
DQ_1-DQ_4	Data In/Out
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling; @t_{RC} = min.)	KM41464A-12 KM41464A-15	I_{CC1}	— —	75 65	mA mA
STANDBY CURRENT ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 $\overline{RAS}$ cycles min.)		I_{CC2}	—	4.5	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; @t_{RC} = min.)	KM41464A-12 KM41464A-15	I_{CC3}	— —	65 60	mA mA
PAGE MODE CURRENT* ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; @t_{PC} = min.)	KM41464A-12 KM41464A-15	I_{CC4}	— —	55 45	mA mA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT ($\overline{RAS}$ cycling; @t_{RC} = min.)	KM41464A-12 KM41464A-15	I_{CC5}	— —	65 60	mA mA
INPUT LEAKAGE CURRENT (Any input $0 \leq V_{IN} \leq 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$		I_{DOL}	−10	10	μA
OUTPUT HIGH VOLTAGE LEVEL ($I_{OH} = -5mA$)		V_{OH}	2.4	—	V
OUTPUT LOW VOLTAGE LEVEL ($I_{OL} = 4.2mA$)		V_{OL}	—	0.4	V

*Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_7)	C_{IN1}	—	7	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	10	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1,2)

KM41464A STANDARD OPERATION

Parameter	Symbol	KM41464A-12		KM41464A-15		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	220		260		ns	
Read-modify-write cycle time	t_{RWC}	305		355		ns	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	3, 4
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	3, 5
Output buffer turn-off delay time	t_{OFF}	0	30	0	40	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		65		ns	
$\overline{CAS}$ precharge time (all cycles except page mode)	t_{CPN}	30		35		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	40		45		ns	
Write command pulse width	t_{WP}	40		45		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	

KM41464A STANDARD OPERATION (Continued)

Parameter	Symbol	KM41464A-12		KM41464A-15		Units	Notes
		Min	Max	Min	Max		
Data-in set-up time	t_{DS}	0		0		ns	
Data-in hold time	t_{DH}	40		45		ns	
$\overline{CAS}$ to write enable delay time	t_{CWD}	100		120		ns	7
$\overline{RAS}$ to write enable delay time	t_{RWD}	160		195		ns	7
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	100		120		ns	
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	100		120		ns	
Access time from $\overline{OE}$	t_{OEA}		30		40	ns	
$\overline{OE}$ to Data in delay time	t_{OED}	30		40		ns	
Output Buffer turn off delay from $\overline{OE}$	t_{OEZ}	0	30	0	40	ns	
$\overline{OE}$ hold time referenced to $\overline{W}$	t_{OEH}	25		25		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		ns	
Din to $\overline{CAS}$ delay time	t_{DZC}	0		0		ns	8
Din to $\overline{OE}$ delay time	t_{DZO}	0		0		ns	8
Refresh period (256 cycles)	t_{REF}		4		4	ms	

KM41464A $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh)	t_{CSR}	25		30		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh)	t_{CHR}	55		60		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	20		20		ns	

KM41464A PAGE MODE

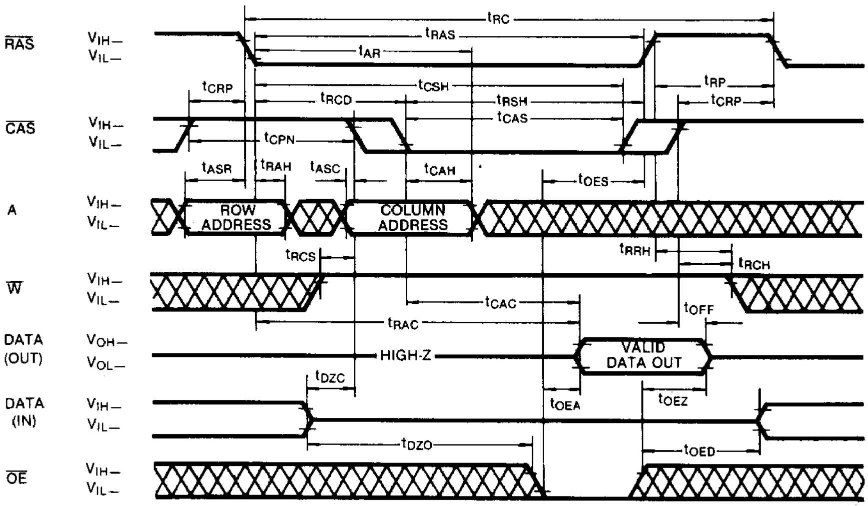
Page mode cycle time	t_{PC}	120		145		ns	
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	50		60		ns	

NOTES

1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{CWD} and t_{RWD} are restrictive operating parameters for the read-modify-write cycle only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} > t_{RWD}$(min), the cycle is a late write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
8. Either t_{DZC} or t_{DZO} must be satisfied for all cycles.

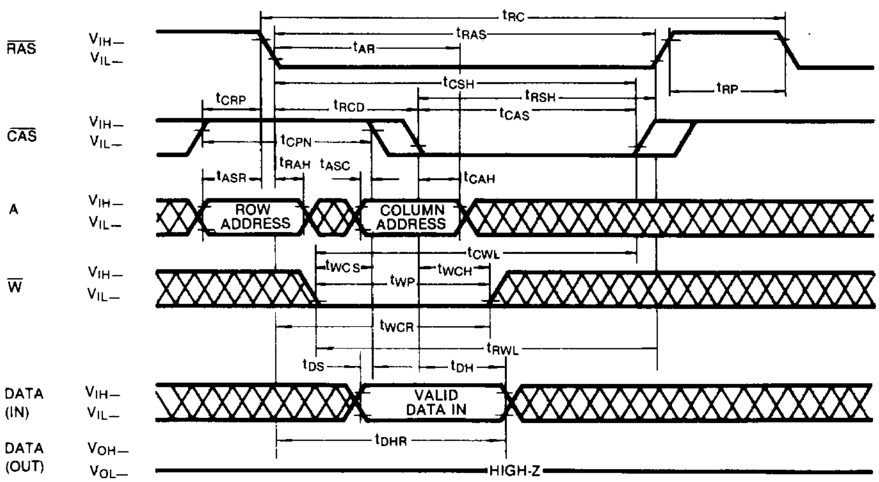
TIMING DIAGRAMS

READ CYCLE



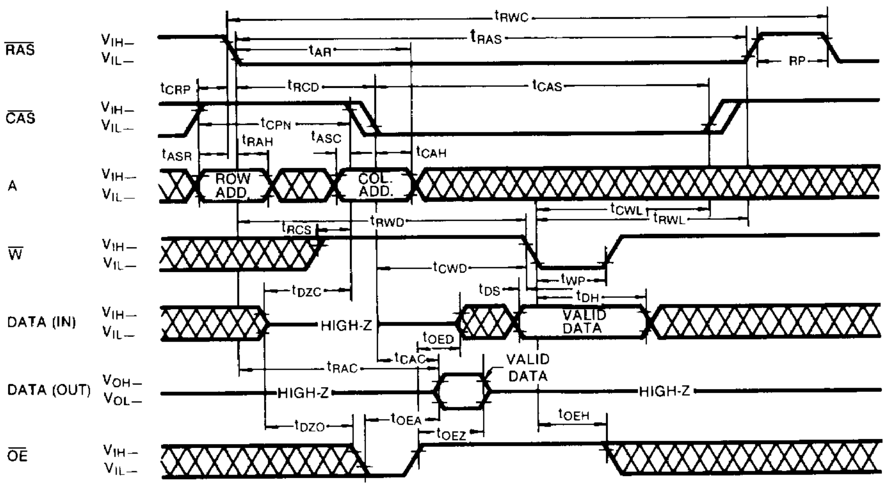
WRITE CYCLE (EARLY WRITE)

$\overline{OE}$ = Don't Care

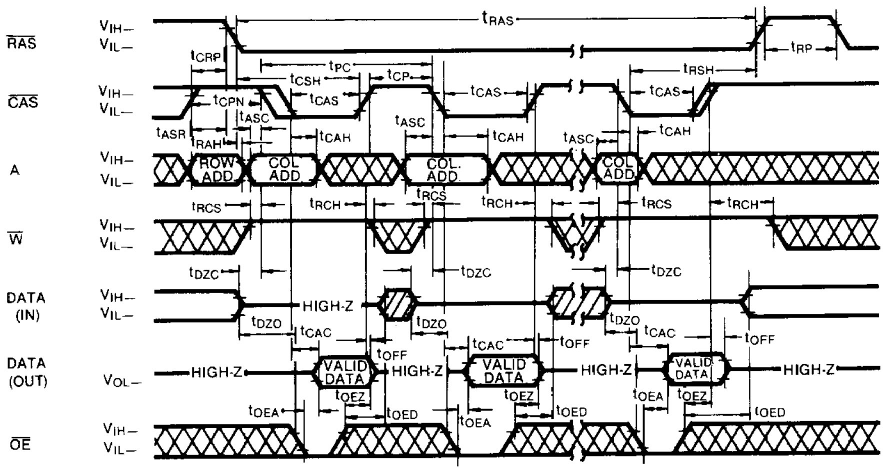


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



PAGE MODE READ CYCLE

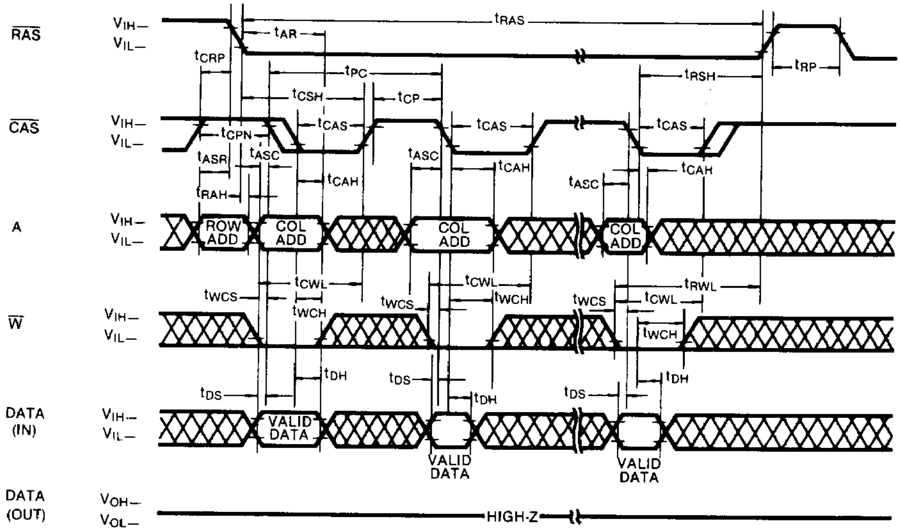


DON'T CARE

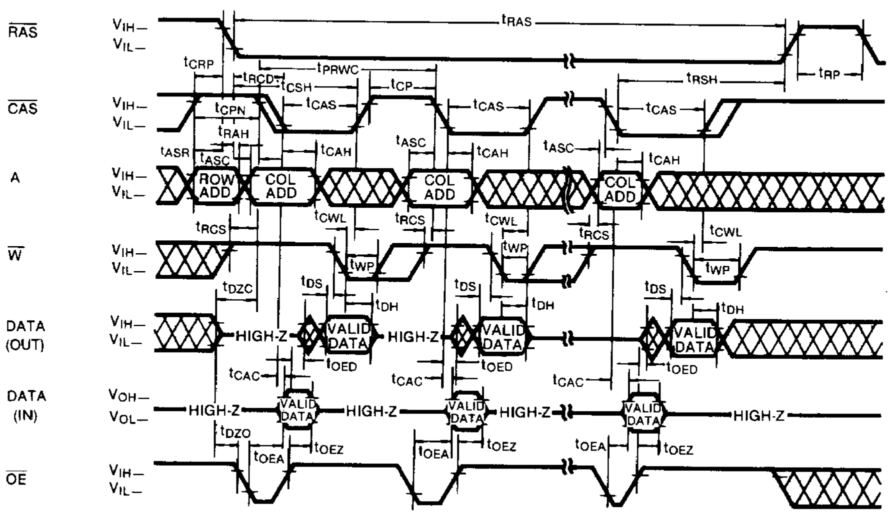
TIMING DIAGRAMS (Continued)

PAGE MODE WRITE CYCLE (EARLY WRITE)

$\overline{OE}$ = Don't Care



PAGE MODE READ-MODIFY-WRITE CYCLE

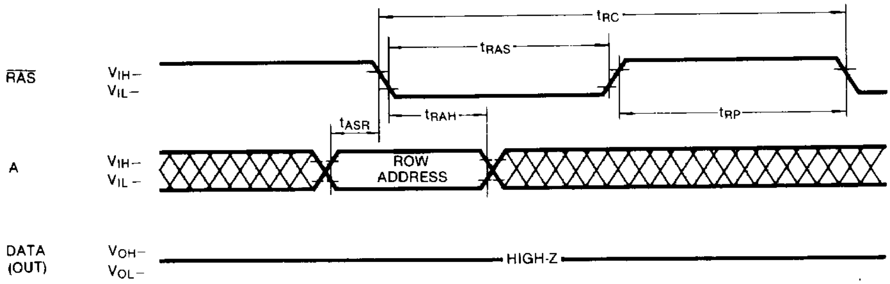


DON'T CARE

TIMING DIAGRAMS (Continued)

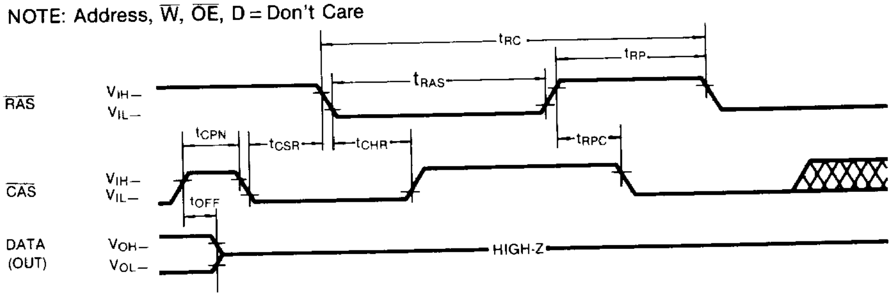
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{CAS} = V_{IH}$; $\overline{W}$, $\overline{OE}$, D = Don't Care

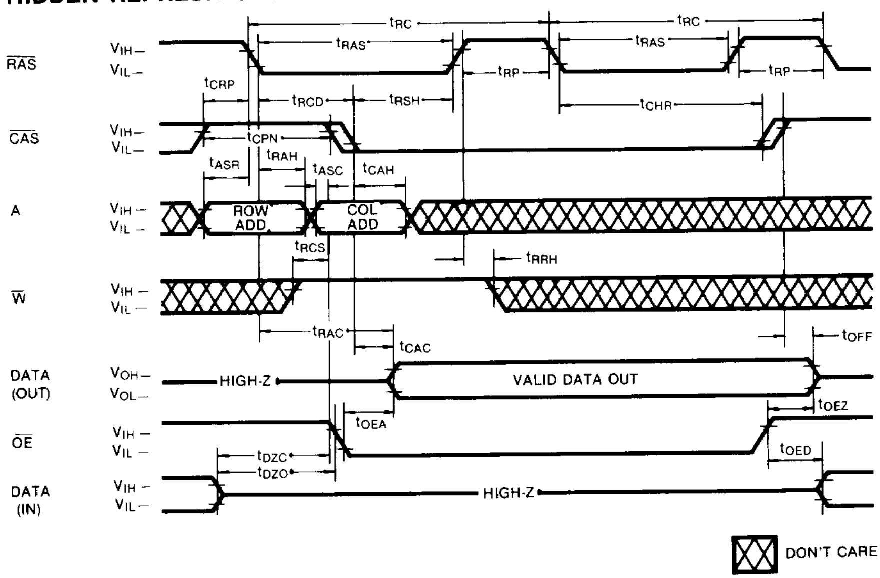


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address, $\overline{W}$, $\overline{OE}$, D = Don't Care



HIDDEN REFRESH CYCLE



KM41464A OPERATION

Device Operation

The KM41464A contains 262,144 memory locations organized as 65,536 x 4-bit words. Sixteen address bits are required to address a particular 4-bit word in the memory array. Since the KM41464A has only 8 address input pins, time multiplexed addressing is used to input 8 row and 8 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM41464A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 8 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41464A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse width are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41464A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The four outputs of the KM41464A remains in the Hi-Z state until valid data appears at the output. The KM41464A has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41464A can perform early write, and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the outputs remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the outputs before and during the time that data is being written into the same cell locations. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM41464's DQ pins.

Data Output

The KM41464A has three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. When either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs first remains in the Hi-Z state until the data is valid and then the valid data appears at the outputs. The valid data remains at the outputs until $\overline{CAS}$ or $\overline{OE}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41464A operating cycles are listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Page Mode Read, Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Page Mode write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM41464A is stored on a tiny capacitor within each memory cell. Due to leakage, the data will leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 4 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method

KM41464A OPERATION (Continued)

for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This must be performed on each of the 256 row addresses (A_0-A_7) every 4ms.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh: The KM41464A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs and the on-chip refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41464A hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required in hidden refresh cycles by DRAMS that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Other Refresh Methods: It is also possible to refresh the KM41464A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh are the preferred methods.

Page Mode

Page mode memory cycles provide faster access and lower power dissipaton than normal memory cycles. In page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS}=V_{SS}$ during power-up the KM41464A might begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 100μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 4 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41464A inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41464A input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMs.

Decoupling

The importance of proper decoupling cannot be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). The total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41464A using the shortest possible traces.

KM41464A OPERATION (Continued)

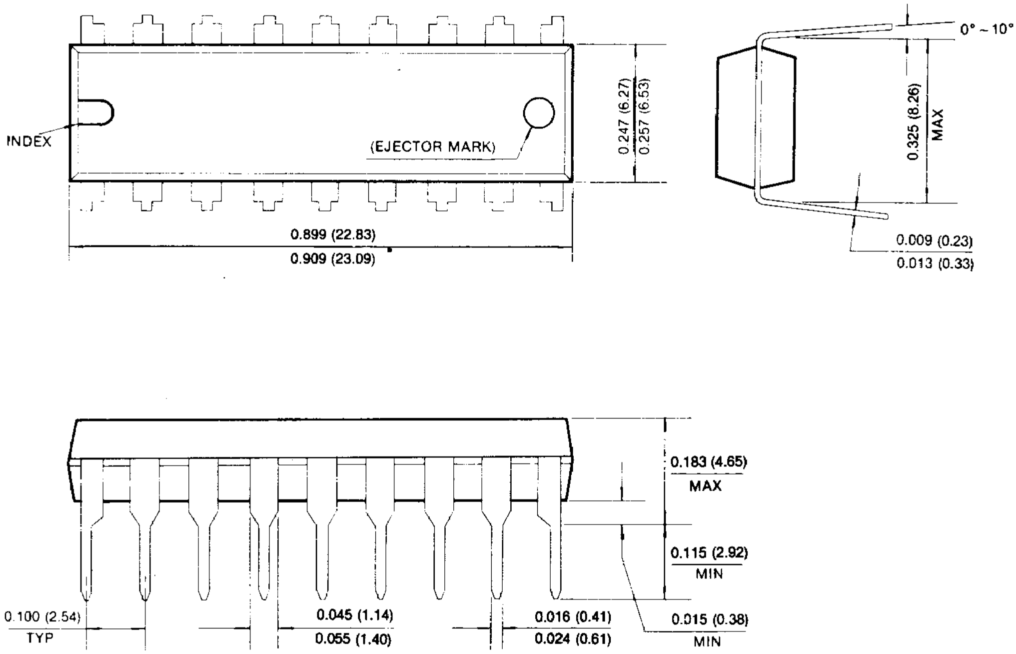
These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41464A and they supply much of the current used by the KM41464A during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

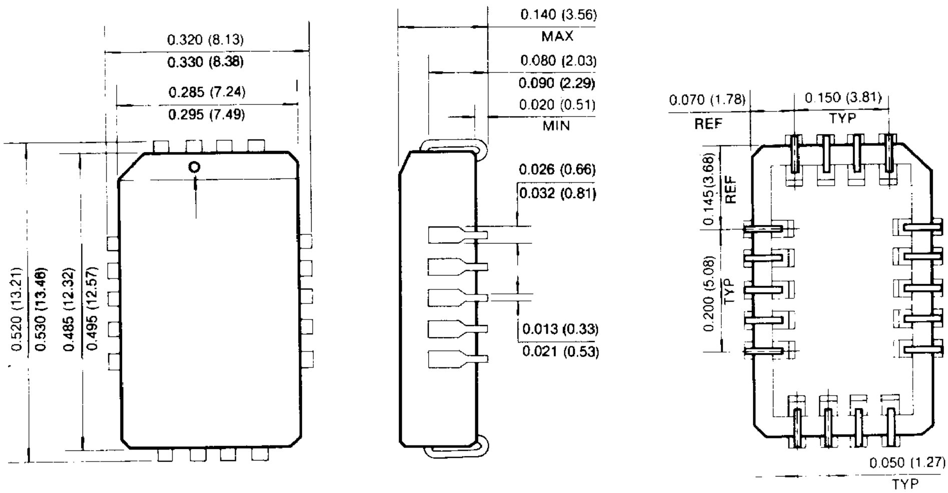
Units: Inches (millimeters)



PACKAGE DIMENSIONS (Continued)

18-PIN PLASTIC LEADED CHIP CARRIER

Units: Inches (millimeters)



20-PIN PLASTIC ZIGZAG-IN-LINE PACKAGE