FUJITSU

PARALLEL DATA I/O INTERFACE

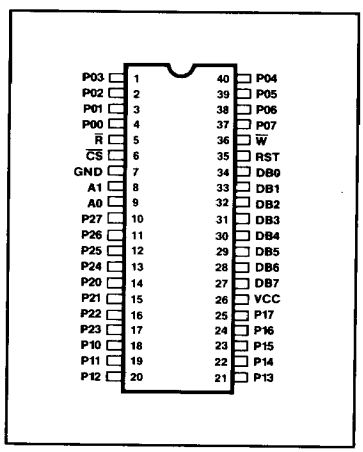
MB89255A

April 1986

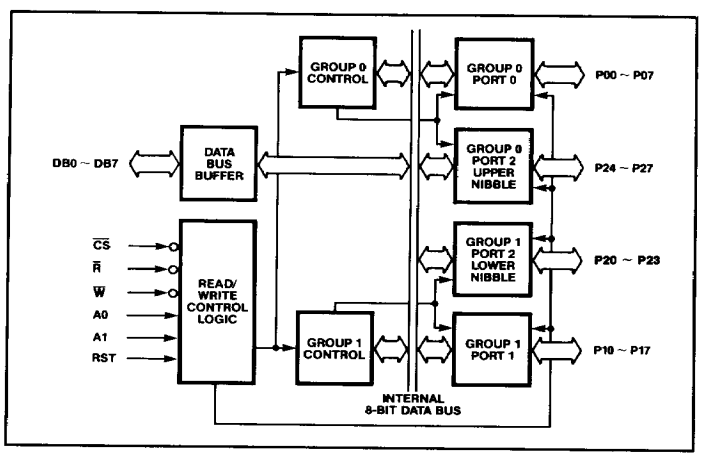
DESCRIPTION

The Fujitsu MB89255A Parallel Data I/O Interface provides an 8-bit bi-directional data-bus port and three 8-bit parallel I/O ports. Two of the I/O ports provide data transfers in byte segments whereas the other port is split with the upper and lower nibbles being transferred by separate busses. Thus, the MB89255A can be easily interfaced to hybrid 4-bit/8-bit systems. The user can choose either of three operating modes and can set or reset the state of each port bit. The MB89255A is fabricated in CMOS and is housed in a 40-pin plastic DIP. The device is functionally compatible with the Intel 8255A NMOS device.

PIN CONFIGURATION



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.