FUJITSU INTEGRATED CIRCUIT

FUJITSU

990684

PARALLEL DATA INPUT OUTPUT INTERFACE LSI

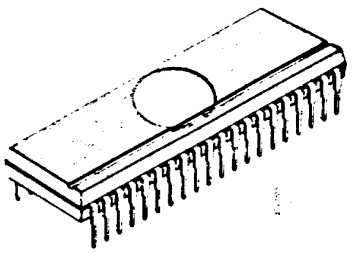
MB89255A

PARALLEL DATA INPUT OUTPUT UNIT

ADVANCED INFORMATION

REV.1.0 MAY 1987

Fujitsu MB89255A is one of the peripheral devices to be hooked up to standard microprocessors. This is a general purpose parallel interface device which has functions to select or detect parallel data input output operation by program. This device has three different modes (basic I/O mode, handshake mode etc.) as the operation modes This device has three 8-bit parallel I/O ports in between itself and peripheral terminals, and executes input output operation according to the operation mode defined by program, dividing those three 8-bit parallel ports to group of 12-bit ports Designed with CMOS technology to reduce power consumption, and housed in 40-pin standard DIP package.



DIP-40P-M01

Main features

+ Three operation modes
  Mode 0 : basic input output operation mode
  Mode 1 : handshake input output mode
  Mode 2 : bi-directional operation mode

+ Three of 8-bit parallel I/O ports
  port 0, port 1, port 2

+ Two groups of I/O ports
  group 0 : port 0 8-bit and upper nibble of port 2
  group 1 : port 1 8-bit and lower nibble of port 2

+ Programmable function operation mode selection

+ Set/reset function on each individual bit

+ Standard MPU interface

+ TTL level interface, +5V single power supply

+ Silicon gate CMOS process, Standard 40-pin DIP package

31 Researched orig

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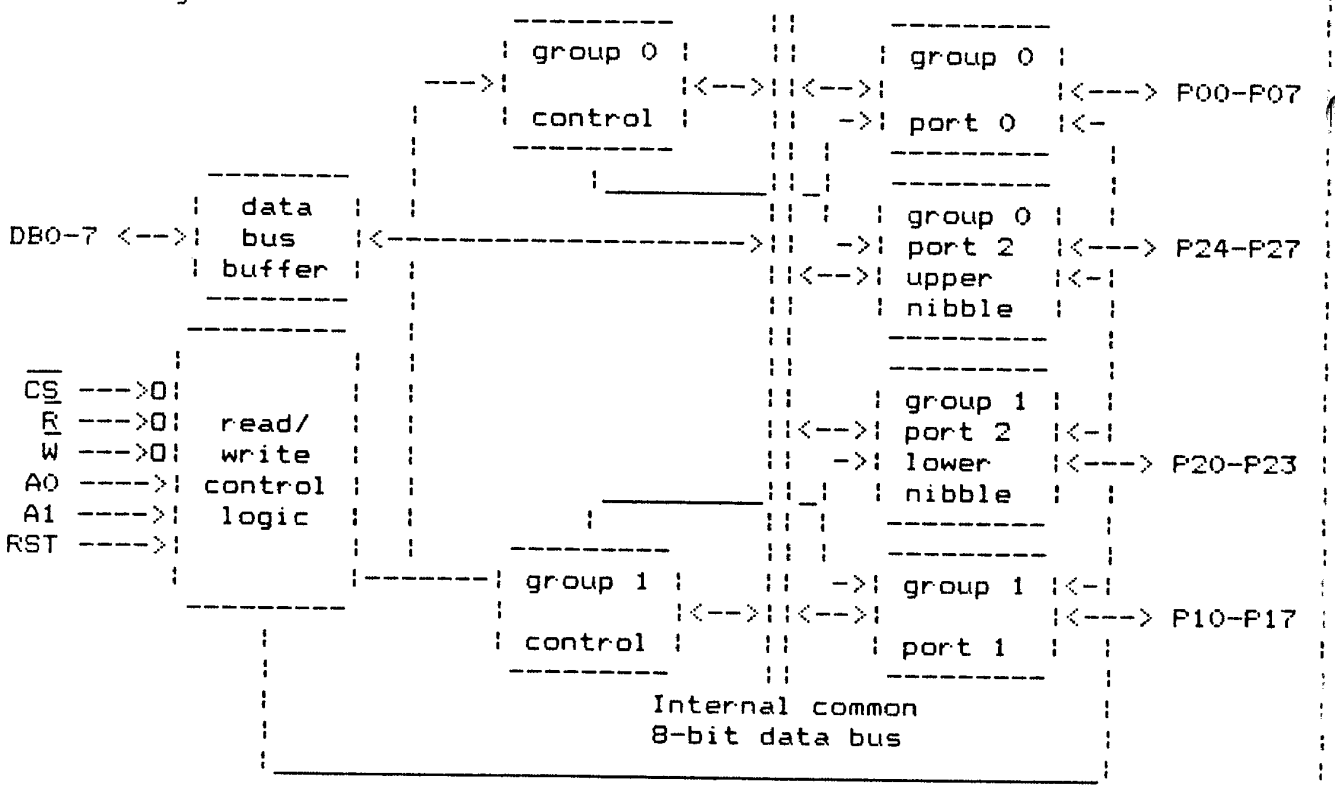
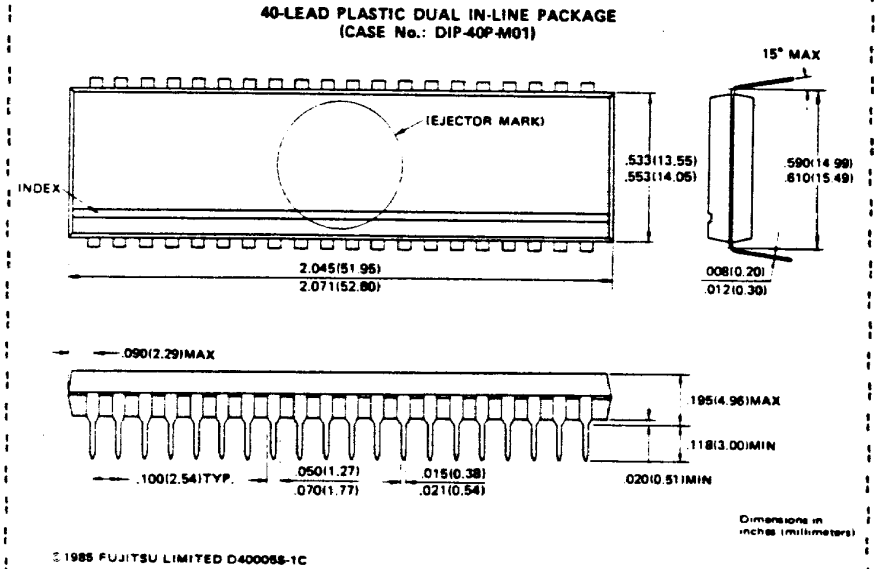
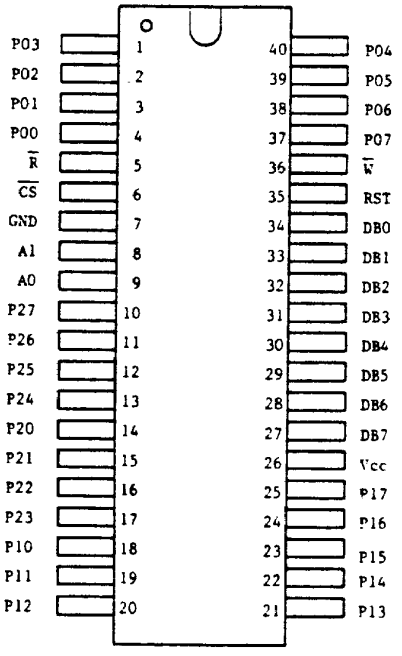
Block diagram



Package mechanical drawing



Signal pin assignment



Signal descriptions

Symbol	Pin No.	I/O	Descriptions
Vcc	40	-	+5V power supply
GND	20	-	Ground (0V)
P00-P07	1 - 4 37 - 40	I/O	8-bit general purpose I/O port 0 This port is included in group 0. By setting control parameters with software, three types of operation modes are used.
P10-P17	18 - 25	I/O	8-bit general purpose I/O port 1 This port is included in group 1. By setting control parameters with software, two types of operation modes are used.
P20-P27	10 - 17	I/O	8-bit I/O port 2. This port is used as general I/O port, handshake control, status data bit input, according to the operating function or mode setting on group 0 or 1.
DB0-DB7	27 - 34	I/O	8-bit bi-directional data bus to communicate with MPU. Gating and data transfer direction are controlled by CS, R, W signals.
$\overline{R}$	5	I	Read enable strobe input. Active "L" input signal to read data from the internal port, which is selected by combination of A0 and A1.
$\overline{W}$	36	I	Write enable strobe input. Active "L" input signal to write data to the internal port, which is selected by combination of A0 and A1.
$\overline{CS}$	6	I	Chip select input. When this input goes "L", DB0-7 are opened and MB89255A/B is allowed to communicate to MPU.
RST	35	I	Device initialization pulse input. When "H" level pulse is input to this pin, MB89255A/B is initialized. Initial stage settings are control parameter is 9B(HEX), mode of all ports is input in mode 0.

Electric characteristics

1. Absolute maximum ratings

Parameter	Symbol	Condition	Spec Min	Spec Max	Unit
Supply voltage	Vcc	GND = 0V Ta = 25degC	-0.3	+7.0	V
Input voltage	Vin		-0.3	Vcc+0.3	V
Output voltage	Vout		-0.3	Vcc+0.3	V
Operating temperature	Ta		0	70	degC
Storage temperature	Tstg		-55	150	degC

2. Recommended operating conditions

Supply voltage Vcc ..... +5V ± 10%
Vss 0V
(voltage is based on Vss level)

Operating temperature Ta .... 0 - 70 degC

3. DC characteristics

Vcc = +5V ± 10%, Vss = 0V, Ta = 0-70 degC

Parameter	Symbol	Condition	Spec Min	Spec Max	Unit
Supply current	Icc	All outputs open I/O write cycle time:400ns		10	mA
Standby current	Iccsb	All outputs open Standby		10	
Input leakage current	Iilk	0V < Vin < Vcc	-10	10	
Output leakage current	Iofl	0V < Vout < Vcc	-10	10	uA
Bus hold current	Ibhh	Vout = 3.0V, port0,1,2	-50	-300	

3. DC characteristics (Continued)

Vcc = +5V ± 10%, Vss = 0V, Ta = 0-70 degC

Parameter	Symbol	Condition	Spec Min	Spec Max	Unit
Darlington current	Idar	Vout = 1.5V, 750 ohm port 1,2 Up to any 8 ports out of port 1,2 The total current of those 8 ports is 45 mA at maximum	-2.0		mA
Input "L" voltage	Vil		-0.3	0.8	V
Input "H" voltage	Vih		2.0	Vcc+0.3	V
Output "L" voltage	Vol	Iol = 2.5mA		0.4	V
Output "H" voltage	Voh	Ioh = 2.5mA	3.0		V
		Ioh = -100uA	Vcc-0.4		V

4. Capacitance

Ta = 25 degC, Vcc = 0V

Parameter	Symbol	Condition	Spec Min	Spec Max	Unit
Input capacitance	Cin	fc = 1MHz, Unmesured pins returned GND		10	pF
Input/Output capacitance	Ci/o			20	pF

5. AC characteristics

Vcc = 5V ± 10%, Vss = 0V, Ta = 0 - +70 degC

Parameter	Symbol	Condition	Spec Min	Spec Max	Unit
Read pulse width	tRD		150		ns
Address set up time (to $\overline{R}$)	tADRD		0		
Address hold time (to $\overline{R}$)	tRDAD		0		
Data output delay time	tRDDT	CL = 150pF		120	
Data floating time	tDTRD		10	75	
Write pulse width	tWT		100		
Address set up time (to $\overline{W}$)	tADWT		0		
Address hold time (to $\overline{W}$)	tWTAD		20		
Data set up time (to $\overline{W}$)	tDTWT		100		
Data hold time (to $\overline{W}$)	tWTDT		20		
Access interval time	tRV		300		
Peripheral data set up time (to $\overline{R}$)	tSRD		0		
Peripheral data hold time (to $\overline{R}$)	tHRD		0		
$\overline{W}$ "H" to Output delay time	tWTOT	CL = 150pF		350	
Peripheral data set up time (to $\overline{STB}$)	tPTS		0		
Peripheral data hold time (to $\overline{STB}$)	tPTH		180		
$\overline{STB}$ pulse width	tSB		500		
$\overline{STB}$ "H" to INTR "H"	tSBIR	CL = 150pF		300	
$\overline{R}$ "L" to INTR "L"	tRDIR			400	
$\overline{R}$ "H" to IBF "L"	tRDI			300	
$\overline{STB}$ "L" to IBF "H"	tSBI			300	

5. AC characteristics (Continued)

Vcc = 5V ± 10%, Vss = 0V, Ta = 0 - +70 degC

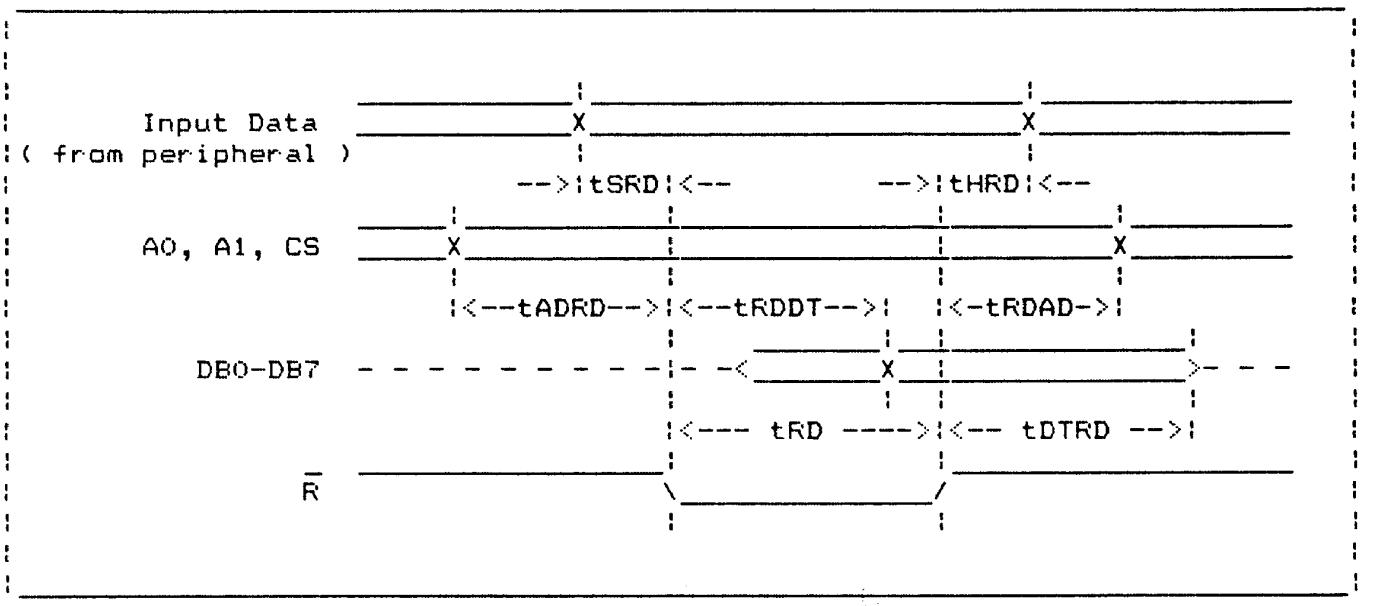
Parameter	Symbol	Condition	Spec		Unit
			Min	Max	
$\overline{W}$ "H" to $\overline{OBF}$ "L"	tWTO	CL = 150pF		650	ns
$\overline{ACK}$ "L" to $\overline{OBF}$ "H"	tAO			350	
$\overline{ACK}$ pulse width	tA		300		
$\overline{W}$ "L" to INTR "L"	tWTIR	CL = 150pF		450	
$\overline{ACK}$ "H" to INTR "H"	tAIR			350	
$\overline{ACK}$ "L" to Output delay time	tADTB			300	
$\overline{ACK}$ "H" to Output disable time	tADTF		20	250	
Reset pulse width	tRES		500		

Notes : The all timings of both input and output are in condition of Vl = 0.8V, Vh = 2.0V

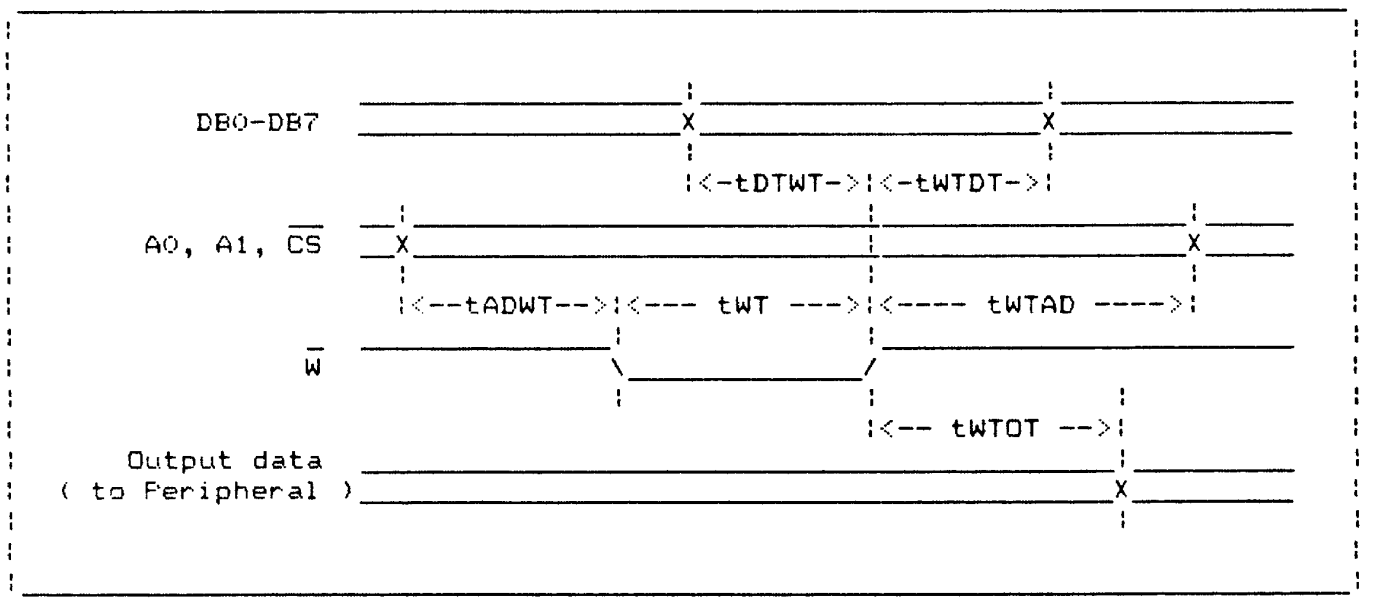
Reset pulse width (tRES) : The first reset pulse signal to be input right after power goes on is 50us at minimum.

Signal timing chart

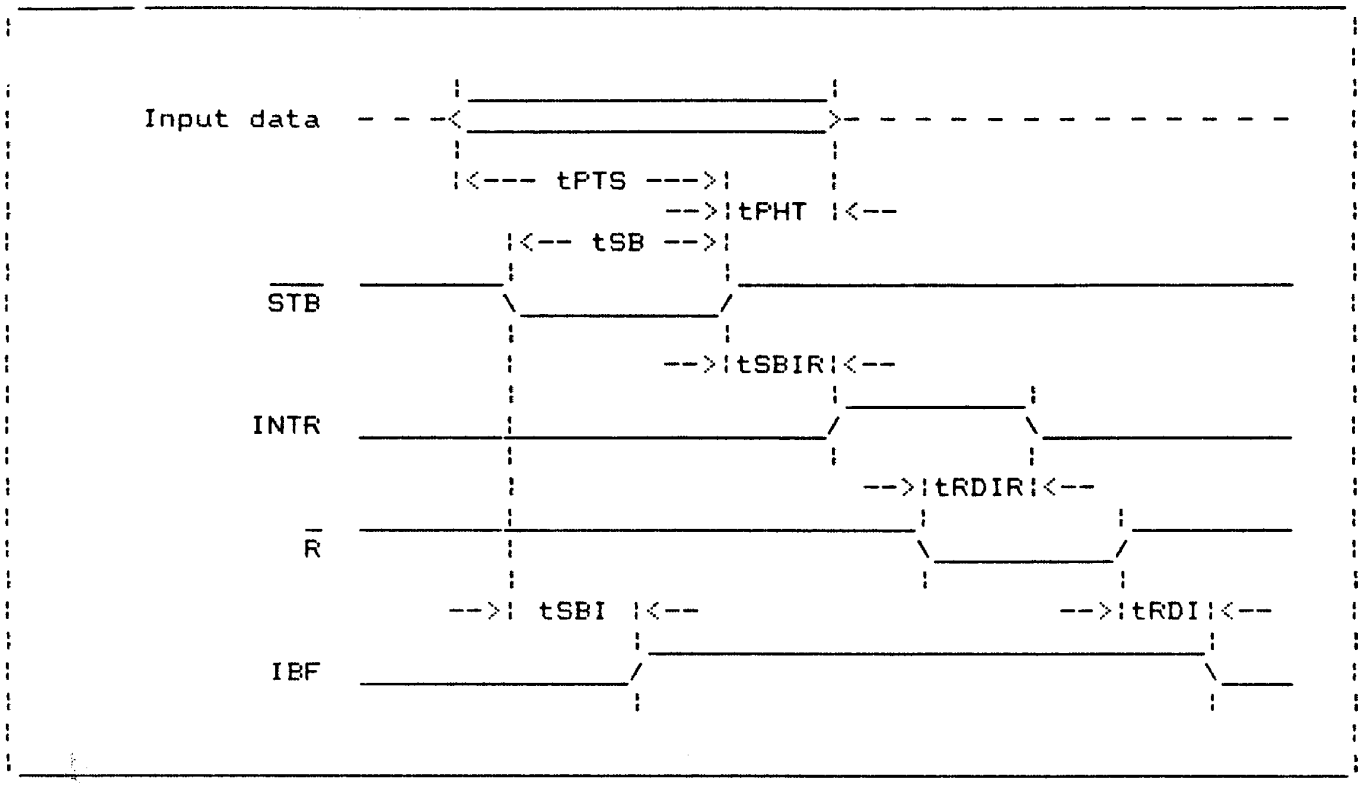
1. Mode 0 Input timing



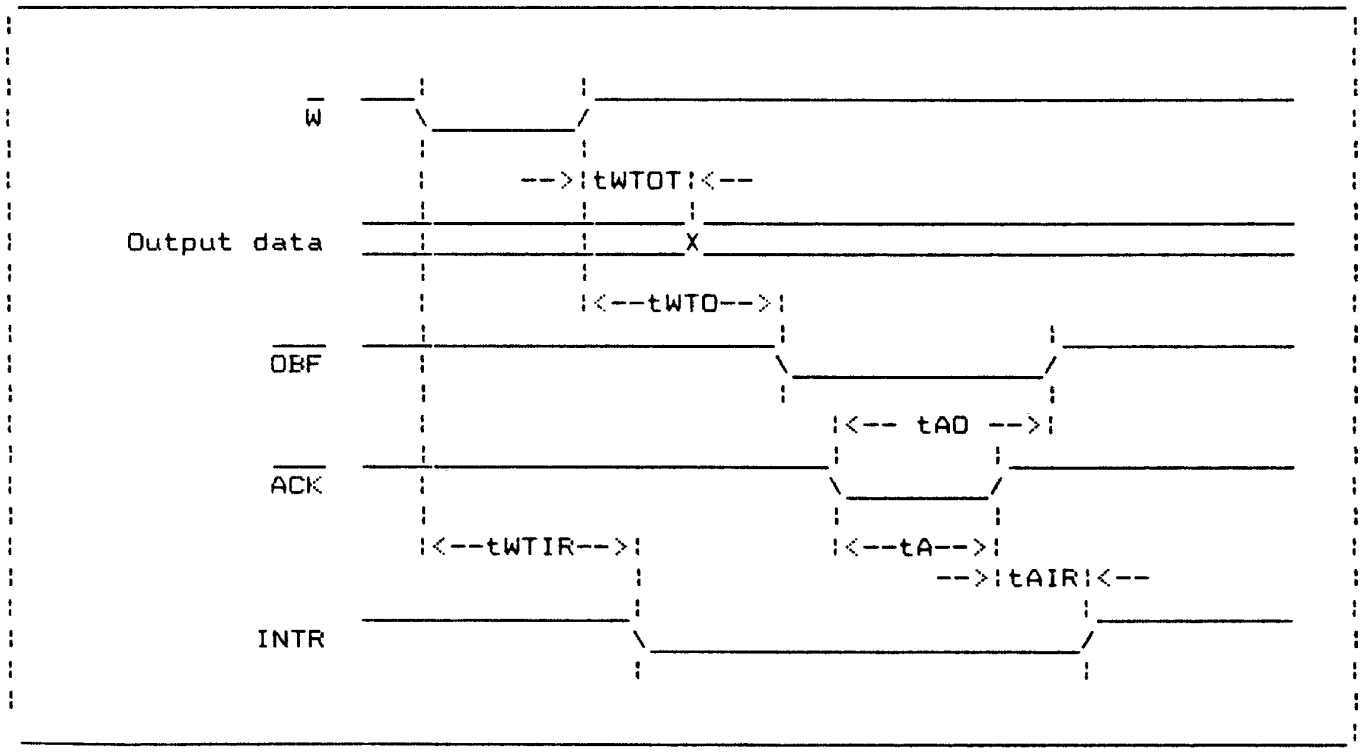
2. Mode 0 Output timing



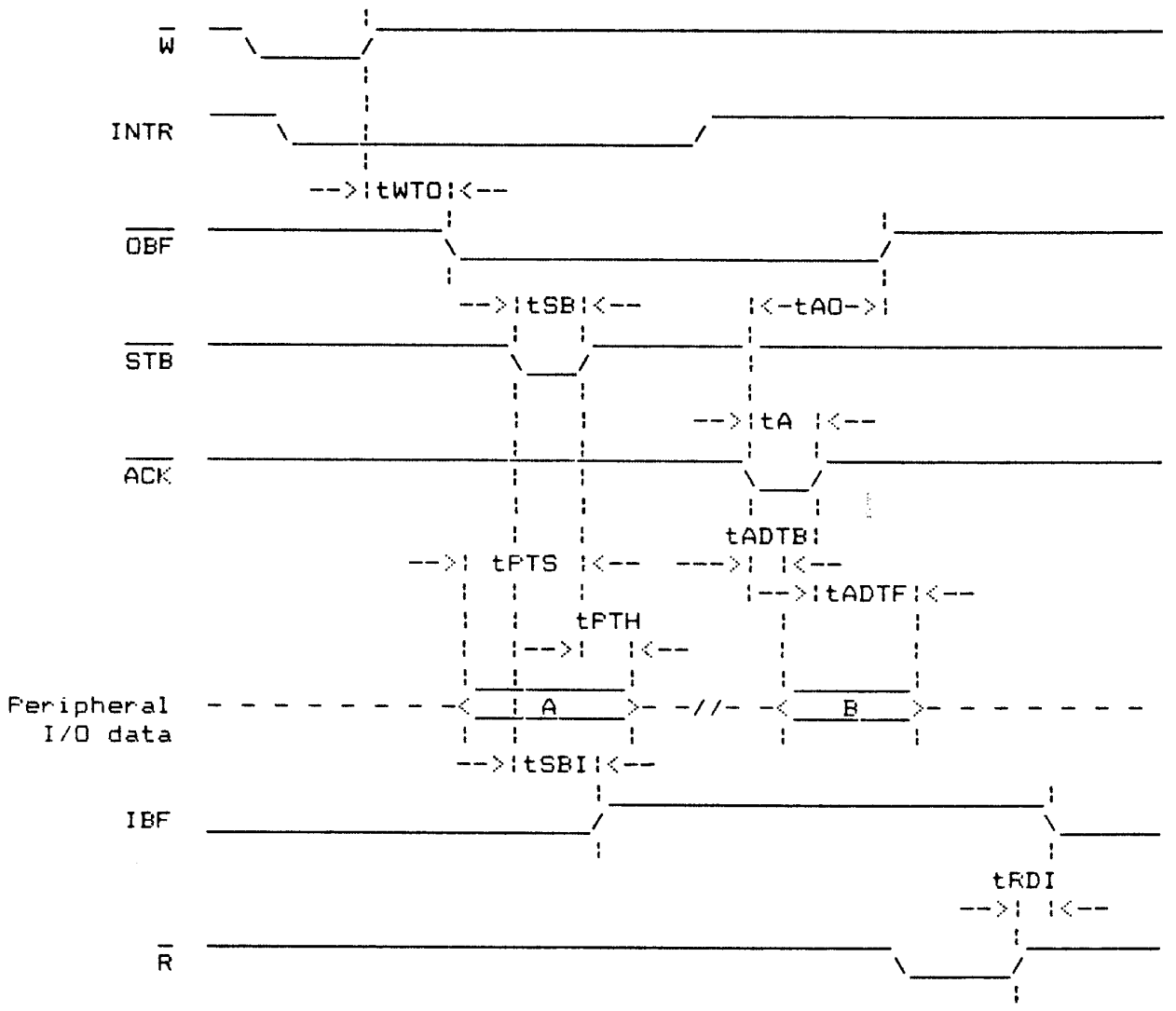
3. Mode 1 Input timing



. Mode 1 Output timing



This is the timing in case that pheripheral device has sent data right before MPU intent to send data to peripheral.

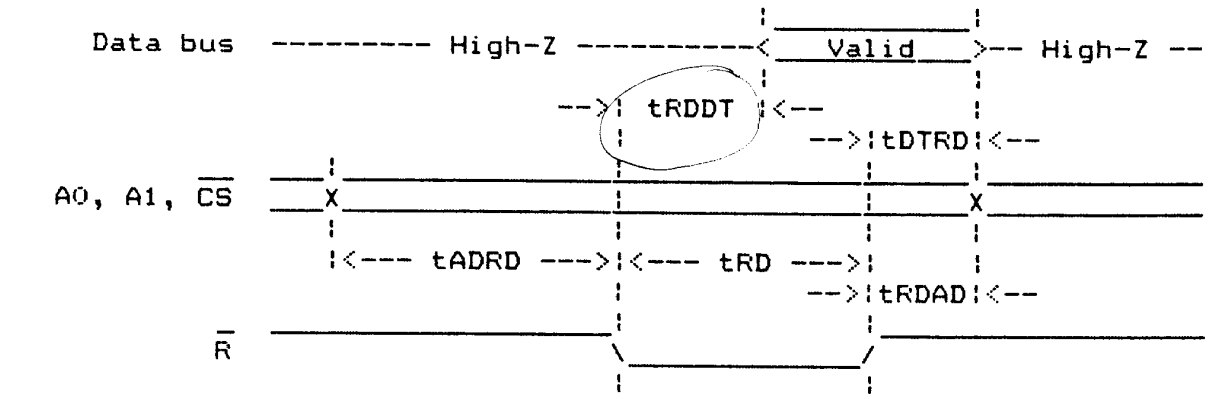


Data A : from peripheral to MB89255A

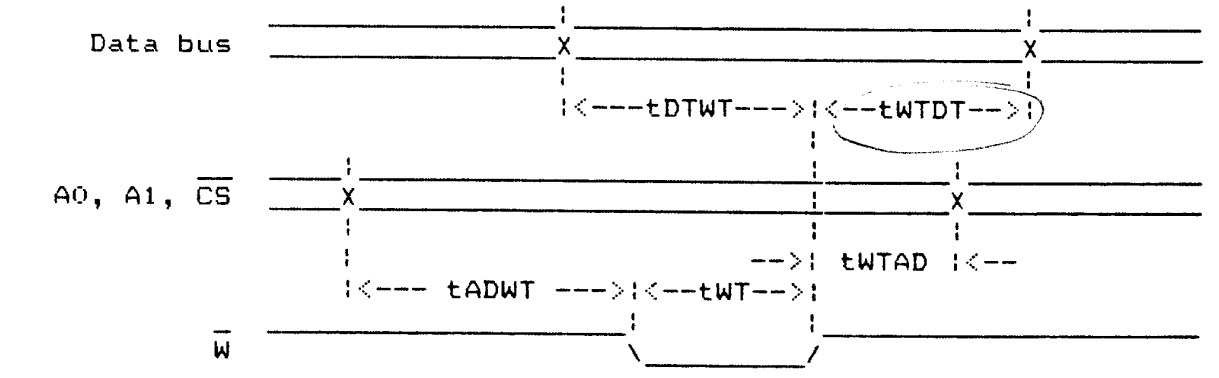
Data B : from MB89255A to peripheral

6. MPU access timing

Read timing



Write timing



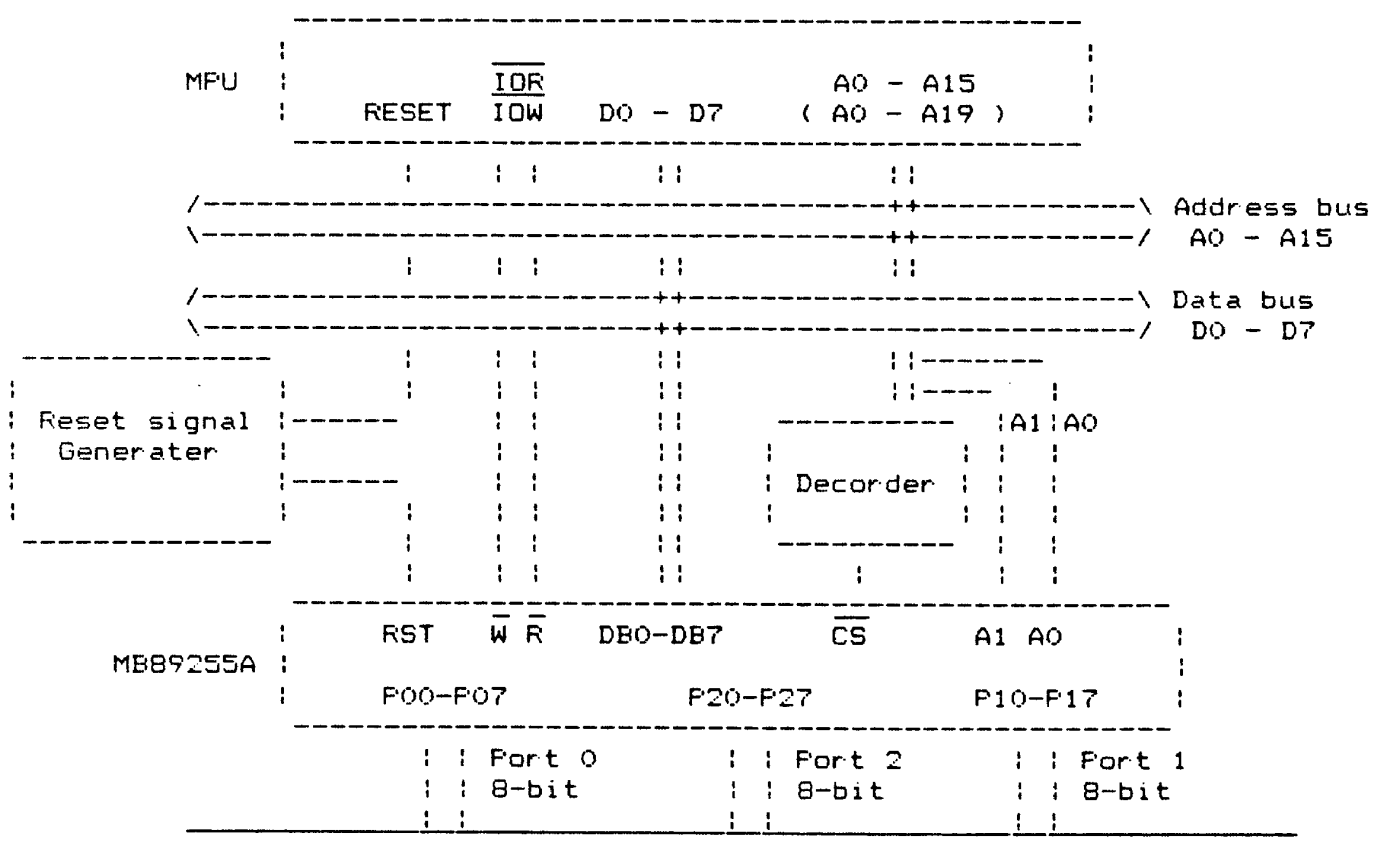
Connection to microprocessor

The following descriptions indicate the connecting method of MB89255A to standard microprocessor (MPU).

Signal relations

MPU		MB89255A
Bi-deirectional data bus	D0 - D7 (D8 - D15) <---------->	DB0 - DB7
Address bus	A0 - A15 (through decorder) ---------->	$\overline{CS}$, A0, A1
I/O read strobe	$\overline{IOR}$ ---------->	$\overline{R}$
I/O write strobe	$\overline{IOW}$ ---------->	$\overline{W}$
Initialization RESET	---------->	RST

MPU - MB89255A signals connection diagram



Peripheral device interface

Data transfer direction and access target

The data transfer in_between_microprocessor and MB89255A is controlled by the signals input to CS, R, W, A0, and A1. By those signals data transfer direction, bus open/close, and access target are determined. The condition of those signals and it's cooperate data bus operation is shown as follows:

CS	R	W	A1	A0	Data bus operation	
0	0	1	0	0	Port 0 data ---> MPU	Read
0	0	1	0	1	Port 1 data ---> MPU	
0	0	1	1	0	Port 2 data ---> MPU	
0	1	0	0	0	MPU ---> Port 0 data	Write
0	1	0	0	1	MPU ---> Port 1 data	
0	1	0	1	0	MPU ---> Port 2 data	
0	1	0	1	1	MPU ---> Control parameter	
1	X	X	X	X	Bus is closed (Tri-state level)	Other
0	0	1	1	1	Inhibitted	
0	1	1	X	X	Bus is closed (Tri-state level)	

Functional overview

Control word can't be read ⇒ no possibility for control word → MPU above

The parallel 24-bit I/O por o groups as group 0 (P00 - P07, P24 - P27) and group 1 - P23). Group 0 has 3 operation modes and group 1 has ion modes and to set (or reset) each bit on port 2, co used. Some certain value is set by program. The f s explain about each function on the operation mode and function on each bit of control parameter

Operation mode and it's function

Mode 0 : Basic input / output operation (group 0, group 1)

When MPU executes read operation (IN command, LOAD command), the data stored in each bit of the port is output to data bus and read by MPU at that time. When MPU executes write operation (OUT command, STORE command), the output data from MPU is latched and stored to the each bit of the port.

Mode 1 : Handshake input / output operation (group 0, group 1)

Handshake signals are used to define acurate data transfer timing between MB89255A and peripheral devices. STB signal (Strobe signal, from MB89255A to peripherals), IBF signal (Input Buffer Full, from MB89255A to peripherals), and INTR signal (Interrupt signal, from MB89255A to MPU) are used as the handshake signals, when data is input to MB89255A from peripherals. The input data to MB89255A's port is latched by STB signal.

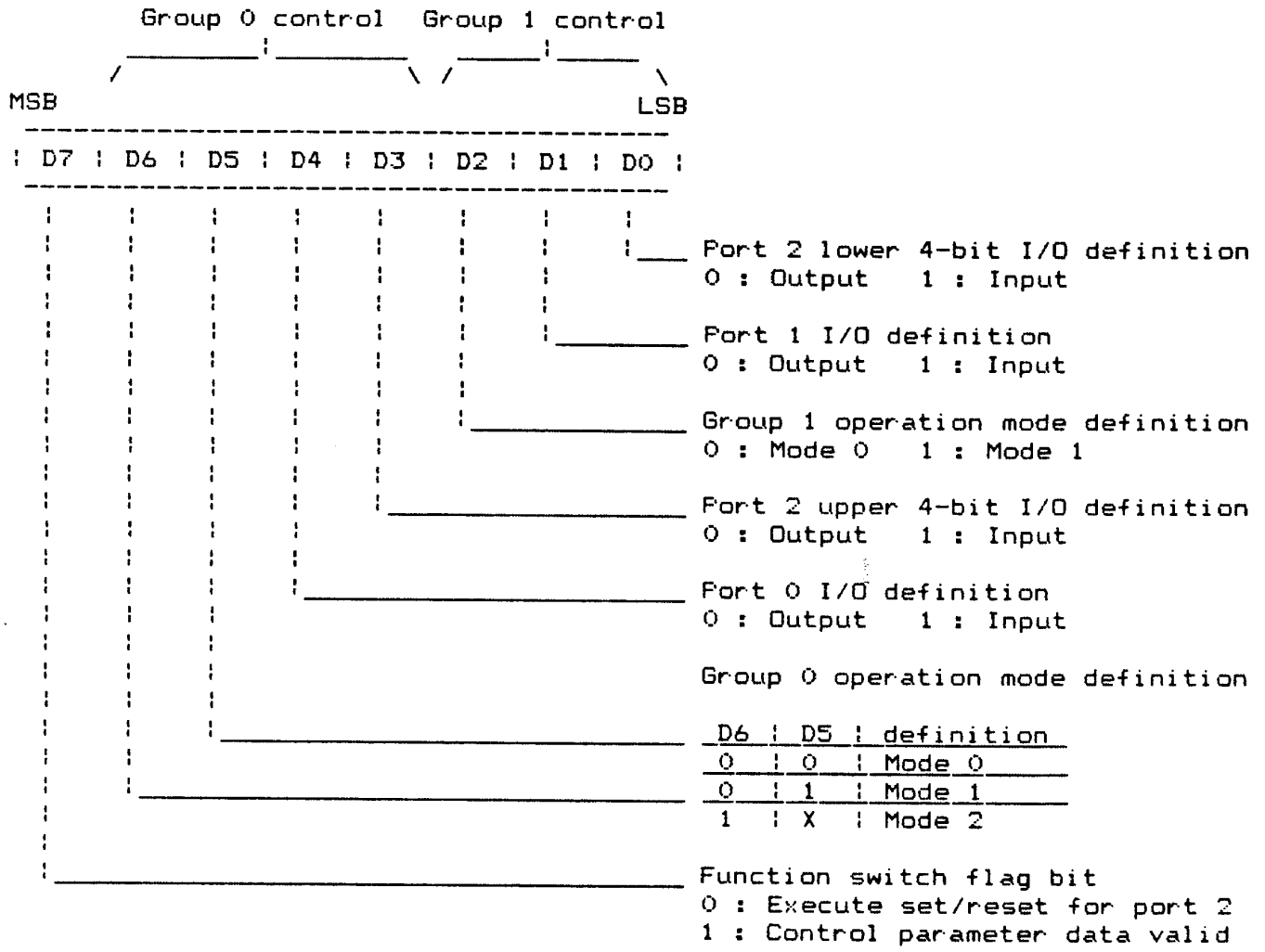
$\overline{\text{ACK}}$ signal (Acknowledge signal, from peripherals to MB89255A), $\overline{\text{OBF}}$ signal (Output Buffer Full, from MB89255A to peripherals), and INTR signal (Interrupt signal, from MB89255A to MPU) are used as the handshake signals when data is output to peripherals from MB89255A. MB89255A recognizes the data was received by peripherals, by ACK signal.

Mode 2 : Bi-directional operation (group 0)

This function is approxmately similar to the function of input operation + output operation on mode 0. Since port is used bi-directionally switching data transfer direction actively, consecutive data output operation is forbidden. Therefore, the port keeps high-impedance level till ACK signal (Acknowledge signal) commes, when that is used as an output port. Right after ACK signal is received, the data is output from that port

Control parameters

The operation on group 0 and 1 is selected by control parameter. The function on each bit of this control parameter is as follows:



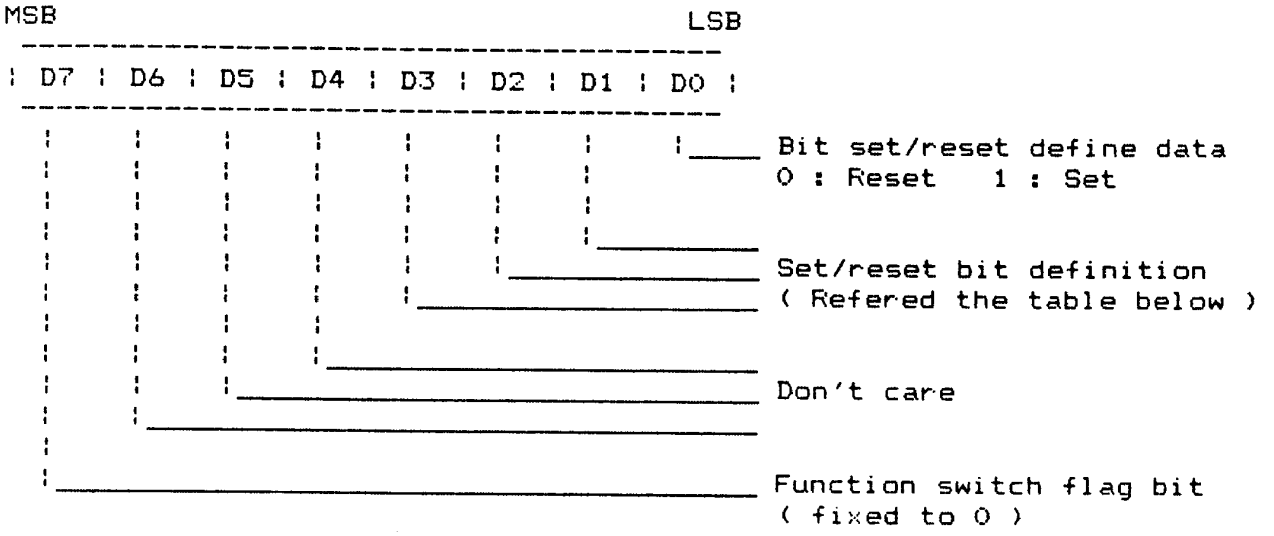
When control parameter is set, the data latch in each port is cleared Especially when operation mode is defined to Mode 1 or Mode 2, INTE bit (interrupt enable bit) of port 2 is also cleared, so interrupt operation is not done. To generate interruptions, INTE bit should be set to "1" by using port 2 bit set/reset function.

When initialization RST signal is provided, 9B HEX is automatically set as an initial control parameter.

```
D6, D5 : 00 --- Set Mode 0 to group 0
    D4 : 1  --- Define port 0 to input mode
    D3 : 1  --- Define upper 4-bit on port 2 to input mode
    D2 : 0  --- Set Mode 0 to group 1
    D1 : 1  --- Define port 1 to input mode
    D0 : 1  --- Define lower 4-bit on port 2 to input mode
```

Bit set/reset function

The all bits assigned on port 2 can be individually set or reset. This operation is executed by setting control parameters following the format as follows (data with MSB = 0). This function is applicable on all operation modes. For the bit which is on input mode, this function just change the internal latch's data and doesn't affect any other things.



Destination bit	P20	P21	P22	P23	P24	P25	P26	P27
D1	0	1	0	1	0	1	0	1
D2	0	0	1	1	0	0	1	1
D3	0	0	0	0	1	1	1	1

Detail functional descriptions

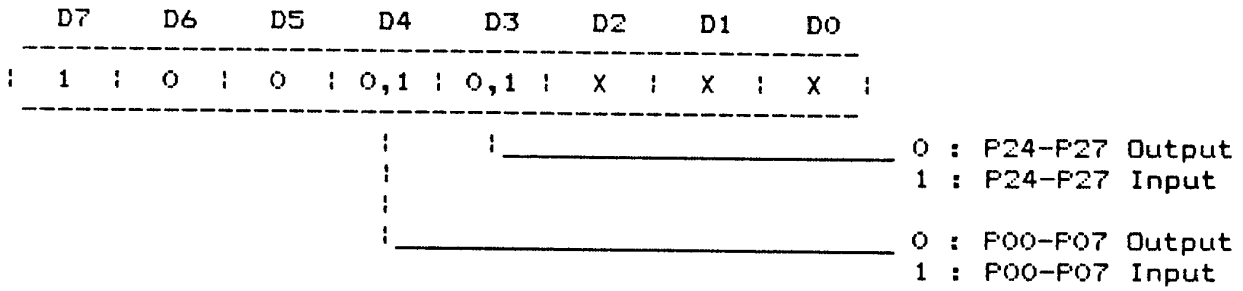
Status data

Port 2, which belongs to the group, which was defined to either mode 1 or 2, supplies status data to MPU, and on the other hand that is used as handshake control port by peripheral devices. Once each port is defined to either mode 1 or mode 2, INTE bit (interrupt enable bit) in status data is cleared, so interrupt function is no longer valid. When interrupt function is enabled, set "1" on this INTE bit using port 2 bit set/reset function Once a group is defined to either mode 1 or mode 2, data can't be written to the port 2 bits assigned in that group. And P23 (bit-3 of port 2) belongs to group 1, however that bit is used as a control pin for group 0 and isolated from group 1, if group 0 is in either mode 1 or mode 2.

Mode 0 : Basic input/output operation

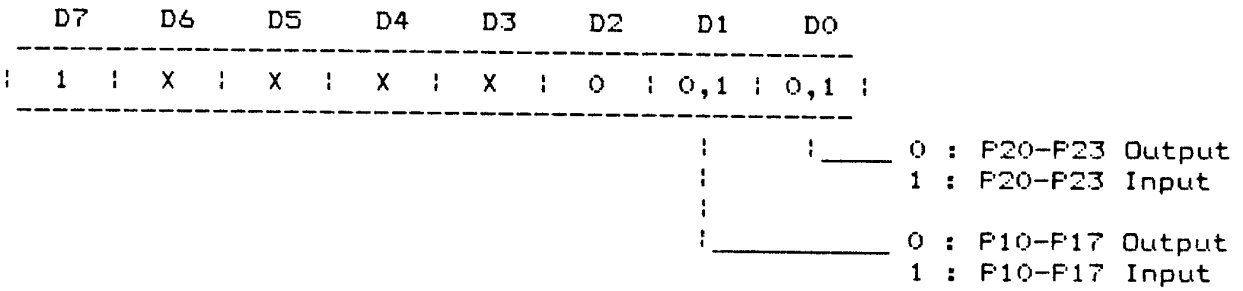
Group 0

Control parameter D3 and D4 define port 0 (P00-P07) and upper 4-bit on port 2 (P24-P27) individually to be used either input mode or output mode. The input/output operation is as described on the functional overview The control parameter in this case is as follows:



Group 1

Control parameter D0 and D1 define port 1 (P10-P17) and lower 4-bit on port 2 (P20-P23) individually to be used either input mode or output mode. The input/output operation is as described on the functional overview Especially on P23, the point described on status data should be payed attention to. The control parameter in this case is as follows:



Mode 1 : Handshake input/output operation

Input handshake operation signals

$\overline{STB}$ (Strobe signal)

When data is transfered from peripheral to MPU, peripheral sets this signal "L" and indicates to MB89255A that there is a valid data. MB89255A receives data while this signal is "L" and latches that data at the rising edge of this signal.

$\overline{IBF}$ (Input Buffer Full signal)

MB89255A informs to peripheral that he latched a new data by setting this signal "H". This signal is set to "H" at the falling edge of STB signal and reset to "L" at the rising edge of R signal from MPU.

INTR (Interrupt signal)

MB89255A informs to MPU that he latched a new data on a port by setting this signal "H". Since this signal is logical AND of IBF signal and INTE bit on status data, INTE bit should be set to "H" before using this signal.

Group 0

The followings indicate the control parameter to set mode 0 input mode to group 0 and status data.

Control parameter value

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0,1	X	X	X

D3: 0 : P26,27 Output
1 : P26,27 Input

Function of each bit on status data

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBF0	INTE0	INTR0	X	X	X

Group 1

The followings indicate the control parameter to set mode 1 input mode to group 1 and status data.

Control parameter value

D7	D6	D5	D4	D3	D2	D1	D0
1	X	X	X	X	1	1	0,1

D0: 0 : P23 Output
1 : P23 Input

Function of each bit on status data

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	I/O	INTE1	IBF1	INTR1

Output handshake operation signals

$\overline{ACK}$ (Acknowledge signal)

Peripheral device informs to MB89255A that he received data from MB89255A by setting this signal "L".

$\overline{OBF}$ (Output Buffer Full signal)

MB89255A informs to peripheral device that a new data is output by setting this signal "L". This signal is set to "L" a little later than the rising edge of W signal from MPU and reset to "H" at the falling edge of ACK signal.

INTR (Interrupt signal)

MB89255A informs to MPU that the port is ready to receive a new data by setting this signal "H". Since this signal is logical AND of ACK signal and INTE bit on status data, INTE bit should be set to "H" before using this signal.

Group 0

The followings indicate the control parameter to set mode 1 output mode to group 0 and status data.

Control parameter value

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	0,1	X	X	X

D3 : 0 : P24,25 Output
1 : P24,25 Input

Function of each bit on status data

D7	D6	D5	D4	D3	D2	D1	D0
OBF0	INTE0	I/O	I/O	INTR0	X	X	X

Group 1

The followings indicate the control parameter to set mode 1 output mode to group 1 and status data.

Control parameter value

D7	D6	D5	D4	D3	D2	D1	D0
1	X	X	X	X	1	0	0,1

D0 : 0 : P23 Output
1 : P23 Input

Function of each bit on status data

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	I/O	INTE1	OBF1	INTR1

Mode 2 : Bi-directional operation

Handshake signals

$\overline{STB}$ (Strobe signal)

Peripheral device informs to MB89255A that valid data is output to the port by setting this signal to "L". MB89255A receives daTa while this signal is "L" and latches the data at the rising edge of this signal.

IBF (Input Buffer Full signal)

MB89255A informs to peripheral that he latched a new data on his port by setting this signal "H". This signal is set to "H" at the falling edge of STB signal from peripheral, and reset to "L" at the rising edge of R signal from MPU.

$\overline{ACK}$ (Acknowledge signal)

Peripheral device informs to MB89255A that he is ready to accept a new data from MB89255A by setting this signal "L". MB89255A outputs data to the port only while this signal is "L", and keeps port in high impedance level for the rest of time.

$\overline{OBF}$ (Output Buffer Full signal)

MB89255A informs to peripheral that he is ready to output a new data from the port by setting this signal "L". This signal is set to "L" a little delayed from the rising edge of W signal from MPU, and reset to "H" at the falling edge of ACK signal from peripheral.

INTR (Interrupt signal)

MB89255A generates interrupt to MPU by setting this signal "H". This signal indicates that the data on the output latch is received by peripheral while INTE 1 bit (Interrupt enable bit) on status data is "1". Also this signal indicates that a new data is written to the input latch while INTE 2 bit is set to "1". If "1" is set to both INTE 1 and INTE 2, this signal goes "H" at the timing when either condition as above appears.

Group 0

The followings indicate the control parameter to set mode 2 to group 0 and status data.

Control parameter value

D7	D6	D5	D4	D3	D2	D1	D0
1	1	X	X	X	X	X	X

Function of each bit on status data

D7	D6	D5	D4	D3	D2	D1	D0
OBF0	INTE1	IBF0	INTE2	INTR0	X	X	X

This mode switches the data transfer direction of the port actively, so that the following attentions are required:

* The peripheral device mustn't either output data or set $\overline{\text{STB0}}$ signal "L" while keeping ACK0 signal "L".

* Peripheral device mustn't set $\overline{\text{ACK0}}$ signal "L", while keeping $\overline{\text{STB0}}$ signal "L".