Centro de Investigación y de Estudios Avanzados

TAE 2023 – ASIC DESIGN

DDS

SoC Design Methodology

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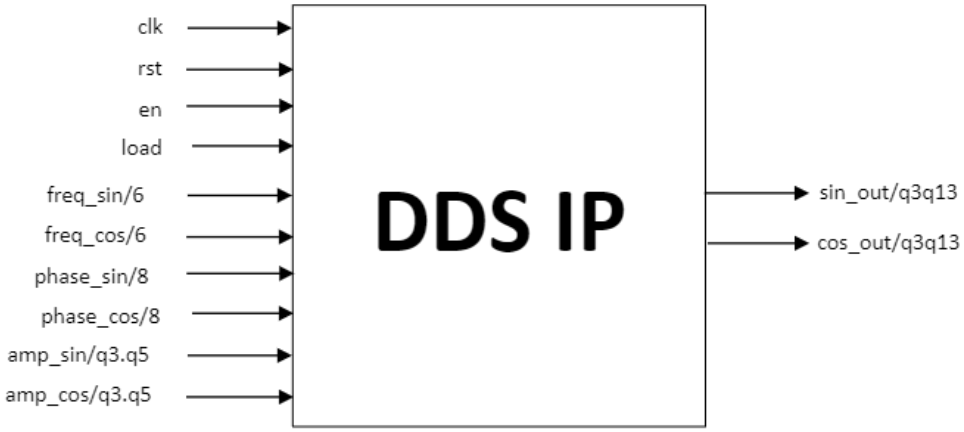
PROBLEM DESCRIPTION

We must design and implement a complex-value Direct Digital Synthesizer in SystemVerilog HDL, wit a fixed point, dynamic range of (+4 ,- 4).

BLACK BOX



The top level block will require the following I/O ports:

Inputs:

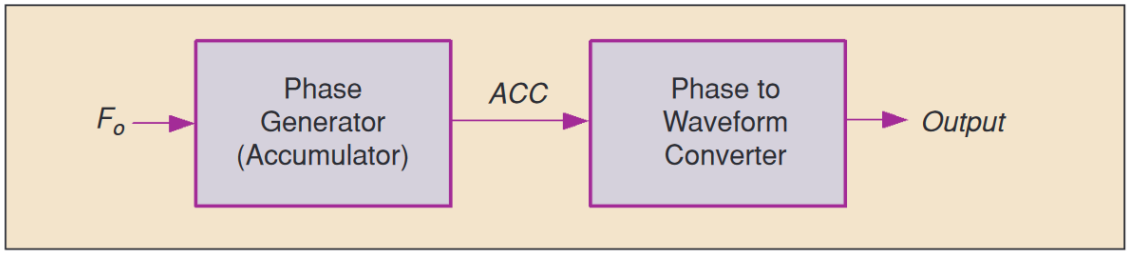
- clk & rst = Signals for synchronization and reseting.
- en = It will determine whether we have an output signal or not.
- load = It will eventually allow us to write our own signals in the LUT.
- freq_sin & freq_cos = They will adjust the frequency of the output signals.
- phase_sin & phase_cos = They will adjust the phase of the output signals.
- amp_sin & amp_cos = They will adjust the amplitude of the output signals.

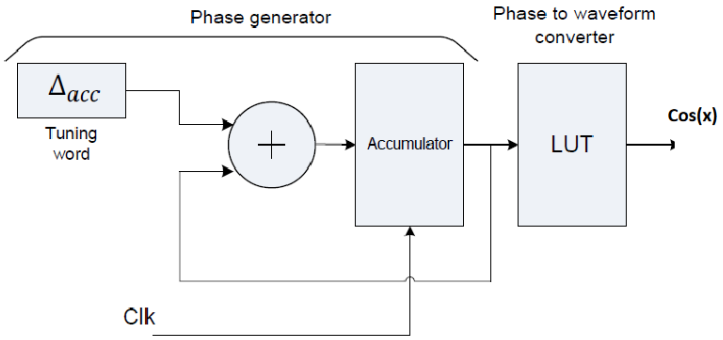
Outputs:

- sin_out & cos_out = They are the output signals, in a fixed point q3.q13 format.

PSEUDOCODE GENERATION

To generate our pseudocode, we start by analyzing the DDS basic theory:





Pseudocode

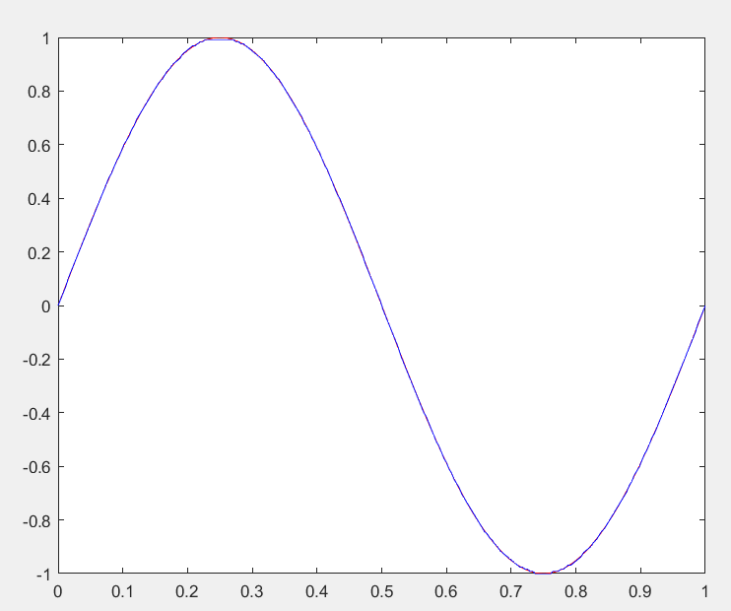
1.- sin_out = 0;
2.- cos_out = 0;
3.- if en = 1, goto 6;
4.- else goto 1
5.- if load = 1, goto 5
6.- else goto 7;
7.- sin_LUT_out = reg_acc_sin + phase_sin;
8.- cos_LUT_out = reg_acc_cos + phase_sin;
9.- reg_acc_sin = reg_acc_sin + freq_sin_in;
10.- reg_acc_cos = reg_acc_cos + freq_cos_in;
11.- sin_out = amp_sin * sin_mem_out;
12.- cos_out = amp_cos * cos_mem_out;
13.- goto 1

Now, we have to select the fixed point format for our ouptput, to compy with our requisites of an output of (+4 ,- 4) . To comply, we determine our output to have a signed, 16 bit word of q3.q13. To make sure this configuration works, we simulate its resulting signal with the follwing Matlab code:

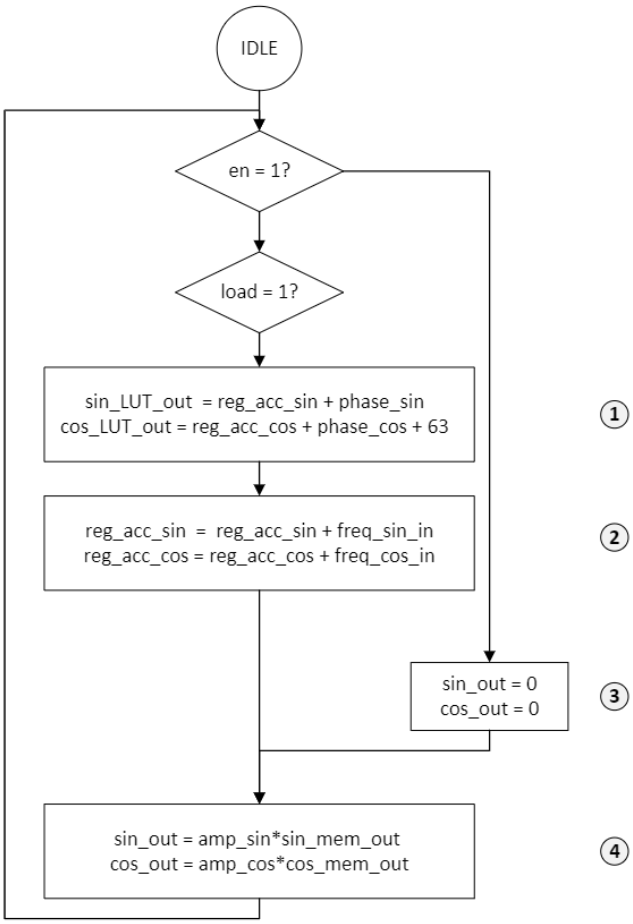
Pseudocode

```
Clc
close all
clear all

fmax = 1
Fs = fmax*255
Time = 0:1/Fs:1;%linspace(0,1,1024);
fo = 10;

sinusoid = sin(2*pi*fmax*Time);
amplitud = 2;
sinusoid_amp_out = sin(2*pi*fmax*Time)*amplitud;

WordLength = 8
QI_sinusoid = 1;
QF_sinusoid = WordLength-QI_sinusoid;

signalfxp = fi(sinusoid,1,WordLength,QF_sinusoid);
figure;plot(Time,sinusoid,'r');

hold on;plot(Time,signalfxp,'b');
```

With it, we get the resulting graph of "true" output vs fixed-point output, which, as we can see, is a very Good aproximation:

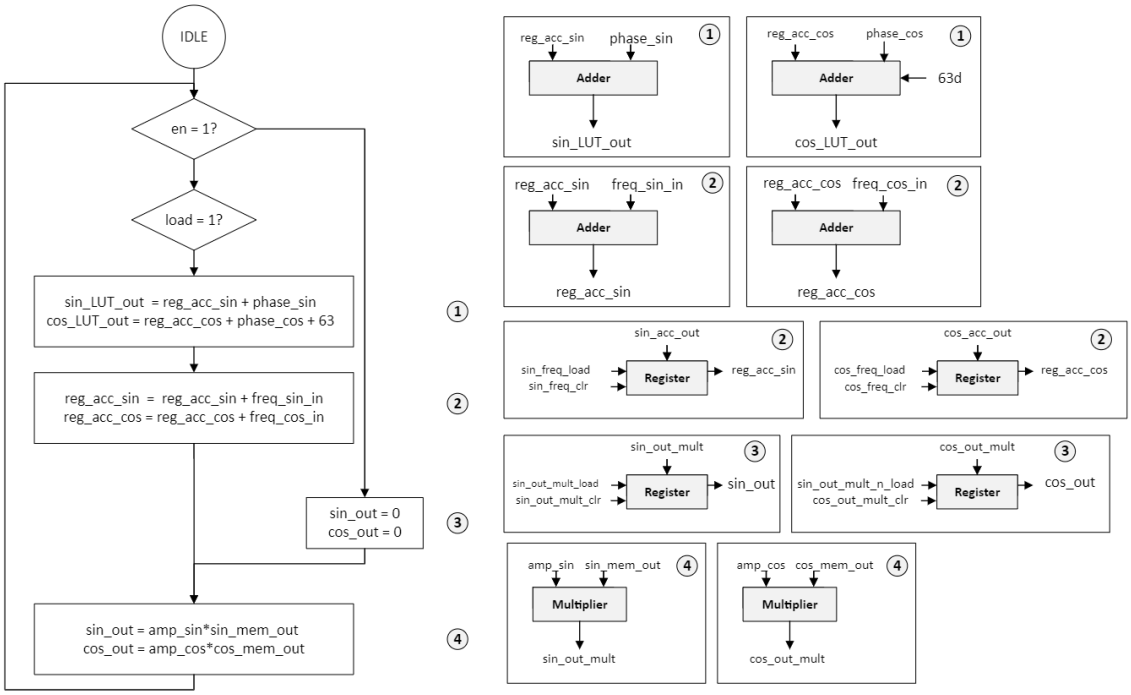


ASM DIAGRAM

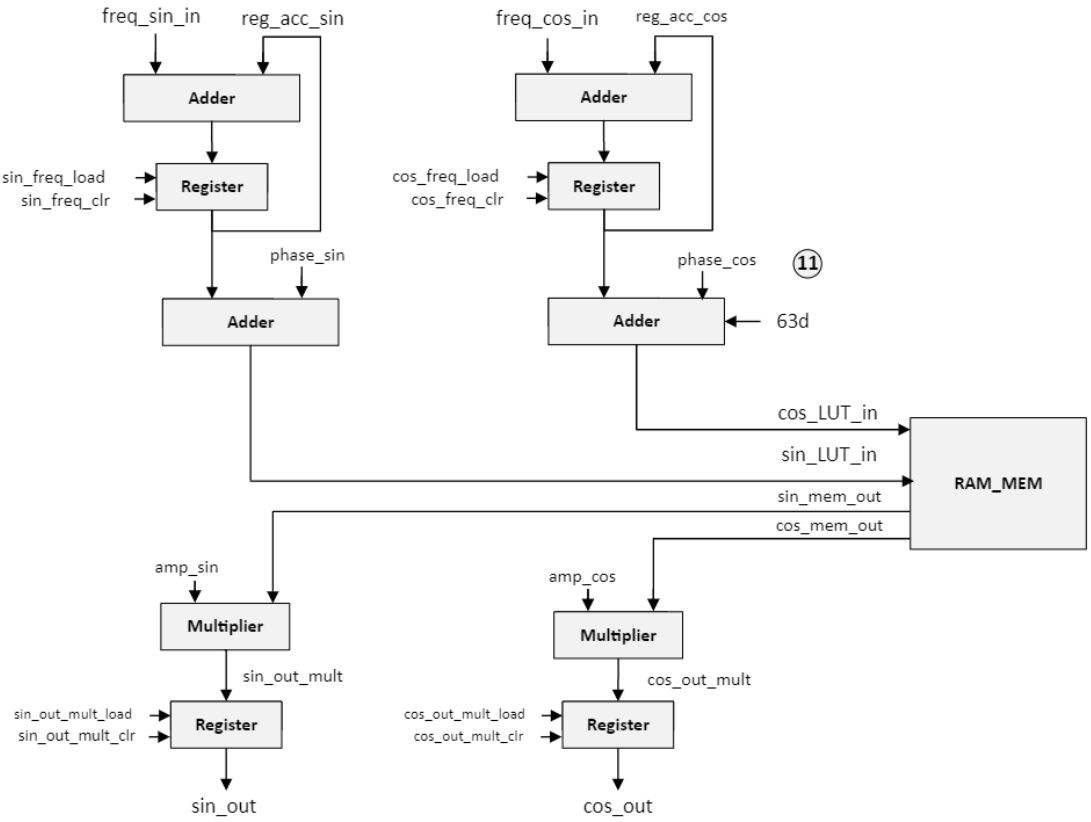


From this ASM diagram, we can start generating the "optimum" Building Blocks for the datapath:

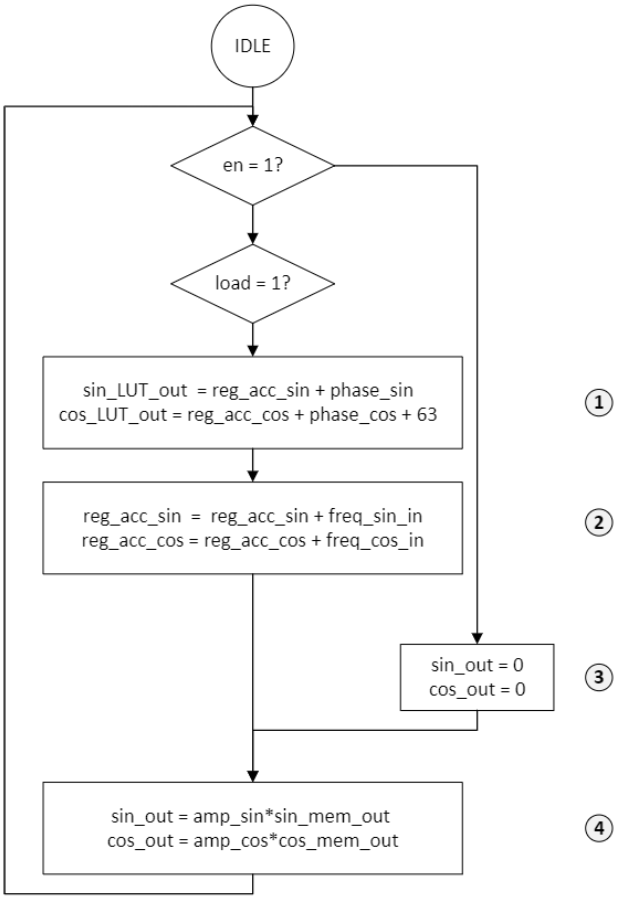
BUILDING BLOCKS GENERATION



DATAPATH CONSTRUCTION

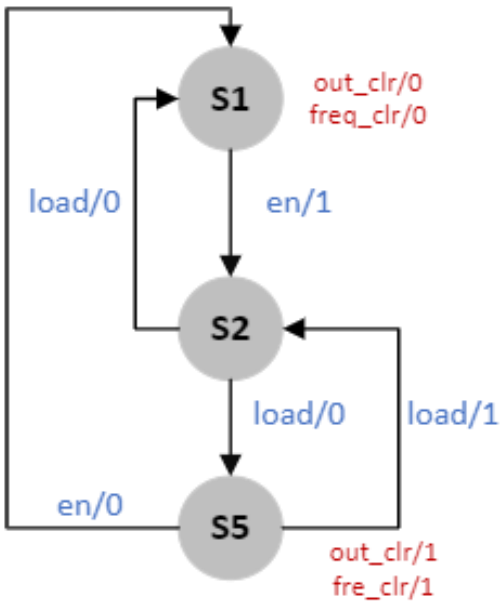


CONTROL SIGNALS FOR DATAPATH



Control FSM		
State	Input/Value	Output/Value
1	en/0 load/0	sin_freq_clr/1
2	en/0 load/1	
3	en/0 load/0	sin_freq_load/1

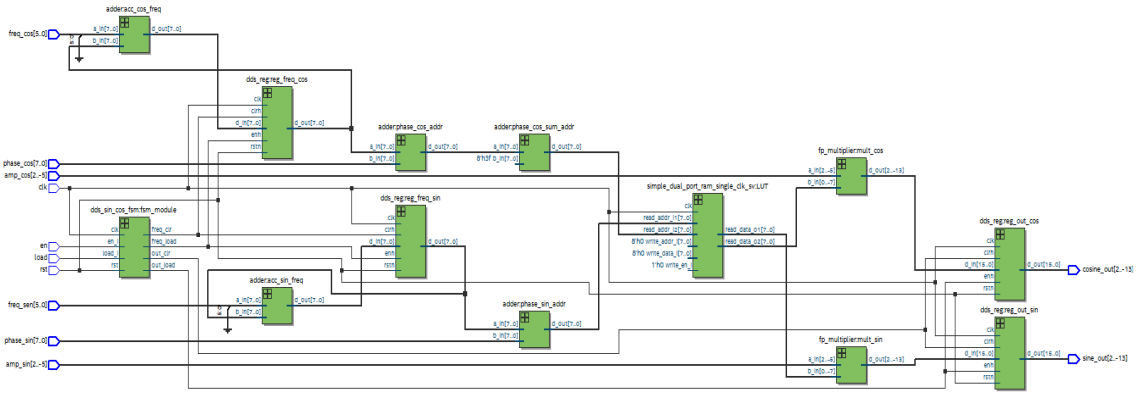
FSM: (inputs and outputs)



Control FSM		
State	Input/Value	Output/Value
1	en/0 load/0	sin_freq_clr/1
2	en/0 load/1	
3	en/0 load/0	sin_freq_load/1

FPGA SIMULATION AND SYNTHESIS

TOP LEVEL SCHEMATIC:



MEMORY FILE GENERATOR:

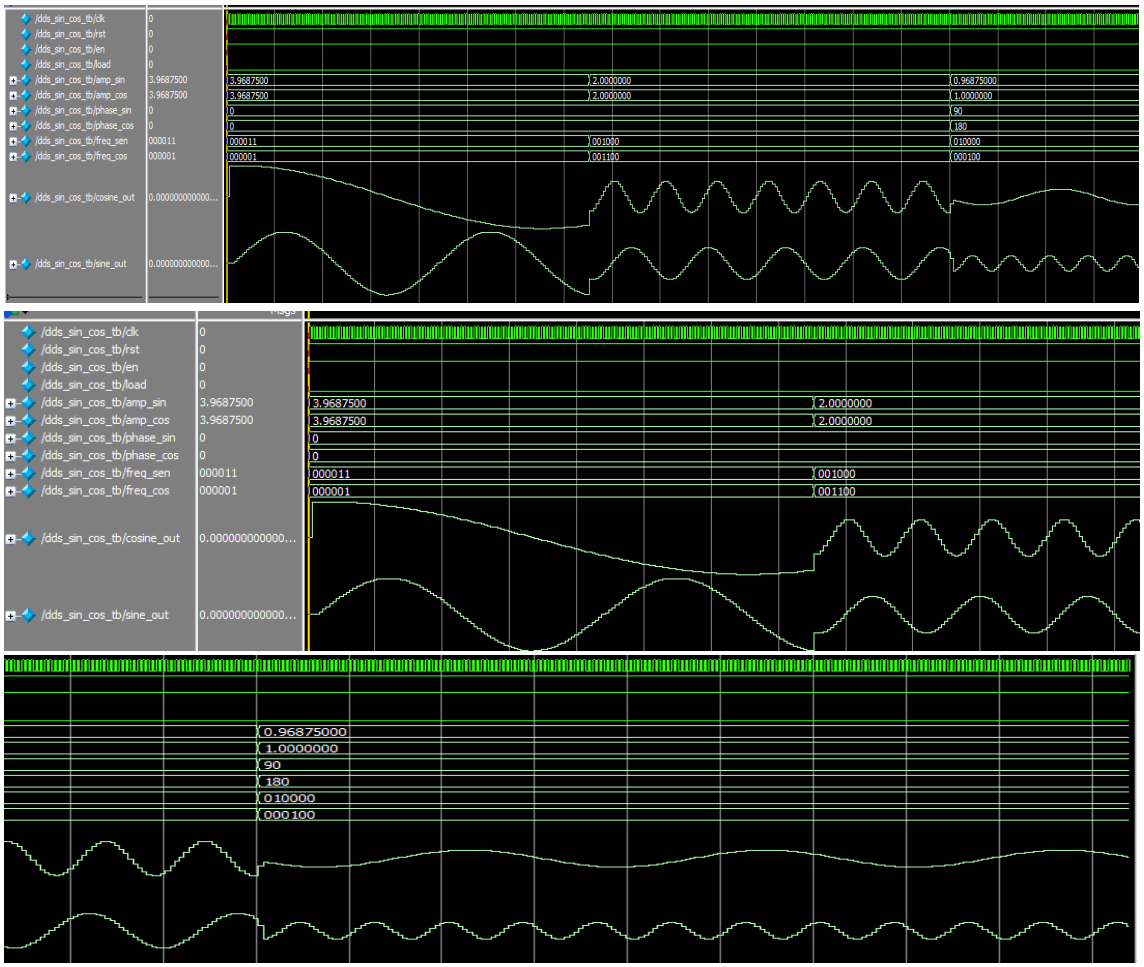
We use the former Matlab code to obtain the necesary values

Memory File Generator (Maltab .m code)

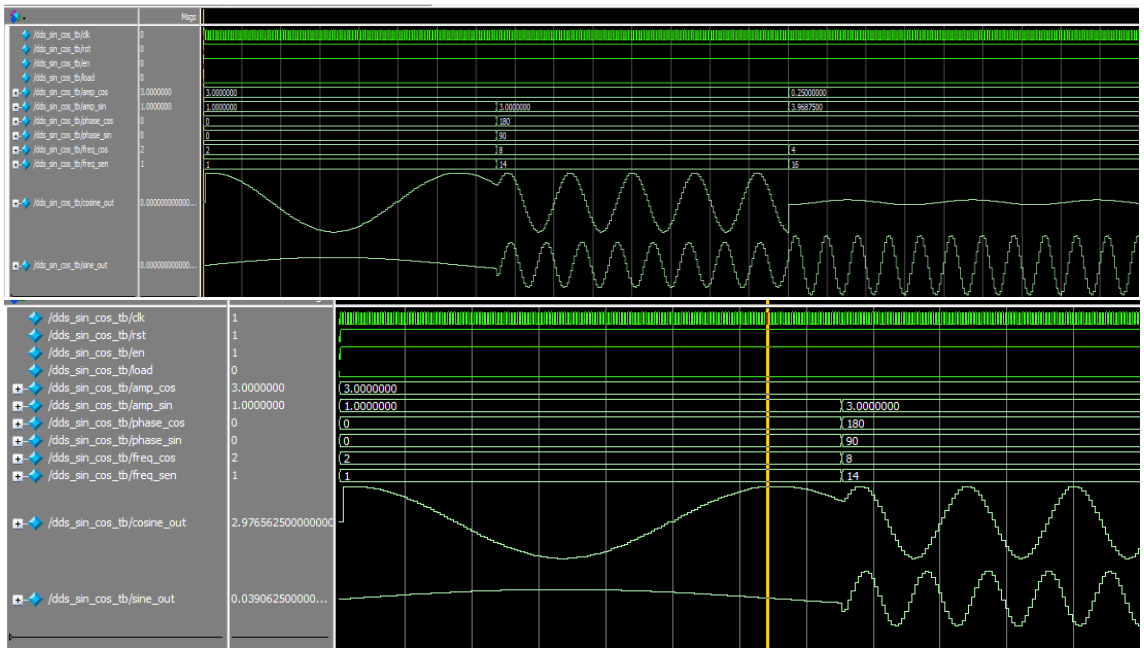
```
Clc
close all
clear all

fmax = 1
Fs = fmax*255
Time = 0:1/Fs:1;
fo = 10;

sinusoid = sin(2*pi*fmax*Time);
amplitud = 2;
sinusoid_amp_out = sin(2*pi*fmax*Time)*amplitud;

WordLength = 8
QI_sinusoid = 1;
QF_sinusoid = WordLength-QI_sinusoid;

signalfxp = fi(sinusoid,1,WordLength,QF_sinusoid);

figure;plot(Time,sinusoid,'r');

hold on;
plot(Time,signalfxp,'b');

SQNR = 10*log(sum((sinusoid).^2)/sum((sinusoid-signalfxp.data).^2))

%Write file location
fileID = fopen('C:/juanquart/conv_proy/mem_X.txt','w');

%Write the signal in HEX,  with in the required format for the RAM module
for k = 1:length(signalfxp)
    fprintf(fileID, '%02X\r', str2num(dec(signalfxp(k))));
end
fclose(fileID);
```

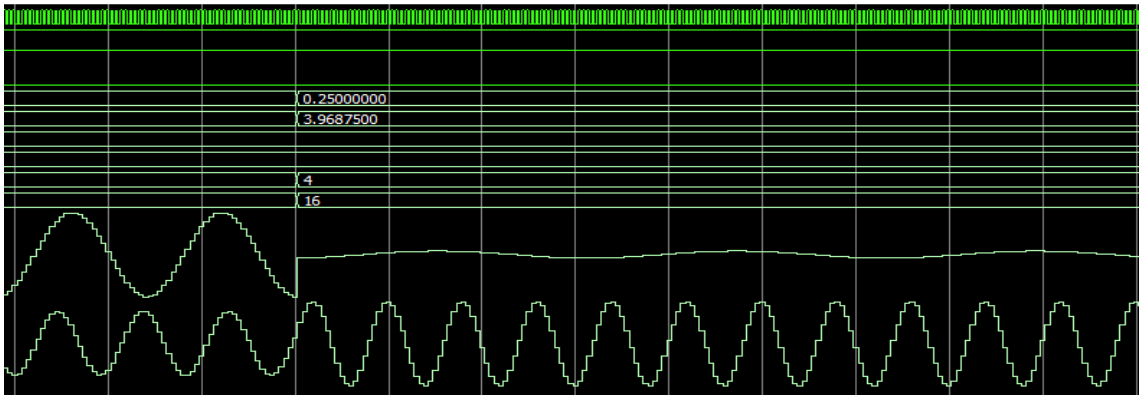
SIMULATION WAVEFORM:

TB SIMULATION 1:



TB SIMULATION 2:





AREA

Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	21 / 32,070 (< 1 %)
Total registers	48
Total pins	80 / 457 (18 %)
Total virtual pins	0
Total block memory bits	2,048 / 4,065,280 (< 1 %)
Total DSP Blocks	2 / 87 (2 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

MAXIMUM FREQUENCY

Slow 1100 mV 85C model

	Fmax	Restricted Fmax	Clock Name	Note
1	130.77 MHz	130.77 MHz	clk	

Slow 1100 mV 0C Model

	Fmax	Restricted Fmax	Clock Name	Note
1	128.78 MHz	128.78 MHz	clk	