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LAB 7 REPORT

WATCHDOG TIMER

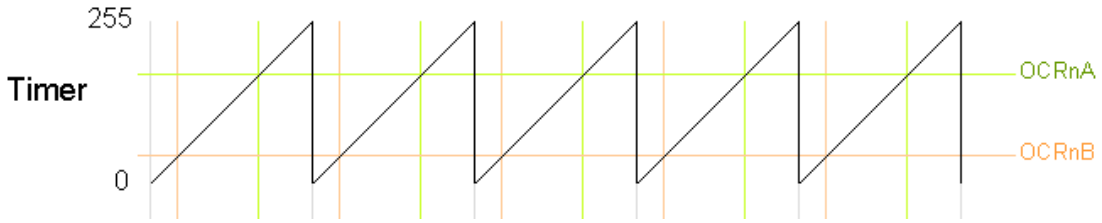
The Watchdog timer is one of the several timers present in MSP430 family of processors. It is a timer peripheral device whose primary function is to perform a restart after a software problem occurs. However, if this function is not needed it can also be used as an interval timer which generates an interrupt after each interval is done. The interrupt is accessed after WDTIE and GIE bits are set. The flag is reset when the request is serviced. Watchdog timer has several intervals available whose macros are defined in the msp430f5529 header file. These modes vary in their interval length and in their source clock. For example WDT_MDLY_8 is clocked by SMCK and has an interval of 8ms, WDT_ADLY_1000 is clocked by ACLK and has an interval of 1000ms. This is for interval mode, another mode is that watchdog resets after expired time. Some examples for the same length as before but different mode are: WDT_MRST_32 and WDT_ARST_32.

TIMERS

There are other timers present in MSP 430, the ones we have seen in this lab are Timer A and Timer B. This timers are used to raise exceptions every certain time we want to avoid implementing counting cycles. There are several modes that these timers support: STOP, UP, CONTINUOUS and UP/DOWN. We can as well set the source where these timers are being clocked. For example with the statement TA0CTL = TASSEL_1 | MC_1; w are setting timer in the UP mode and we are saying that is being clocked by ACLK. Changing the source clocks is important since we have to take into account the different frequencies of operation.

MODES

UP: In this mode, the interrupt will trigger at a given time set in the register TAxCCRn and will then reset. We can have two values TAxCCRn+1 that will trigger two interrupts when thy are reached. This is the graph:



UP/DOWN: In this mode the interrupt will trigger at a given time set in register TAxCCRn but then will go down the same way it went up. We can have two values TAxCCRn+1 that will trigger two interrupts when thy are reached. This is the graph:

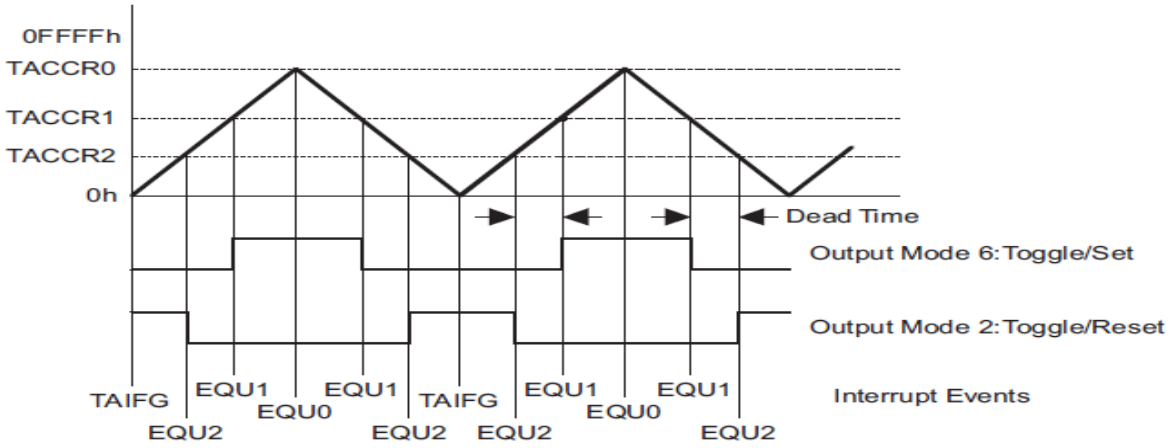


Figure 12-9. Output Unit in Up/Down Mode

CONTINUOUS: In the continuous mode the clock will count from 0 to FFFF. When the counter value reaches 0x0000, the EQU1 will be asserted indicating that the counter has the same value as the TA2CCR1.

CALCULATIONS:

For program 1 the calculations I have used have been to set the number of watchdog interrupts. This is 3 (seconds) / WDT interval. I have chosen 8ms so that the intensity transition is fluent enough. This has given me 375 changes for TA0CCR1.

For program 2 we know that the clock interval is 0.5ms and we wait 1000 accesses to the interrupt before toggling the LED. This means that the led will be toggled every 0.5 seconds, which gives us a frequency of 1Hz.