Test 1 W24 - Results

Attempt 1 of 1

Written Feb 10, 2024 2:10 PM - Feb 10, 2024 2:50 PM

This shows your answers, correct answers, and marks. If you detect a marking error, must email a correctly completed CPS590 Re-evaluation Form to TA within 24 hours for consideration. (Form is in Content area.)

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Attempt Score **46.25 %**
Overall Grade (Highest Attempt) **46.25 %**

Question 1 **1 / 1 point**

Suppose 4 jobs, A, B, C, and D, are submitted for execution at the same time (t=0). The jobs each require some amount of time to complete, and some percentage of a specific resource, as given in the table below. Assume an operator batches the jobs (in the order shown above) in a uniprogramming, simple batch OS.

What is the mean response time of these 4 jobs, in minutes? Your answer must given as **a single integer** only (no spaces, units, etc.) Round if necessary; e.g., 10.5 rounds to 11, and 10.4 rounds to 10.

	Job A	Job B	Job C	Job D
Resource Utilization (in %)	25	10	5	20
Time to Complete (in minutes)	25	20	15	25

Answer: 54 ✓

Question 2 **0 / 1 point**

The two major problems with early serial processing systems were scheduling and _____.

- ➡ ◯ set-up time
- ✖ ◯ the need to hire a full-time operator
- ◯ the complexity of the operating system
- ◯ printer paper jams
- ◯ Choose this if none of the others is correct

Question 3 **0.75 / 1 point**

When a user program executes in user mode, these are true (select ALL that apply).

- ➡ ✔ ☐ certain areas of memory are protected from the user's use
- ✔ ☐ certain processors are protected from the user's use
- ➡ ✔ ☐ certain instructions may not be executed
- ✖ ☐ certain interrupts must be disabled

Question 4 **1 / 2 points**

Use the drop-down to select the system that best matches the statement.

- ✖ __2__ (3) First to support concurrent interactive jobs
- ✔ __1__ First to require JCL
- ✖ __3__ (1) First to stop user from directly accessing the processor
- ✔ __3__ First to use time-slicing

1. Simple batch system
2. Multiprogramming batch system
3. Time-sharing system

Question 5 **0.75 / 1 point**

Consider the C program below. Suppose you have 2 terminals open on the same moon, T1 and T2. Suppose in T1 you compile and execute the program, and that it has Process ID 123456. How could you make this program print "Hello" on stdout? Select all that apply.

```
#include <stdio.h>
#include <stdlib.h>
#include <signal.h>
#include <unistd.h>

void Func(int sigNum) {
  if (sigNum == SIGINT) printf("\nHello\n");
}

int main (void) {
    signal(SIGINT, Func);
    for (int i=0;i<3;i++) sleep(1);
    printf("\nBye\n");
}
```

- ➡ ✖ ☐ in T1, type ctrl-c before program terminates
- ✔ ☐ in T2, type kill -SIGKILL 123456 before program terminates
- ✔ ☐ in T1, type kill -SIGKILL 123456 before program terminates
- ➡ ✔ ☐ in T2, type kill -SIGINT 123456 before program terminates

Question 6 **0 / 1 point**

The _____ is the interface that is the boundary between hardware and software.

- ISA (Instruction Set Architecture)
- Choose this if none of the others is correct
- IBP (Instruction Binary Program)
- ABI (Application Binary Interface)
- API (Application Programming Interface)

Question 7 **1 / 1 point**

_____ memory is a facility that allows programs to address memory from a logical point of view, without regard to the amount of main memory physically available.

- Cache
- Logical
- Choose this if none of the others is correct
- Virtual
- Secondary

Question 8 **1 / 1 point**

The portion of the monitor that is always in main memory and available for execution is referred to as the _____.

- available monitor
- main monitor
- Choose this if none of the others is correct
- in-memory monitor
- resident monitor

Question 9 **0.75 / 1 point**

Which of these are true of Linux? Select ALL that apply.

- [ ] It is typically more expensive to purchase than a comparable Windows product.
- [x] It architecture is microkernel, not monolithic.
- [x] The quality of its kernel has contributed its penetration into the corporate world.
- [x] Part of Linux's success is due to its development model.

Question 10 **1 / 1 point**

Suppose a processor has access to two levels of memory: L1 (cache) and L2 (main memory) as follows:

Level	Amount in bytes	Access time in microseconds (µs)	Cost
L1 (cache)	1,000	T1=0.40	C1=0.01 cents/bit

L2 (main memory)	100,000	T2=1.00	C2=0.001 cents/bit

Assume that if a byte to be accessed is in L1, then the processor accesses it directly. If it is in L2, then the byte is first transferred to L1 and then accessed by the processor. Ignore time required for processor to determine which level the byte is in, and time to transfer it from L2 to L1.

When the hit ratio is 0.25, what is the **system's average access time** in microseconds (μs)? Enter answer rounded to 2 decimal places--include no spaces, commas, units, etc. e.g. 0.30

Answer:

1.15 ✔

Question 11 **0 / 1 point**

Each location in Main Memory contains a binary number value that can be interpreted as:

- ◯ either an instruction or an address
- ◯ Choose this if none of the others is correct
- ➡ ◯ either an instruction or data
- ✖ ◯ either an instruction or data or address
- ◯ either an address or data

Question 12 **0 / 1 point**

The four main structural elements of a computer system are:

- ✖ ◯ Processor, Registers, I/O Modules and Main Memory
- ◯ Processor, Registers, Main Memory and System Bus
- ➡ ◯ Processor, Main Memory, I/O Modules and System Bus
- ◯ Processor, I/O Modules, System Bus and Secondary Memory
- ◯ Choose this if none of the others is correct

Question 13 **0 / 1 point**

For a multiple-word I/O transfer, which is most efficient:

- ◯ Interrupt-enabled I/O
- ➡ ◯ Direct Memory Access
- ✖ ◯ Interrupt-driven I/O
- ◯ Programmed I/O
- ◯ Choose this if none of the others is correct

Question 14 **1 / 1 point**

A Control/Status register that contains the address of the next instruction to be fetched is called the _____.

- ◯ Instruction Register
- ◯ Choose this if none of the others is correct
- ◯ Accumulator
- ◯ Memory Address Register
- ✔ ◯ Program Counter

Question 15 **0 / 1 point**

Assume there are 4 different types of interrupts possible (A, B, C, D), each with its own handler. Assume a user program starts running at time t=0µs (microseconds), and that interrupts A, B, C, and D occur at times 10µs, 20µs, 30µs, and 40µs, respectively. If the user program and interrupt handlers run without interruption, they would each take 41µs to complete; if interrupted, they may take more time. e.g., B occurs at time t=20µs; if its handler starts immediately, and is not interrupted, it finishes at time t=61µs; if interrupted, it may finish later. In keeping with the description from Chapter 1 of your text, there is no lag-time between when one interrupt handler finishes and the next starts; only consider time taken for user program and interrupt handlers.

Multiple interrupts are handled using a priority scheme. For each type of interrupt, the OS has assigned a priority, shown in the following table, where 1 is the lowest priority and 4 the highest:

A	B	C	D
4	1	3	2

At what time (µs) does D's **handler** start executing? Enter your answer in the box below. Enter a single integer only--include no spaces, commas, units, etc. Note: do not give the time of the interrupt itself--give the time the **handler starts**.

Answer:

82 ✖ **(92)**

Question 16 **1 / 1 point**

A hypothetical machine has 16-bit words, which contain either instructions or integers. The first 4 bits of an instruction designate the opcode. The first bit of an integer designates its sign (0=positive; 1=negative).

The machine's registers include PC (program counter) and AC (accumulator). A partial opcode list is:

- 0001 = load AC from memory
- 0002 = store AC to memory
- 0003 = add to AC from memory
- 0004 = subtract memory from AC
- 0005 = load PC with address

Suppose an array of 6 integers, A, is stored in memory starting at location 600; i.e., A[0] at 600, A[1] at 601, etc. Suppose a partial "program" is stored in memory starting at location 200. Memory is shown below (displayed horizontally, in hexadecimal). Suppose PC starts with 200.

When the execute stage for address 206 is complete, **what integer is stored in A[1]?** Enter a single integer only, **IN DECIMAL FORM.** Include no spaces, commas, units, etc. Only include a sign if the integer is negative. e.g., enter negative sixteen as: -16

200	201	202	203	204	205	206	...	600	601	602	603	604	605
1602	3601	4602	5205	3604	3601	2601	...	0009	0008	0005	0006	0007	0008

Answer:

16 ✓

Question 17 **0 / 1 point**

Keeping recently used instructions and data values in cache memory is most likely exploiting this:

- ➡ ◯ Temporal locality
- ◯ Choose this if none of the others is correct
- ✗ ◯ Cluster memory
- ◯ Prefetching
- ◯ Spatial locality

Question 18 **0 / 1 point**

A hypothetical system contains 2^8 addressable words, with each word having a unique 8-bit address. Memory is divided into blocks of size 2^4 words. Each cache tag must be how many bits long? Enter a **single integer** only--include no spaces, commas, units, etc.

Answer:

12 ✗ **(4)**

Question 19 **0 / 1 point**

The cache write policy determines:

- ◯ Which cache level to write a block into.
- ✗ ◯ Which memory blocks to write into which cache slots.
- ◯ When to write an altered memory block into the cache.
- ◯ Choose this if none of the others is correct
- ➡ ◯ When to write an altered cache block back to memory.

Done