

NASBUS FUNCTIONAL SPECIFICATION

Document No. PF/007
Issue No. 1

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ISSUE	DATE	REVISED SHEETS	REMARKS
1	18.9.78	(i)-(ii), 1-1, 2-1, 3-1-3.3, 4-1,5-1, A.1-A.2, B.1-B.2, C.1-C.2.	First formal issu
ORIGINATOR:	A.R.Rundle	APPROVAL: AR	Rundlo

Specification

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# 1. <u>Introduction</u>

The NASBUS is a bus used to add extra boards (e.g. memory and I/O) to the basic NASCOM Microcomputer. It consists mainly of buffered Z80 input and output signals together with some additional bus control lines.

The equipment practice used has been chosen for its wide availability and low cost.

This document defines the electrical and physical charateristics of the NASBUS.

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  - VERO catalogue. 2.

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Page 2-1

## 3. Functional Description

The Nasbus is a 77 way bus, with signals allocated as described below. Please see the Z80 cpu manual (1) for details of timing and operation of Z80 derived

Note that lines marked "Reserved" have already been allocated for future use. Lines marked spare may be used for any purpose but we do not guarantee not to redefine and use them in the future.

PIN	SIGNAL NAME	Description S
1 2 3 4	Ov Ov Ov	Power supply and system ground
5 6 7 8	Clock (spare) (spare) (spare)	2 MHZ buffered system clock
9	RAM DIŚABLE*	An active low signal which disables output from any RAM card on the bus. Used to give ROM priority over RAM.
10	RESET SWITCH *	An active low signal which initiates a short pulse on the RESET line (pin 14), to reset the system without destroying dynamic RAM contents.
11	NASCOM MEM	A decoded signal from one of the RAM boards in the system defining which 4K memory block is used by the NASCOM. (Usually 0000H - OFFFH).
12	NASCOM 10	A decoded signal from an IO extension card defining which ports are used on the NASCOM.
13	DBDR *	This signal 'Data bus drive' determines the direction of the bidirectional data bus buffers on the NASCOM Buffer card. It is a decoded signal made active by any device transferring data to the NASCOM card. Active low to

Chagna taken 25 26 IORO 27 MREQ 28

Transfer temos

29 30 AO 31 **A1** 

**A2** 

33 A3 34 **A4** 35 **A5** 36 **A6** 37 **A7** 38 **A8** 39 A9

32

control of the data, address

signal

Buffered Z80 MI signal.

Tristate buffered Z80 IORQ

Tristate buffered Z80 MREQ

Tristate buffered Z80 WR

Tristate buffered Z80 RD

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Tristate Z80 Address lines 0 to 15

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PIN	SIGNAL NAME	DESCRIPTION	
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44	A14.		
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49			
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50	<b>DO</b>		
51	D1		
5 <del>2</del>	DZ		
53	D3	Bidirectional,	Tristate Z80
54	D4	Data lines 0 to	
55	<b>D5</b>	Dava lines o co	1.74
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68	-5 V	Power supply	
69	-5V	Power supply	
70	-12V	tt	
71	-12V	11 11	SCHOOL STORM
72	Keyway		•
73	+12V		4
		Power Supply	
74	+12V	11 11-	
	and the second of the second o		9.0
<b>7</b> 5	+ 5V	11 11	
76	+ 5V	11 11	
77	+ 5V	11 11	, ,
78		11 11	
10	+ 5V	.,	21.7

<sup>\* = &</sup>quot;Open Collector" signal line

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## Electrical Specification

#### 4.1 Tristate Logic

rootenti sari enser These lines are driven by low power Schottky tristate buffers capable of sinking 16 mA in excapable of driving 10 standard TTL loads (1.6mA sinking, 40 & A source) or approximately 40 low power Schottky inputs (0.36 mA sinking, 20 M A source) while retaining logic zero 0.4v and logic 1>2.4v. You had a though control

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## 4.2

Open collector lines are pulled up to 5 v. Any board can pull down to zero provided it is capable of sinking 16 mA.

#### 4.3 Power supplies

In order to avoid overloading the motherboard and the system power supplies the following rules should be applied.

- All bus fines of the same voltage should be commoned on the board. The thought the transfer.
- No board should draw a total of more than: (b)
  - 2.0 Amps
  - 5v 0.5 Amp
  - + 12v 1.0 Amp
  - 12v 0.5 Amp
- The whole occupied Nasbus should not draw more than: (c)

and the large of the large of the

- 8 Amps 5v
- 5v 1 Amp
- + 12v 2 Amps
- 12v 1 Amp

#### 4.4 General Design Points

Boards should be designed where possible to apply no more than 2 or 3 low power loads to any signal line of the Nasbus. In any event, a maximum of 1 TTL load must not be exceeded.

Note that tristate lines will float if the Nascom cpu is disabled e.g. by a bus request.

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Electrical Specification

# 5. <u>Physical Specification</u>

# 5.1. Board Specification significant value of the series of series of the series of t

## 5.1:11 vite Board Dimensions Am Di patrici to bidegen eventue

The standard board size is 203,20 mm long to 0.00, 
0.30 by 203.20 mm. high + 0.00, - 0.25 (i.e. 8 x 8 inches).

The thickness should be 1.60 nominal (including copper)

See also Appendix A.

A suitable prototyping board is Vero type 10-0155 F (up to 45 DIPs) Type Nos 2 06-3462C and 06-3463J can also be useo as 21 11 2-2000 can also be useo as 21 11 2-2000 can

# 5.1.2 Contact Pitch

The contact pitch is 2.54 mm. 77 of the possible 78

ways are used, with a reference key 7 from the bottom

(component side). The contacts used are on the solder side.

# 5.2. Connector Specification

Suitable connectors are Vero type 14-0998G or Varelco type 00.6072-080-657-101 with polarising key at position 73, position 1 and 80 blank. (See Appendix B).

20mi 0.8

0.5 Amp

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vota 1855 LIGUA NEWOT

VSI

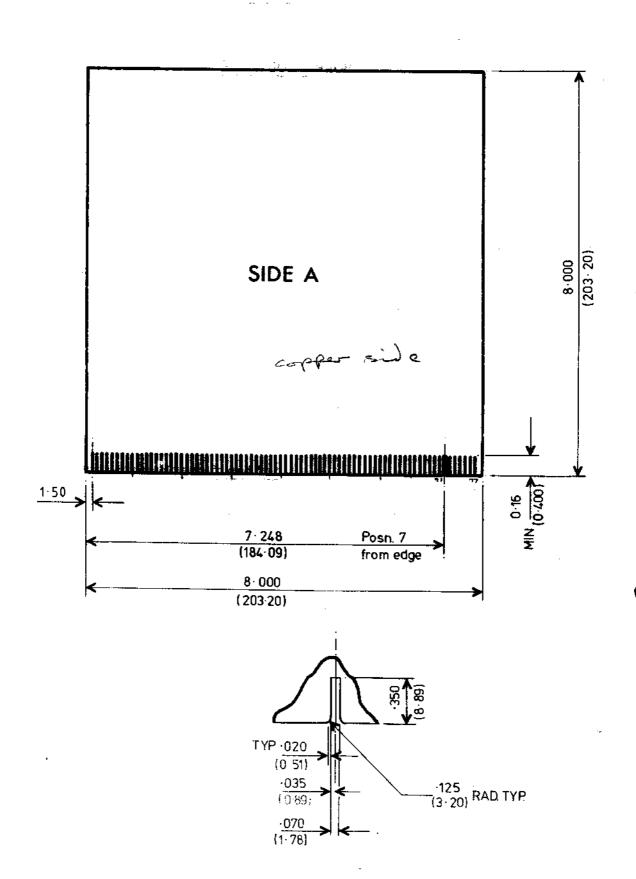
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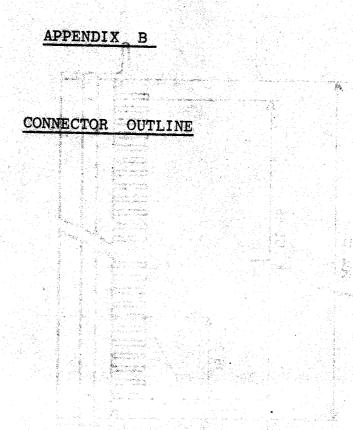
## APPENDIX A

BOARD OUTLINE

(000 8) (000 6)

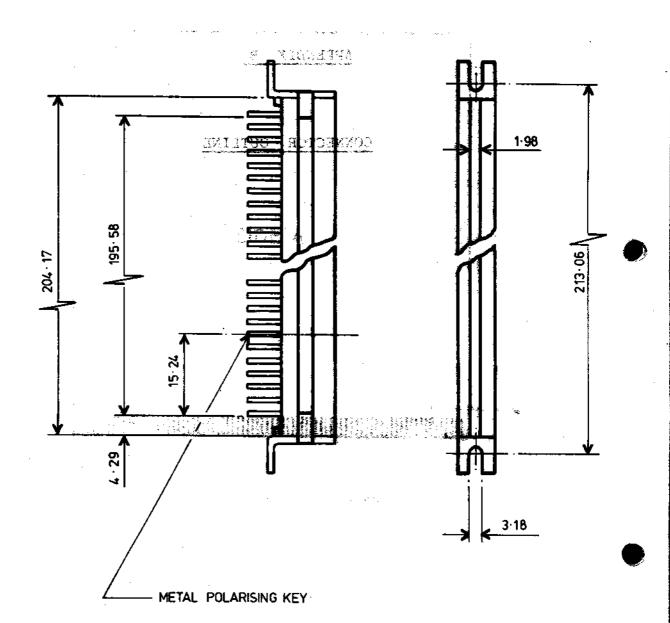


Detail of Polarising Key



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Page B.1 Issue !



APPENDIX C

NASBUS SUMMARY

Lines marked \* are open collector; those overlined are  $\overline{\text{NOT}}$  (logic level).

revel).	
1 2 3 4	AV. CROUND
1,2,3,4 5	ØV: GROUND
	Ø (buffered)
6,7,8	spare
9	RAMDISABLE*
10	RESET SWITCH
11	MEMEXT
12	TOEXT
13	DRIVE *
14	RESET
15	
	HALT
16	BUS AK IN
17	BUS AK OUT
18	BUS RQ*
19	IEI
20	IFO
21	Reserved for WMI
22	INT*
23	WAIT*
24	
	RFSH
25	$\frac{\overline{\mathrm{MI}}}{2}$
26	IORQ
27	MREQ
28	$\overline{ m WR}$
29	RD
30	AO
31	A1
32	$\frac{1}{4}$
33	A3
34	
	$\frac{A4}{A}$
35	A5
36	A6
37	A7
38	A8
39	AQ
40	A10
41	A11
42	A12
43	A13
44	114 114
45	
	A15
46,47,48,49	Reserved
50	00
51	${ m D1}$
52	D2
53	D3
54	Ŋ4
55	D5
56	D6
57	D7
58,59,6065	
	Reserved
66,67	To separate signal and power lines
68,69	-ve 5V
70,71	-ve 12V
72	KEY
73,74	+ve 12V
75,76,77,78	+ve 5V