SECTION 1 - HARDWARE MANUAL

Contents

1.1 Introduction

1.2 Links/Switches LSW1 and LSW2

1.3 Memory decode header LKS1

1.4 Memory type linkblocks LKB 1-9

1.5 Memory addressing

1.6 Video memory addressing

1.7 Input/output port addressing

1.8 Power supply requirements and connections

1.9 Tuning the TV

1.10 Cassette interface adjustment

1.11 External connections

1.12 External socket assignments

1.13 Test points

1.14 Component list, circuit reference order

1.15 Component list, numerical order

1.16 Component changes for use outside UK

1.17 Component and board layout

1.1 Introduction

The Nascom 2 is an exceptionally flexible computer system, and can be set up to operate in a number of different ways. However in order to ensure correct operation it is important that the correct switch and wire link options are present to suit the user's application. Those who have bought their board ready-assembled should have had these options set by the supplier, and therefore need not dwell on this section initially. Those who have bought a kit, or who are planning changes to the hardware configuration of their system will find in this section details of how to select the mode of operation which they require.

The flexibility of the system means that there are a number of choices to be made. We recommend that you should read through the instructions which follow twice before proceeding with the configuration process, and that you should proceed through the steps methodically.

Please note particularly the following warnings:

1. Any error in matching the wiring of linkblocks 1-9 with the type of integrated circuit inserted in the associated socket will cause malfunction, and may cause damage.

2. ANY incorrect external connection may cause both internal and external damage.

****
3. *****MOST IMPORTANT*****
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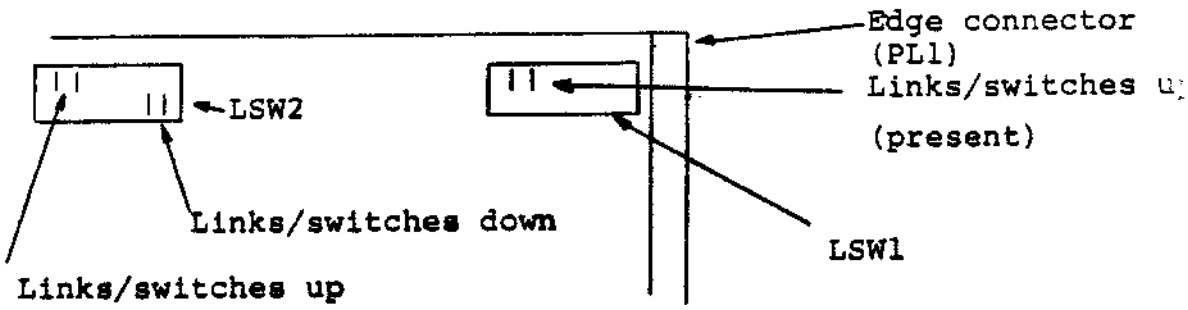
The keyboard must be connected ONLY to PL3, and UNDER NO CIRCUMSTANCES to PL2, which carries voltages capable of destroying the keyboard.
****

1.2 Links/switches LSW1 and LSW2

Two areas on the extreme edge of the Nascom board contain links or switches which are used to select various run options for the computer. Either wire links or switches may be provided. The locations of these links or switches are shown below:



Note that where the user intends to change any of these links frequently it will be more convenient to take wires from the appropriate link pads to a front-panel switch (eg if baud rate for printers is to be changed frequently).

The functions of these switches can be summarised as follows:

Link/switch	Function	Link made /switch up	Link absent /switch down
LSW1/0	Memory wait	On	Off
LSW1/9	CPU clock select	Internal	Bus
LSW1/8	4K/8K Memory decode	8K	4K
LSW1/7	4K/8K Memory decode	8K	4K
LSW1/6	50/60Hz (625/525 ln)	50Hz/625line	60Hz/525 line
LSW1/4	Restart address A15	0	1
LSW1/3	Restart address A14	0	1
LSW1/2	Restart address A13	0	1
LSW1/1	Restart address A12	0	1

Link/switch	Function	Link/switch upper	Link/switch lower
LSW2/0	CPU clock frequency	4 MHz	2 MHz
LSW2/9	Alpha/graphics select	Auto	Alpha only
LSW2/8	Port addressing	External	Internal
LSW2/7	Serial input device	Terminal	Cassette
LSW2/6	Receive speed	Extnl clock	TTY 110 baud
LSW2/5	Receive speed	Use LSW2/6	Use LSW2/4(cassette)
LSW2/4	Cassette receive speed	1200 baud	300 baud
LSW2/3	Transmit speed	Extnl clock	TTY 110 baud
LSW2/2	Transmit speed	Use LSW2/3	Use LSW2/1(cassette)
LSW2/1	Cassette transmit speed	1200 baud	300 baud

Link/switch functions
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1. LSW1/1 to LSW1/4 fix the restart address to which the computer will jump when power is applied or the 'reset' button is pushed. Normally the links are all made (switches up) so that restart occurs in NAS-SYS. If, for example, the links LSW1/4, LSW1/3 and LSW1/2 were not made (switches up) and link LSW1/1 were made then on power on or manual reset the computer would start up in BASIC, performing a cold start.

2. LSW1/5 selects the number of stop bits separting characters sent by the serial output interface. Normally only one stop bit will be required, except at 110 baud.

3. LSW1/6 allows selection between TV receivers desisned for 50Hz (625 line) or 60 Hz (525) lines.

4. LSW1/7 and LSW1/8 allow the on-board memory in sockets 35 to 42 to be treated as one continuous block of 8K or as 2 independent 4K blocks. See also notes on the header plug (section 1.3).

5.LSW1/9 allows for selection between the on-board processor clock (normal state) or a clock on the NASBUS.

6. LSW1/0 allows an additional wait state to be used with certain slower memory devices. It may be necessary to turn memory wait on when running BASIC at 4MHz.

7. LSW2/1 to LSW2/3 allow switching of the serial input speed for a cassette or a terminal. LSW2/2 selects whether the speed is to be set by LSW2/1 or LSW2/3. If Cassette is selected then LSW2/1 determines whether 1200 or 300 baud will be used. If Cassette is NOT selected then LSW2/3 determines whether the standard 110 baud teletype rate or an external clock is to be used to control the speed of data transfer.

8. LSW2/4 to LSW2/6 perform similar functions for the receive data rate.

9. LSW2/7 selects whether the source of serial input is the cassette unit or a terminal.

10. LSW2/8 selects whether any external input/output ports are to be addressed. For a Nascom 2 in isolation only internal ports should be specified.

11. LSW2/9 selects whether the graphic characters are to be used. If the graphics generator chip is not present the alpha only mode should be used.

12. LSW2/0 selects between a 4MHz and 2MHz clock speed for the microprocessor. Normaly a 4MHz clock will be used.

The normal configuration for the switches when using a 4MHz clock, 1200 baud cassette tape and an 8k memory block is:

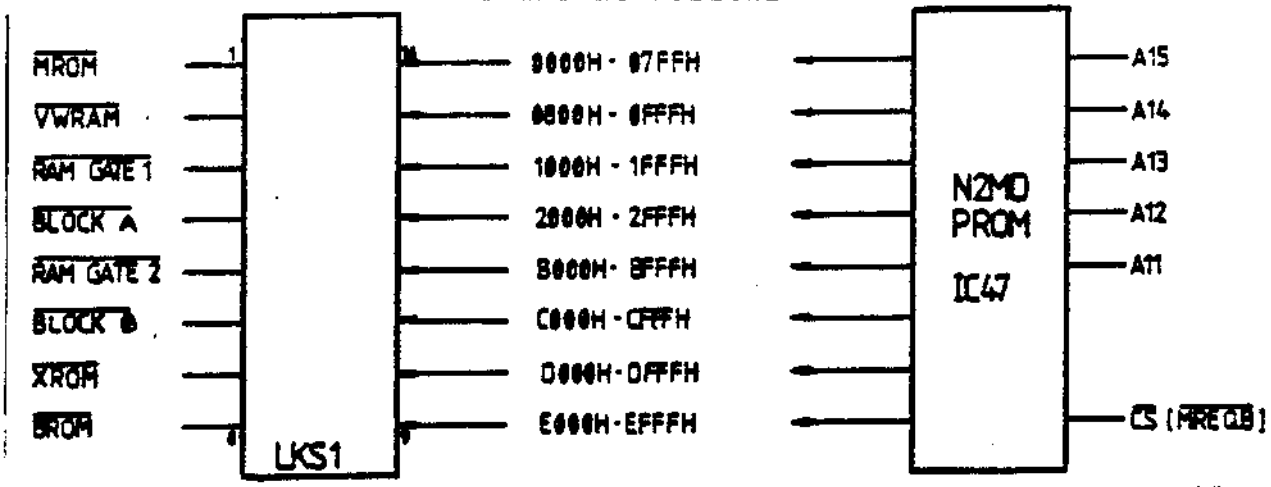
LSW1 1,2,3,4,,5,6,7,8,9 link made (switch up)
0 link open (switch down)

LSW2 0,1,4 switch/link upper position
2,3,5,6,7,8,9 switch/link lower position

1.3 LKS1 Header Plug

It is recommended when altering the wiring of this header that it should be left plugged into its socket while soldering. This avoids pins becoming displaced as a result of heating.

The header determines the address and type of the on-board memory contained in sockets 35 to 42 and 48. The functions of the connections on the pins are as follows:



1. Pin 1, MROM determines the address of the monitor ROM , IC34. It will normally be connected therefore to Pin 16 of the header.

2. Pin 2, determines the address of the video and work area chips on the Nascom board, IC's 50 and 48 respectively. It will normally therefore be connected to Pin 15 on the header.

3. Pin 8 determines the address to be used for IC43, the BASIC ROM. It is therefore normally connected to Pin 9.

4. Pins 3 and 5 are used in conjunction with either Pin 4 or Pin 6 to allow read/write memory, RAM, to be used in the positions IC35 - 42.

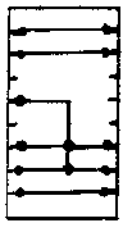
5. Pin 4 determines the address of one of the 4K memory blocks A or B located in IC35 - 42. Pin 5 fulfills a similar function for the second block of memory. If the two 4 K blocks of memory have been specified as a contiguous block of 8K then both Pins 4 and 6 are connected to the two appropriate address Pins. The logic of the circuitry is such that block A, in IC35 - IC38, will have the even block address (C000 or E000) and block B, IC39 - IC42, will have the odd block address (B000 or D000).

6. Pin 7, XROM is used to enable one of the memory blocks for reading only, and is therefore used when 2708 EPROM's are located in the A block (IC35 - 38) or the B block (IC39 - 42).

The normal configuration of the header for a system with monitor and BASIC, but with no on-board memory in IC35 - IC42 would therefore be:

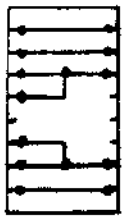
LSW1/7,8 down
(no connection)

If the sockets IC35 - IC42 are being used for 8K of 2708 EPROM located at C000 to DFFF (such as NAS-DIS and ZEAP) then the A block will have the C000 starting address and the header will be as follows.



LSW1/7,8 down
(no connection)

If 4K of 4118 RAM is required at location 1000, with 4K of 2708 EPROM at D000 (ZEAP, for example) then the header would be as follows:



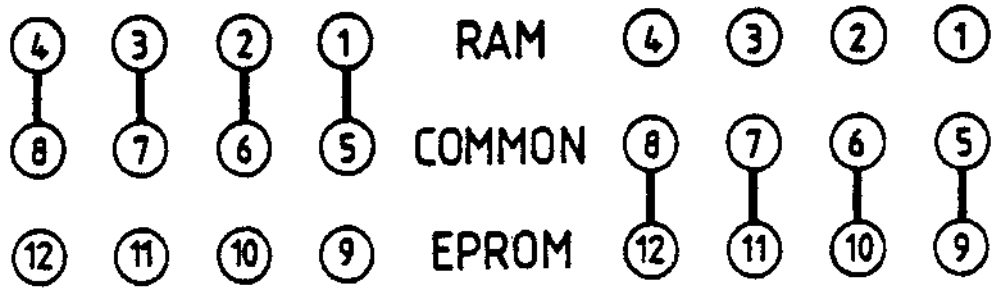
LSW1/7,8 up
(linked)

1.4 Memory type linkblocks LKB 1-9

An additional set of 4 connections must be made for each of IC's 35 - 42 and IC48. This is necessary in order to use either 2709 EPROM's or 4118 RAM's in these locations. These connections are

made at the linkblocks 1 - 9. If terminal blocks are fitted it will be found most convenient to wire-wrap these connections, although soldered connect- ions are quite satisfactory.

The centre row of pins contains a common line which is either connected to the row nearer the centre, for 4118 RAM chips, or to the row nearer the edge of the board for 2708 EPROM chips, as shown below.



4118 RAM 2708 EPROM

The actual functions performed by the individual connections are as follows:

LINKBLOCK PIN	SOCKET PIN	RAM	EPROM	4118	2708
5	21	WRB	-5V	WE	Vbb(-5V)
6	20	RDB	CS	OE	CS/WE
7	19	+5V	+12V	L	Vdd(+12V)
8	18	CS	0V	CS	PROGRAM

By selecting combinations of connections it is possible to use certain other type of memory components.

The linkblock LKB9 must be linked in the same way, but in this case the chip used is normally a 4118 for video RAM, and the block should be wired accordingly.

1.5 Memory addressing

The Nascom 2 has been designed to allow complete flexibility in the use of different forms of memory - RAM, EPROM and ROM. However in the normal non-disc system the following allocation of memory on the main board is used:

0000 - 07FF NAS-SYS monitor program

0800 - 0BFF Video display memory

0C00 - 0FFF Workspace, used by various standard programs

E000 - FFFF BASIC ROM

The remaining memory in locations 1000 to DFFF (52 K bytes) is available to the user. However, to avoid potential clashes in utility programs which may be developed in the future it is suggested that the following areas should be reserved for the purposes indicated.

1000 - 8FFF	General RAM space for user programs
9000 - 9FFF	Programmable graphics RAM or general RAM space
9800 - AFFF	Colour graphics RAM or general RAM space
B000 - B7FF	Extensions to the operating system and/or NASPEN
B800 - BFFF	NASPEN or other word processing
C000 - CFFF	NASDIS or other disassembler/debug programs or colour graphics control software
D000 - DFFF	ZEAP or other assembler type software

It should be emphasised that these are only recommendations, and it cannot be guaranteed that some alterations to these assignments may not be required as a result of future developments.

1.6 Video memory addressing

The video screen display is stored in memory locations 0800 to 0BFF, and this may be accessed directly from programs to output or input data. This memory is organised as shown below:

Margin	Start display line ...	... end of line	Margin
0BC0(3008)	0BCA(3018).....	.....0BF9(3065)	0BFF(3071)
0800(2048)	080A(2058).....	.....0839(2105)	083F(2111)
0840(2112)	084A(2122).....	.....0879(2169)	087F(2175)
0880(2176)	088A(2186).....	.....08B9(2233)	08BF(2239)
08C0(2240)	08CA(2250).....	.....08F9(2297)	08FF(2303)
0900(2304)	090A(2314).....	.....0939(2361)	093F(2367)
0940(2368)	097F(2378).....	.....0979(2425)	097F(2431)
0980(2432)	098A(2442).....	.....0989(2489)	098F(2495)
09C0(2496)	09CA(2506).....	.....09F9(2553)	09FF(2559)
0A00(2560)	0A0A(2570).....	.....0A39(2617)	0A3F(2623)
0A40(2624)	0A4A(2634).....	.....0A79(2681)	0A7F(2687)
0A80(2688)	0A8A(2698).....	.....0AB9(2745)	0ABF(2751)
0AC0(2752)	0ACA(2762).....	.....0AF9(2809)	0AFF(2815)
0B00(2816)	0B0A(2826).....	.....0B39(2873)	0B3F(2879)
0B40(2880)	0B4A(2890).....	.....0B79(2937)	0B7F(2943)
0B80(2944)	0B89(2954).....	.....0BB9(3001)	0BBF(3007)

NOTE:-

The margin area is not displayed, and as the monitor affects these locations they should not be used.

The top row of the display is protected from scrolling, so that titles can be maintained on the screen. It can, however, be cleared using a 'clear screen' (CS, shift/backspace) or by a reset of the computer.

1.7 Input/output port addressing

The subject of input and output is described in more detail in the input/output section of this manual (section 6). The allocation of input and output addresses used on the Nascom 2 board itself is as follows:

PORT	Output Bit	Input bit
P0	7 Not available	7 Unused
	6 Not used	6 Keyboard S6
	5 Unused	5 Keyboard S3
	4 Tape drive led	4 Keyboard S5
	3 Single step	3 Keyboard S4
	2 Unused	2 Keyboard S0
	1 Reset keyb'd count	1 Keyboard S2
	0 Clock keyb'd count	0 Keyboard S1
P1	0 - 7 Data to UART (Serial port)	0 - 7 Data from UART (Serial port)
P2	0 - 7 Not assigned	7 Data received from UART
		6 UART TBR empty
		5 Not assigned
		4 Not assigned
		3 F error on UART
		2 P error on UART
		1 O error on UART
		0 Not assigned
P3	Not assigned	Not assigned
P4	PIO Port A data input and output	
P5	PIO Port B data input and output	
P6	PIO Port A control	
P7	PIO Port B control	

The PIO, IC19, although physically one component, contains two almost identical input output ports, which are referred to as Port A and Port B of that PIO. These are assigned separate absolute addresses for access by the computer as shown above.

The remaining ports P8 to PFF can be used on expansion boards. If they are not present the link/switch LSW2/8 should be set for INTERNAL operation. If these ports are used then it must be set to external.

1.8 Power supply requirements and connections

The power supply requirements are :			CONNECT TO
+5v	@	2A (max, typically 1.5A)	TP 17
+12v	@	250mA max	TP 16
-5v	@	250mA max	TP 14
-12v	@	25mA (for RS232 interface only)	TP 15
OV			TP 13

Notes

1) These figures are for the N2 main board only and do not allow for any expansion.

2) If the wires connecting the power supply unit (PSO) to the CPU board exceed 18" (45cm) in length additional electrolytic decoupling capacitors should be fitted to all power supply rails on the CPU board.

3) Use very thick wires for OV and +5V to avoid significant voltage drop between PSU and CPU board.

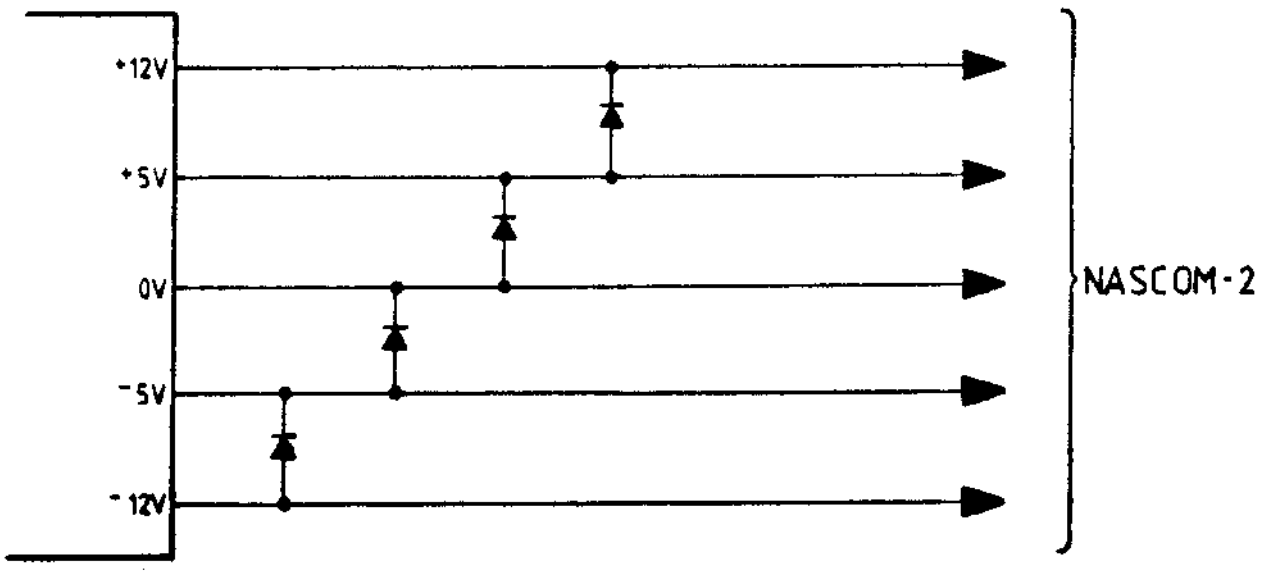
4) All power supply rails on the CPU board must be correct to 5%.

5) NASCOM produce two power supplies, the 3 amp and the 8 amp. The current ratings of these units are:

	3 amp	8 amp
+12V	1A	2A
+5V	3A	8A
-5V	0.5A	1A
-12V	0.5A	1A

The 3 amp supply in capable of driving a NASCOM 2 together with at least 2 RAM boards, whilst the 8 amp unit has power in hand for further expansion and peripherals - disc drives etc. All supply rails have short circuit, Thermal and overload protection. Voltage crossover protection diodes are incorporated in both NASCOM PSU's.

If a power supply which does not have voltage crossover protection in use, diodes should be connected as shown below. (A suitable type is the IN4001)



1.9 Tuning the TV

The output from the modulator should be connected to the aerial socket of the TV. The power should then be turned on and the TV tuned through the UHF band until the computer output becomes visible. Ther should be several points at which it is possible to obtain a picture.

1.10 Cassette interface adjustment

The cassette interface is switchable to speeds of either 300 baud or 1200 baud. For speed of operation the 1200 baud rate is recommended - the main reasons for the 300 rate are for replay of tapes recorded at this rate and for operation with serial printers operating at 30 characters per second. It is also possible to use the cassette unit at 2400 baud by connecting TP4 to TP20 (transmit) and by connecting TP21 to TP5 (receive). Link/switches LSW2/2 and 3 should be in the upper position when using this 2400 baud option for transmitting and links/switches LSW2/5 and 6 should be up for receiving at 2400 baud.

Connections between the cassette unit and computer should be made using screened cable. Two different output levels have been provided from the computer to the recorder - high, which provides 500 mV and low which provides 50 mV. On most recorders it is preferable to use the microphone input and headphone/monitor/external speaker connection. It is also noted that some recorders produce better results when the high output from the computer is connected to the microphone input, even though this might not appear to be what one would expect.

The connections required are as follows:

Cassette output to Nascom - link to TP9 or PL2 pin 16.

Nascom output to cassette unit -
Connect to TP7 or PL2 pin 14 for low output.
Connect to TP6 or PL2 pin 13 for high output.

The common (earth) connections should be linked to TP9 or PL2 pin15 or PL2 pin 11 using the screen of the interconnecting cable.

To obtain optimum results from the tape recorder interface it is necessary to adjust the potentiometer VR1. This can be done in two ways, depending on the availability of a multimeter.

1. Without a meter

Set VR1 to mid range. This can be done by turning the adjusting screw 15 turns anti-clockwise, followed by 5 turns clockwise (since it is a 10 turn potentiometer).

Copy a single character into a block of memory using the M and C commands of NAS-SYS.

Enter X mode.

Dump data onto cassette for about 5 minutes at 300 baud, using the T command from NAS-SYS.

Rewind the cassette. Set volume and tone controls to mid range.

Replay the data into memory using the L or V commands.

The incoming data will be written across the bottom line of the screen, and if it has not been corrupted it will then disappear. Any errors will cause the lines concerned to be scrolled up the screen.

The cassette replay volume should now be adjusted to find the levels between which it can be set without data corruption. If there are problems then the setting of VR1 should be altered by one turn and the procedure repeated.

Finally the whole procedure should be carried out at 1200 baud to confirm correct operation at that speed.

2. Use of a multimeter

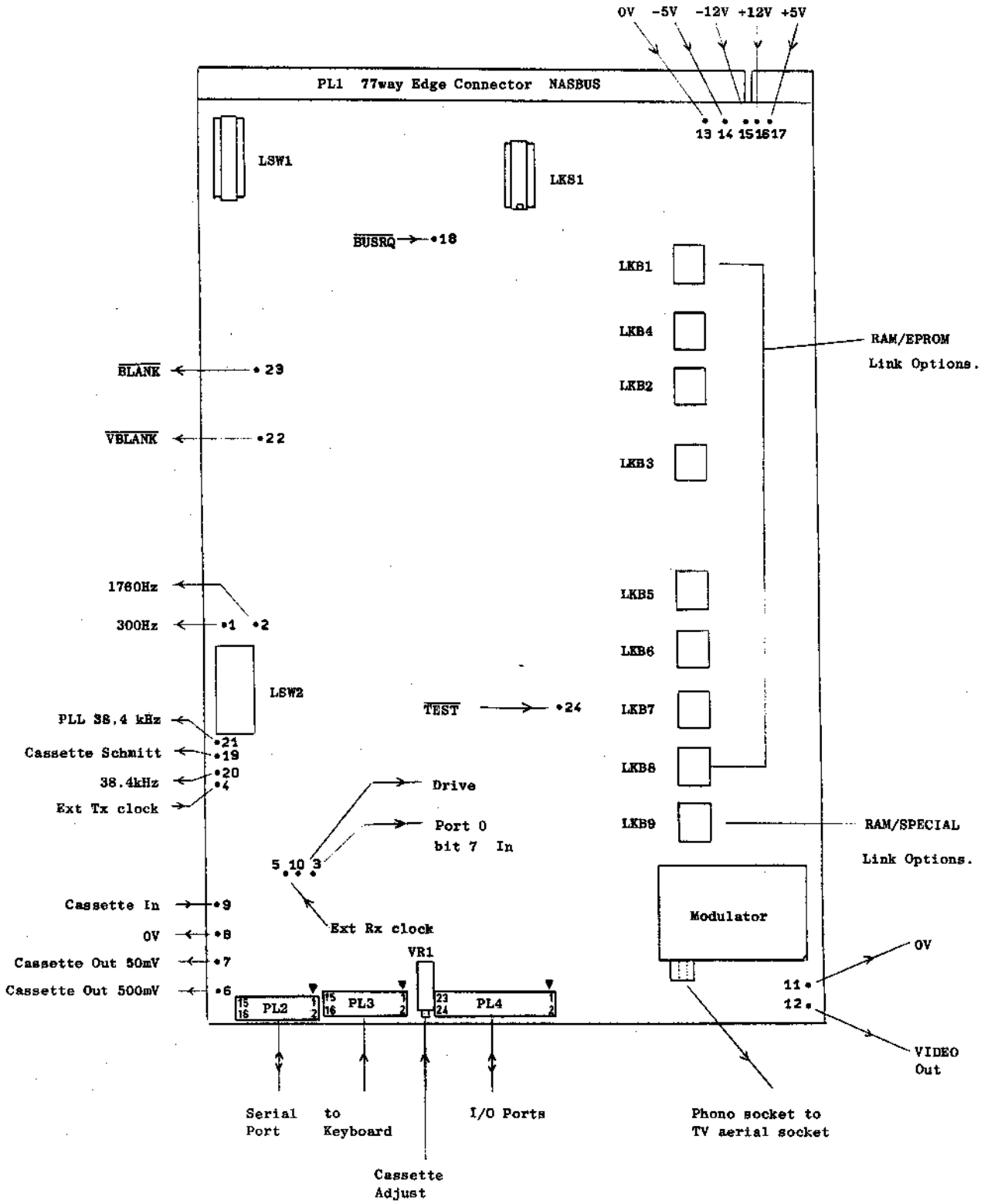
Adjustment of the cassette interface can be carried out more easily if a multimeter is available using the following procedure:

Temporarily connect TP6 to TP9.

Type R <ENTER> from NAS-SYS

Adjust VR1 so that the voltage reading on the meter is the same between TP19 and 0 volts as between TP19 and +5 volts. This has the effect of achieving an equal mark/space ratio on the signal.

1.11 External Connections



1.12 External Socket Assignments

The four main interconnection sockets are assigned as follows:-

PL1 refer to NASBUS functional specification

PL2 (SERIAL)	1	DRIVE	9	20mA LOOP IN
	2	+5V	10	+12V
	3	RS232 IN	11	GND
	4	EXT TX CLOCK	12	20mA LOOP OUT
	5	EXT RX CLOCK	13	CASS. OUT HI
	6	RS232 OUT	14	CASS. OUT LO
	7	-12V	15	GND
	8	spare	16	CASS IN

PL3 (KEYBOARD)	1	DØ	9	D4
	2	+5V	10	$\overline{\text{RESET SWITCH}}$
	3	D1	11	D5
	4	$\overline{\text{NMLSW}}$	12	IC24/2(QØ)
	5	D2	13	D6
	6	IC24/15 (Q5)	14	IC24/5 (Q1)
	7	D3	15	D7
	8	IC24/7 (Q2)	16	GND

PL4	1	B5	14	NC
	2	B4	15	A1
	3	B6	16	GND
	4	B3	17	A2
	5	B7	18	GND
	6	B2	19	A3
	7	ARDY	20	+5V
	8	B1	21	A4
	9	$\overline{\text{BSTB}}$	22	+5V
	10	BØ	23	A5
	11	$\overline{\text{ASTB}}$	24	A7
	12	BRDY	25	A6
	13	AØ	26	NC

IMPORTANT

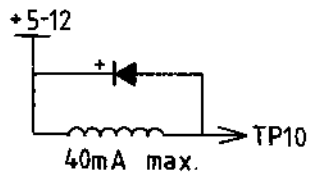
PL2 CARRIES ±12V RAILS ; THE KEYBOARD MAY BE SERIOUSLY DAMAGED IF IT IS CONNECTED TO PL2.

1.13 Test Points

POINT	PARAMETER	CCT. DIAGRAM SHEET
TP1	300Hz from IC31/3	2
TP2	1760 Hz from IC21/1 (see note (1))	2
TP3	Keyboard port ø bit 7	2
TP4	Ext TX clock input	2
TP5	Ext Rx clock input	2
TP6	Cassette 500mV (HI) output	2
TP7	Cassette 50 mV (LO) output	2
TP8	Ov for cassette 1/0	2
TP9	Cassette Input	2
TP10	Cassette Drive (see note (2))	2
TP11	Ov for video	4
TP12	video output signal	4
TP13	Ov	
TP14	-5V	
TP15	-12V PSU inputs	
TP16	+12V	
TP17	+5V	
TP18	BUSRQ (Bus Request) NASBUS line 18	1

(1) Actual Frequency 1748Hz

(2) May be used to drive a relay:



TP19	Cassette Schmitt output (Input signal after squaring)	2
TP20	38.4KHz (IC22/1)	2
TP21	38.4KHz from PLL (IC23/IC306)	2
TP22	$\overline{\text{VBLANK}}$ Vertical blanking signal from IC59/2	4
TP23	$\overline{\text{BLANKING}}$ Combined blanking signal from IC8/3	4
TP24	$\overline{\text{BAO}}$ / $\overline{\text{TEST}}$ from NASBUS line 16	1

1.14 Component List, Circuit Reference Order

IC	TYPE	LAYOUT REF.	INSERTED CHECK.
1	MK 3880 -4	S9	( )
2	74LS257	W6	( )
3	81LS97	T11	( )
4	81LS97	W8	( )
5	DP8304	W12	( )
6	74LS04	U5	( )
7	81LS97	T7	( )
8	74LS08	R4	( )
9	N2DB	W5	( )
10	74LS32	P5	( )
11	74LS14	M5	( )
12	74LS221	C7	( )
13	74LS74	E12	( )
14	74LS74	P2	( )
15	74LS74	P4	( )
16	74LS74	R5	( )
17	74LS74	W4	( )
18	7406	U4	( )
19	MK 3881 -4	E9	( )
20	6402	I9	( )
21	4526B	J5	( )
22	4526B	M7	( )
23	MC 14046B	M4	( )
24	74LS378	F5	( )
25	81LS97	D5	( )
26	N2IO/1	P7	( )
27	4070 B	H5	( )
28	4011 B	F7	( )
29	4013 B	J4	( )
30	4520 B	H7	( )
31	4024 B	J7	( )
32	4049 UB	H4	( )
33	4027 B	F4	( )
34	NAS-SYS 1	M18	( )
35	MK 4118**	U18	( )
36	MK 4118**	Q18	( )
37	MK 4118**	P18	( )
38	MK 4118**	S18	( )
39	MK 4118**	L18	( )
40	MK 4118**	J18	( )
41	MK 4118**	I18	( )
42	MK 4118**	G18	( )
43	MK 36271	V18	( )
44	74LS10	G10	( )
45	DP8304	W15	( )
46	74LS155	N16	( )
47	N2MD/3	W10	( )
48	MK 4118	F18	( )
49	74LS193	G12	( )
50	MK 4118	T14	( )
51	74LS163	R11	( )
52	74LS163	D14	( )
53	74LS161	E10	( )
54	NAS - GRA**	J14	( )
55	74LS13	F14	( )
56	74S04	I10	( )
57	74LS123	B12	( )
58	74LS123	C10	( )
59	N2V/2	O12	( )
60	74LS00	K10	( )
61	74LS11	B14	( )
62	74LS157	R12	( )
63	74LS157	P9	( )
64	74LS157	T12	( )
65	74LS165	J12	( )
66	NAS - A/N	M14	( )
67	74LS273	Q14	( )
68	74LS193	L12	( )
69	74LS32	R7	( )
70	DP8304	W13	( )
71	74LS13	M8	( )

RESISTORS

R	TYPE	LAYOUT REF.	INSERTED CHECK
1	2K2	R3	(✓)
2	10K	U2	(✓)
3	10K	V2	(✓)
4	10K	T2	(✓)
5	10K	T2	(✓)
6	2K2	V2	(✓)
7	2K2	U2	(✓)
8	2K2	T2	(✓)
9	2K2	U2	(✓)
10	10K	D7	(✓)
11	10K	R2	(✓)
12	470R	R3	(✓)
13	10K	M2	(✓)
14	150R	T2	(✓)
15	10K	V2	(✓)
16	10K	V2	(✓)
17	470R	L10	(✓)
18	10K	T2	(✓)
19	47K	K2	(✓)
20	47K	B2	(✓)
21	4K7	B2	(✓)
22	560R	C2	(✓)
23	390K	H2	(✓)
24	22K	H2	(✓)
25	100K	H2	(✓)
26	1MO	H3	(✓)
27	100K	H3	(✓)
28	47K	L2	(✓)
29	47K	L2	(✓)
30	100K	M2	(✓)
31	47K	L2	(✓)
32	390K	L2	(✓)
33	1KO	C2	(✓)
34	470R	C2	(✓)
35	2K7	C2	(✓)
36	2K7	E2	(✓)
37	10K	E2	(✓)
38	10K	E2	(✓)
39	470R	U2	(✓)
40	10K	E2	(✓)
41	1MO	E1	(✓)
42	150R	C4	(✓)
43	4K7	C3	(✓)
44	10K	O2	(✓)
45	1KO	O2	(✓)
46	1KO	R2	(✓)
47	1KO	R2	(✓)
48	1KO	E2	(✓)
49	1KO	D2	(✓)
50	1KO	G2	(✓)
51	1KO	F2	(✓)
52	470R	R3	(✓)
53	1KO	F2	(✓)
54	1KO	M10	(✓)
55	1KO	M10	(✓)
56	10K	U2	(✓)
57	10K	V2	(✓)
58			
59			
60			
61	15K	C12	(✓)
62	10K	C12	(✓)
63	10K	H14	(✓)
64	820R	H13	(✓)
65	820R	H13	(✓)
66	2K2	B18	(✓)
67	*	B19	( )
68	4K7*	B15	(✓)
69	4K7*	B15	(✓)
70	6K8*	B17	(✓)
71	220R	B18	(✓)
72	68R	B18	(✓)
73	560R	B16	(✓)
74	10K	D12	(✓)
75	10K	D12	(✓)
76	68R*	B18	(✓)
77	2K7	P11	(✓)
78			
79			
80			
81	10K	B7	(✓)
82	1K2	P11	(✓)
83	220R	L10	(✓)
84	22R	M10	(✓)
85	33R	L10	(✓)
86	2K2	L10	(✓)
87	820R	***	

* indicates the possibility of a different component see page 21.

** OPTIONAL.
*** See construction notes

CAPACITORS

C	TYPE	LAYOUT REF.	INSERTED CHECK
1	1nF	C7	( )
2	68uF	S2	( )
3	68uF	M2	( )
4	2·2uF	X18	( )
5	33pF	P14	( )
6			
7			
8	10nF	B3	( )
9	10nF	F2	( )
10	100pF	G2	(✓)
11	100pF	L2	(✓)
12	2·2uF	M2	( )
13	1nF	D3	( )
14	2·2uF	X16	( )
15	100pF	G5	(✓)
	2·2uF	X17	( )
19	68uF	O11	( )
20	33pF	B7	( )
21	47nF	C13	( )
22	1nF	B12	( )
23	47nF	I13	( )
24	330pF	I13	( )
25	330pF	E11	( )
26	100pF	D11	(✓)
27	1nF	C11	( )
28	10uF	P15	( )
29	10uF	B11	( )
30	10uF	X18	( )

DECOUPLING CAPACITORS

	10nF	X4	( )
	"	V4	( )
	"	S4	( )
4	"	Q4	( )
5	"	Q2	( )
6	"	O4	( )
7	"	K4	( )
8	"	I4	( )
9	"	G4	( )
10	"	X6	( )
11	"	V5	( )
12	"	S5	( )
13	"	Q5	( )
14	"	N5	( )
15	"	K5	( )
16	"	I5	( )
17	"	G5	( )
18	"	E5	( )
19	"	Y7	( )
20	"	S7	( )
21	"	Q7	( )
22	"	N7	( )

DC	TYPE	LAYOUT REF.	INSERTED CHECK
23	10nF	K7	( )
24	"	I7	( )
25	"	G7	( )
26	"	E7	( )
27	"	Y8	( )
28	"	Y10	( )
29	"	V10	( )
30	"	N8	( )
31	"	X11	( )
32	"	V11	( )
33	"	S11	( )
34	"	H11	( )
35	"	F10	( )
36	"	D11	( )
37	"	Y12	( )
38	"	U12	( )
39	"	S12	( )
40	"	P12	( )
41	"	M12	( )
42	"	K12	( )
43	"	F12	( )
44	"	D12	( )
45	"	N14	( )
46	"	Y15	( )
47	"	S14	( )
48	"	L13	( )
49	"	G14	( )
50	"	E14	( )
51	"	C14	( )
52	"	B17	( )
53	"	C17	( )
54	"	V16	( )
55	"	T16	( )
56	"	Q16	( )
57	"	M16	( )
58	"	K16	( )
59	"	J16	( )
60	"	G16	( )

TRANSISTORS

1	BC557	S3	( )
2	BC557	F2	( )
3	BC107	B4	( )
4	2N3904	B17	( )
5	2N3906	O11	( )

DIODES

1	1N4148	N2	(✓)
2	"	C2	(✓)
3	"	D2	(✓)
4	"	C4	(✓)
5	1N4001	X19	( )
6	"	X19	(✓)
7	"	X15	(✓)
8	"	X16	(✓)

ZENER DIODES

ZD	TYPE	LAYOUT REF.	INSERTED CHECK
1	BZY88C6V2	B15	(✓)

LIGHT EMITTING DIODES (LED)

1	TIL 209	S4	( )
2	"	D4	( )

VARIABLE RESISTOR (VR)

1	10K Linear	B8	( )

CRYSTAL (XT)

1	16 MHz	H14	( )

MODULATOR (VIDEO) (MD)

1	ASTEC UM1111E36*	D17	( )

DIL/TIL SWITCHES (LSW) *

1	Erg 10 way SPST	X2	( )
2	Erg 10 way SPDT	I2	( )

LINK BLOCKS (LKB)

1	Each of these is made up from 3 sets of 4 pin plugs (27 in all)	U16	( )
2		R16	( )
3		P16	( )
4		S16	( )
5		L16	( )
6		J16	( )
7		I16	( )
8		H16	( )
9		F16	( )

PLUGS (PL)

1	77 way edge	Y10	
2	16 pin plug	B3	( )
3	"	B6	( )
4	26 pin plug	B10	( )

CABLE ASSEMBLIES (CBS)

1	16 way Double ended
2	16 way Single ended
3	26 way Single ended

* In some kits these switches are omitted, and wire links should be substituted as described in the manual.

1.15 Component List, Numerical Order

NO. USED	TYPE	PINS	CIRCUIT REF.	DESCRIPTION	OBTAINED CHECK
MOS IC's (see handling instructions)					
1	4011B	14	IC 28	Quad 2-input NAND Gate	( )
1	4013B	14	IC 29	Dual D-type flip/flop	( )
1	4024B	14	IC 31	7 stage binary ripple counter	( )
1	4027B	16	IC 33	Dual J-K flip/flop	( )
1	4049UB	16	IC 32	Hex inverting buffer	( )
1	4070B	14	IC 27	Quad 2-input EOR Gate	( )
1	4520B	16	IC 30	Dual 4 bit binary up counter	( )
2	4526B	16	IC 21,22	Programmable ÷ N counter	( )
1	6402	40	IC 20	UART (for Serial I/O) (CMOS)	( )
1	MC 14046B	16	IC 23	Micropower PLL	( )
1	MK 3880-4	40	IC 1	Z80A CPU	( )
1	MK 3881-4	40	IC 19	Z80A PIO	( )
10	MK 4118	24	IC 35-42,48, & 50	RAM (1K x 8)	( )
MEMORY IC's (ROMS)					
1	7602-5	16	IC 47	Open Collector 32 x 8 PROM (N2MD)	( )
2	7603-5	16	IC 26,59	Tristate 32 x 8 PROM (N2IO and N2V)	( )
1	7611-5	16	IC 9	Tristate 256 x 4 PROM (N2DB)	( )
1	NAS-SYS	24	IC 34	ROM 2K x 8 NAS-SYS Monitor	( )
1	NAS-GRA *	24	IC 54	ROM 2K x 8 Std. Graphics Character Gen.	( )
1	NAS A/N	24	IC 66	ROM 2K x 8 Std. Alpha/Num.Character Gen.	( )
1	MK 36271	24	IC 43	ROM 8K x 8 NASCOM 8K BASIC	( )
	*optional				
TTL IC's					
1	74LS00	14	IC 60	Quad 2-input NAND Gate	( )
1	74LS04	14	IC 6	Hex Inverter	( )
1	74S04	14	IC 56	Hex Inverter (High Speed)	( )
1	7406	14	IC 18	Hex Inverter (Open Collector)	( )
1	74LS08	14	IC 8	Quad 2-input AND Gate	( )
1	74LS10	14	IC 44	Triple 3-input NAND Gate	( )
1	74LS11	14	IC 61	Triple 3-input AND Gate	( )
1	74LS14	14	IC 11	Hex Schmitt Trigger Inverter	( )
2	74LS20	14	IC 55,71	Dual 4-input NAND Gate	( )
2	74LS32	14	IC 10, 69	Quad 2-input OR Gate	( )
5	74LS74	14	IC 13-17	Dual D-type flip/flop	( )
2	74LS123	16	IC 57,58	Dual Retriggerable Monostable	( )
1	74LS155	16	IC 46	Dual 1-of-4 Decoder	( )
3	74LS157	16	IC 62-64	Quad 2-input Multiplexer (or 74LS257)	( )
1	74LS161	16	IC 53	4 bit binary counter	( )
2	74LS163	16	IC 51,52	4 bit binary counter (OR 74LS161)	( )
1	74LS165	16	IC 65	8 bit PISO Shift Register	( )
2	74LS193	16	IC 49, 68	4 bit up/down binary counter	( )
1	74LS221	16	IC 12	Dual Monostable	( )
1	74LS257	16	IC 2	Quad 2-input Multiplexer	( )
1	74LS273	20	IC 67	Octal D-type flip/flop	( )
1	74LS378	16	IC 24	Hex D-type flip/flop (OR AMD25LS07)	( )
4	81LS97	20	IC 3,4,7,25	Hex buffer (IC's 3,4,25 may be 81LS95)	( )
3	DP 8304	20	IC 5,45,70	Hex bi-directional buffer (OR 1NS8203)	( )

NO. USED	TYPE	CIRCUIT REF.	DESCRIPTION	OBTAINED CHECK
TRANSISTORS and DIODES				
1	2N3904	TR.4.	NPN TRANSISTOR	( )
1	2N3906	TR.5.	PNP TRANSISTOR	( )
1	NAS 1-03	TR.3.	NPN TRANSISTOR	( )
2	NAS 1-05	TR.1,2.	PNP TRANSISTOR	( )
4	1N4001	D5-8.	DIODE	( )
4	1N4148	D1-4.	DIODE	( )
1	BZY88C6V2	ZD.1.	ZENER DIODE (6·2V)	( )
2	TIL209	LED.1,2.	RED Light Emitting Diode	( )
RESISTORS				
1	22R	R 84	R/R/Bk	(✓)
1	33R	R 85	O/O/Bk	(✓)
2	68R	R 72, 76	Bl/Gr/Bk	(✓)
2	150R	R 14, 42	Br/Gn/Br	(✓)
2	220R	R 71, 83	R/R/Br	(✓)
5	470R	R 12, 17,34,39, & 52	Y/V/Br	(✓)
2	560R	R 22, 73	Gn/Bl/Br	(✓)
3	820R	R 64, 65, 87	Gy/R/Br	(✓)
11	1KO	R 33, 45-51, 53-55	Br/Bk/R	(✓)
1	1K2	R 82	Br/R/R	(✓)
7	2K2	R 1, 6-9,66,86	R/R/R	(✓)
3	2K7	R 35, 36, 77	R/V/R	(✓)
4	4K7	R 21, 43, 68, 69	Y/V/R	(✓)
1	6K8	R 70	Bl/Gy/R	(✓)
21	10K	R 2-5,10,11,13, 15,16,18,37,38, 40,44,56,57,62, 63,74,75,81	Br/Bk/O	(✓)
1	15K	R 61	Br/Gn/O	(✓)
1	22K	R 24	R/R/O	(✓)
5	47K	R 19,20,28,29, 31	Y/V/O	(✓)
3	100K	R 25, 27,30	Br/Bk/Y	(✓)
2	390K	R 23, 32	O/W/Y	(✓)
2 +2	1MO	R 26, 41	Br/Bk/Gn	(✓)
VARIABLE RESISTOR				
1	10K	VR.1.	Linear Potentiometer type 43p.	( )
CAPACITORS				
2 ✓	33pF	C 5,20	Ceramic	( )
4 ✓	100pF	~~C 10,11,15,26~~	Ceramic	( )
2 ✓	330pF	~~C 24,25~~		( )
4 ✓	1nF	~~C 1,13,22,27~~	Ceramic	( )
62	10nF	C 8,9,DC1-60	Ceramic	( )
			Ceramic DC indicates DECOUPLING CAPACITOR	( )
				( )
2	47nF	~~C 21, 23~~	Ceramic	( )
4	2·2uF	~~C 4,12,14,18~~	Tantalum Bead (15 volt)	(✓)
3	10uF	~~C 28,29,30~~	Tantalum Bead (15 volt)	( )
3	68uF	C2, 3, 19	Tantalum Bead (6 volt)	( )
IC SOCKETS				
	PINS			
3	40 ✓			( )
14	24 ✓			( )
8	20 ✓			( )
26	16 ✓			( )
21	14			( )

KEYBOARD

NO. USED	CIRCUIT REF.	DESCRIPTION	OBTAINED CHECK
1	KBD	Built and tested solid state keyboard with 57 keys and associated circuit on PCB.	( )
1		Switch to be added to above.	( )
1		Keytop marked 'RS' or 'Reset' for Reset function	( )
MISCELLANEOUS			
1		12" x 8" Double sided PCB with through hole plating and solder resist on both sides, yellow silk screen legend on the component side and a gold plated edge connector on the other side.	( )
1		16 MHz Xtal	( )
27	LKB.1-4	4 pin plugs for Linkblocks	( )
2	PL 2,3	16 pin plugs	( )
1	PL 4	24 pin plug	( )
1	LSW 1 *	DIL 10 way SPST Switch	( )
1	LSW 2 *	TIL 10 way SPDT Switch	( )
1	MD1	ASTEC UHF Modulator UM1111E36 (or type UM1231 for France)	( )
1		16 way double ended ribbon cable assy for PL3-KBD	( )
1		16 way single ended ribbon cable assy for PL2	( )
1		26 way single ended ribbon cable assy for PL4	( )
24	TP1-24	Solder pins push fit in 1 mm dia.hole (for video, cassette connections etc.)	( )
1		Phono Plug	( )
1		Belling Lee Co-ax Plug (for TV)	( )
2 metres		Co-ax Cable to TV set aerial skt.	( )
10 metres		22 Gauge Solder	( )

* These switches may be omitted from kits, in which case wire links are used in their place as detailed in the manual.

1.16 Component changes for use outside UK

CHANGES FOR VHF 60Hz TV FIELD SYSTEMS

(USA, Japan etc.)

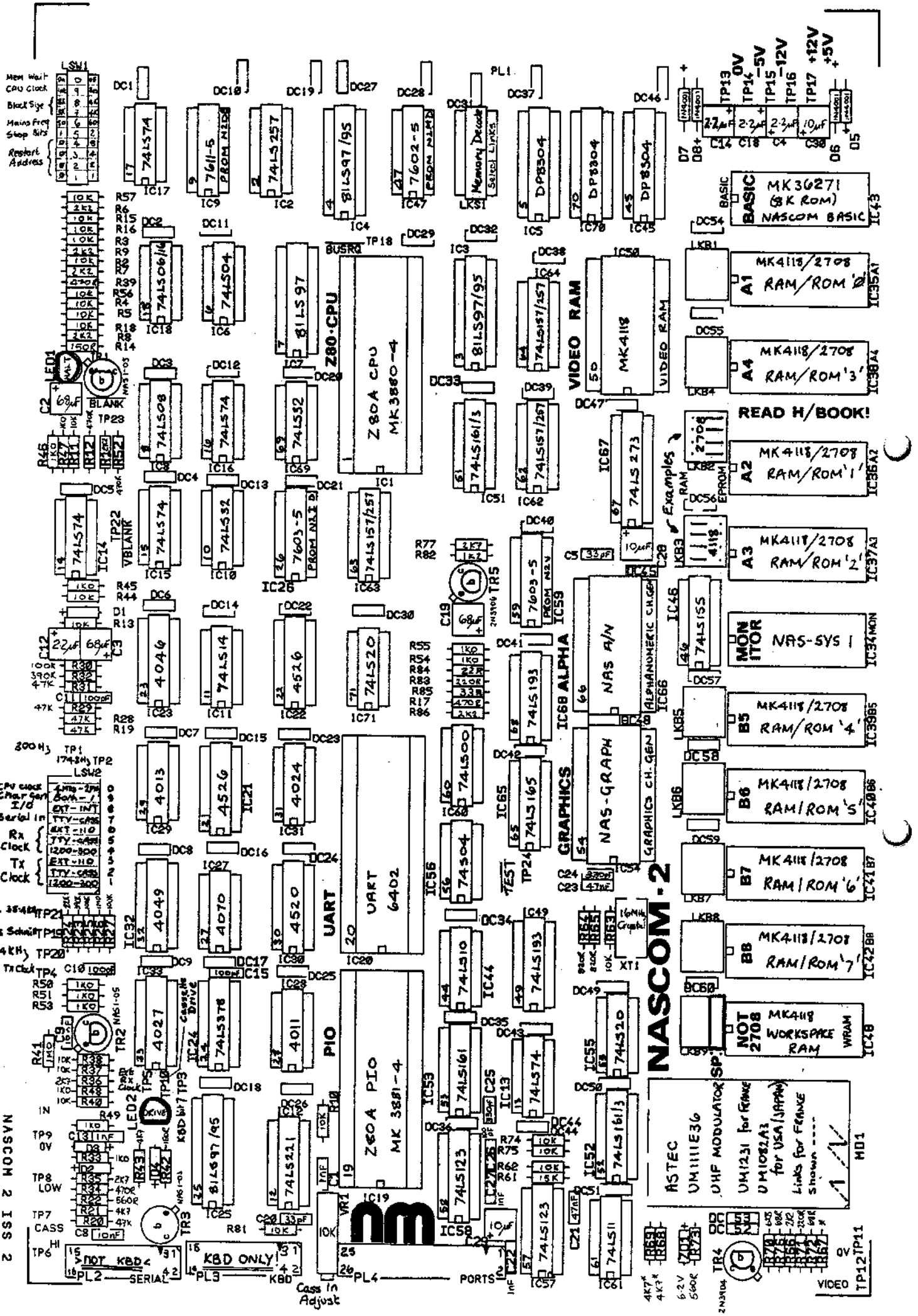
R68	6K8	REPLACES	4K7
MD1	UM1082A3	"	UM1111E36

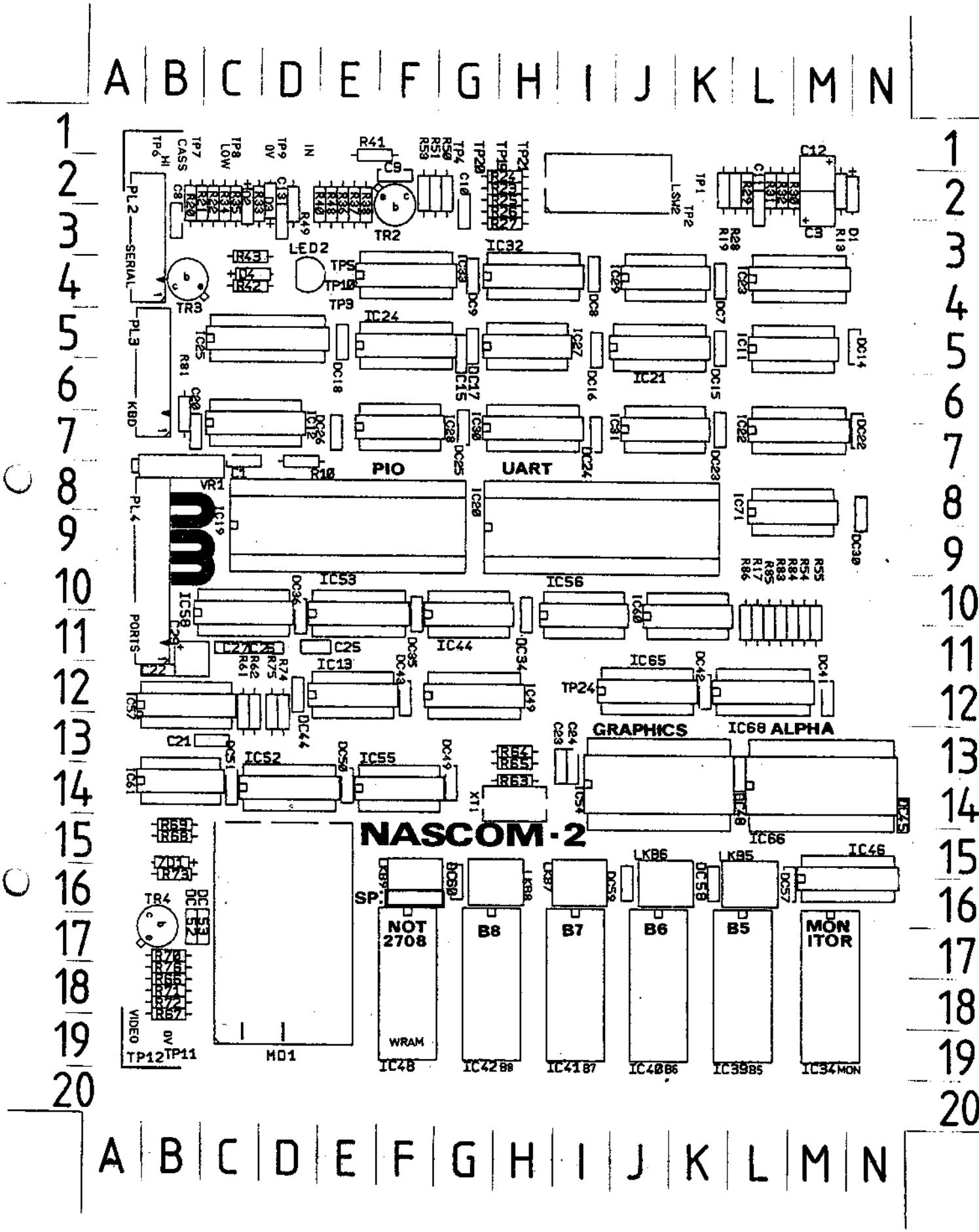
CHANGES FOR POSITIVE MODULATION (UHF) TV SYSTEMS

(France etc.)

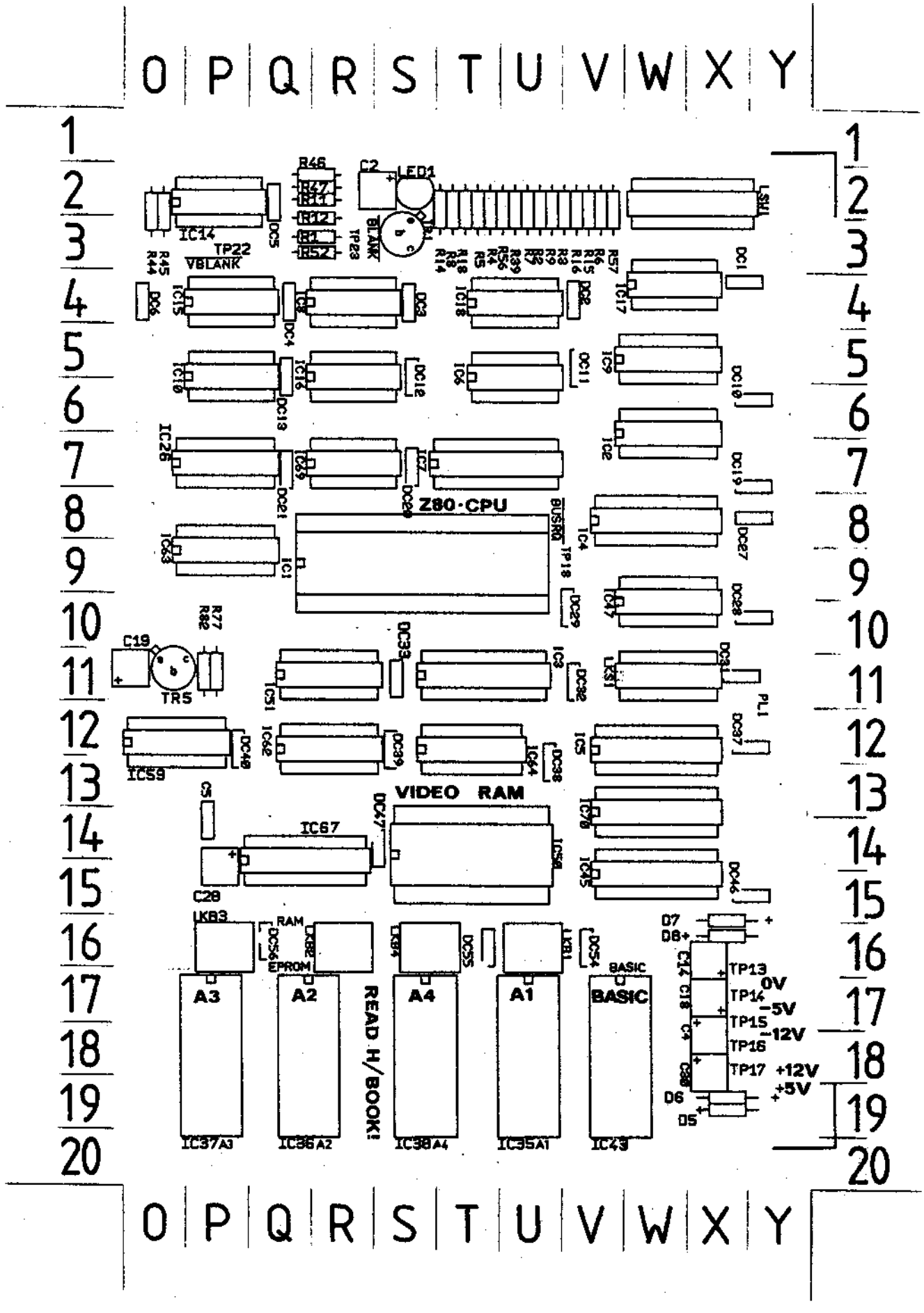
R67	1K0	ADDED	
R76	2KO	REPLACES	68R
R70	2K4	"	6K8
R68, 69	3K9	"	4K7
MD1	UM1231	"	UM1111E36

1.17 Component and Board Layout

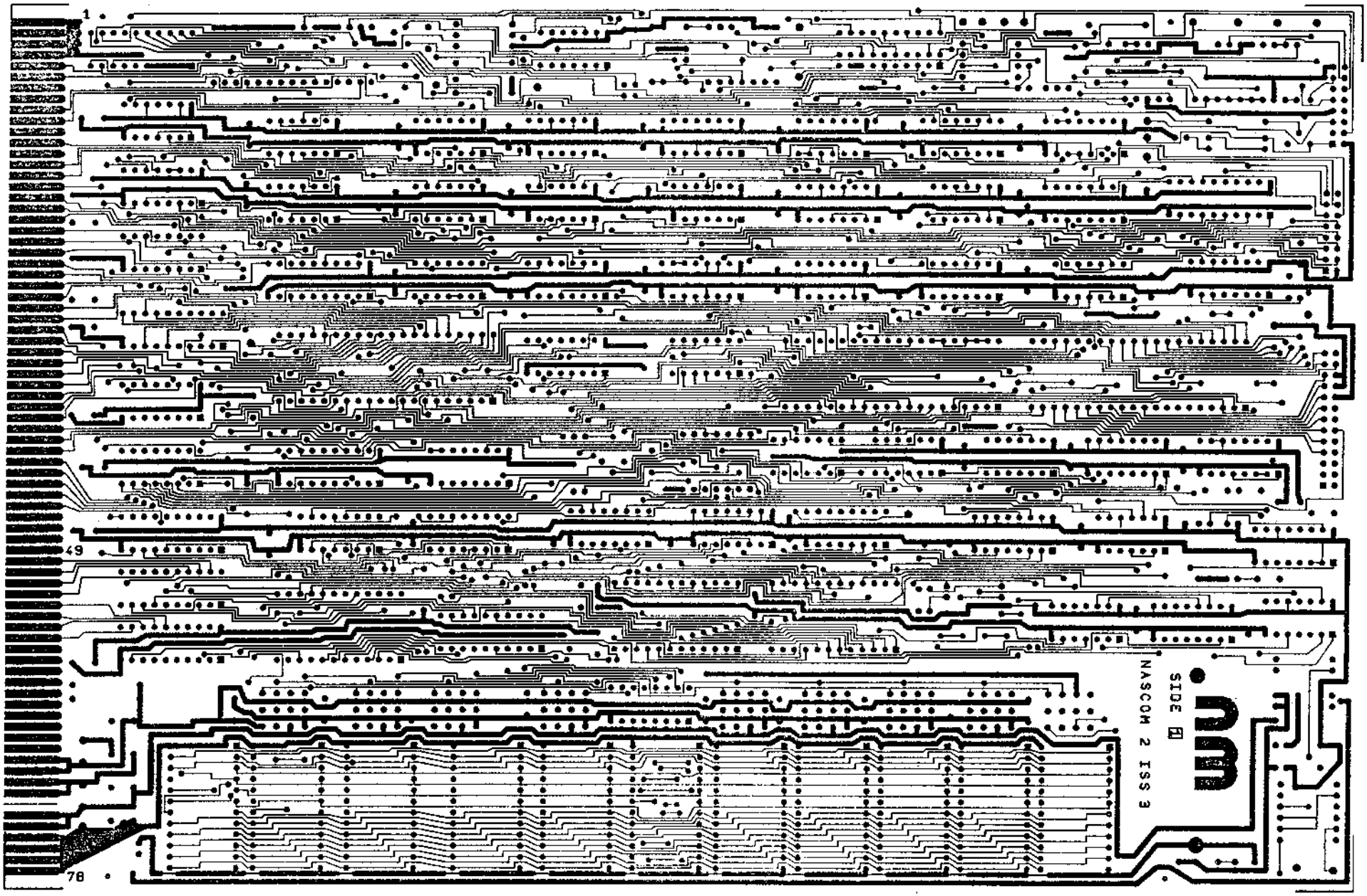




NASCOM-2
PIO
UART
GRAPHICS
ALPHA
NOT 2708
B8
B7
B6
B5
MON ITOR
WRAM
SP
MO1
IC48
IC42 B8
IC41 B7
IC40 B6
IC39 B5
IC34 MON
IC32
IC24
IC21
IC53
IC56
IC44
IC13
IC65
IC52
IC55
IC68
IC66
IC46
IC58
IC20
IC19
IC71
IC60
IC49
IC57
IC61
IC54
IC28
IC30
IC31
IC22
IC25
IC27
IC11
IC12
IC26
IC29
IC23
IC33
IC36
IC35
IC43
IC42
IC41
IC40
IC39
IC34
TR2
TR3
TR4
LED2
VR1
PL2
PL3
PL4
SERIAL
KBD
PORTS
VIDEO
TP12
TP11
TP24
XT1
LSW2



O P Q R S T U V W X Y
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
R46
R47
R11
R12
R1
R52
C2
LED1
BLANK
TP23
TP1
LSH1
IC14
DC5
TP22
VBLANK
R45
R44
R57
R6
R15
R16
R3
R9
R7
R39
R56
R4
R5
R18
R8
R14
DC1
DC6
IC15
IC8
DC3
IC18
DC2
IC17
DC4
IC10
IC16
DC12
IC6
DC11
IC9
DC10
DC13
IC26
IC69
IC7
IC2
DC19
DC21
DC20
Z80·CPU
BUSRQ
IC4
DC27
IC63
IC1
TP18
DC29
IC47
DC28
R77
R82
C19
TR5
DC33
IC3
DC32
LKS1
DC31
IC51
PL1
IC59
DC40
IC62
DC39
IC64
DC38
IC5
DC37
VIDEO RAM
C5
IC67
DC47
IC70
IC50
IC45
DC46
C28
LKB3
RAM
DC56
LKB2
EPROM
LKB4
DC55
LKB1
DC54
BASIC
D7
D8+
C14
C18
C4
C30
TP13
TP14
TP15
TP16
TP17
0V
-5V
-12V
+12V
+5V
D6
D5
A3
A2
A4
A1
BASIC
READ H/BOOK!
IC37A3
IC36A2
IC38A4
IC35A1
IC43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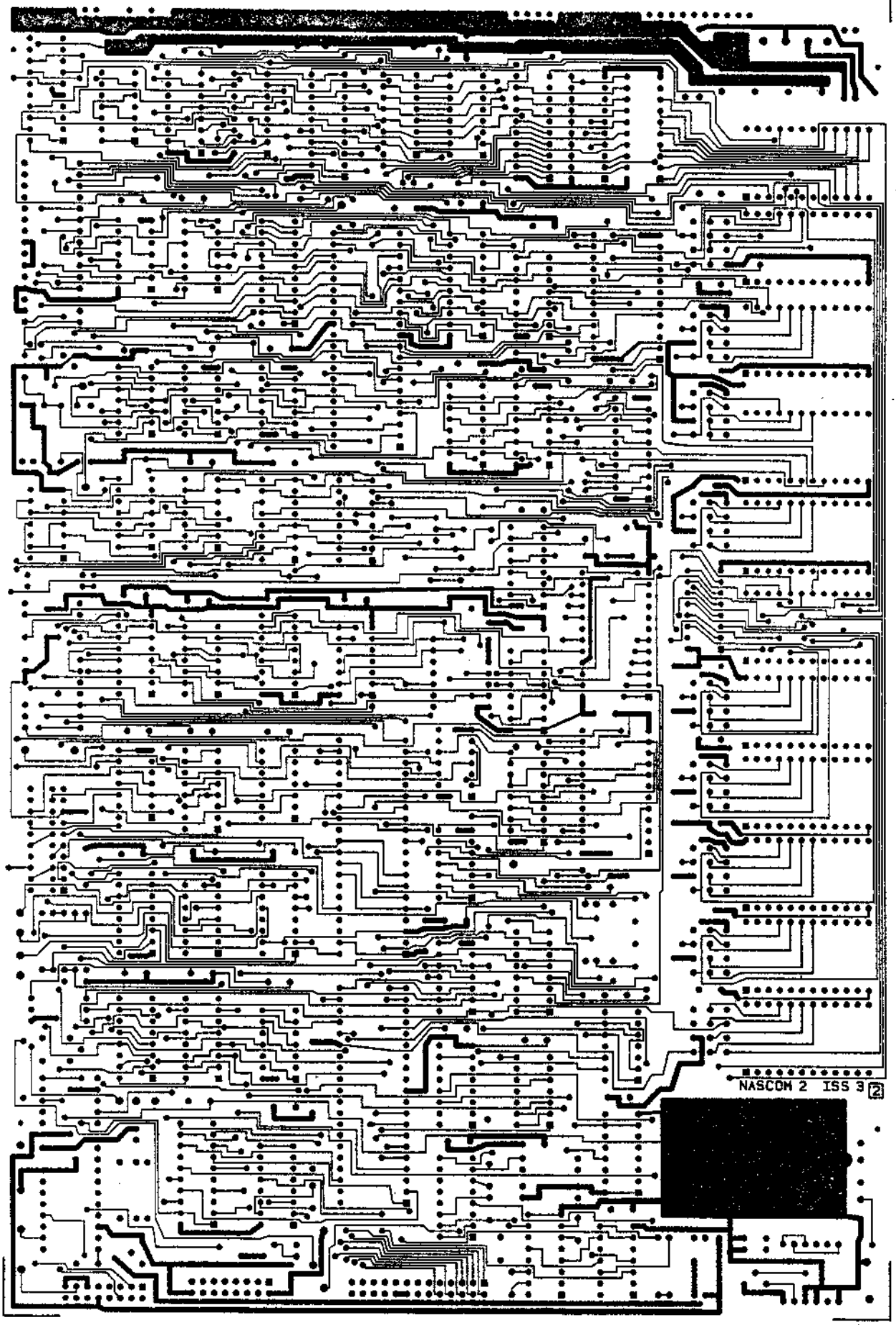
49
78
NASCOM 2 ISS 3
SIDE 2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