

NASBUS FUNCTIONAL SPECIFICATION

Document No. PF/007 Issue No. 1

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ISSUE	DATE	REVISED SHEETS	REMARKS
1	18.9.78	(i)-(ii), 1-1, 2-1, 3-1-3.3, 4-1,5-1, A.1-A.2, B.1-B.2, C.1-C.2.	First formal issue
ORIGINATOR:	A.R.Rundle	APPROVAL: AR	Rundo

Specification

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1. <u>Introduction</u>

The NASBUS is a bus used to add extra boards (e.g. memory and I/O) to the basic NASCOM Microcomputer. It consists mainly of buffered Z80 input and output signals together with some additional bus control lines.

The equipment practice used has been chosen for its wide availability and low cost.

This document defines the electrical and physical charateristics of the NASBUS.

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The beginning a 77 way bus, with specula cliccated as

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2. (1) References 083 odd son canel 9 yalmad at traditional and by Fig. Getality grational and operation of 789 deposed

This specification should be read in conjunction with most the following documents: begins seaff last stoke

- situated in littore use. Hines marked spares of the best 1. Z80 Microcomputer devices Technical Manual MK 3880 Central Processing Unit - Mostek.
 - VERO catalogue. 2.

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3. Functional Description

The Nasbus is a 77 way bus, with signals allocated as described below. Please see the Z80 cpu manual (1) for details of timing and operation of Z80 derived

Note that lines marked "Reserved" have already been allocated for future use. Lines marked spare may be used for any purpose but we do not guarantee not to redefine and use them in the future.

	PIN	SIGNAL NAME	Description S
	1 4 2 3 4	Ov Ov Ov	Power supply and system ground
	5 6 7 8	Clock (spare) (spare) (spare)	2 MHZ buffered system clock
	9	RAM DISABLE*	An active low signal which disables output from any RAM card on the bus. Used to give ROM priority over RAM.
	10	RESET SWITCH *	An active low signal which initiates a short pulse on the RESET line (pin 14), to reset the system without destroying dynamic RAM contents.
	11	NASCOM MEM	A decoded signal from one of the RAM boards in the system defining which 4K memory block is used by the NASCOM. (Usually 0000H - OFFFH).
	12	NASCOM 10	A decoded signal from an IO extension card defining which ports are used on the NASCOM.
	13	DBDR *	This signal 'Data bus drive' determines the direction of the bidirectional data bus buffers on the NASCOM Buffer card. It is a decoded signal made active by any device
³ ex			transferring data to the NASCOM card. Active low to

drive data to the NASCOM.

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PIN	SIGNAL NAME	Description MAR LAVOUR MAR
14	<mark>- Passan</mark> Gold Saide Color. De l'Angele de Carta de la gradient de la color.	The main system reset line. The duration of the RESET pulse is restricted to
	in the first of the first of the second of t	maintain dynamic RAM refresh.
15	HALT Magazines and declaration (ACC) (Armed Controls)	Buffered Z80 HALT signal.
16 17	BAI BAO STA STA CARTANTA	These signals are used to provide a 'daisy chain' Bus acknowledge signal for priority bus control.
18	BUSRQ *	Z80 BUSRQ signal. Used by external devices to request
	e de la companya del companya de la	control of the data, address and control lines.
19 20	IEI De la	These signals form a 'daisy chain' connection for
21	(reserved for NMT) *	interrupt priority control. On the NASCOM the Z80 Non Maskable Interrupt is
	and the second of the second o	dedicated to the monitor single step feature. <u>Th</u> is
	The Control of the Co	line is reserved for NMI for users who require this signal on the bus.
22	INT *	Z80 Interrupt request line.
23	WAIT *	Z80 WAIT line
24	RFSH 7 Transport	Tristate buffered Z 80 RFSH signal
25	MI , Virgar Comit	Buffered Z80 MI signal.
26	IORQ	Tristate buffered Z80 TORQ
27		Tristate buffered Z80 MREQ
28 _. 29		Tristate buffered Z80 WR
30	AO	Tristate buffered Z80 RD
31 32 33 34	A1	To the color was to A fair the 1996. Filipina of state (1999) was to a second
35 36 37 38 39	A5 A6 A7 A8 A9	Tristate Z80 Address lines 0 to 15

		issue 1	
	The state of the s	ARM YOUR	
PIN	SIGNAL NAME	DESCRIPTION	
o teat † ∫	of the coast of an edition		
40	$\in \mathbf{A}, 10$. The constant $x \in \mathbb{R}^n$	· •	
41	A11		
42	A12		
43	410		
44	A14.		
44	A14		
45	A15	•	
		•••	
46			
47	rajoje programa i kaj		
48) Peserved	·	
49	in 🐧 in the control of the State of the Control of		
	•		
50	DO	• देशकृति	
51	D1	•	
	Di		
52	<i>D2</i>		
53	100	Bidirectional, Tristate Z8	80
54	D4	Data lines 0 to 7.	
55	D5	: *}	
56	D6		
57	D7		
•			
58	The state of the s		
59	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		
60	· /		
61) Reserved		
62	S The second of		
63	Section 1981 Section 1985		
64)	•	
65	- 1	<i>i</i>	
	•		
		· 1.7	
66	Unused to provide separation	of signal and power lines.	
6 7 🧷			
	- 1	**	
68	-5 V	Power supply	
69		Power supply	
70	-5V -12V	rower supply	•
70	-127	11 11 NO TO 10 10 10 10 10 10 10 10 10 10 10 10 10	
71	-12V , ·	11 X X X	
72	Keyway		
73	+12V	Power Supply	
74	+12V	11 1 15 - 2	
	and the second of the second		
7 5	+ 5V	11 11	
76	+ 5V	If It	
77	+ 5V	11 11	-
78	+ 5V	11 11	
10	T 01		

^{* = &}quot;Open Collector" signal line

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Electrical Specification

4.1 Tristate Logic

robation the section of These lines are driven by low power Schottky tristate buffers capable of sinking 16 mAriae capable of driving 10 standard TTL loads (1.6mA sinking, 40 a A source) or approximately 40 low power Schottky inputs (0.36 mA sinking, 20 M A source) while retaining logic zero 0.4v and logic 1>2.4v. Ton Table ad Almoda Correct

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Open Collector But Dakou pur protocod ar e con e 4.2

Open collector lines are pulled up to 5 v. Any board can pull down to zero provided it is capable of sinking 16 mA.

4.3 Power supplies

In order to avoid overloading the motherboard and the system power supplies the following rules should be applied.

- (a) All bus fines of the same voltage should be commoned on the board. The those off the white transfer .
- No board should draw a total of more than: (b)
 - 2.0 Amps
 - 5v 0.5 Amp
 - + 12v 1.0 Amp
 - 12v 0.5 Amp
- The whole occupied Nasbus should not draw more than: (c)

and the second section of the second section is a second section of the second section in the second section is a second section of the second section in the second section is a second section of the second section in the second section is a second section of the second section in the second section is a second section of the section of

- 8 Amps 5v
- 5v 1 Amp
- + 12v 2 Amps
- 12v 1 Amp

4.4 General Design Points

Boards should be designed where possible to apply no more than 2 or 3 low power loads to any signal line of the Nasbus. In any event, a maximum of 1 TTL load must not be exceeded.

Note that tristate lines will float if the Nascom cpu is disabled e.g. by a bus request.

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Electrical Specification

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5. Physical Specification

5.1. Board Specification Signature of the second s

5. 1.11 wird Board Dimensions As all pathala to eldeges expres-

The standard board size is 203,20 mm long t 0.00,
0.30 by 203.20 mm. high + 0.00, - 0.25 (i.e. 8 x 8 inches).

The thickness should be 1.60 nominal (including copper)

See also Appendix A.

A suitable prototyping board is Vero type 10-0155 F (up to 45 DIPs Type Nos - 06-3462C and 06-3463J can also be useous 21 Ji beliver one of such the

is order to avoid overleading the retheringerd

5.1.2 Contact Pitch

The contact pitch is 2.54 mm. 77 of the possible 78

ways are used, with a reference key 7 from the bottom

(component side). The contacts used are on the solder side.

5.2. Connector Specification

Suitable connectors are Vero type 14-0998G or Varelco type 00.6072-080-657-101 with polarising key at position 73, position 1 and 80 blank. (See Appendix B).

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reards should be designed where position to sight so millioned 2 or 2 low power loads to any signal line of the Mastro. In any event, a maximum of the load, pure son

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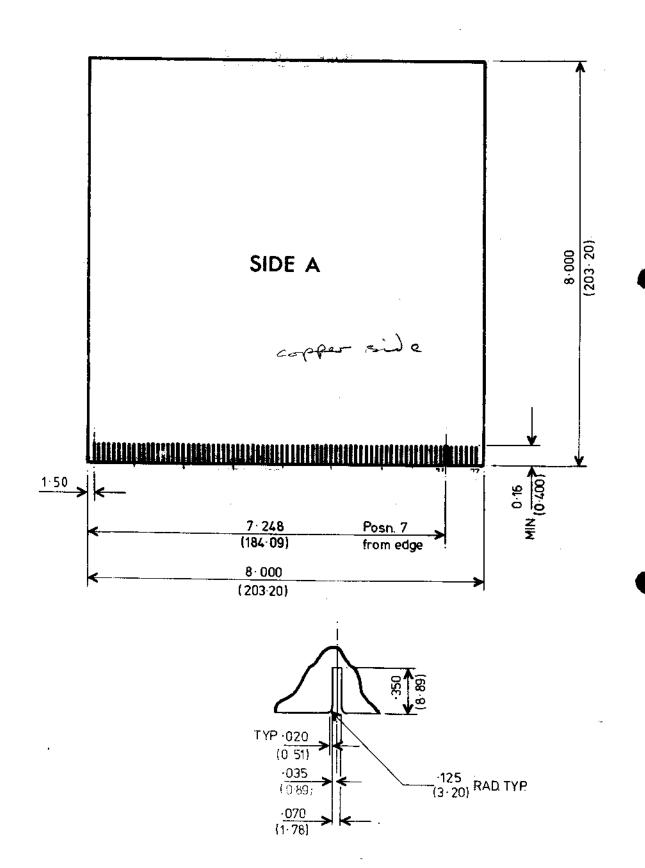
APPENDIX A

BOARD OUTLINE

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Dated of Reading Key

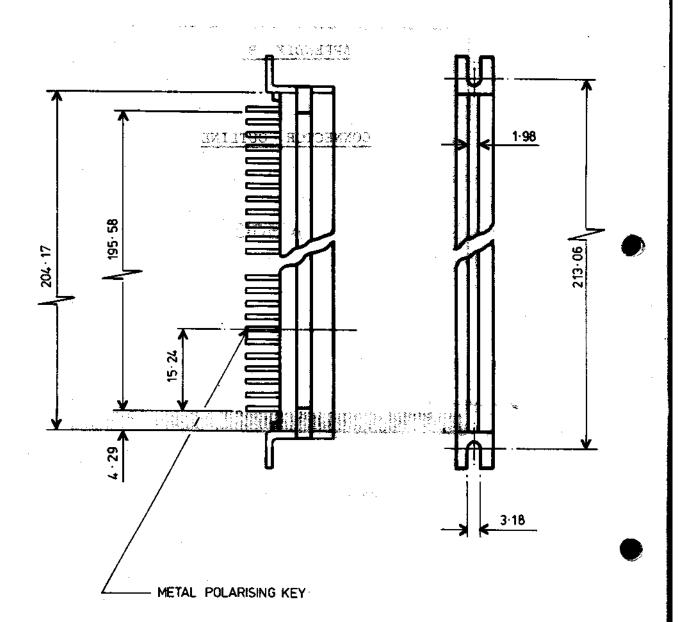


Detail of Polarising Key

CONNECTOR OUTLINE

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APPENDIX C

NASBUS SUMMARY

Lines marked * are open collector: those overlined are $\overline{\text{NOT}}$ (logic level).

```
1,2,3,4
                                    ØV: GROUND
5
                                    Ø (buffered)
6,7,8
                                    spare
                                    RAMDISABLE*
                                    RESET SWITCH
11
                                    MEMEXT
                                    TOEXT
                                    DRIVE *
RESET
HALT
13
14
17
                                    BUS AK OUT
18
                                    BUS RQ*
19
                                    IEI
                                    IFO
21
                                    Reserved for NMI
22
                                    WAIT*
24
                                    M1
25
26
                                    TORO
27
                                    MRFO
28
                                    WR
29
                                    PD)
                                    A0
31
                                    A1
                                    A2
                                    A3
34
                                    Α4
                                    A5
                                    A6
37
                                   A7
                                    A8
                                   AO
40
                                   A10
41
                                    A11
42
                                   A12
43
                                   A13
44
                                    A14
45
                                   A15
46,47,48,49
                                   Reserved
50
                                   DO
51
                                   D1
                                   D2
                                   D3
54
                                   D4
55
                                   D5
56
                                   D6
57
                                   1)7
58,59,60....65
                                   Reserved
66,67
                                   To separate signal and power lines
68,69
                                   -ve 5V
70,71
                                   -ve 12V
72
                                   KEY
73,74
                                   +ve 12V
75,76,77,78
                                   +ve 5V
```