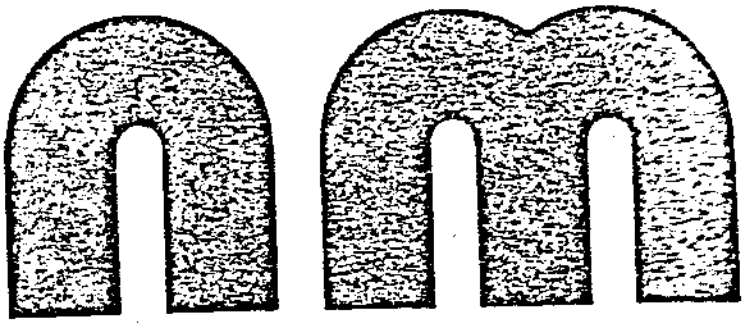


Nascom Microcomputers

MEMORY CARD

FUNCTIONAL SPECIFICATION

Document No. PF/003

Issue No. 2

CONTENTS

1. INTRODUCTION

The Nascom Extended memory card is designed to provide extra memory for the Nascom 1*microcomputer. It connects directly to the 77 way Nasbus and has sockets for up to 32k of RAM (read-write memory) and 4k of ROM (read only memory). The RAM circuitry uses industry standard 16 pin chips.

This document defines the electrical and physical characteristics of the Extended Memory card.

2. REFERENCES

1. Z80 CPU Technical Manual
2. Nasbus Functional Specification. Nascom Microcomputers Document No. PF/007 Issue 1.
3. MOSTEK 4027 RAM data sheet
4. MOSTEK 4116 RAM data sheet
5. Intel 2708 EPROM data sheet
6. Nascom Buffer Board Functional Specification. Nascom Microcomputers Document No. PF/003
7. Nascom 1 Construction Notes

3. FUNCTIONAL DESCRIPTION

The Extended memory card is a fully buffered memory system contained on a single circuit board compatible with the Nasbus. It provides extra program and data storage for users of Nascom microcomputers. The card has sockets for up to 32k bytes of read write memory (RAM) and 4k bytes of read only memory (ROM). All IC numbers refer to the Nascom Memory Extension card circuit diagram.

3.1 RAM MEMORY

3.1.1 GENERAL DESCRIPTION

The RAM circuitry has been designed to use industry standard 16 pin dynamic memory devices. Sockets are provided for sixteen chips, ICS 4-19 arranged in two banks of eight providing the following memory configurations:-

	8 off 4k x 1 chips	4k bytes
or	16 off 4k x 1 chips	8k bytes
or	8 off 16k x 1 chips	16k bytes
or	16 off 16k x 1 chips	32k bytes

The Z80 address space is fully decoded on card for both 4k and 16k memory blocks and the address of each bank is selected by wire links from the outputs of IC22 and 23. By using the 'wired-OR' capability of these ICs 16k banks of memory may be located on any 4k boundary.

The RAM refresh is performed by the Z80 CPU without any loss of processing speed. For refresh to be maintained it is essential that CPU operation is not suspended by either a WAIT or BUS REQUEST for longer than two milliseconds.

The Nasbus RAM DISABLE feature is supported by the extended memory card. If Nasbus line 11, (RAM DISABLE) is held low RAM output buffer, IC2 will remain in the high impedance state preventing RAM data reaching the Nasbus. This allows either external or on board ROM tc take priority over RAM if address overlap is necessary in a system with large amounts of RAM.

3.1.2 MEMORY ACCESS TIMING

The following memory access timing assumes a Nascom 1 running at 2MHz, and a Nascom Buffer card. Timing is referenced to the Z80 CPU, see Reference 1 for detailed timing diagrams.

The access time for 16 pin dynamic RAMS is measured from the active edge of "column address strobe", CAS (see refs. 3 and 4 for further details). In this memory design CAS is generated from the rising edge of the Z80 T2 clock state. The critical memory access time for the Z80 occurs during the op-code fetch or M1 cycle and in this case data must be available from memory 50nS before the end of the T2 clock state. This allows 450nS maximum access time including all buffer delays.

The following is a breakdown of the actual timing for the Extended memory board.

Memory access time components		Cumulative delay from start of T2 clock
1. System. Clock delay from CPU clock (Negative because there are two gate delays between the Nasbus and CPU see Ref 6 for details)		-25nS
2. Set time for 74LS74 (IC31)	25nS	OnS
3. Transition time for address multiplexers ICs 20 & 21	20nS	20nS
4. Three gate delays to leading edge of CAS	60nS	80nS
5. Memory chip access time:- slowest is for MK4027-4. CAS access time	165nS	245nS
6. Memory board data buffer delay	15nS	260nS
7. Buffer board data buffer delay	15nS	275nS

This leaves a margin of 175nS in the minimum required access time of 450nS. Maximum CAS access time permitted with slower memory chips is 330nS.

3.1.3 16k/4k RAM SELECTION

Two wire links are provided to make the circuit changes necessary to accomodate 16k or 4k chips.

For 4k chips Link 3 should have common connected to "4k" and P1 connected to P2.

For 16k chips Link 3 should have common connected to "16k" and P1 connected to P3.

3.1.4 'ROW-ADDRESS STROBE' OPTIONS

Provision has been made for the possible future use of alternative dynamic RAM devices which may require a +12V signal for the 'Row Address Strobe' (RAS). Wire links must be inserted as follows for each bank of RAM to select the correct RAS option.

IC 4-11	Normal (4027/4116) RAS	Link P12 to P13
IC 4-11	+12V RAS	Link P12 to P11
IC 12-19	Normal (4027/4116) RAS	Link P 9 to P 8
IC 12-19	+12V RAS	Link P 9 to P10

3.2 ROM MEMORY

Sockets are provided for four 2708 Eraseable Programmable Read only Memories (EPROMS) organised as a block of 4k bytes. The start address of the ROM block is fixed by a single wire link. In the case of a system with large amounts of RAM where overlap of RAM and ROM addresses occurs on board gating will give priority to the ROM.

3.3 ADDRESS SELECTION

The sixteen outputs of IC'S 22 and 23 provide select signals for each

4k byte block of memory in the total 64k of Z80 address space. This allows the user to position either RAM or ROM starting at any 4k address boundary. The only exception to this is the memory block from 0000H to 0FFFH which is used by the Nascom 1 board itself. The decode for this block is connected via the Nasbus to Nascom 1 to provide the $\overline{\text{MEXT}}$ signal (see section 5).

3.3.1 ROM ADDRESS SELECTION

The start address of the ROM block is set by a single wire link from P5 to one of the 16 4k decode pads. Table 3.1 shows which pad to select. For example when the start address of the ROM block is to be F000 Hex the link should be from pad 12 to P5.

3.3.2 RAM ADDRESS DECODE - 4k CHIPS

The address select pad for ICs 4-11 is P7 and for ICs 12-19, P6. The start address for each block is set by linking the address select pad for the block with the appropriate 4k decode pad as shown in Table 3.1. For example to fix the start address of ICs 4-11 at 1000 Hex link P7 to decode pad 6. To fix the start address of ICs 12-19 at 2000H link P6 to decode pad 7.

3.3.3 RAM ADDRESS DECODE - 16k CHIPS

There are two possible methods of address selection for banks of 16k chips.

a) When the block of memory is to start on a 16k boundary (0000H, 4000H, 8000H or C000H) the 16k decode pads can be used. A single wire link between the address select pad (P6 or P7) and one of the four 16k decode pads will fix the start address for the block. Table 3.2 shows the memory addresses selected by the 16k decode pads. Note that if the addresses selected are 0000-3FFF Hex the first 4k bytes, 0000-0FFF Hex will be lost since this address space is already occupied by memory on the Nascom 1.

b) The alternative method of address selection allows the user to fix the start of a 16k block at any 4k address boundary. Four of the 4k address decodes are connected together to form a composite 16k decode which is then linked to the memory bank address select pin (P6 or P7). For example, to fix the start address of ICs 4-11 at 1000 Hex 4k decodes 6,7,8 and 1 should be linked to P7. Table 3.3 shows the connections necessary for other memory addresses.

TABLE 3.1

4k memory decode pads

Pad No.	4k Block Memory Address (Hexadecimal)
1	4000-4FFF
2	5000-5FFF
3	6000-6FFF
4	7000-7FFF
5	0000-0FFF
6	1000-1FFF
7	2000-2FFF
8	3000-3FFF
9	C000-CFFF
10	D000-DFFF
11	E000-EFFF
12	F000-FFFF
13	8000-8FFF
14	9000-9FFF
15	A000-AFFF
16	B000-BFFF

TABLE 3.2

16k memory decode pads

Pad No.	16k Block Memory Address (Hexadecimal)
0	0000-3FFF
1	4000-7FFF
2	8000-BFFF
3	C000-FFFF

TABLE 3.3

'Wired-OR' Address Selection for 16k Chips

Memory Block Addresses (Hexadecimal)	4k decodes linked together
0000-3FFF	5,6,7,8
1000-4FFF	6,7,8,1
2000-5FFF	7,8,1,2
3000-6FFF	8,1,2,3
4000-7FFF	1,2,3,4
5000-8FFF	2,3,4,13
6000-9FFF	3,4,13,14
7000-AFFF	4,13,14,15
8000-BFFF	13,14,15,16
9000-CFFF	14,15,16,9
A000-DFFF	15,16,9,10
B000-EFFF	16,9,10,11
C000-FFF	9,10,11,12

4. SUMMARY OF WIRE LINK OPTIONS

4.1 4k/16 select

For 4k chips	Link P1 to P2	Link 3	Common to 4k
For 16k chips	Link P1 to P3	Link 3	Common to 16k

4.2 Memory Block Selects

P4	$\overline{\text{Nascom MEM}}$ select
P5	4k ROM block select
P6	RAMS IC 12-19 select
P7	RAMS IC 4-11 select

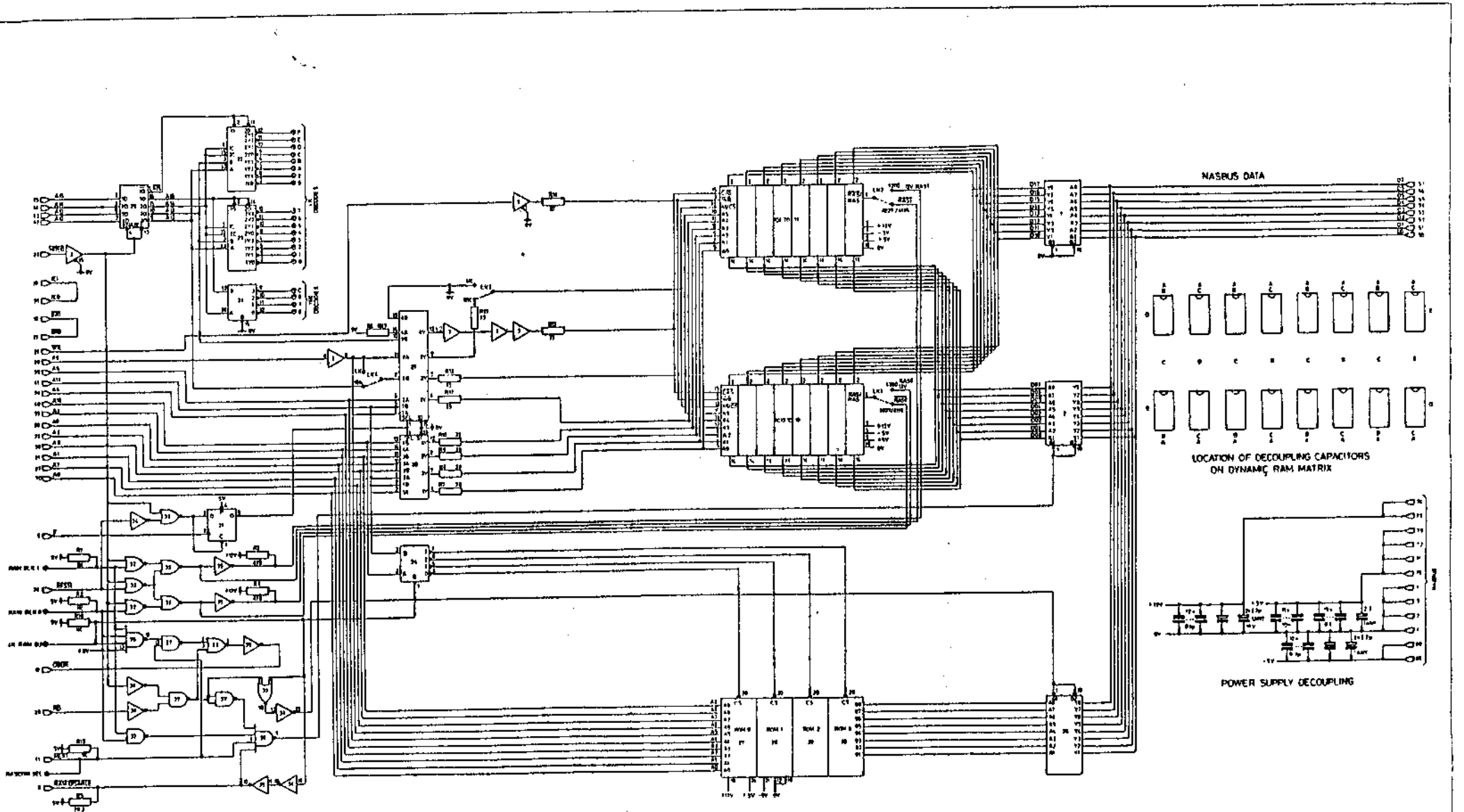
4.3 Row Address Strobe options

For 'normal'	RAS (4027/4116)	ICs 4-11	Link P12-13
For 'normal'	RAS (4027/4116)	ICs 12-19	Link P 9-P8
For + 12V	RAS	ICs 4-11	Link P12-P11
For +12V	RAS	ICs 12-19	Link P 9-P10

5. MODIFICATIONS AND DECODING FOR NASCOM 1

Assuming the correct modifications have already been made to Nascom 1 for addition of the Buffer card (see Ref.6) the only further change is to LK5. This must be changed from Internal to External (see Ref.7 page 28).

The memory on the Nascom 1 occupies the 4k memory block from 0000 to OFFF Hex. In an extended system the start address of this memory area is fixed by linking $\overline{\text{Nascom MEM}}$ select, P4 to 4k decode pad 5.



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RAM/BOARD