

The Gemini MultiBoard Microsystem

'SVC'

80-BUS

SUPER VIDEO-CONTROLLER
BOARD

HARDWARE MANUAL

GM331
ISSUE 2
15-02-85

THE COPYING OF THIS DOCUMENT IS
FORBIDDEN FOR ANY REASON WHATSOEVER
WITHOUT WRITTEN CONSENT FROM GEMINI
MICROCOMPUTERS LTD. 1985

© COPYRIGHT GEMINI MICROCOMPUTERS LTD. 1985



18 Woodside Road Amersham Bucks HP7 0BH England.

TABLE OF CONTENTS

1. Introduction.....	1
1.1. This Manual.....	1
1.2. The SVC.....	1
1.3. Guarantee.....	1
2. Commissioning.....	2
3. Connectors.....	2
3.1. PL1 - 80-BUS.....	2
3.2. PL2 - Video Out.....	2
3.3. PL3 - Light Pen Socket.....	3
3.4. PL4 - Serial Keyboard Input.....	4
3.5. PL5 - Expansion Connector.....	4
3.6. PL6 - Parallel Keyboard Input.....	5
4. On-board Switches.....	5
5. On-board Links.....	6
5.1. /NASIO.....	6
5.2. Clock Select.....	6
6. SVC-Host Interface.....	6
Appendix	
A. Serial Keyboard Specification.....	8

3.2. PL2 - Video Out

This socket is provided for connection of a video monitor to the GM832 board. PL2 is a 5 pin "domino" DIN socket, providing the video output signal from the GM832. Looking at the edge of the board with the component side up, and with PL2 on the left, the pin numbering is:

5 4
1 3

These are connected as follows:

- Pin 1 Vertical Synch. output of CRTIC IC (unbuffered)
- Pin 2 Ground
- Pin 3 Ground
- Pin 4 Video out (Composite video, 1V peak-to-peak)
- Pin 5 Horizontal Synch. output of CRTIC IC (unbuffered)

Normally connection will only be required to the composite video out (pin 4) and Ground (pins 2 and/or 3). However, occasionally certain monitors may require the separate synchronisation pulses to be supplied, and hence these are supplied on pins 1 and 5 of PL2.

The composite video out signal is also available from the two pins adjacent to PL2:

- Pin 4 Video out (composite video, 1V peak-to-peak)
- Pin 5 Ground

There is a link option on the board to allow a modification to be made, if required, to the video output stage of the GM832. A 100uF coupling capacitor may be inserted into the composite video output. This is done by cutting the trace "C3" on the component side of the board alongside the PL2 connector, and soldering in a capacitor.

3.3. PL3 - Light Pen Socket

PL3 is a 5 pin 180° DIN socket, providing a light pen input facility to the GM832. Looking at the edge of the board with the component side up, and with PL2 on the left, the pin numbering of PL3 is:

3 1
5 4
2

These are connected as follows:

- Pin 1 +12 volt output
- Pin 2 Ground
- Pin 3 Light pen switch input
- Pin 4 +5 volt output
- Pin 5 Light pen strobe (to CRTIC IC)

3.4. PL4 - Serial Keyboard Input

The Gemini GM852S series of serial connection keyboards may be used with the GM832 board. PL4 is a 6 pin 240° DIN socket, providing the GM832 with a serial keyboard input. Looking at the edge of the board with the component side up, and with PL4 on the right, the pin numbering is:

5 1
6 2
4 3

These are connected as follows:

- Pin 1 +12 volt output
- Pin 2 Clock input (TTL)
- Pin 3 Ground
- Pin 4 Serial data input (TTL)
- Pin 5 +12 volt output
- Pin 6 Ground

Note:

1) This serial keyboard input is designed specifically for the Gemini range of serial keyboards, and conventional RS232 serial keyboards may NOT be connected to this socket. See Appendix A for further details.

2) When a serial keyboard is in use then two links on the GM832 must be set accordingly. These are LKA (found between IC6 and IC16) and LKB (found between IC21 and IC26). For serial keyboard operation these links must both be inserted.

3.5. PL5 - Expansion Connector

PL5 is a 26 way ID connector, found between IC27 and IC39, to allow for I/O expansion of the GM832. The connections present are:

+5V	1	2	/RD
/INT	3	4	D1
/IORQ	5	6	D0
RESET	7	8	D7
GND	9	10	D2
3MHz CLK	11	12	/WR
D5	13	14	A0
D6	15	16	A1
D3	17	18	A2
D4	19	20	N.C.
N.C.	21	22	N.C.
+12V	23	24	N.C.
-12V	25	26	A7

This connector has been placed on GM832 to allow for the addition of an RS232 serial board using an 8250 type UART, occupying 8 I/O ports. As the GM832 is NOT decoded fully internally, A7 is used to select the I/O expansion, and so the 8 ports will repeat from 80H-87H to F7H-FFH. The 3MHz clock is provided for division by the 8250 to generate programmable baud rates.

Two mounting holes are provided on the GM832 for the attachment of an I/O expansion board in a 'piggy-back' fashion. One hole is between IC21 and IC26, and the other hole is between IC17 and IC18.

If required other boards may be added to the GM832 using the PL5 connector. Note that the Z80 on the GM832 will normally be running at 6MHz and thus any expansion board must be capable of running at this speed.

N.B. In the current release of the SVC Monitor program (Vers. 4.01) there is NO software support for any expansion board, and consequently the addition of a board would entail either modification to the monitor program, or a down-loaded user program (see the SVC software manual).

3.6. PL6 - Parallel Keyboard Input

PL6 is a 16 pin ID connector, providing the GM832 with a parallel keyboard input. The Gemini GM821 59 key keyboard, GM827 87 keyboard, and GM852P series of low profile parallel keyboards may be attached directly to this connector. Looking at the board with the component side up, and with PL6 on the right, pin 1 of the connector is on the right.

N.B. Take great care when connecting a parallel keyboard to ensure that you are connecting the keyboard cable the correct way round, or damage WILL occur to both the keyboard and the GM832.

The connections on PL6 are as follows:

+5V	1	2	/STROBE
GND	3	4	GND
D5	5	6	D4
D6	7	8	GND
GND	9	10	D2
D3	11	12	D0
D1	13	14	+5V via 220R resistor
-12V	15	16	D7

Note: When a parallel keyboard is in use then two links must be set accordingly. These are LKA (found between IC6 and IC16) and LKB (found between IC21 and IC26). For Parallel keyboard operation these links must both be removed.

4. On-board Switches

There are four switches on the GM832, S1-4. The state of these is read by the SVC monitor program, and they are used to specify certain default power-up conditions. The exact use of the switches will therefore depend upon the SVC monitor program in use, and so reference should be made to the SVC software manual.

With SVC monitor Vers. 4.01 the switches are used as follows:

S1 - determines whether the keyboard in use outputs only single-byte codes, e.g. GM821, or double-byte codes, e.g. GM827 or GM852.

S2, S3 and S4 - Select optional foreign language character sets. Note these may also be selected in software.

5. On-Board Links

There are five on-board links which may be modified by the user. Three of these have already been covered above:

C3 - To be cut if a coupling capacitor is to be added in the video out signal.
LKA - Inserted for serial keyboard, omitted for parallel keyboard.
LKB - " " " " " "

5.1. /NASIO

The fourth link determines whether or not the GM832 generates a /NASIO signal onto the bus. The link is positioned close to one of the on-board crystals, XTAL 2. If the link is made a /NASIO signal will be generated. The /NASIO signal is ONLY required for systems based on the Nascom 1 or Nascom 2 boards. Only one board in a system needs to generate /NASIO. If the GM832 is to be used with a Nascom then the IOEXT link (Nascom 1) or switch (Nascom 2) should be set to 'External'. With Nascom 1 there is a decode fault that necessitates the removal of the Z80 PIO when external I/O is used.

NOTE: The GM832 does not normally produce the Nasbus DBDR signal that is required by Nascom 1. If it is required to use GM832 in a system based on a Nascom 1 then there are two ways of doing this:

- 1) Add an open collector buffer onto the GM832 between the pin 3 output of IC33 and bus line 13. (Through-plated holes are provided for connection.)
- 2) Implement additional circuitry on the Nascom to establish the required databus direction, and switch DBDR accordingly. The advantage of this approach is that other 80-BUS boards that do not provide DBDR may be used in the Nascom system without modification.

5.2. Clock Select

The final link on the GM832 is used to select the clock speed for the on-board Z80 processor, and it is located between IC36 and IC41. This link may be set to provide a clock of either 3MHz or 6MHz. The GM832 is normally supplied fitted with a 6MHz Z80B, and the link is set accordingly. If, however, a slower Z80 processor is to be fitted for any reason, then it is necessary to cut the link on the reverse side of the board joining the pins marked '6M', and fit a link to join the pins marked '3M'.

6. SVC-Host Interface

The GM832 occupies three I/O ports belonging to the host system. The first port is for the transfer of data between the host and the GM832. The second port is for the handshake signals between the host and the GM832. The third port is to enable the host system to reset the GM832, as the bus reset line is not connected to the GM832. As multiple GM832 boards may be used in a single system, this allows them to be reset independently.

The bottom eight address lines of the 80-BUS (A0-A7) are connected to the eight address inputs of the port decode PROM (IC44). /IORQ and M1 are connected to the /CE inputs of the PROM to ensure that it only decodes valid I/O port addresses. The four data outputs from the PROM are pulled up by 4K7 resistors to ensure that the outputs remain high when the PROM is not enabled. The data outputs from the PROM are assigned as detailed below.

Data output Function

	Function
D0	/NASIO
D1	Data transfer
D2	Handshaking
D3	Reset

The PROM is coded in the following manner:

- Select the ports to which you wish the above functions to be assigned. It would be usual to assign the lowest eight ports to decode a Nascom 1 or 2 via /NASIO.
- The 256 locations in the PROM are directly mapped to the 256 I/O ports available. One merely has to load the particular location in the PROM with the contents which will take the appropriate data output low and enable the specific circuitry.
- D0 will go low if the location contains an E, D1 will go low if the location contains a D, D2 will go low if the location contains a B and D3 will go low if the location contains a 7.

The following table gives the contents for the standard GM832 PROM (VID-1):

PROM location	Contents	Function
00-07	E	/NASIO
08-80	F	No function
B1	D	Data port
B2	B	Handshake
B3	7	Reset

The PROM used is a 256 x 4 open collector type. The part is available from numerous sources, programming however is unique to each part. For a custom PROM please contact your Gemini dealer.

Below is a list of suitable parts:

Manufacturer	Part Number
AMD	27S20C
Fairchild	93A17DC
Fujitsu	MB7052
Harris	7610-5
Intel	3621
Intersil	5603AC
MMI	6300-1
Nat. Semi.	74S387
NEC	uPB403D
Signetics	N82S126 - recommended part.
Texas Inst.	TBP24SA10

A. Serial Keyboard Specification

The Serial Keyboard Input of the GM832 is designed to be used with Gemini GM852S range of keyboards. The following data is provided for those wishing to connect alternative keyboards to the GM832 via this input.

The keyboard should produce a serial data stream together with a clock in place of the usual parallel data and strobe. These should both be TTL level signals.

The characteristics of the data stream are as follows:-

- the active edge of the clock is the rising (or +ve) edge
- the data should be stable about this edge
- for each byte transferred to the SVC the keyboard should generate nine active clock edges. The data line should be set to a binary one (high) for the first clock pulse, and for the remaining eight it should be set to the successive bits of the data byte, starting with the most significant bit. NB: the data is not inverted

Clock Rate

The data setup and hold times are in the range 5-20ns, but the actual figures used in practice will be governed by the characteristics of the cable used to interconnect the keyboard and the SVC, and the line drivers and receivers. The required transfer rate is not high, and ample settling time can be allowed for on the data line. Care should be taken that no ringing exists on the clock line which might result in false clocking of data into the shift register. It might be advisable to limit the rise time of the clock driver. To avoid problems with noise pick-up, etc, the data line should be kept at a logic 0 level except while clocking the data in.

Power Up

On power-up the keyboard should set the data line to 0, and provide at least 9 clock pulses on the clock line.