The Gemini MultiBoard Microsystem

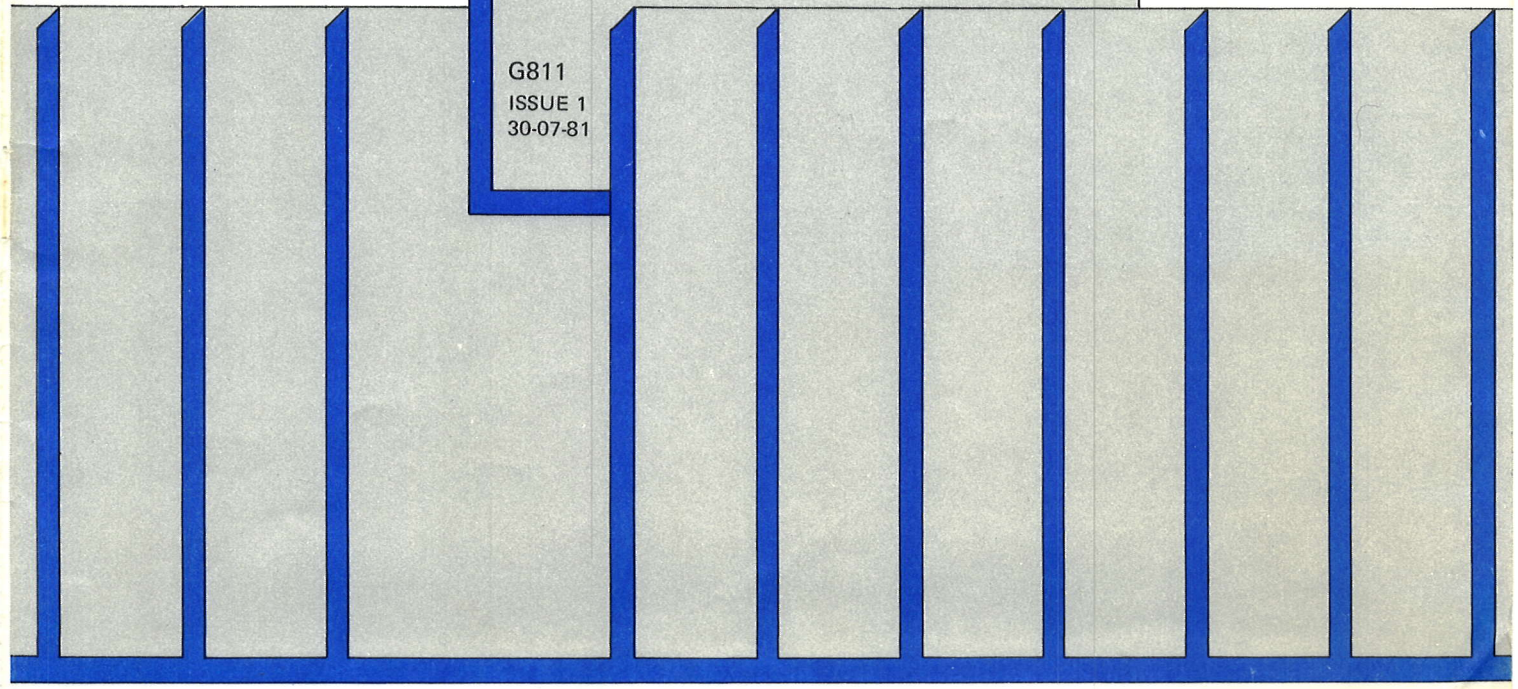
Z80 CPU

80-BUS

Z80A PROCESSOR CARD

INSTRUCTION MANUAL
AND
FUNCTIONAL SPECIFICATION

G811
ISSUE 1
30-07-81



Introduction

G811 is a Z80 CPU card for use on GEMINI Multiboard systems. A great deal of flexibility has been built into the card to allow it to be used in a wide variety of configurations. It is possible to use the card by itself as, for example, a controller, or in combination with other 80-BUS compatible cards as a very powerful software development system including disk storage, video output and EPROM programming capability.

The CPU section of the card uses a Z80A processor, the Z80 being fully buffered to the 80-BUS specification and able to run at either 2 or 4 MHz. Power-on reset initialises the card at switch on, and a `reset jump' facility allows the controlling program to reside on any 4K address boundary.

Four `bytewide' sockets are provided for onboard memory, allowing a large variety of memory ICs to be accommodated. Wait states may be permanently enabled or disabled, or set to operate only when the memory on the CPU card itself is accessed. This allows different speeds of memory ICs to be used. Additionally the on-board memory block may be disabled from the Z80 address map under software control.

The input/output section of the card consists of an ASCII keyboard port, a dual parallel interface in the form of a Z80A PIO, and a serial interface which includes programmable baud rates, full modem support signals, inputs and outputs at RS232 levels, and a 1200 baud Kansas city/CUTS tape interface. Switching between RS232 and cassette interfaces may be done under software control.

This manual is in three sections, a user section instructing the user in commissioning G811, a functional description section detailing the design, and a copy of the 80-BUS specification.

Contents

1 Introduction / Commissioning
2 Functional description
3 Gemini 80-BUS description

Commissioning

Carefully unpack your G811 and examine it for any mechanical damage. In the event of any damage please inform your dealer immediately.

Your G811 will have been shipped to you fully tested and working, all that may be required is for the board to be plugged into the bus. However please take the time to read through this manual as it should prove useful.

When plugging G811 into the bus please take great care, excessive force should not be required, any difficulty that is encounted will (in all probability) be due to the keyway of the edge connector not slotting accurately into the slot in the edge of the card. Ensure that the card is plugged in with the edge connector going in first and the correct way around, it is not possible to plug the board in the incorrect way around because of the keyway. Power is connected to the card through the bus - refer to the 80-BUS description for further details.

80-BUS & Multiboard are trademarks of Gemini Microcomputers Limited.

Input/Output Connections

There are five I/O connectors on the board edge - Keyboard, PIO, Serial, Aux. and Tape. The connections are detailed below.

Keyboard Connector

The keyboard port is for a standard 7 bit ASCII keyboard with a positive strobe. A suitable keyboard is the Gemini G613 keyboard, and the socket on G811 (marked 'KBD') is configured specifically for this keyboard. The Gemini keyboard is simply connected to G811 via a 16 way cable fitted with IDS connectors, and this cable is supplied with the keyboard. When connecting the keyboard care should be taken to ensure that the marking on the cable connector (indicating pin 1) coincides with the pin 1 identification on G811 next to the keyboard socket. Failure to connect the cable the correct way round may result in damage to the keyboard.

Other keyboards may be utilised, in which a special cable will have to be made up. Details of the connector are given below.

+5 volts	1	2	Strobe
Ground	3	4	Ground
D5	5	6	D4
D6	7	8	Ground
Ground	9	10	D2
D3	11	12	D0
D1	13	14	Power Led drive
-12 volts	15	16	Halt Led drive

PIO Connector

The PIO (Parallel Input/Output Controller) has two eight bit data ports, one known as A and one as B, so they are numbered A0 to A7 and B0 to B7, A0 and B0 represent the least significant bits, A7 and B7 represent the most significant bits. In addition each port has two handshake lines, one for input and one for output. Below are the details of the connector on G811 (marked 'PIO'). +5 volts and ground are also provided on the connector to drive a small amount of external circuitry. However, users should beware of drawing excessive currents. Further details of the operation of the PIO are given in the G811 functional description. Full details can be found by obtaining an MK3881 PIO manual.

B5	1	2	B4
B6	3	4	B3
B7	5	6	B2
/ARDY	7	8	B1
/BSTB	9	10	B0
/ASTB	11	12	/BRDY
A0	13	14	Ground
A1	15	16	Ground
A2	17	18	Ground
A3	19	20	+5 volts
A4	21	22	+5 volts
A5	23	24	A7
A6	25	26	Ground

Serial Connector

The Serial connector (marked 'Serial') is used for connecting RS232 type printers, terminals or modems to G811. It is quite involved and so it will be explained pin by pin. Selection between RS232 and cassette interfaces is controlled by the /OUT 1 output of the 8250 UART. This means that the selection is under software control. See the 8250 section of the functional description, and the software manual for further details.

Pin 1, RLSD (Received Line Signal Detector). An input to G811, this would normally come from a modem or similar piece of equipment. When positive it indicates that the modem etc, is receiving a signal. This signal is also known as Data Carrier Detect. On a DB25 type connector this would be pin number 8. The signal is at RS 232 levels.

Pin 2, +5 volt output for driving external circuitry. Maximum allowable current is 250mA.

Pin 3, SIN (Serial INput). Marking (high) when negative and spacing (low) when positive, this is the RS 232 data input to G811. This signal is also known as RxD. The DB25 pin number is 2 if G811 is to be the host, or 3 if G811 is to be a peripheral. RS 232 levels.

Pin 4, /BAUDOUT. This signal, from the WD8250 UART, is a clock signal of 16x the 8250 receive clock. It is at TTL levels, is not symmetrical, and has not been buffered. Also detailed in the description of LKB1.

Pin 5, RCLK. This is connected to the receive clock input pin of the 8250 and should be 16x the receive clock. It is normally connected to /BAUDOUT, but is available to allow an external clock input. This signal should be at TTL levels - do not drive with RS 232 levels. Also detailed in the description of LKB1.

Pin 6, SOUT (Serial OUT). This is the RS232 data out from G811, also known as TxD (Transmitted Data). DB25 pin number is 2 if G811 is a peripheral or pin 3 if G811 is the host. This is an RS232 level output, and must not be connected directly to TTL.

Pin 7, -12 volts output for powering external circuitry. Maximum load 100mA.

Pin 8, CTS (Clear To Send). An input to G811, this would originate at a modem or similar device and indicates that the modem etc is ready to transmit data on behalf of G811. Positive when clear to send, negative when not clear. RS 232 levels. DB25 pin 5.

Pin 9, DSR (Data Set Ready). An input to G811, this would come back from a modem after it has attempted to establish a communications channel. It does not however indicate the existance of a communications channel. Positive to indicate the attempt has been completed. RS 232 levels. DB25 pin 6.

Pin 10, RTS (Request To Send). An output from G811 which, when positive, tells the modem to transmit. If the link is half-duplex the receive will be supressed. When the RTS line goes low to high the modem will respond by taking the CTS line high and data may then be transmitted. When RTS goes low it must remain low until the modem has taken CTS low in response. RTS is DB25 pin 4.

Pin 11, Ground. This is the system ground and is not to be connected to safety ground. DB25 pin 7. (Not DB25 pin 1, which is safety ground.)

Pin 12, DTR (Data Terminal Ready). An input to G811, this has to be positive to maintain the communications channel. When taken negative the modem will complete the current transmission, and then close down the channel. RS 232 levels. DB25 pin 20.

Pin 13, +12 volts for powering external circuitry. Maximum load 100mA.

Pins 14 & 15, Ground. Please see comments re. pin 11.

Pin 16, +5 volts for powering external circuitry. Maximum load 250mA.

In different manufacturers equipment the RS232 standard has been implemented in a variety different ways. The instruction manual for the other equipment should be carefuly read. As the protocol has to be implemented on G811 in software, it can easily be changed to suit individual requirements.

The RS232 outputs swing from -12 volts to +12 volts. The inputs will accept the same voltage swings, but they can also work with TTL levels. However, it must be pointed out that in this case the noise rejection will be impared. The threshold charactistics of the RS232 receivers can be modified by varying the values of the resistors R11 to R14 on G811. The standard value is no resistor. (For further details see the 75189A (Texas) data sheet.)

The connector details of G811s Serial connector are given below:

	RLSD	1	2 +5 volts
	SIN	3	4 /BAUDOUT
	RCLK	5	6 SOUT
-12 volts		7	8 CTS
	DSR	9	10 RTS
	Ground	11	12 DTR
+12 volts		13	14 Ground
	Ground	15	16 +5 volts

Aux. pins

Two pins are provided (adjacent to the 5 pin DIN socket and marked 'AUX') for switching an external device. The pin furthest from the DIN socket is connected to +5 volts, the pin closest to the DIN socket is connected to the collector of an NPN transistor, TR1. TR1 is switched "on" whenever the /OUT 1 of the 8250 goes high, /OUT 1 is also used to switch the 8250 input between the RS232 interface and the tape interface circuitry. The transistor could therefore be used to switch a tape recorder on or off. Precise details are not provided as the external circuitry will vary from tape recorder to tape recorder. Please, however, ensure that any relay used has an anti-backlash diode and does not sink more than 250mA into the transistor.

Five pin DIN socket

The DIN socket is provided for the tape interface and has two sets of links associated with it. Selection between RS232 and tape interfaces is controlled by the /OUT 1 output of the 8250 UART. This means that the selection is under software control. See the 8250 section of the functional description, and the software manual for further details. Details of the links are given below.

LK5 is to set the output level of the tape interface. By connecting the centre pin to the pin nearest the centre of the card the output will be about 100mV; by connecting the centre pin to the pin nearest the edge of the card the output level will be decreased to about 10mV. The correct pin can be selected by experimentation. G811 is supplied with the output level set to 10mV. Data should be recorded at about 0VU.

LK7 selects the input channel. If a mono recorder is in use this will not matter, however if a stereo recorder is used it is extremly important that the two channels are not mixed when the tape is played back. The data can, however, be recorded on both channels. This is because of the phase variances between the channels, which will result (if the two are mixed) in a "lumpy" frequency response. The right hand channel is recorded nearest the centre of the tape, so it is recommended that the centre pin of LK7 is linked to the pin nearest the centre of the card if a stereo recorder is used. Many mono machines however, only output on pin 3 of their DIN connectors. If this is the case then the centre pin should be connected to the pin nearest the outside of the card. As supplied G811 has all three pins connected together.

The output levels of tape recorders will vary over a very wide range. If G811 is found to be insensitive R9 (47k) can be decreased. Any value of resistor (within reason) may be used.

```
Ground   2
Output   4    5   Input
Output   1    3   Input
View from back of plug.
```

VR1

The potentiometer on the edge of G811, VR1, is to adjust the centre frequency of the data recovery circuit. This has been set electronically at manufacture and should not be altered.

Reset Switch and HALT LED

Also provided on the edge of the G811 card is a small push button, marked 'Reset'. Depressing this causes a reset pulse to be applied to the Z80 CPU, PIO, 8250 UART and line 14 of the bus (/RESET). A reset pulse is also generated when power is first applied to the card, and can also be generated by connecting a switch between line 10 of the bus (RESET SWITCH) and Ground. The result of a Reset will be to reinitialise the system.

Alongside the Reset Switch is a red LED that monitors the state of the Z80 HALT output. Refer to the Z80 manual for further details.

Link Options
============

There are a wide variety of link options on G811. The appropriate links for most applications have been made during manufacture, however full details are provided below. All links should be made by soldering wire from one connection on a header plug to the other, but please take great care as an incorrect link may do damage and a poor connection will result in an unreliable system. Care must also be taken when links "crossover" on the linkblocks to ensure that shorts do not occur.

LKB1

Reset Jump Option

The reset jump circuit is programmed by making links from pins 11-14 to ground (pins 5 and/or 6) and it is possible to program one of sixteen addresss from 0000H to F000H. The four bit binary number represented by the links is used to program the four most significant bits of the address to which the CPU will jump to following a reset or switch on. Pin 14 is the most significant bit (8), pin 13, 4, pin 12, 2 and pin 11, 1. If all the pins are left unconnected the CPU will jump to F000H on reset, if all the pins are grounded by connection to pins 5 and/or 6 the CPU will reset to 0000H. It should be noted that with the exception of 0000H the first instruction at the reset address should be an absoulute and unconditional jump, ie C3 03 F0 could be used if a reset jump to F000H was programmed. Reset jump on G811 is normally to F000H.

Reset Jump Link Table

Address of jump	Pins 14	13	12	11
F000	X	X	X	X
E000	X	X	X	L
D000	X	X	L	X
C000	X	X	L	L
B000	X	L	X	X
A000	X	L	X	L
9000	X	L	L	X
8000	X	L	L	L
7000	L	X	X	X
6000	L	X	X	L
5000	L	X	L	X
4000	L	X	L	L
3000	L	L	X	X
2000	L	L	X	L
1000	L	L	L	X
0000	L	L	L	L

L = Link the pin in question to ground
X = No link required

RAM Disable

A line on the bus (line 9) has been allocated the name of /RAMDIS and its function is to prioritise memory (for further details see the 80-BUS specification). This line is connected to pin 8 on LKB1. If pin 8 is connected to pin 9 then the assertion of a /RAMDIS signal by another card will disable any memory (EPROM/ROM or RAM) on G811 at the same address. If pin 8 is connected to pin 10 then the accessing of memory on G811 will generate a /RAMDIS signal. The latter is the normal configuration.

System Configuration Option

Pin 7 on LKB1 is connected to the /RI (ring indicator) input of the 8250, the logic state of which can be read by the CPU via the 8250. If this pin is left unconnected the CPU will read a low, if linked to ground (pin 6) the CPU will read a high. This pin can be used by the system software to determine a power-on option of the card. Where implemented the appropriate position will be given in the software manual.

Keyboard Interrupts

The state of the strobe line of the keyboard on G811 is normally monitored by software. However the strobe line is also brought to pin 16 on LKB1 and could be connected to pin 1. This pin goes to port A (D0) of the PIO so that the keyboard can generate a vectored interrupt via the PIO. The appropriate software for this would have to be incorporated in the system monitor.

UART Interrupts.

The WD8250 UART has an interrupt output that indicates when certain operations have been completed. This line is brought to pin 15 on LKB1 and could be connected to pin 2. This pin is connected to port A (D1) of the PIO so that the 8250 can generate vectored interrupts via the PIO. The appropriate software for this would have to be incorporated in the system monitor.

UART Receive Clock

The 16x receive clock used in the 8250 is brought out of the device, and in most cases is fed straight back in. However, in some applications it is useful to have the receive clock connected to an external source. Pin 3 on LKB1 is connected to the RCLK input of the 8250 and pin 4 is connected to the /BAUDOUT of the 8250. Normally pins 3 and 4 would be linked. For further details see the section on the serial connector.

A summary of the functions of LKB1 is shown below:

PIO port A D0	1	16	KBD strobe
PIO port A D1	2	15	8250 interupt
8250 RCLK	3	14	8) Reset
8250 /BAUDOUT	4	13	4) jump
GND	5	12	2) address
GND	6	11	1)
8250 /RI	7	10	/RAMDIS out
80-BUS line 9	8	9	/RAMDIS in

LKB3

Clock Options

There are a variety of clock options available on G811, by the appropriate linking on LKB3. The 'Master Clock' is determined by the crystal (XTAL1, normally 16MHz) and various divisions of this frequency are present at LKB3 - /2 (8MHz) at pin 5, /4 (4MHz) at pin 6 and /8 (2MHz) at pin 7.

The CPU clock, pin 9 of LKB3, is normally 4MHz and should therefore be connected to pin 6.

The WD8250 UART requires a clock input of 2MHz at pin 8 of LKB3, and this should therefore be connected to pin 7.

The 80-BUS clock line should be driven by G811, and this is enabled by connecting the clock driver (at pin 2) to the bus line (at pin 3). In certain situations the 80-BUS clock line may be driven by another card. In this case the clock drive link (2-3) would be removed, and the CPU clock input (9) connected to the bus clock (4).

Finally, a 4MHz clock signal must be provided on the bus if the bus master (G811) is not running at 4 MHz. If the bus master is running at 4 MHz there is no need to connect this pin. If the bus master is running at a different frequency then the 80-BUS AUX CLK line (at pin 10 on LKB3) should be connected to a 4 MHz clock. For further details refer to the 80-BUS specification.

Wait States

With certain memory devices it is necessary to provide wait states to the Z80 during memory accesses. The wait states are enabled by linking pin 11 to pin 12 on LKB3. The wait states can be selected to be on for all memory accesses, or only those to memory on G811 itself. Link pin 1 to pin 14 if onboard memory only to have wait states, link to pin 13 if a wait state on all memory cycles is required.

A summary of the functions of LKB3 is given below:

Z80 wait generator	1	14	G811 /MEM EN
Bus clock drive	2	13	Ground
Bus clock	3	12	Wait enable
Bus clock	4	11	Z80 wait input
X 0.5	5	10	AUX CLK
X 0.25	6	9	CPU CLK
X 0.125	7	8	8250 clock

Memory selection

The memory sockets on G811 will take a range of memory chips, as a consequence it is necessary to "program" the type of chip by making the appropriate links on link blocks LKB2 and LKB4.

The individual pins will be described, and a set of link tables given for the more popular devices.

Socket Selection

If any of the memory sockets are to be used, it is necessary to enable them into the Z80 memory map by providing a chip select signal. Each socket can be enabled separately, and should only be enabled as required. The /OUT 2 output of the 8250 UART controls whether or not the on-board memory is selected into the Z80 memory map. It is therefore possible, for example when running a disk system, to disable the on-board memory under software control, and run a 64K RAM system. See the 8250 section of the functional description.

To enable:	Make link:
Socket I (IC23)	LKB2 Pin 1 to 20
Socket II (IC28)	LKB2 Pin 10 to 11
Socket III (IC32)	LKB4 Pin 1 to 20
Socket IV (IC37)	LKB4 Pin 10 to 11

Memory device selection

In the `bytewide' concept many different types of chip can be used in the same socket provided it is possible to make a variety of different signal connections to pins 21, 23, and 26 of the memory sockets. Having selected the socket, as detailed above, it is then necessary to set further links to provide the required signals to pins 21, 23, and 26 of the `bytewide' memory sockets. A chart of the pin requirements of some common memory chips is given below:

Part number	Pin 21	Pin 23	Pin 26
4118	+5V	/WE	+5V
4801	+5V	/WE	+5V
2758	GND	+5V	+5V
2759	+5V	+5V	+5V
2016	A10	/WE	+5V
6116	A10	/WE	+5V
4016	A10	/WE	+5V
4802	A10	/WE	+5V
4816	A10	N.C.	+5V
2716	A10	+5V	+5V
2032	A10	A11	N.C.
2732	A10	A11	+5V
4864	A10	A11	+5V
2764	A10	A11	+5V
27128	A10	A11	A13

The following memory chips cannot be accomodated; 2708, 2532, 2564.

ROMs have not been listed as their chip selects may vary, however a ROM marked 23xx will generally work in a socket linked for a 27xx.

When plugging in 24 pin memory chips they must be "justified" towards pins 14 and 15, ie when correctly plugged in pin 1 of the chip will go into pin 3 of the socket.

Details of the connections on the link blocks may be determined from the following tables:

	Pin 21	Pin 23	Pin 26
Socket I	LKB2/13	LKB2/14	LKB2/12
Socket II	" " 3	" " 4	" " 2
Socket III	LKB4/13	LKB4/14	LKB4/12
Socket IV	" " 3	" " 4	" " 2

	GND	+5V	/WE	A10	A11	A13
LKB2 & 4	8 or 18	6 or 16	5	7 or 17	15	9

Summaries of LKB2 and LKB4 are given below:

LKB2

Decode PROM o/p D0	1	20	/CS for Socket I (IC 23)
Socket II (IC 28) pin 26	2	19	A13
Socket II (IC 28) pin 21	3	18	Ground
Socket II (IC 28) pin 23	4	17	A10
/WE	5	16	+5 volts
+5 volts	6	15	A11
A10	7	14	Socket I (IC 23) pin 23
Ground	8	13	Socket I (IC 23) pin 21
A13	9	12	Socket I (IC 23) pin 26
/CS for Socket II (IC28)	10	11	Decode PROM o/p D1

LKB 4

	Decode PROM o/p D2	1	20	/CS for Socket III (IC 32)
Socket	IV (IC 37), pin 26	2	19	A13
Socket	IV (IC 37), pin 21	3	18	Ground
Socket	IV (IC 37), pin 23	4	17	A10
	/WE	5	16	+5 volts
	+5 volts	6	15	A11
	A10	7	14	Socket III (IC 32) pin 23
	Ground	8	13	Socket III (IC 32) pin 21
	A13	9	12	Socket III (IC 32) pin 26
	Decode PROM o/p D3	10	11	/CS for Socket IV (IC 37)

G811 Functional description

Section 1 - Processor Circuitry
1.1 Clock
1.2 Reset
1.3 Reset jump
1.4 Wait state generator
1.5 NMI pulse shaper
1.6 Bus signals and control

Section 2 - Memory Circuitry
2.1 Memory enabling and decode
2.2 Memory data bus control
2.3 The Bytewide concept

Section 3 - Input/Output Circuitry
3.1 I/O decode
3.2 PIO
3.3 8250 UART
3.4 RS232 interface
3.5 Tape interface
3.6 Keyboard interface
3.7 I/O data bus control

Section 4 - PROM Types
4.1 PROM part numbers

Section 1 - Processor Circuitry

1.1 Clock

The master clock is a crystal oscillator formed by two 74S04 inverters (IC's 36b/c), the inverters being biased into a linear region of operation by the two 820R resistors Rs 44 & 45. A crystal is connected across the two inverters to provide feedback and hence oscillation at the desired frequency. The oscillator will oscillate at the series resonant frequency of the crystal. The 47nF capacitor (C40) is used to couple the two inverters together, the 10pF capacitor (C41) being an anti-jitter capacitor. The output of the oscillator can be monitored at TP7. The output of the oscillator is divided by three 74LS74 flip-flops (IC 31a/b and IC 27a) in succession to yield the oscillator frequency divided by 2, 4, & 8, all three clocks being available at LKB3. LKB3 is provided with clocks from four sources, three from the division chain and one from the bus. It also has provision for outputting to the CPU, 8250 UART, and to the bus. There is provision for two clocks on the bus, one being the system clock (CLOCK) which must be the same clock as that used to drive the CPU, and the other an auxilliary clock (AUX CLK) for use by expansion cards when the CPU is not running at 4MHz. Many permutations are possible. However in the standard 4MHz system the master oscillator would run at 16MHz, the CPU at 4MHz, the 8250 at 2MHz, and the bus clock would come from the G811. If the G811 was run at 6MHz the master oscillator would run at 16MHz as before and the results would feed both the 8250 (at 2MHz) and the AUX CLK line on the bus (at 4MHz). The 6MHz for the CPU would come from the system clock line on the bus. The CPU clock is also connected to the wait state generator and the PIO. For both the CPU and PIO the clock has to swing from 0 volts to 5 volts, this swing being provided by a push-pull transistor arrangement (TR2 and TR3) driven by an 74S04 (IC 36e).

1.2 Reset

Reset can come from one of two sources. On power up a 47uF capacitor (C15) will be charged up via a 22k resistor (R20). While the input of the 74LS14 (IC 9a) which is connected to the junction of the resistor and capacitor is less than approximately 2 volts, the output will remain high and this will ensure that the output of the 74LS32 (IC10a) is high. As a consequence, Bus line 14 and the reset input of the Z80 will be low. Once the 47uF capacitor (C15) has charged past the threshold of the LS14, bus line 14 and the reset input to the Z80 will go high.

The second source of a reset is either a high to low on line 10 of the bus or the closing of switch SW1. When a reset occurs during operation two criterions must be met.

a) The reset pulse must not be so long as to prevent dynamic RAM from being correctly refreshed.
b) The reset pulse must not occur during T3 of an /M1 cycle. If the reset pulse was to occur during T3 of an /M1 cycle, /MREQ will go indeterminate for one T state some 10 T states later. This could damage the contents of dynamic RAM.

The reset switch is connected between bus line 10 and ground. Bus line 10 goes via a 470 ohm resistor (R 22) (which limits the current) to the input of a 74LS14 (IC 9c), the input having a 22k pullup resistor (R21) and a 47uF capacitor (C16) to ground to act as a debounce circuit. Users are however cautioned that this may not be sufficient in all cases and that in extreme cases two or more resets may occur. While the reset switch is open the input to the 74LS14 (IC 9c) is high and the output low. The low on the output of the LS14 causes the Q output of the 74LS74 (IC 27 b) to go low, the low remaining until the output of the LS14 goes high (as a result of the switch being closed) and the LS74 is clocked by M1 going low to high which in turn is caused by /M1 going high to low. When the Q output of the 74LS74 (IC 27b) goes high the 74LS221 (IC 16a) will be triggered and will produce a short pulse (going low) of about 50uS duration on its Q output. This is connected to the 74LS32 (IC 10a) and on via the 74LS14 inverter (IC 9a) and the open collector 7407 (IC 15a) buffer to bus line 14 and the reset input of the CPU. It should also be noted that the reset is triggered on the high to low transition of line 10. If line 10 or the reset switch is held low multiple resets will not occur.

1.3 Reset jump

The reset jump is effected with the 74LS257A (IC 39) multiplexer along with a dual 74LS74 (IC 41) flip-flop. A multiplexer is a device which selects from one of two sets of inputs. In this case one set of four inputs is connected to the four most significant address lines of the Z80 while the other set of four inputs goes to four resistors which pull the inputs high. The inputs are also connected to LKB1. By making links to ground the inputs can be pulled low. When the select line is high the information on the second set of four inputs is output onto the address bus. An LS74 is D type flip-flop. When the clock input (of the flip-flop) goes from low to high the state of the D input is transferred to the Q output, the /Q output always being complementary to the Q output.

When a reset occurs the sequence of events is as follows.

a) A low on the /RESET line causes the Q output of IC 41b to go high and the /Q output of IC 41a to go high. This switches the LS257A inputs from the Z80 address lines to the inputs which program the reset jump address.
b) The /RESET line goes high, the Z80 fetches the first byte of the first instruction with an /M1 cycle, the Z80 "thinks" it is fetching the instruction from 0000, however the LS257A is putting the reset jump information from pins 11 to 14 of LKB 1 onto the most significant four bits of the address bus.
c) The low to high of the /M1 at the end of the first /M1 cycle clocks IC 41a, the net result being that the /Q output goes low. There is no effect on IC 41b.
d) The Z80 has fetched the first part of its first instruction, not from 0000 but from the address programmed on the links. The subsequent bytes of the instruction will be read from memory at the reset jump address, +1, +2.
e) The Z80 will execute the instruction read from the location determined by LS257A.
f) The next /M1 cycle will take place and on its completion /M1 will go high. This will clock IC 41a and cause its output to go high and this will in turn clock IC 41b (LS 74's being clocked by the low to high edge). Clocking IC 41b will take the Q output low and switch the LS257A back to the four most significant address lines of the Z80.

Normally the instruction at the reset jump address would be an absolute unconditional jump to the next address. If, for example, the G811 was reset jumping to F000, the instruction at F000 would be C3 03 F0, a jump to F003.

1.4 Wait state generation

The G811 can generate wait states either during all memory cycles or only on memory cycles involving the onboard memory or not at all. Selection of the type of wait state is performed by the 74LS32 (IC 20b). If LKB 3 pin 1 is connected to pin 14 which goes low whenever an onboard memory address is detected, the LS32 will gate out all /MREQ's which do not concur with the use of onboard memory. If however LKB 3 pin 1 is connected to pin 13 which is ground, a wait state will be generated during all memory cycles (/MREQ). Wait states can be totally disabled by not connecting pins 11 to 12 on LKB 3. If wait states are enabled the sequence of events is as follows.

a) /MREQ goes low and as a consequence the D input of the 74LS74 (IC 22a) also goes low.
b) The Q output of IC 22a goes low when the flip-flop is clocked by the low to high of the system clock at the beginning of T2. The Q output of IC 22a is ORed with the /Q output of IC 22b by the 74LS32 (IC 10b). The output of the LS32 goes to a 7407 which takes the /WAIT line of the bus low.
c) During the high to low transition of T2 the Z80 will sample the wait line and if it is low a wait cycle will be inserted.
d) The rising edge of the clock at the beginning of Tw (the extra cycle inserted by the wait state generator) will clock the second half of the 74LS74 (IC 22b), causing the /Q output to go high. This will result in the /WAIT line being taken high.

1.5 NMI pulser

Provision has been made for the generation of an /NMI pulse from a high to low transition on Bus line 6. Line 6 goes via a 470 ohm resistor (R 57) to the input of a 74LS14 (IC 9e), the input having a 22k pullup resistor (R27) and a 47uF capacitor (C19) to ground to act as debounce circuit, the intention being that Bus line 6 would be connected to a switch in the same manner as the reset switch is connected to line 10. The output of the LS14 is connected to a 74LS221 (IC 16b) which generates a negative going pulse from the low to high output of the LS14. The /NMI pulse is buffered onto Bus line 21 and into the Z80's /NMI pin with a 7407 (IC 15d). As with the reset input, switch bounce may give more than one /NMI.

1.6 Bus control

The address lines from the Z80 are buffered onto the bus via 74LS244 type buffers (A0 to A3 1/2 IC 35, A4 to A11 IC 34) for the least significant 12 lines. The most significant 4 lines are buffered onto the bus via a 74LS257A multiplexer (IC 39) (for further details see section 1.2 re. reset jump). The only control is the /BUSAK control signal which, when asserted, tristates all the address lines. The control signals from the Z80 are buffered with a 74LS244 (IC 40) buffer which is controlled in the same manner by the /BUSAK, the only difference being that the outputs of the buffers are pulled up to +5 volts with 10k resistors to ensure that in the event of the bus being "floated" all the control lines go high. The data bus is bidirectional and uses a 74LS245 (IC 29) and as a consequence the direction of operation and the state has to be controlled. The state is controlled by the same /BUSAK which also controls the other buffers. The direction in which the buffers "buffer" is determined by a combination of three signals, /RD, /IORQ and /M1. The data bus buffer will buffer "out" unless /RD is low (data into the Z80) or an /INTAK (interrupt acknowledge) cycle is being executed. The Z80 will execute an /INTAK cycle when it wants an interrupt vector. An /INTAK cycle is signalled by the Z80 taking both /IORQ and /M1 low, this condition being detected by a 74LS32 (IC 8d). /INTAK is ANDED with /RD by a 74LS08 (IC25d) which drives the direction input of the 74LS245 (IC 29). The direction input is low when the Z80 is inputting data from the bus and high when outputting data to the bus. The input signals to the Z80 (/RESET, /WAIT, /INT, /NMI, /BUSAK) are input directly to the Z80 from the bus with 2k2 pullup resistors.

Section 2 - Memory Circuitry

2.1 Memory enabling and decode

The decodes for the four memory sockets on the G811 come from a bipolar PROM (IC 19), the address inputs of the PROM being connected to address lines A8 to A15. By coding the PROM in the appropriate manner it is possible to decode any multiple of 256 bytes to any location in the memory map with a resolution of 256 bytes. Coding a PROM is very simple. First make a note of the addresses you wish decoded for each memory socket then convert the actual addresses to PROM addresses by discarding the 8 least significant bits of the address, i.e. CFFF becomes CF. Next, note against each series of socket decodes, the PROM contents to decode the appropriate socket. Socket I (IC 23) is decoded by an "E", socket II (IC 28) by a "D", socket III (IC 32) by a "B" and socket IV (IC 32) by a "7". Addresses which do not decode any of the four sockets should be programmed with an "F".

For example, if we wish to decode the memory sockets to the addresses in the table below

```
C000 - CFFF  Socket I
D000 - DFFF  Socket II
E000 - EFFF  Socket III
F000 - FFFF  Socket IV
```

we would code the PROM in the following manner:-

```
00 - BF   F   No decoding from 0000 to BFFF
C0 - CF   E   4K in socket I
D0 - DF   D   4K in socket II
E0 - EF   B   4K in socket III
F0 - FF   7   4K in socket IV
```

This is the code in the PROM normally supplied with G811 (PM-1). The PROM itself is a 256 X 4 tristate or open collector type. The part is available from many sources, programming however is unique to each part. For a full list of PROM types please see section 4.1.

The outputs of the PROM go via links on LKB2 and LKB4 to the /CE pins on the sockets. This makes it possible to disable sockets that are not required. Pull up resistors are provided on the socket side of the links to ensure that the memory chips are disabled both when the links are not present and when the decode PROM is disabled. The 8250 UART used in the I/O section of G811 has two outputs (/OUT1 and /OUT2) which can be changed by writing to a 8250 register. On reset both outputs go high. /OUT2 is connected via a 74LS04 (IC 12a) to a /CE input of the decode PROM. This makes it possible for the on board memory to be disabled under software control.

2.2 Memory data bus control

The 74LS245 (IC 38) data bus buffer is shared between the memory and I/O section of G811. The memory section of the control logic is explained in this section. For the description of the I/O data bus control please refer to section 3.6. /MREQ and /RD are ORed together by a 74LS32 (IC 14c) to create a signal /MEMRD, which goes low when the CPU performs a memory read. This signal is connected to the /OE (Output Enable) pin of the sockets (a memory IC requires both a /CE and either an /OE or a /WE for operation). In the same manner /MREQ and /WR are ORed together by a 74LS32 (IC 14b) to produce a signal /MEMWR which is fed to the /WE pins on LKB2 and 4, and pin 27 of the memory sockets.

The data bus buffer control defaults to the condition where it is buffering in from the data bus. When one of the four /CE inputs (on the memory sockets) goes low the output of the 74LS21 (IC 18a) will also go low. This signal goes to two places, LKB3 pin 14 as part of the wait state generation circuitry (please refer to section 1.4), and to the 74LS32 (IC 20a). The LS32 ORs the signal from the LS21 with /MEMRD. The output of the LS32 will therefore go low whenever a read from the onboard memory takes place. The output of the LS32 goes to the 74LS08 (IC 25c) where it is ANDed with the signal which goes low whenever an I/O read is taking place (see section 3.7). The output of the LS32 (IC 20a) goes via a 7407 (IC 15c) buffer to pin 10 of LKB1. When pin 10 of LKB1 is connected to pin 8 the /RAMDIS line on the bus will go low whenever the memory onboard the G811 is accessed. This means that a RAM board (e.g. Gemini G802) with a /RAMDIS input can have its memory disabled whenever the G811 memory is accessed.

It is also possible to input the /RAMDIS signal into G811 so that the onboard memory is disabled by a /RAMDIS generated elsewhere. This is effected by connecting pin 9 of LKB1 to pin 8 which is the /RAMDIS line on the bus. Pin 9 of LKB 1 is pulled up by the 2k2 resistor R25 and connected to the 74S04 (IC 36a). The output of the S04 is connected to the chip enable input of the 74LS245 (IC 38). When the /RAMDIS line goes low the output of the S04 goes high and disables the buffer. Users should however take care when using this facility because if a vectored interrupt occurs and the RETI instruction is in an area of memory which generates a /RAMDIS, the /RAMDIS will disable the 74LS245 (IC 38) and prevent the G811's PIO (which shares the 74LS245) from picking up the RETI. This could cause problems.

2.3 The Bytewide memory concept

The bytewide concept is an attempt by manufacturers to enable users to use a wide variety of different memory chips in the same socket. The basis of the concept is that all the memory chips have a chip enable (aka chip select) (/CE), an output enable (/OE) and if the chip can be written to, a write enable (/WE). It is also necessary for the /CE to be asserted with one of the other signals before the memory chip will become active. As a result, the address is decoded straight into the /CE, the /RD signal is ORed with /MREQ and the result connected to the /OE (output enable) pin. In a similar manner the /WR is ORed with /MREQ and connected to the /WE input.

Section 3 - Input/Output Circuitry

3.1 I/O address decoding

When the Z80 executes an input or output instruction the port address appears on the bottom eight address lines (A0 to A7). The bottom eight address lines are connected to the 256 X 4 bipolar PROM (IC 17). The D0 output of the PROM is used to enable the PIO. D1 is a spare output and is brought out to a test point TP2. D2 is used to enable the keyboard port and D3 is used to enable the 8250. In addition to the device enables, two further signals are generated, /IORD which is /IORQ ORed with /RD by the 74LS32 (IC 8c) and /IOWR which is /IORQ ORed with /WR by the 74LS32 (IC 8b), these two signals being used by the keyboard interface and the 8250 UART.

The PROM is coded in the following manner.

a) Select the ports to which you wish the various functions to be assigned.
b) The 256 PROM locations are directly mapped to the 256 I/O ports which are available. One merely has to load the particular location in the PROM with the contents which will take the appropriate data output of the PROM low and as a consequence enable the specific device.
c) D0 will go low if the location contains an E, D1 will go low if the location contains a D, D2 will go low if the location contains a B and D3 will go low if the location contains a 7.

Below is a table of contents for the standard I/O PROM for G811. (PIO-1)

PROM location	Contents	Function
00 - AF	F	No function
B0	B	Keyboard interface
B1 - B3	F	No function
B4 - B7	E	PIO
B8 - BF	7	8250 UART

3.2 PIO

The PIO provides two sets of eight bit input/output lines. The PIO is selected by a /CE from the port address decode PROM (IC 17). It also inputs the control signals /IORQ, /M1 & /RD from the system. The PIO uses these signals to determine the particular cycle that is being executed. /M1 is gated with the reset pulse from bus line 14 by the 74LS08 (IC 13c). When a reset occurs /M1 is interrupted and the PIO is reset. It must be pointed out that the actual reset only takes place on the restoration of /M1. The PIO has two further outputs and four inputs from the system. /INT goes low to generate an interrupt. Interrupt priority arbitration with other devices in the vectored interrupt structure takes place via the IEI and IEO lines. The PIO is clocked with the system clock in the same manner as the Z80 itself from the same clock driver circuitry. Address lines A0 and A1 are input to the PIO to determine the particular port that is being addressed. The eight bit data bus to the PIO is buffered by the same 74LS245 (IC 38) that is used to buffer the memory section of the G811. The two sets of eight bit input/output lines appear on a 26 way IDS connector along with four ground lines and two +5 volt lines. The PIO is divided into two eight bit ports, port A and port B, each port having a data port and a control port. The port allocations are as listed below. It must be explained that the location of the PIO in the logical port address map is described as a port and the input/output lines are often also described as ports, please do not get confused.

Port A data	B4
Port B data	B5
Port A control	B6
Port B control	B7

The data ports are read/write. The control ports are write only. The PIO has four modes of operation.

0) Output mode. The data lines are configured as outputs, data written to the data port will appear on the output lines.
1) Input mode. The data lines are configured as inputs, and data can be read via the data port.
2) Bidirectional mode. The configuration depends upon the state of the handshake lines.
3) Control mode. Inputs and outputs amongst the eight lines can be mixed.

When the PIO is reset it goes into input mode and the inputs float (users should however note that when the PIO is not powered the input/output lines are grounded). Changing the configuration is effected by writing to the control port pertaining to the appropriate data port. The sequence is as follows.

1) First load the interrupt vector. This is the least significant eight bits of the memory address where the Z80 expects to find the address of a routine which it will execute. The least signifcant bit (D0) must be 0. If you are not going to use vectored interrupts this stage can be omitted.
2) Tell the PIO its mode of operation.

Mode number	Type of mode	Code
0	Output	0F
1	Input	4F
2	Bidirectional	8F
3	Control	CF

Load the control port with one of the above codes.

3) This next stage is only required if you have selected mode 3 at stage 2. In mode 3 you select which lines are going to be outputs and which lines are going to be inputs. This is done by selecting the lines which are going to be inputs and adding up their binary weighted value. If, for example, you wish bits 7, 6 & 2 to be inputs you add 80 + 40 + 04 giving C4. You then output C4 to the control port assigning the appropriate bits as inputs. The remaining bits will default to being outputs.
4) The next byte is only necessary if interrupts are being used. Its value is obtained by adding up the numbers in the table below appropriate to what is required.

Enable interrupts	80	(disable interrupts)
AND function	40	(OR function)
High state	20	(low state)
Mask will follow	10	(no mask)
+	07	

On the left hand side of the table is the effect of adding in a particular number and on the right hand side (in brackets) is the effect of not adding in a particular number. 07 must always be added in.
5) The final byte is the mask. This is obtained in the same manner as the byte used to program which lines are inputs and which are outputs in step 3. The bits you do not wish to monitor should be added up in proportion to their binary weightings. For example, if you do not wish to monitor bits 6, 3 & 2, adding 40 + 08 + 04 will give 4C, and loading the PIO with 4C would mask out bits 6, 3 & 2 which as a consequence would not be monitored.

It is not possible, in this somewhat brief description, to go into complete detail on the use of a most versatile device. For complete details please see the PIO manuals from Mostek or Zilog.

However, here are three examples of the use of a PIO on the G811.

1) PIO into output mode, load the control port with 0F. Any data sent to the data port will be output.
2) PIO into input mode, the PIO will reset into input mode. To read the inputs simply read the data port. If, however, it is already in another mode, load the control port with 4F.
3) Running vectored interrupts on the keyboard strobe line.
 a) Load the Z80's I register with the eight most significant bits of the interrupt vector.
 b) Put the Z80 into interrupt mode 2 (IM 2).
 c) Load the locations of the interrupt vector with the address of the keyboard service route.
 d) Load the PIO control port with the least significant eight bits of the interrupt vector. Note that the least significant bit has to be a 0.
 e) Put the PIO into mode 3 by loading the control port with CF.
 f) Make all the lines inputs by loading the control port with FF.
 g) We wish to, enable interrupts, OR all the bits, look for a high, and tell the PIO that a mask will follow, so 80 + 20 + 10 + 07 = B7, so load the control port of the PIO with B7.
 h) Now we wish only to monitor the least significant bit so the control port is loaded with FE.
 i) Now enable interrupts.

Points to remember, the IEI and IEO daisy chains on the system back plane must be set up, otherwise the PIO will never return from the interrupt (see the Gemini-80 BUS specification). Pin 1 should be linked to 16 on LKB1 (to connect the keyboard strobe line to the PIO). An interrupt will disable any further interrupts so the keyboard service routine should re-enable them.

3.3 8250 UART

The 8250 is a very sophisticated asynchronous communications element. It includes a baud rate generator and full modem control facilites.

The 8250 receives its chip enable from the I/O decode PROM (IC 17). It has been allocated ports B8 to BF. The read enable input /DISTR is fed from the 74LS32 (IC 8c) which generates /IORD (I/O read). The write enable input /DOSTR is fed from the 74LS32 (IC 8b) which generates /IOWR (I/O write). Reset from bus line 14 is inverted by the 74LS04 (IC 12d) and connected to the reset input, reset being active high. The clock input to the 8250 comes from LKB3 and in a 4MHz system would be 2MHz. Address lines A0, A1 & A2 are also input and are used to select between the registers. The interrupt output is connected to LKB 1 pin 15 where it can be linked to pin 2 and hence to the PIO to generate a vectored interrupt.

8250 registers

Line Control Register (port BB read/write)

Bits 0 & 1 determine the number of bits in each transmitted or received character.

Character length	Bit 1	Bit 0
5 bits	0	0
6 bits	0	1
7 bits	1	0
8 bits	1	1

Bit 2, determines the number of stop bits in each character. If a logic 1, 1.5 stop bits for a 5 bit character, 2 stop bits for the 6, 7 & 8 bit character lengths. If a logic 0, 1 stop bit whatever the character length.

Bit 3, parity enabled when logic 1, causes parity generation on transmit and verification on receive.

Bit 4, parity select, logic 0 for odd parity, logic 1 for even parity. Odd parity means that the character will have an odd number of ones. Even parity means the character will have an even number of ones.

Bit 5, stick parity, inverts the effect of bit 4.

Bit 6, set break, when logic 1 the serial output from G811 is forced to the spacing state, i.e. negative. This is irrespective of transmitter activity.

Bit 7, DLAB bit, this bit is used to switch ports B8 and B9 between the receive/transmit buffers (B8), the interrupt enable register (B9), and the baud rate divisor registers. When logic 1 the divisors are accessable and when logic 0 the receive/transmit buffers and the interrupt enable register are accessable.

Line Status Register (port BD read/write)

Bit 0, data ready indicator, logic 1 whenever a complete character has been received and is ready to be read. Reset either by a read of the receiver data register or by writing a 0 to this location.

Bit 1, overrun error indicator, set to logic 1 if the receive buffer was not read prior to the current character being loaded in. Reset by a read of the line status register.

Bit 2, parity error indicator, set if a parity error is detected. Reset by a read of the line status register.

Bit 3, framing error, set if the received character did not have a valid stop bit. Reset by a read of the line status register. This is the most common type of error from tape interfaces.

Bit 4, break interrupt indicator, set to a logic 1 whenever the serial input to G811 is held in spacing (-12 volts) for longer than a full character period.

Bit 5, transmitter holding register empty indicator, set to a logic 1 whenever the holding register is ready to accept a new character. Reset by loading the transmitter holding register (port B8).

Bit 6, transmitter shift register empty indicator, set to a logic 1 whenever the transmitter shift register becomes empty. Reset by the transmit shift register becoming active. This bit is read only.

Bit 7, there is no bit 7, this location is permanently set to logic 0.

Modem Control Register (port BC read/write)

Bit 0, DTR output, set to logic 1 to set the DTR output from G811 positive. Reset to take the DTR output negative.

Bit 1, RTS output, set to logic 1 to set the RTS output from G811 positive. Reset to take the RTS output negative.

Bit 2, /OUT 1 output, set to logic 1 to select RS 232 input and output, reset to 0 to enable the tape interface. Also controls the transistor TR1, which is switched on with the tape interface.

Bit 3, /OUT 2 output, used to enable the G811 onboard memory, set to logic 1 to disable the onboard memory, reset to logic 0 to enable the onboard memory.

Bit 4, loopback when set to logic 1, normal operation when reset to logic 0. When set to logic 1 the following events occur.

a) The serial output is set to marking, logic 1.
b) The serial input is disconnected.
c) The output of the transmitter shift register is connected to the receive shift register.
d) The following status bits are linked, CTS to DTR, DSR to RTS, RLSD to OUT1, RI to OUT2.

This enables all the 8250's functions and software to be checked. It should be noted that the interrupts are still operational.

Bits 5 to 7, there are no bits 5 to 7, they are all set to logic 0.

Modem Status Register (port BE read/write)

Bit 0, delta Clear To Send (CTS), if set to logic 1 indicates that the CTS line has changed state since the modem status register was last read.

Bit 1, delta Data Set Ready (DSR), if set to logic 1 indicates that the DSR line has changed state since the modem status register was last read.

Bit 2, trailing edge Ring Indicator (RI), if logic 1 indicates that the /RI input to the 8250 has gone from logic 1 (high) to logic 0 (low) since the modem status register was last read. For further details on the ring indicator please refer to bit 6 of the modem status register.

Bit 3, delta Received Line Signal Detector (RLSD), if logic 1 indicates that the RLSD has changed state since the modem status register was last read.

Bit 4, Clear To Send (CTS) input, logic 1 if the CTS input to G811 is positive, logic 0 if CTS is negative. If bit 4 (loopback) of the modem control register is a logic 1 this bit indicates the state of RTS (bit 1) in the modem control register.

Bit 5, Data Set Ready (DSR) input, logic 1 if the DSR input to G811 is positive, logic 0 if the DSR input is negative. If bit 4 (loopback) of the modem control register is logic 1, this bit indicates the state of DTR (bit 0) in the modem control register.

Bit 6, Ring Indicator (RI) input, logic 0 if the /RI input is high, logic 1 if the input is low. If bit 4 (loopback) of the modem control register is logic 1, this bit indicates the state of OUT 1 (bit 2) in the modem control register. It should be noted that on the G811 the /RI input to the G811 is pulled up by a 10k resistor R59 and it is also connected to pin 7 of link block 1 where it may be grounded. It is intended that this should be used by the software to indicate the board status. If this is implemented further details will be in the software manual.

Bit 7, Received Line Signal Detect (RLSD) input, logic 1 if the RLSD input to G811 is positive, logic 0 if RLSD is negative. If bit 4 (loopback) of the modem control register is set, this bit indicates the state of OUT 2 (bit 3) in the modem control register.

Interrupt Enable Register (port B9 read/write)

Bit 7 of the line control register (port BB) must be logic 0 for access.

Bit 0, Received Data Available interrupt, when set to logic 1, an interrupt will be generated whenever data is available to be read.

Bit 1, Transmitter Holding Register Empty interrupt, when set to logic 1, an interrupt will be generated whenever the transmit holding register becomes empty.

Bit 2, Receiver Line Status interrupt, when set to logic 1, an interrupt will be generated whenever any of bits 1 through 4 of the line status register go high to indicate an error condition.

Bit 3, Modem Status interrupt, when set to logic 1, an interrupt will be generated whenever any of bits 0 through 3 of the modem status register go high to indicate a change in modem status.

Bits 4 through 7, always set to logic 0.

Interrupt Identification Register (port BA read only)

Bit 0, Interrupt Pending, when logic 0 an interrupt is pending. When the interrupt identification register is accessed all interrupts are frozen and no further interrupts will be acknowledged until the cause of the interrupt has been serviced or cleared.

Bit 1 = logic 1 & bit 2 = logic 1,
Highest level of interrupt priority, caused by a Receiver Line Status Register interrupt. Source of error, Overrun error, Parity error, Framing error or Break interrupt. Reset by reading the Line Status Register.

Bit 1 = logic 0 & bit 2 = logic 1,
Second highest level of interrupt priority, caused by receive data becoming available. Reset by reading the receiver buffer register.

Bit 1 = logic 1 & bit 2 = logic 0,
Third highest level of interrupt priority, caused by the transmitter holding register becoming empty. Reset by either reading the interrupt identification register or by writing into the transmitter holding register.

Bit 1 = logic 0 & bit 2 = logic 0,
Fourth highest level of interrupt priority, caused by a modem status register interrupt. Source of the interrupt is a change in status of one of the following signals, CTS, DSR, RI or RLSD. Reset by reading the modem status register.

Bits 3 through 7, set permanently to logic 0

Baud Rate Generator

Most significant byte port, B9 (read/write)
Least significant byte port, B8 (read/write)
Bit 7 of the Line Control Register (port BB) must be set to 1 for access.

The baud rate is generated by dividing down the clock input of the 8250. The equation for determining the baud rate is as below.

$$\text{Divisor} = \frac{\text{8250 clock frequency}}{\text{(Baud rate x 16)}}$$

The divisor should be split into two bytes. The most significant byte should be loaded into the most significant divisor latch, the least significant byte being loaded into the least significant divisor latch. It should be noted that,

a) The divisor is in Hex.
b) The bytes should be loaded even if zero (some 8250's have been observed to power up loaded with FF).

The divisors for a 2MHz clock are tabulated below. The numbers in the hex column should be loaded.

Baud Rate	Divisor (decimal)	Divisor (hex) MSB	LSB
50	2500	09	C4
75	1667	06	83
110	1136	04	70
134.5	929	03	A1
150	833	03	41
300	417	01	A1
600	208	00	D0
1200	104	00	68
1800	69	00	45
2000	63	00	3F
2400	52	00	34
3600	35	00	23
4800	26	00	1A
7200	17	00	11
9600	13	00	0D

Data Holding Register (port B8 write only)

Bit 7 of the line control register (port BB) must be logic 0 for access.

Data from this register is output from the 8250 in serial form.

Receiver Buffer Register (port B8 read only)

Bit 7 of the line control register (port BB) must be logic 0 for access.

This register contains the received data.

Further data on the 8250 can be obtained from the relevant data sheet. (e.g. National Semiconductor INS8250), or see An Introduction to Microprocessors Volume 3, by Osborne.

3.4 RS 232 interface

The RS 232 interface is implemented with the use of two IC's. A 75188 (IC 3) is used for output and converts from TTL levels to RS232 levels (+/- 12 volts). The 75188 also inverts the signal in that a high from the 8250 produces a -12 volt signal and a low produces +12 volt signal. It should be noted that the discussion of the 8250 (section 3.3) referred to the signals output from the G811 and not from the 8250. The RS 232 data output from G811 can be inhibited by the /OUT 1 signal, which is also used for switching between the tape and RS 232 interfaces.

The RS 232 input buffering is handled by a 75189A (IC 2). The 75189A translates RS 232 levels to TTL levels. The signal is inverted in the same manner as the 75188, a negative signal producing a TTL high output. The discussion of the 8250 (section 3.3) made reference to signals into the G811. The signal will be inverted between the 75189A and the 8250. The hysteresis of the 75189A can be adjusted by varying the values of Rs 11, 12, 13 and 14. The G811 will have been shipped without any resistors in these positions as under normal circumstances none should be required. If however particular operating conditions required different hysteresis, resistors can be added. Please first read the data sheet for the 75189A. It is possible to input at TTL levels to the G811 but the noise margin will be reduced. Further data on the 75188 and and the 75189A may be obtained from Texas Instruments Data Sheets.

3.5 Tape interface

The tape interface is based on the original Kansas City format (aka CUTS). The original specification called for a low (from the UART) to be represented by four cycles of 1200 Hz and a high to be represented by eight cycles of 2400 Hz. This resulted in a transmission rate of 300 baud (300 bits per second (30 characters per second)). To speed up the data rate this has been changed to 1200 baud by representing a low with one cycle of 1200 Hz and a high with two cycles of 2400 Hz. The encoding is done in the following manner by the 74LS113 (IC 6), which consists of two JK flip-flops. If the J input of an LS113 is held high and the K input is also high the falling edge of the clock pulse will cause the Q output to change state. If the K input is then taken low the Q output will go high on the next falling edge of the clock. If both inputs are low the outputs will not change on the falling edge of the clock. The net result is a synchronous programmable frequency divider. The serial data from the 8250 goes via a 74LS04 inverter (IC 12f) to the K input of the 74LS113 (IC 6a). When the data output of the 8250 is high the input to the LS 113 is low. This has the effect of causing the Q output of the LS113 (on the next high to low of the clock) to go high. The Q output of IC 6a is connected to both the J and K inputs of IC 6b. The net effect of taking both the inputs high is that the Q output of IC 6b will "toggle" on each high to low of the clock. This will result in a frequency of half the clock frequency being output. If, however, the serial data output of the 8250 is low the K input of the 74LS113 will be high. This will have the effect of causing IC 6a to "toggel" i.e. the output will change state each time the clock goes high to low. This will have the net effect of dividing the clock to the LS113 (both parts) by four, resulting in an output frequency of 1200 Hz. The output of IC 6b is connected to a combined low pass filter and attenuator. The low pass filter is formed by the 47k resistor R8 and the 10nF capacitor C49. The low pass filter prevents the harmonics in the encoded data signal causing problems. The encoded data signal is connected to one of the pins of link 5 and to a potential divider formed by the 4k7 resistor R7 and the 470 ohm resistor R2. A second pin on link 5 is connected to the junction of the two resistors to provide the option of a low level signal out of the G811.

The clock to the LS113 is the 16x baud rate clock used to clock the shift register in the 8250, divided by four by the 74LS74 (IC 11) dual D-type flip-flop.

Tape decode circuitry

The signal from the tape is attenuated by Rs 9 and 10 which form a potential divider. In the standard G811 these resistors will both be 10k, however they may be changed to suit individual conditions. The signal is coupled to the input of the XR2211 by a 100nF capacitor (C5).

The XR2211 is a FSK (Frequency Shift Keying) decoder consisting of a phase comparator, a VCO (voltage controlled oscillator) (which together with the phase detector forms a phase lock loop), a voltage comparator and a lock detector. The signal is input to the 2211 which amplifies and limits it. It then goes to a phase detector which generates a voltage which is proportional to the phase difference between an incoming signal and the onboard oscillator. The free running frequency of the oscillator is determined by the 22nF capacitor (C1) and can be fine tuned by the 10k variable (RV1). The output of the phase comparator appears at pin 11 of the 2211. The output of the phase comparator is filtered with a 2n2F capacitor (C3) and coupled back to the VCO via a 33k resistor (R3), thus forming a phase locked loop. The output of the phase comparator is further filtered by the 100k resistor (R4) and the 2n2F capacitor (C4). It is then input to the voltage comparator (pin 8).

The voltage comparator compares the voltage from the phase detector with a reference and causes the output to go high or low depending on whether the incoming frequency is lower or higher than the free running frequency of the VCO. The data output is connected back to the input to the voltage comparator via a 510k resistor (R5), this acting to speed up the transitions. The data output is also connected to a 5k1 pull up resistor (R28) and to the input of the 74LS04 (IC 12b), the inverter being required as the decoder produces a low for a high frequency input and a high for a low frequency input.

The output of the LS04 is connected to the 74LS08 (IC 13a), the other signal into the LS08 is the /OUT 1 signal from the 8250 which goes high to enable the tape interface. The output of the LS08 goes to the 74LS32 (IC 8a) whose output is connected to the serial data input of the 8250.

The reference voltage against which the output of the phase comparator is compared is available at pin 10, where it is also decoupled by the 100nF capacitor (C2). The 2211 also has a lock detector which will inhibit the output of spurious data from the 2211. The output of the 2211 will go low when the phase lock loop goes out of lock. The lock detection circuitry has a time constant formed by the 100k resistor (R6) and the 33nF capacitor (C6) associated with it.

3.6 Keyboard interface

The keyboard interface consists of a 74LS244 (IC 4). The port assigned to the keyboard is detected by the I/O decode PROM (IC 17). The output of the PROM is ORed with the /IORD (I/O read) signal by the 74LS32 (IC 14d). The output of the LS32 is connected to the enable inputs of the LS244. Also associated with the keyboard port is the Halt LED drive circuitry. There is provision for two Halt LEDs, one on the G811 itself and one on the keyboard. Both are driven by the 74N07 (IC 15e) whose output goes low whenever the Halt line on the bus goes low. The output of the N07 is connected to the two LEDs via two 150 ohm resistors (Rs 16 and 17) which serve to limit the current.

3.7 I/O Data Bus Control

The I/O section of G811 shares the same 74LS245 (IC 38) data bus buffer as the memory section. The LS245 will normally buffer data from the bus to the I/O circuitry. It must buffer in the opposite direction under the following conditions.

a) one of the three outputs of the I/O decode PROM has gone low to indicate an I/O address for the G811's I/O and this has concurred with an /IORD.
b) an /INTAK cycle has been executed by the Z80 and this has concurred with IEI being high and IEO being low, which would indicate that the Z80 is expecting an interrupt vector from the G811's PIO.

The first condition is detected by the 74LS21 (IC 18b) ANDing together the three active data outputs of the I/O decode PROM. The output of the LS21 will go low whenever any of the onboard devices is addressed. The output of the LS21 is ORed with /IORD by the 74LS32 (IC 14a). The output of the LS32 will go low whenever a read takes place from the G811's I/O section.

The second condition is detected in the following manner. IEI is inverted by the 74LS14 (IC 9d) to create /IEI. IEO is ORed with /IEI by the 74LS32 (IC 20c) to detect the condition that the G811's PIO is the interrupting device (IEI high, IEO low). The output of the LS32, which will go low when the G811's PIO is the interrupting device, is connected to a second LS32 (IC 20d). The second LS32 will OR together /INTAK from the LS32 IC8d with the output of IC20d. The output of the LS32 (IC20d) will go low whenever the PIO generates an interrupt vector.

The two conditions are ANDed by the 74LS08 (IC 25b) whose output will go low whenever the bus buffer has to buffer onto the bus. This signal is ANDed with the signal from the memory data bus control circuitry (see section 2.2) by the 74LS08 (IC 25c). The output of IC 25c goes to the direction control input of the 74LS245 (IC 38). The direction control input of the LS245 will go low whenever it is buffering from the I/O or memory sections onto the system data bus.

Section 4 - PROM Types

The recommended part is the Texas 74S287, however here is a list of equivalents. If you require a custom PROM for a particular application please contact Gemini or a Gemini distributor.

Brand	Part number
AMD	27S21C
Fairchild	93427DC
Futitsu	MB7057
Harris	7611-5
Intel	3601
Intersil	5623C
MMI	6301-1
Nat semi	74S287
NEC	uPB423D
Signetics	N82S129
Texas	74S287

80-BUS - a functional description

The Multiboard range of 8"x8" cards have been designed so that they may be used together in a wide variety of configurations. All of the cards have a 77 way PCB edge connector which carries signals to the 80-BUS specification, as detailed below. Cards are simply connected together by soldering the edge connectors supplied with the cards into a motherboard, and then plugging the cards into the connectors. The motherboard provides interconnection of each of the edge connector pads on each card to the same pad on every other card. The only exceptions to this are the 'daisy chain' lines, and details of these are given in the specification.

Power is supplied to the cards by connecting the relevant supply rails to the motherboard. Each power supply rail occupies two or more bus lines, and in these cases should therefore be connected to all of the relevant bus lines, this is particularly true of the Ground (0V) rail.

80-BUS has many similarities to Nascom's Nasbus. The Nasbus, unlike many other bus systems, has had a very ordered development. However, when we started developing the Multiboard range of cards it became apparent that a new revision to the Nasbus specification was urgently required. After a great deal of careful thought and many hours of deliberation the following document was drawn up. It expands on the third issue of the Nasbus functional specification giving timing and other details never previously published and also attempts to anticipate some of the possible future developments of the bus.

The original Nasbus specification made provision for the extra address and data lines of 16 bit processors. Careful consideration reveals that the bus would not be suitable for this, and so a number of new signals have been defined for the lines made free. The importance of good ground signals can not be overemphasised, and so extra ground lines have also been added.

When defining this bus a great deal of thought went into deciding whether or not to maintain the NAS MEM, NAS IO, and DBDR signals. These signals are particular to Nascom 1 (and NAS IO also to Nascom 2) and are unlikely to be required by any future cards. They therefore constitute a 'nuisance'. However, for the sake of compatibility, to avoid the S100 situation, and with pressure from INMC80, the Nascom Users' Club, it was decided that 80-BUS would maintain support for these signals.

Because of the above considerations 80-BUS remains fully Nascom 1 and 2 compatible. It is Gemini Microcomputers intention to allow any manufacturer who produces a card that fully complies with the 80-BUS specification to advertise accordingly. Cards should be submitted for approval. The 80-BUS is a Z80 bus and no attempt has been made to make it compatible with any other processor.

One final point relevant to the design of 80-BUS compatible cards is that all cards, including the bus master, should provide a means for being switched out of the memory map under software control. This may be by means of implementing the Page Mode structure, or by some alternative method. This condition also applies to any I/O card that is memory mapped.

Multiboard & 80-BUS are trademarks of Gemini Microcomputers Limited.
Nasbus is a trademark of Lucas Logic Limited (Nascom Microcomputers Division).

80-BUS pin allocation

PIN		SIGNAL	DESCRIPTION
1		GND	Ground
2		GND	Ground
3		GND	Ground
4		GND	Ground
5		CLOCK	System clock
6	*	/NMI SW	A low on this line initiates a short pulse on line 21
7		RSFU	Reserved for future use
8		AUX CLK	4MHz clock signal (optional)
9	*	/RAM DIS	Ram disable
10	*	/RESET SW	Reset switch
11	*	/NAS MEM	Memory decode to Nascom 1
12	*	/NAS IO	I/O decode to Nascom 1 and 2
13	*	/DBDR	Data bus drive, used to change the direction of the data bus buffers on the Nascom buffer board or Gemini `Supermum'.
14	*	/RESET	50uS reset pulse, resets entire system.
15		/HALT	Z80 halt signal
16		/BAI	DMA
17		/BAO	daisy chain
18		/BUSRQ	Z80 bus request
19		IEI	Interrupt
20		IEO	daisy chain
21	*	/NMI	Z80 NMI line, (not used by Nascom 1)
22	*	/INT	Z80 interrupt line
23	*	/WAIT	Z80 wait line
24		/RFSH	Z80 refresh signal
25		/M1	Z80 opcode fetch signal
26		/IORQ	Z80 input/output signal
27		/MREQ	Z80 memory signal
28		/WR	Z80 write signal
29		/RD	Z80 read signal
30		A0	
31		A1	
32		A2	
33		A3	
34		A4	
35		A5	
36		A6	
37		A7	
38		A8	Z80 16 bit
39		A9	address bus
40		A10	
41		A11	
42		A12	
43		A13	
44		A14	
45		A15	
46		A16	Optional implementation
47		A17	for extended
48		A18	addressing.
49		GND	Ground to seperate the data and address busses.
50		D0	
51		D1	
52		D2	
53		D3	Bidirectional data bus.
54		D4	
55		D5	
56		D6	
57		D7	

58	RSFU	Reserved for future use
59	INT 0	Interrupt
60	INT 1	request
61	INT 2	lines
62	INT 3	
63	/PWRF	Powerfail warning
64	AUX PWR	Backup power
65	NDEF 1	Not to
66	NDEF 2	be defined
67	GND	Ground to seperate power and signal lines.
68	-5V	
69	-5V	
70	-12V	
71	-12V	
72	keyway	
73	+12V	
74	+12V	
75	+5V	
76	+5V	
77	+5V	
78	+5V	

Notes
---

1) * is an open collector line.
2) IEI to be linked to IEO on cards not using the interrupt daisy chain.
3) /BAI to be linked to /BAO on cards not using the DMA daisy chain.
4) Bus drivers must be able to drive 75/15 U.L.
5) Bus receivers must not load the bus past 1/0.25 U.L.
6) Bus master to pull up all open collector lines with 2k2.
7) Bus master to pull up the following lines with 10k, /HALT, /MREQ, /IORQ, /RD, /WR, /M1, /RFSH.
8) Bus timing reference point is pin 6 of the Z80. As the bus is in essence a buffered Z80, the timing of bus signals is as the Zilog/Mostek Z80 data book. All Z80 signals are buffered onto the bus with 20nS +/- 10nS buffers, the sole exception being the bus clock which should be 20nS (+/- 10nS) ahead of the Z80 clock (pin6). The timing of other signals is detailed in the description of the particular signal. All expansion card timing must, however be referenced to the bus.
9) Cards using /BAI, /BAO, IEI & IEO should pull them up with 2k2.
10) Bus termination. Long buses may require termination. 220R on each line to a 2.6V low impedance source should solve 99% of problems.
11) Grounding. The ground line to the PSU should be as short as possible and as thick as possible.
12) The names of the various bus signals are as detailed above, please do not change them or abbreviate them, ie AUX CLK not AUX CLOCK or A CLOCK etc.

Comments

The following is a line by line description of the bus and should help resolve any ambiguities.

Lines 1-4, GND.

The quality of the system ground cannot be overemphasised. Ground noise problems were at the root of the now infamous Nascom "Memory plague". The faster that systems go the more critical the noise problem will become. Noise problems will manifest themselves as a generally unreliable system with a predilection to do "odd" things.

Line 5, CLOCK.

This line is important as all the bus timing is derived from it. It should spend at least 46% of its time below VOL (0.4V) and at least 46% of is time above VOH (2.4V), it has the other 8% spare to go up and down. The clock on the bus should be 20nS (+/- 10nS) ahead of the clock on pin 6 of the Z80.

Line 6, /NMI SW.

Provision has been made on the bus for an NMI switch and this line is to be held high by the bus master. Grounding it will initiate a short pulse on line 21 and the Z80 /NMI input. Users are cautioned that switch bounce may cause more than one NMI.

Line 7, RSFU.

This line is reserved for allocation at a later date, please do not use.

Line 8, AUX CLK.

This line is a new allocation. Many boards (eg disk controllers) require a 1, 2 or 4 MHz signal. This was easily provided when the CPU clock was 2 or 4 MHz, however the advent of the 6 MHz Z80 changes the situation. Any bus master not running at either 2 or 4 MHz must provide a 4 MHz clock on this line. Designers of expansion cards should take note of this and provide a link to allow the board to use this line instead of line 5.

Line 9, /RAM DIS.

This signal is intended to prioritise memory. Normally this signal would be generated by memory on the bus master, an EPROM card or any other high priority memory when a memory read took place. A RAM card would normally gate /RAM DIS with the output buffer, so that in the event of /RAM DIS being asserted the output buffer would fail to be enabled, this would have the effect of "overlaying" RAM with EPROM/ROM. /RAM DIS should not inhibit a write cycle; it should also remain high for any cycle apart from a memory read.

Line 10, /RESET SW.

A high to low on this line will initiate a reset cycle. It is intended that a switch be connected between this line and ground. The actual RESET line is line 14.

Line 11, /NAS MEM.

This signal is only used by Nascom 1 and is asserted when a Nascom memory address is detected. It would normally be provided by a memory board and would typically be 0000H to 0FFFH or F000H to FFFFH. This is an obsolete signal and no new boards that require it should be designed. This line used to be called MEMEXT.

Line 12, /NAS IO.

This line used to be called IOEXT and many people persist in still calling it that, even though the two are different. In its original form (note that it was active high) it would be taken high to indicate an I/O address external to the Nascom, in its current form it is taken low to indicate a Nascom I/O address, that is to say that it looks for a Nascom I/O address as opposed to looking for an external address. /NAS IO should be taken low within 50nS of a Nascom I/O address and /IORQ, (referenced to the bus). In its original form the onboard ports on the Nascom would remain enabled for a short fraction of an external I/O cycle (the time taken to detect an external address and assert IOEXT) and this was the cause of many obscure problems. If you have problems a good test is to write a short machine code routine to continuously write 80H to port 08H. If the breakpoint register display comes up you have a problem, if not you don't. /NAS IO is a obsolete signal utilised by Nascom 1 and 2 and all new designs should incorporate full I/O decoding.

Line 13, /DBDR.

This signal is used by the Buffer board and Supermum with Nascom 1. It controls the direction of the data bus buffers. When an expansion card outputs data to the bus this line must be taken low, normally this is the same signal as used to turn on the output buffers. Despite being only used by expanded Nascom 1s it is felt that this signal must be provided on all expansion cards. While /DBDR should ideally go low before the data bus driver is enabled, it must be low within 30nS of the data bus driver being enabled and must release /DBDR within 30nS of the data bus drivers being disabled.

Line 14, /RESET.

This line is the "cleaned up" version of line 10. It is important that the falling edge of the reset pulse on this line be synchronised with the falling edge of /M1, and the bus master must provide the appropriate logic to take care of this. The last issue of the Nasbus specification called for a 10uS reset pulse. This has now been extended to 50uS as chips in the 179X family require a 50us pulse. Deep investigation of the matter has yet to yield a 179X chip that can tell the difference between a 10uS pulse and a 50uS pulse. N2 owners who are concerned by this should substitute a 10nF capacitor for C1 (1nF). Supermum owners need not worry as this has been taken care of.

Line 15, /HALT.

Z80 halt signal. Up to this point in time nobody has used it, but it is there.

Lines 16 17 18, /BAI /BAO /BUSRQ.

/BAI and /BAO are the DMA daisy chain. If an expansion card wishes to take control of the bus (an expansion card is any bus card which is not a bus master) it asserts /BUSRQ; the bus master will respond by taking /BAO low. The mother board connects line 17 to 16 between each slot, ie line 17 of the bus master will go to 16 of the adjacent card, line 16 at the bus master is not used although it can be a test point. Between all subsequent cards line 17 goes to line 16 (for full connection details see the section on daisy chains). Cards that do not use the DMA facilities should connect 17 to 16. /BAO will be fed into the /BAI of any potential DMAing device, and the /BAO of the same device will go into the /BAI of the next and so on. If a potential DMAing device has not asserted the /BUSRQ line it will pass on the signal. When the signal reaches the device which originally asserted the /BUSRQ line it will hold /BAO high, at this point it will have taken contol of the bus. The highest priority device is that nearest the bus master.(CPU card).

Lines 19 20, IEI IEO.

Interrupt daisy chain for vectored interrupts. The IEI input of the highest priority device is held high, the IEO output of that device goes to the IEI input of the device with the second highest priority, the daisy chain is continued until the device with lowest priority is reached, its IEO is not connected. It is recommended that line 20 of the bus master is linked to line 19 of the adjacent card and so on down the bus. As the interrupt daisy chain does not involve the Z80 it is possible to move the bus master from slot to slot and vary the level of interrupt priority of the devices on the bus master. The DMA daisy chain however does involve the Z80, and the bus master must always be to one side of the expansion cards which may generate a /BUSRQ. If the motherboard is linked in the recommended manner the device with highest interrupt priority is nearest to the bus master. If the daisy chain is connected the other way arround a problem could arise as the Z80-DMA can also generate interrupts. For further details on connections see the section on daisy chains.

Line 21, /NMI.

A short pulse will be generated on this line by the bus master from a low on line 6 (/NMI SW). On Nascom 1 the NMI is used in the single step feature and is not available.

Line 22, /INT.
Used for the Z80 maskable interrupt. For full details see the book "Z80 family program interrupt structure" available from Zilog.

Line 23, /WAIT.
Used to insert wait states into Z80 machine cycles. Expansion cards that require wait states should provide them.

Line 24, /RFSH.
Used to control the refreshing of dynamic RAM. It should be noted that a refresh cycle is a memory cycle and designers should take appropriate steps. The I register contents will appear as the top eight bits on the address bus during a refresh cycle.

Line 25, /M1.
Z80 /M1 used to indicate an opcode fetch, also used (in conjunction with /IORQ) to indicate an interrupt acknowledge cycle.

Line 26, /IORQ.
Used to indicate a Z80 I/O cycle. The port address will be on the bottom eight address lines (A0 to A7). The top eight will have the contents of the A register on them. If /IORQ is asserted with /M1 it indicates an interrupt acknowledge cycle and the Z80 will expect to receive an interrupt vector.

Line 27, /MREQ.
Used to indicate a Z80 memory cycle.

Line 28, /WR.
Used to indicate a Z80 write cycle, asserted in conjunction with /IORQ or /MREQ.

Line 29, /RD.
Used to indicate a Z80 read cycle, asserted in conjunction with /IORQ or /MREQ. It should be noted that /RD is not asserted during an interrupt acknowledge.

Lines 30 to 45, A0 to A15.
Z80 address lines, should be tristated during a /BUSAK.

Lines 46,47,48, A16, A17, A18.
Optional implementation for extended addressing, should be tristated during a /BUSAK.

Line 49, GND.
An additional ground line to reduce system noise. Must be implemented on both the mother board and on expansion boards.

Lines 50 to 57, D0 to D7.
Z80 data lines, should be tristated during /BUSAK.

Line 58, RSFU.
This line is reserved for allocation at a later date. Please do not use.

Lines 59 60 61 62, INT 0 1 2 3.
Interrupt request lines, used to generate interrupt vectors from devices that are not capable of generating their own interrupts. These lines would be monitored by an interrupt controller which would be capable of generating interrupt vectors, the controller must be capable of being programed with the sense of a particular line (i.e. whether its active high or

active low) and the vector. A device unable to generate a vector would assert one of these lines when it required to interrupt, expansion cards availing themselves of this facility should provide it via links so that the particular line can be selected by the user.

Line 63, /PWRF.

Powerfail warning. This line is to be taken low 100mS before the power rails drop by more than 5% and held low until 100mS after the power on reset. For use by backup memory etc. An optional signal which would be provided by the power supply circuitry if implemented.

Line 64, AUX PWR.

An auxilary +5 volt supply for the use of backup devices. Absolute maximum current when the main power supplies are off is 100mA. Implementation is optional.

Lines 65 66, NDEF1 NDEF2.

Not to be defined. These are lines for users to allocate as they require, there are only two restrictions and one provision.

a)TTL levels only, ie no voltage greater than 5 volts and no voltage less than 0 volts.

b) No transition until 100nS after the previous transistion, ie don't put a 16MHz clock on this line.

c) A link must be provided to disable the use of NDEF 1,2.

Line 67, GND.

An additional ground line to separate the power lines from the rest of the bus.

Lines 68,69, -5 volt supply.

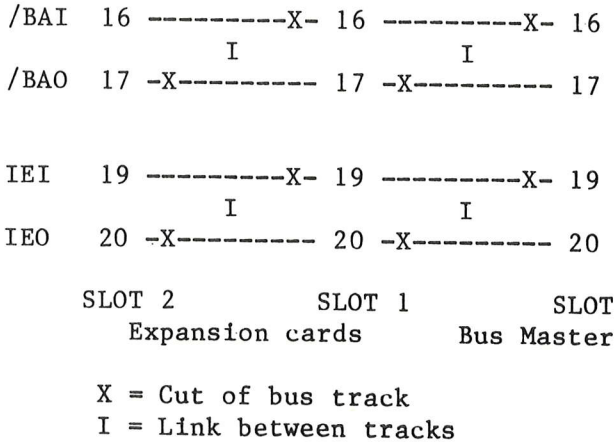
Lines 70,71, -12 volt supply.

Line 72, Keyway

Lines 73,74, +12 volt supply.

Lines 75,76,77,78, +5 volt supply.

Daisy chains



X = Cut of bus track
I = Link between tracks

active low) and the vector. A device unable to generate a vector would assert one of these lines when it required to interrupt, expansion cards availing themselves of this facility should provide it via links so that the particular line can be selected by the user.

Line 63, /PWRF.

Powerfail warning. This line is to be taken low 100mS before the power fails drop by more than 5% and held low until 100mS after the power on reset. For use by backup memory etc. An optional signal which would be provided by the power supply circuitry if implemented.

Line 64, AUX PWR.

An auxiliary +5 volt supply for the use of backup devices. Absolute maximum current when the main power supplies are off is 100mA. Implementation is optional.

Lines 65,66, NDEF1,NDEF2.

Not to be defined. These are lines for users to allocate as they require, there are only two restrictions and one provision.

a) The 1 veis only, ie no voltage greater than 5 volts and no voltage less than 0 volts.

b) No transition until 100nS after the previous transistion, ie don't put a 10MHz clock on this line.

c) A link must be provided to disable the use of NDEF 1,2.

Line 67, GND.

An additional ground line to separate the power lines from the rest of the bus.

Lines 68,69, -5 volt supply.

Lines 70,71, -12 volt supply.

Line 72, Reveal

Lines 73,74, +12 volt supply.

Lines 75,76,77,78, +5 volt supply.

Daisy chains

```
/BAI  16 ---------X- 16 ---------X- 16
                  I                I
/EAI  17 -X---------- 17 -X---------- 17

IEI   19 ---------X- 19 ---------X- 19
                  I                I
IEO   20 -X---------- 20 -X---------- 20

     SLOT 2        SLOT 1        SLOT 0
     Expansion cards        Bus Master

     X = Cut of bus track
     - Link between tracks
```

THE COPYING OF THIS DOCUMENT IS FORBIDDEN FOR ANY REASON WHATSOEVER WITHOUT WRITTEN CONSENT FROM GEMINI MICROCOMPUTERS LTD. 1981.

© COPYRIGHT GEMINI MICROCOMPUTERS LTD. 1981

Gemini Microcomputers

Oakfield Corner Sycamore Road Amersham Bucks HP6 5EQ