## Homework #3

Digital System Design 2022 Spring

DUE: 2022-04-09

- total 104 pts = maximum 100 pts + 4 bonus pts
- Extension limit = { png , jpg , heic , zip , pdf }
- ▲ You must hand your answer in at the board before due time (2022-04-09 11:59 PM KST).

The problems start from the next page.

## Name

72年2

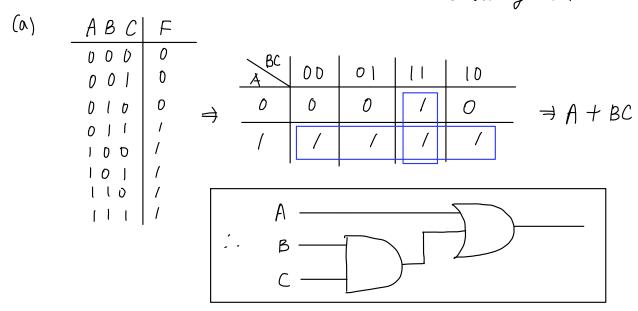
In Korean

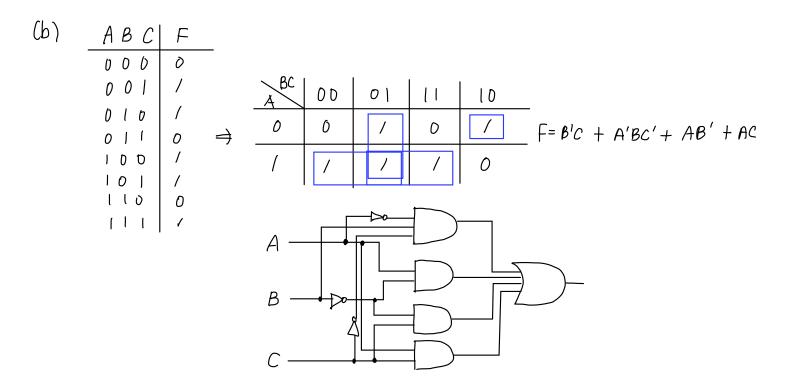
## **Student ID**

202/01/14

8 digits

- 1. Design a combinational circuit with three inputs and one output.
  - (a) The output is when the binary value of the inputs is more than 2. The output is 0 otherwise.
  - (b) The output is 1 when the binary value of the inputs is not divisible by 3.  $\Rightarrow$  divisible by 3  $\Rightarrow$  0.



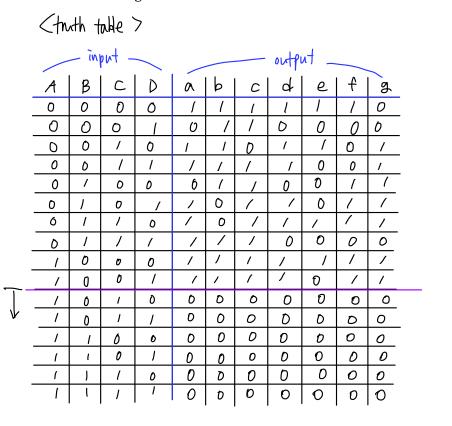


2. A BCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, g) select the corresponding segments in the display, as shown in Fig. 1. The numeric display chosen to represent the decimal digit is shown in Fig. 2. Using a truth table and Karnaugh maps, design the BCD-to-seven-segment decoder using a minimum number of gates. The six invalid combinations should result in a blank display.

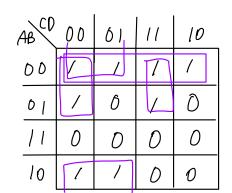


Fig. 1. Segment designation

Fig. 2. Numerical designation for display



@ output: b => A'B'+ B'c'+ A'c'p'+A'cp



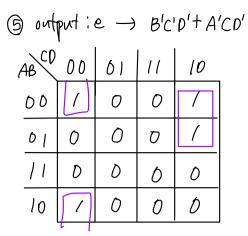
3 output : C = A'B+B'C'+A'D

QΟ	61	11	10
1	/	/	0
\	/	/	/
0	0	O	0
1	/	0	0
	00 /	00 61 / / / / 0 0	/ / / / / / 0 0 0

AB CD	00	61	11	10
00	1	D	/	7
01	0	/	D	/
11	0	0	٥	0
10	/	/	D	0

\_ @ output : d= AB'C'+A'BC'D+A'B'D' + A'B'C+ A'CD'

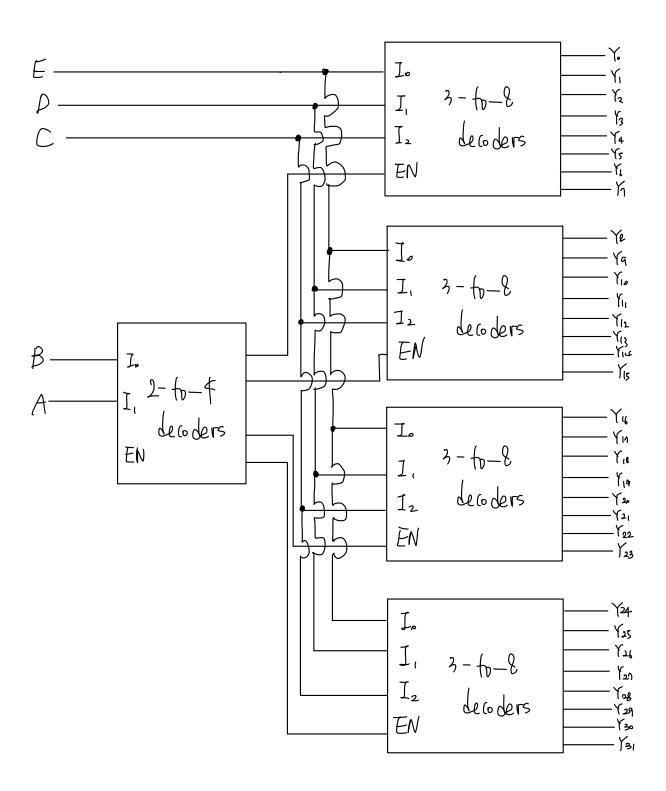
CSED273S2022\_hw3: page 3



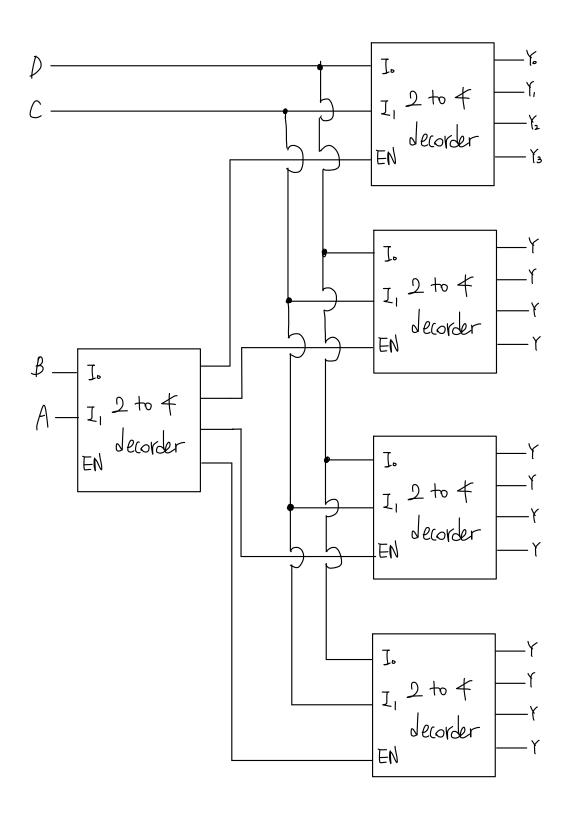
+ AB'CI

(2) output : g = A'B'C + A'CD' + A'BC' + AB'C' 61 11 DD Ô D D 

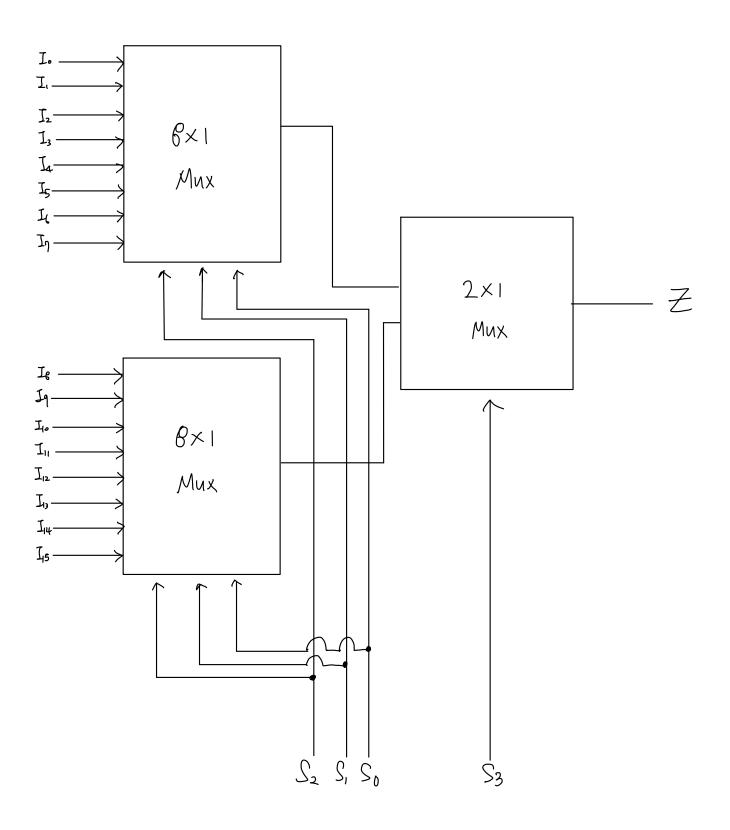
3. Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and 2-to-4-line decoder. Use block diagrams for the components.



4. Construct <u>a 4-to-16-line decode</u>r with <u>five 2-to-4-line decoders with enable.</u>



5. Construct a  $16 \times 1$  multiplexer with two  $8 \times 1$  and one  $2 \times 1$  multiplexers. Use block diagrams.



6. Implement the following Boolean function with a multiplexer:

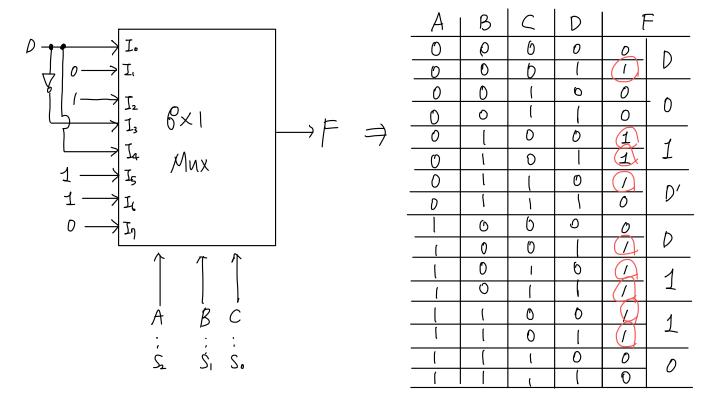
 $F(A, B, C, D) = \sum (0, 2, 5, 8, 10, 14)$ 

	Α	B	<u></u>	D	1	=	
•	O	0	Ø	G	1	D'	(A,B,C; control input D; data input.
	O	0	6	- 1	0	V	
	0	0	(	0	1		D: data Input.
	0	0	(	(	0	D'	
	0	[	0	Ø	0	D	
	0	١	D	l	1	D	
_	0	l	(	O	0	_	
	D	1	1	\	<i>D</i>	0	
	l	O	6	٥	1	N	
		0	O		0	D'	
	(	0	1	Ó	/	D'	
	[	0	1	-	0	V	_
	(	(	0	0	0	0	
	l	l	0	[	0		
		(	(	0	/	D'	
	(	1	(	(	0		-
		_				_	
<b>-</b>		$\longrightarrow$	I.				
<b>_</b>			I,				
		ı					
<b>†</b> [	_	1	12	2 / 1			
` `	о —	· K	I2 I3 6 I4	) ^ 1			$\longrightarrow$ $\vdash$
•	· · · · · · · · · · · · · · · · · · ·	<u> </u> } .	I4	χΛ <sub>ω</sub> ς			, ,
<u>_</u>			τ_ /	/~  V(X			

7. An  $8\times 1$  multiplexer has inputs A, B, and C/connected to the selection inputs  $S_2$ ,  $S_1$ , and  $S_0$ , respectively. The data inputs  $I_0$  through  $I_7$  are as follows:

$$I_1 = I_7 = 0$$
;  $I_2 = I_5 = I_6 = 1$ ;  $I_0 = I_4 = D$ ; and  $I_3 = D'$ .

Determine the Boolean function that the multiplexer implements

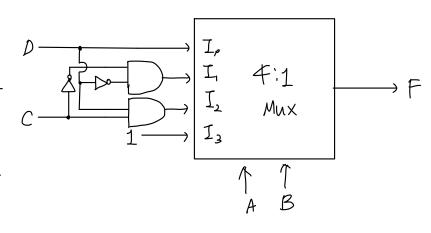


AB CD	00	61	11	10				
DD	0	1	0	0	⇒	F = C'D +	BC' + A'BD' + A'BD'	B'C
0 1	/	1	0	/				
11	/	/	0	0				
10	0	/	/	/				

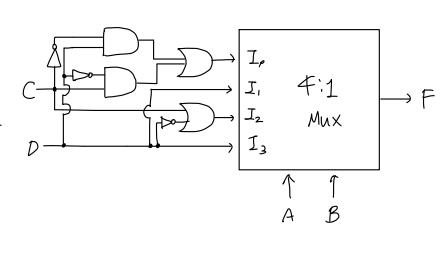
- 8. Implement the following Boolean function with a  $\underbrace{4\times1}$  multiplexer and external gates/
  - (a)  $F_1(A, B, C, D) = \sum (1, 3, 4, 11, 12, 13, 14, 15)$
  - (b)  $F_2(A, B, C, D) = \sum (1, 2, 5, 7, 8, 10, 11, 13, 15)$

Connect inputs A and B to the selection lines. The input requirements for the four data lines will be a function of variables C and D These values are obtained by expressing F as a function of C and D for each of the four cases when AB = 00, 01, 10, and 11. These functions may have to be implemented with external gates.

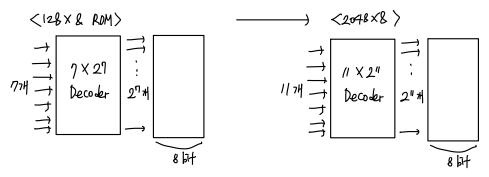
(a)	А	В	<u></u>	D	1	=
	0	0	Ó	0	0	
	0	0	b			D
	0	0	(	Q	0	
		0	(	(		
	0	l	0	O		
	0	١	0		0	C'D'
	0			0	0	
	D	1	1	\	Ď	
•		0	9	9	0	
	(	0	0		0	- 0
	(	0	1	0	0	CP
	(	0	1	-		
		(	0	0		
	(	(	0	l		1
	(	(	_	0	4	
	(	1	(			



(d)	А	B	<u></u>	D	[	=
	0	0	Ó	0	0	- 1-
	O	0	b			C'P + - CD'
	0	0	(	Q		- CD <sup>/</sup>
		0	(		0	
	0		0	O	0	
		l	O			^
	0	l		9	Ó	D
_	D	1	١	-	1	
		9	9	9	(1)	U,
	(	0	O		0	D' + C
	(	0	I	Ο.	4	Ċ
	(	0	1		(1)	
		(	0	0	0	
	[	(	0	l		n
	(	(	ſ	0	0	P
	1	1	(		(1)	



9. How many 128×8 ROM chips are required to construct 2048×8 ROM chip? What is additionally needed and why?



→ 2"+27 = 24 → 各1671年 12&8 ROM chipの1 型計다.

즉, 2<sup>7</sup>개의 output을 자분 decoder들이 (6개가 있다야 2048×8 ROM을 만들수 있어.

그리고, EN를 2절하다 Output 211 개를 구현하기 위해 또 다른 decoder을 취재되고 구현하다하다 한다.

4개의 input을 받아 (6개의 output을 싸움한다. 16개 decoder의 ENOTI 연결하고, 4 to 16 decoder을 한게 만들어줘야 한다.

:. 1674. 4 to 16 decoder

10. Tabulate the truth table for an  $16 \times 4$  ROM that implements the Boolean functions

$$A(w, x, y, z) = \Sigma(0, 2, 5, 7, 8, 14)$$

$$B(w, x, y, z) = \Sigma(3, 5, 7, 9, 11, 13, 15)$$

$$C(w, x, y, z) = \Sigma(0, 4, 8, 12)$$

$$D(w, x, y, z) = \Sigma(0, 1, 2, 4, 7, 9)$$

Consider now the ROM as a memory specify the memory contents at addresses 5 and 15.

W	×	क्	2	A	B	С	P	
0	0	D	0	/	D	/	/	
0	0	0	1	0	0	0	/	
0	0	/	0	1	Ō	0	/	
0	0	/	1	D	/	0	6	
0	/	0	0	0	0	/	/	
0	J	0	/	/	/	0	0	
6	1	-	0	D	б	0	0	
0	1	/	/	1	/	D	/	
1	0	0	0	/	O	_	0	
/	0	O	/	0	/	Ŋ	/	
	0	1	٥	0	O	0	0	
/	0	1	1	0	/	Ð	0	
	1	Ó	0	0	д	/	0	
	ı	0	J	0	/	0	0	
1	J	1	0	/	0	0	д	
1	l	1	1	0	/	Ð	0	

$$\begin{array}{c|c}
 & & & \\
 & \times & & \\
 & \times & & \\
 & & \downarrow & \\
 & \downarrow$$

address: memory contents - 5; 1100 -15; 0100