Homework #5

Digital System Design 2022 Spring

DUE : 2022-05-09

total 104 pts = maximum 100 pts + 4 bonus pts

Extension limit = { `png` , `jpg` , `heic` , `zip` , `pdf` }

You must hand your answer in at the board before due time (2022-05-09 11:00 AM KST).

The problems start from the next page.

Name

김 주 운

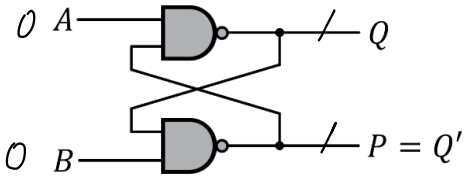
In Korean

Student ID

20210774

8 digits

1. A latch can be constructed from two NAND gates connected as follows:

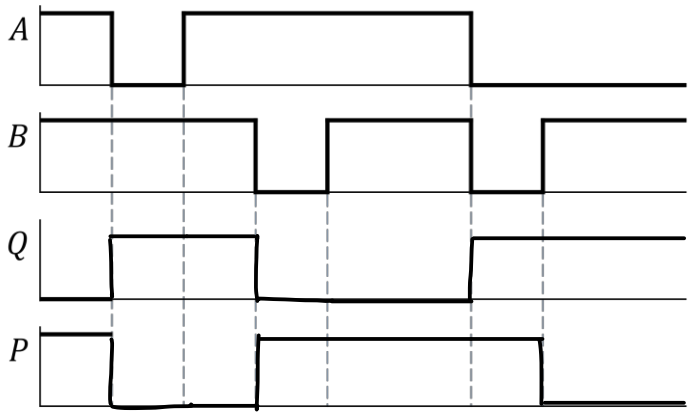


NAND
0 0 1
0 1 1
1 0 1
1 1 0

(a) What restriction must be placed on A and B so that P will always equal to Q'? (4pts)

(b) Derive the characteristic equation for the latch. (8pts)

(c) Complete the following timing diagram assuming no processing delay. (6pts)



(a) A와 B가 모두 0이면 안된다. 이를 식으로 표현하면 $\boxed{A+B=1}$ 이다.

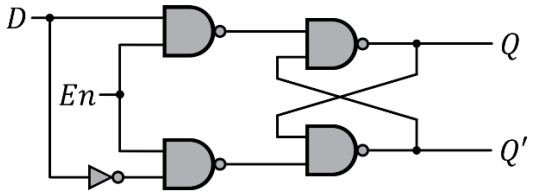
(b) Q^+ - <Table>

Q \ AB	00	01	11	10
0	X	1	0	0
1	X	1	1	0

$Q^+ = A' + QB \quad (A+B=1)$

(c) 위 그림에 답 표시.

2. The D latch of figure below is constructed with four NAND gates and an inverter. Consider the following three other ways for obtaining a D latch. In each case, draw the logic diagram and verify the circuit operation. (24pts = 8pts each)



(a) Logic diagram

En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

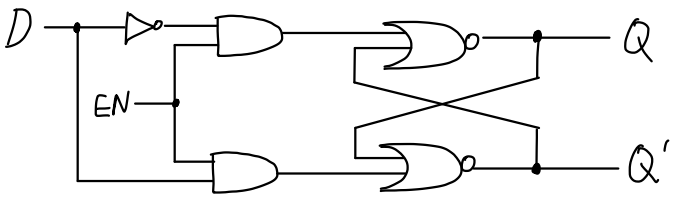
(b) Function table

(a) Use NOR gates for the SR latch part and AND gates for the other two. An inverter may be needed.

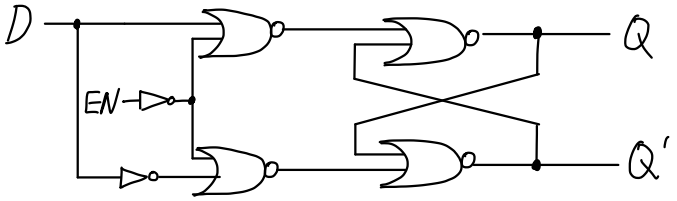
(b) Use NOR gates for all four gates. Inverters may be needed.

(c) Use four NAND gates only (without an inverter). This can be done by connecting the output of the upper gate in figure above (the gate that goes to the SR latch) to the input of the lower gate (instead of the inverter output).

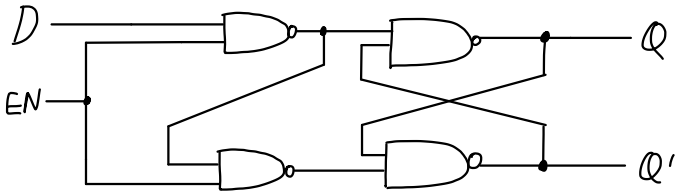
(a)



(b)



(c)



3. Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter. (8pts)

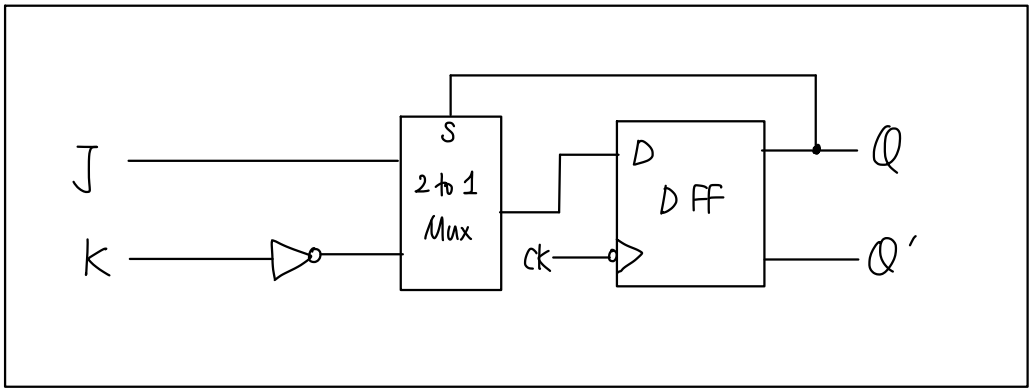
D	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

Q \ JK	00	01	11	10
0	0	0	1	1
1	1	0	0	1

$Q^+ = Q'J + QK' = D$

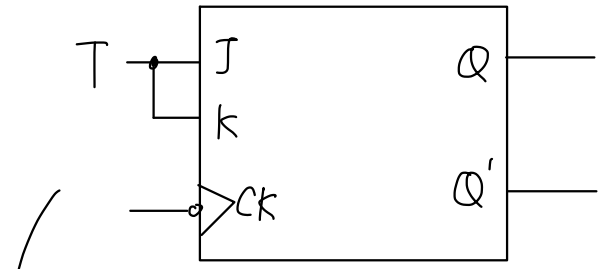
$Q'J + QK'$의 form이고, J와 K'에 Q와 Q'이 곱해졌으므로 Mux로 구현가능

Q가 selection의 값을 따라 J와 K' 중 하나를 output에 보내도록 함.



4. Show that the characteristic equation for the output of a T flip-flop is (6pts)

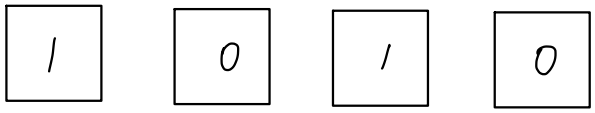
$$Q(t+1) = TQ' + T'Q$$



T Q	Q^+
0 0	0
0 1	1
1 0	1
1 1	0

$\Rightarrow$ $Q^+ = T'Q + TQ'$ //

5. The content of a four-bit register is initially the 4-bit word 1010. The register is shifted six times to the right with the serial input being 1011001. What is the content of the register after each shift? (8pts)

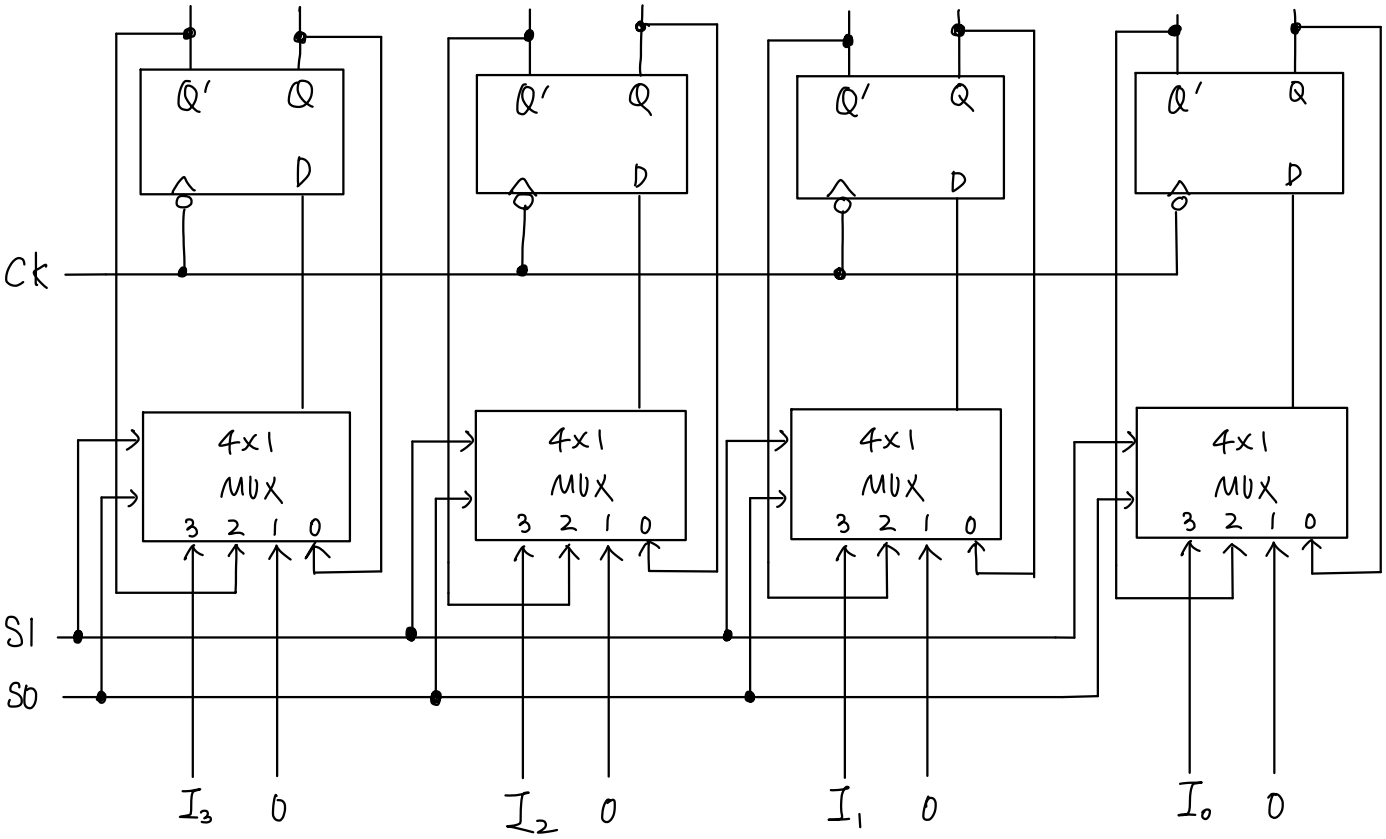


1011001 serial input

shift 1	1	1	0	1
shift 2	0	1	1	0
shift 3	0	0	1	1
shift 4	1	0	0	1
shift 5	1	1	0	0
shift 6	0	1	1	0

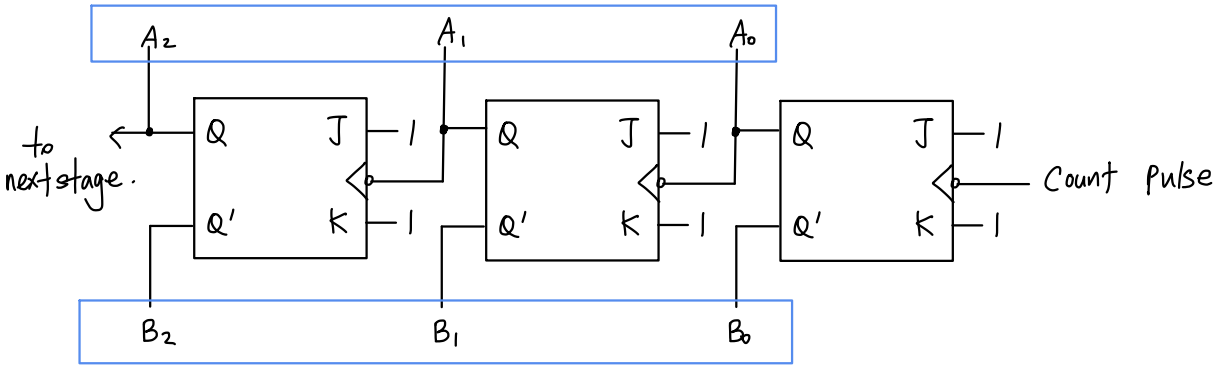
6. Draw the logic diagram of a four-bit register with four D flip-flops and four 4×1 multiplexers with mode selection inputs s_1 and s_0. The register operates according to the following function table. (8pts)

s_1	s_0	**Register Operation**
0	0	No change
1	0	Complement the four outputs
0	1	Clear register to 0 (synchronous with the clock)
1	1	Load parallel data



* $I_3, I_2, I_1, I_0 \Rightarrow$ parallel inputs

7. A binary ripple counter uses flip-flops that trigger on the negative-edge of the clock. What connections will you use to design: (8pts = 4pts each)
   (a) A count – up binary ripple counter; and
   (b) A count – down binary ripple counter?



(a) up-counter : $A_2 A_1 A_0$

(b) down-counter : $B_2 B_1 B_0$

8. How many flip-flops will be complemented in a 12-bit binary ripple counter to reach the next count after the following counts? (12pts = 4pts each)

(a) 110011011011
(b) 000000111111
(c) 111011111111

(a) 110011011011 → 110011011100 으로 바뀌므로

총 3개의 bit가 변하고, 3개의 flip-flop이 complement된다

∴ 3개

(b) 000000111111 → 000001000000 으로 바뀌므로

총 7개의 bit가 변하고, 7개의 flip-flop이 complement된다

∴ 7개

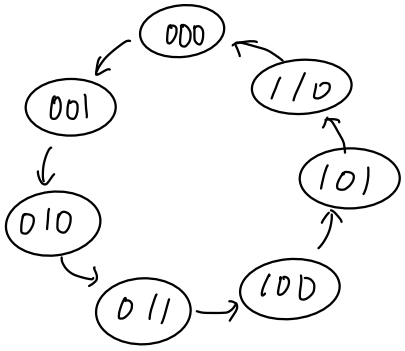
(c) 111011111111 → 111100000000 으로 바뀌므로

총 9개의 bit가 변하고, 9개의 flip-flop이 complement된다

∴ 9개

9. Using *JK* flip-flops:
   (a) Design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6. (8pts)
   (b) Draw the logic diagram of the counter. (4pts)

(a) state diagram ⟶ state transition table



Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

ABC	$A^+B^+C^+$	J_Ak_A	J_Bk_B	J_Ck_C
000	001	0X	0X	1X
001	010	0X	1X	X1
010	011	0X	X0	1X
011	100	1X	X1	X1
100	101	X0	0X	1X
101	110	X0	1X	X1
110	000	X1	X1	0X
111	---	XX	XX	XX

input equations

⟨J_A⟩ $J_A = BC$

A \ BC	00	01	11	10
0	0	0	1	0
1	X	X	X	X

⟨J_B⟩ $J_B = C$

A \ BC	00	01	11	10
0	0	1	X	X
1	0	1	X	X

⟨J_C⟩ $J_C = B' + A'$

A \ BC	00	01	11	10
0	1	X	X	1
1	1	X	X	0

⟨k_A⟩ $k_A = B$

A \ BC	00	01	11	10
0	X	X	X	X
1	0	0	X	1

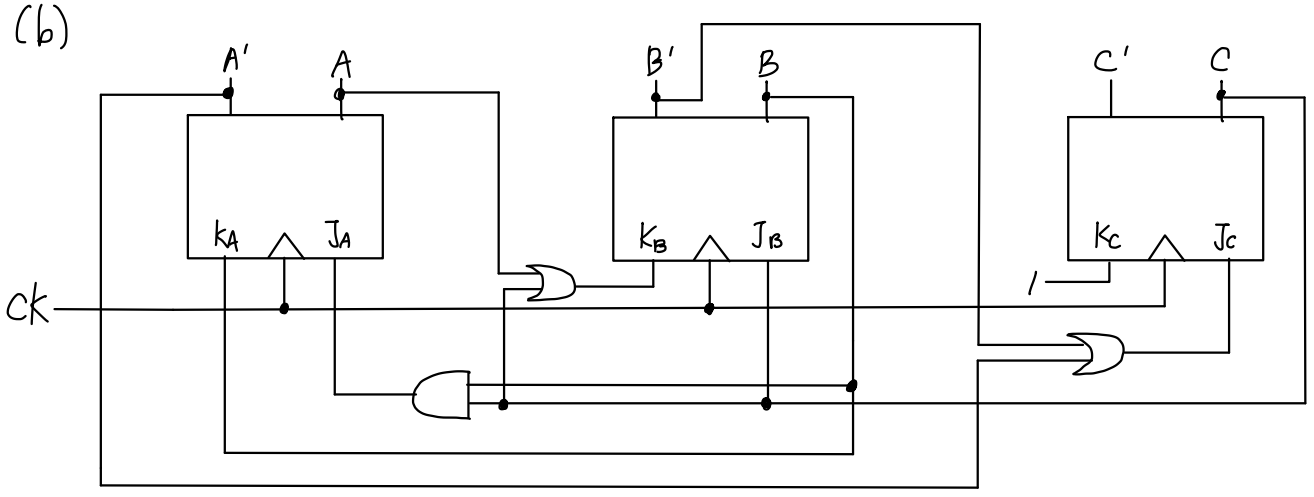
⟨k_B⟩ $k_B = C + A$

A \ BC	00	01	11	10
0	X	X	1	0
1	X	X	X	1

⟨k_C⟩ $k_C = 1$

A \ BC	00	01	11	10
0	X	1	1	X
1	X	1	X	X

(b)



End of the Homework #5