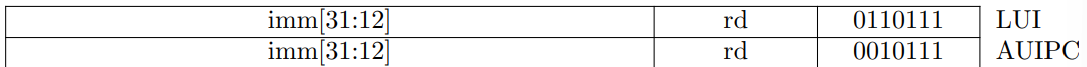
Page 116 for encodings

A white rectangular object with numbers

Description automatically generated



U-type

LUI

Loads the upper immediate into the top 20 bits of the destination register, setting the lower bits to zero.

AUIPC

Creates an offset with the upper immediate, setting lower bits to zero. Adds the offset to PC and places the result in the destination register.

A number in a line

Description automatically generated



UJ-type

JAL

Save PC+4 to destination register. Sign extend J-immediate, imm[0] is 0, add to PC.

A close-up of a number

Description automatically generated



I-type

JALR

Save PC+4 to destination register. Add 12-bit signed immediate to rs1, then set lsb to 0. Write the address to PC.

A close-up of a number

Description automatically generated

A table with numbers and letters

Description automatically generated

SB-type

12-bit signed immediate added to current PC. Imm[0] is 0.

BEQ

Branch if rs1 is equal to rs2

BNE

Branch if rs1 is not equal to rs2

BLT/BLTU

Branch if rs1 is less than rs2, using signed/unsigned comparison

BGE/BGEU

Branch if rs1 is greater than or equal to rs2, using signed/unsigned comparison

A white background with black text

Description automatically generated

A table with numbers and letters

Description automatically generated

I-type, S-type

LB/LH/LW

Address is signed 12-bit immediate added to rs1. Memory content is signed extended and loaded into destination address.

LBU/LHU

Address is signed 12-bit immediate added to rs1. Memory content is zero-extended and loaded into destination address.

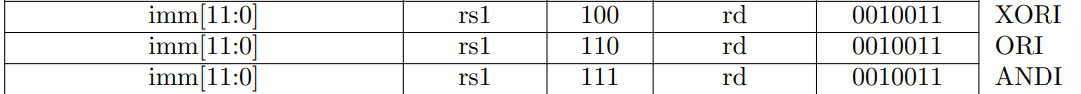
SB/SH/SW

Address is signed 12-bit immediate added to rs1. The lower bits of rs2 (if not word) are stored at the memory address.

A close-up of a number

Description automatically generated





I-type

ADDI

Add sign-extended 12-bit immediate to rs1. Arithmetic overflow is not handled. Store results in destination register.

SLTI (set less than immediate)

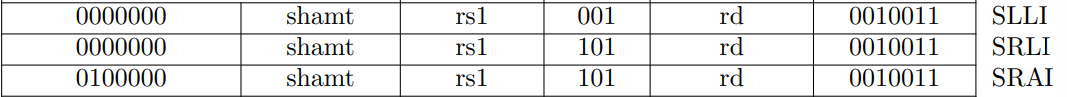
Set destination register to 1 if rs1 is less than signed-extended immediate when both are treated as signed numbers. Else write 0 to rd.

XORI/ORI/ANDI (bitwise op, immediate)

Sign-extend the 12-bit immediate. Perform bitwise XOR/OR/AND on rs1 and store the results in the destination register.

A screenshot of a computer

Description automatically generated



Special I-type

Shift amount is encoded in the lower bits of immediate. Upper bits of immediate determine arithmetic-ness.

SLLI (logical left shift)

Shift rs1 by SHAMT and write to destination register. Shift in zeros.

SRLI (logical right shift)

Shift rs1 by SHAMT and write to destination register. Shift in zeros.

SRAI (arithmetic right shift)

Shift rs1 by SHAMT and write to destination register. Sign extend.

A screenshot of a computer

Description automatically generated

A table with numbers and letters

Description automatically generated

R-type

ADD/SUB

Performs rs1 + rs2 or rs1 – rs2 and writes to destination register. Overflow is ignored.

SLT/SLTU (set less than)

Set destination register to 1 if rs1 < rs2, 0 otherwise, for signed and unsigned comparisons.

SLL/SRL/SRA

Shifts rs1 by lower 5 bits of rs2. Logical left, logical right, or arithmetic right.

XOR/OR/AND

Bitwise logical operations on rs1 and rs2, write result to destination register.