# A MICROPOWER ANALOG HEARING AID ON LOW VOLTAGE CMOS DIGITAL PROCESS


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## ABSTRACT

*A two-chip analog micropower hearing aid circuit is developed which is based on a low voltage three micron CMOS process. The novel features of the circuit are the use of adaptive biasing of MOS Translinear Loop ( MTL ) circuit and an innovative application of an adaptive technique in reducing the value of a degenerating linearising resistor in the input differential stage of the AGC block. The above two measures enable reduction of power consumption and external component count. Class-D amplifier provides high conversion efficiency at the output stage. The proposed configuration is now under integration for developing a one chip general purpose CMOS analog hearing aid with capability to operate with 1.0 volt supply voltage.*


## INTRODUCTION :

Micropower analog CMOS integrated circuits offer an attractive potential for the development of digitally programmable analog hearing aids [1] .Though majority of hearing aids are matured on BJT technology there is a considerable interest in developing CMOS option because of inherent advantages in realization of low power digital control circuits [4] . The key technological consideration in the design of CMOS technology based hearing aids is the realization of the MOS analog circuits operating within prescribed process corners and low battery voltage range of 1.5 V to 1.0 V.

Recently, a four-chip hearing aid based on CMOS technology is reported which is electrically programmable [2]. It is projected that a general purpose, non-programmable and low cost micropower CMOS hearing aid with high reliability offers an attractive developmental challenge.

The present paper reports the successful realisation of a micropower two-chip hearing aid using a low voltage 3micron CMOS process standardised for digital circuits.

## ARCHITECTURE:

The architecture of the hearing aid circuit is shown schematically in fig1, which consists of the following generic building blocks.

1. A low noise preamplifier stage with a differential input and single ended output interfacing the microphone.
2. An adaptively biased variable gain amplifier with MOS

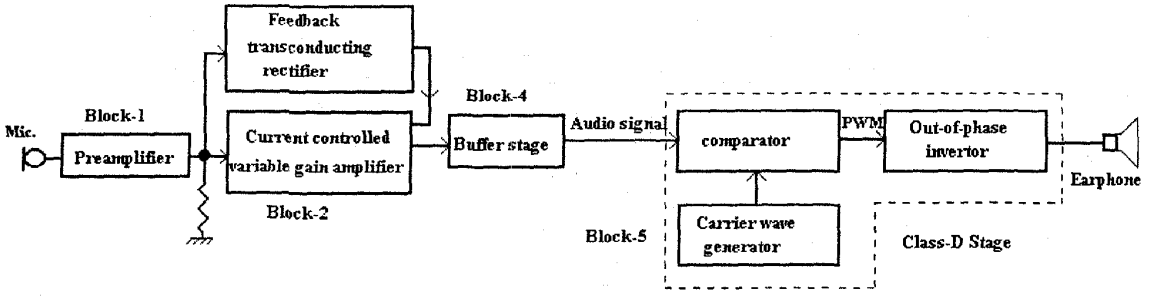


**Fig. 1 Block diagram of the hearing aid**



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translinear loops to control the gain through current sources.

3. An AGC block with transconducting feedback loop in combination with a current controlled variable gain amplifier .

4. A buffer stage offering isolation between the amplifier and the output stage .

5. A class - D amplifier comprising of a sawtooth carrier wave generator and a comparator providing the pulse width modulation (PWM) capability followed by a chain of inverters with earphone connected across out-of-phase PWM signals.

The quiescent current consumption of the complete hearing aid circuit including supporting biasing sources is about 0.6 mA.

In the following section, a brief description of automatic gain control, class-D output and the preamplifier stage is given as these blocks are considered to be the most critical in determining the hearing aid performance.

## ADAPTIVELY BIASED AUTOMATIC GAIN CONTROL BLOCK

An automatic gain control ( AGC ) circuit is considered to be an indispensible building block of any high performance hearing aid system.

Fig. 2 portrays the various functional components in the AGC stage.

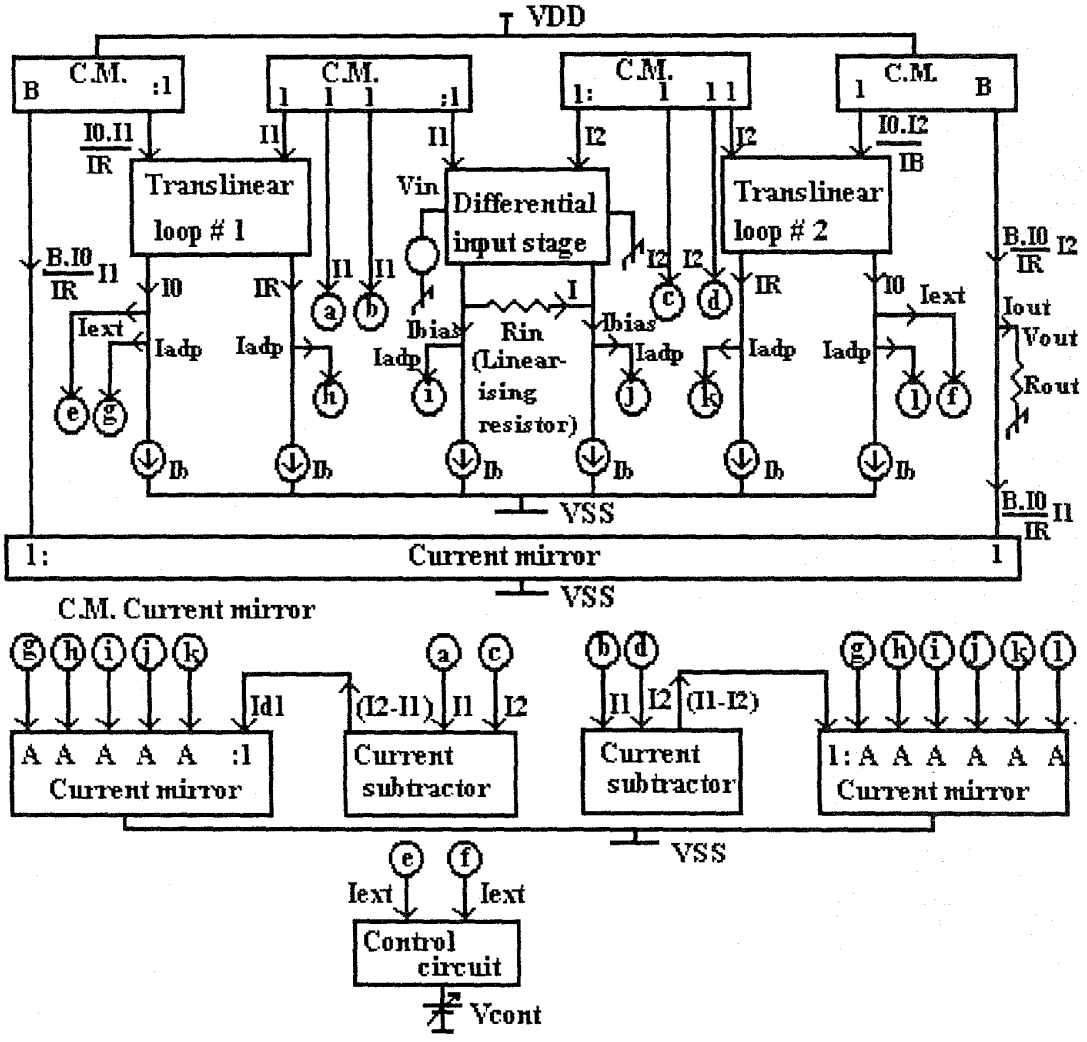


Fig. 2 Block diagram of an adaptively biased CMOS VGA

The AGC stage consists of : (a) The differential input stage with a degenerating linearising resistor to enhance the range of input linearity [6]. (b) two MOS translinear loops ( MTL ), current subtractor and current mirror circuits. For Vin < 0 ( $I_{d1} = I_2 - I_1$; $I_{d2}=0$ ), for Vin>0 ( $I_{d2} = I_1 - I_2$; $I_{d1}=0$). $I_{d1}$ and $I_{d2}$ are added to the biasing sources $I_b$ at nodes ( g - l ) through current mirrors with an amplifying factor A. As can be seen that the adaptive current $I_{adp}$, which is signal dependent, is available at i and j nodes. The multiplying factors A and B of current mirrors are the design parameters optimised. (c) The feedback loop ( shown in fig. 1 ) which comprises of a transconducter rectifier which adds rectified current to $I_R$ in translinear loops in proportion to the amplitude of the input signal.

It may be mentioned that the adaptive biasing of the MTL loop has been experimented for the first time to the best of our knowledge providing advantage in reducing the budget of power consumption in the circuit. The basic MOS translinear loop schematic is shown in fig 3.

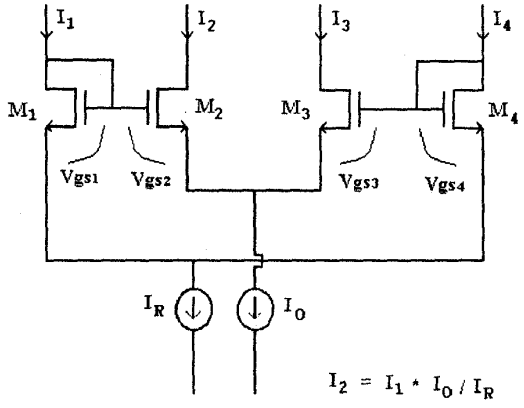


Fig. 3 MOS Translinear Loop

## CLASS-D AMPLIFIER

In the conventional power amplifiers the limitations are due to efficiency, power dissipation and stability of biasing point. These limitations can be avoided by using a Class - D amplifier which has theoretically 100% efficiency and has low power dissipation.[7,8,9].

The present class-D amplifier used is based on pulse width modulation. The pulse width of the output signal is made proportional to the amplitude of modulating signal. The signal at the output is recovered from PWM signal by passing it through a lowpass filter, which in the present case, happens to be the earphone.

The basic building blocks of a class-D amplifier are :

(1) A waveform generator,
(2) A comparator ,and
(3) An output stage with earphone as a floating load in a differential configuration.

The waveform generator consists of a schmitt trigger and a current switch as shown in fig. 4 . These are connected to form a close loop as illustrated. The schmitt trigger generates a square wave of 32 KHz which is fed as an input to the current switch which, in turn, produces a triangular waveform across the output capacitor serving as a carrier signal.

The comparator compares the audio signal and the carrier waveform to produce a Pulse Width Modulated (PWM) signal. The output stage then amplifies the PWM signal and applies it to the load ( Earphone ). The average current flowing through the load gives the amplified signal. When there is no signal we get at the output of the comparator a square wave of 50% duty cycle. So the average output voltage is zero and quiescent power dissipation is ideally zero. The output transistors are designed to drive low impedence earphones.

## PREAMPLIFIER

The special feature of the preamplifier design lies in splitting the gate electrode of large area MOS transistor into strips to reduce noise due to the reduction of poly gate resistance.. The input transistors are laidout in common centroid geometry to reduce offest. The input devices operate in the subthreshold region to give best I/gm ratio [10].

## SYSTEM SIMULATION

The building blocks were configured to realise a two chip version of a hearing aid. A system simulation was carried out before subjecting the design for prototyping . It may be mentioned that while individual analog blocks could be simulated by SPICE at the gate level there are two

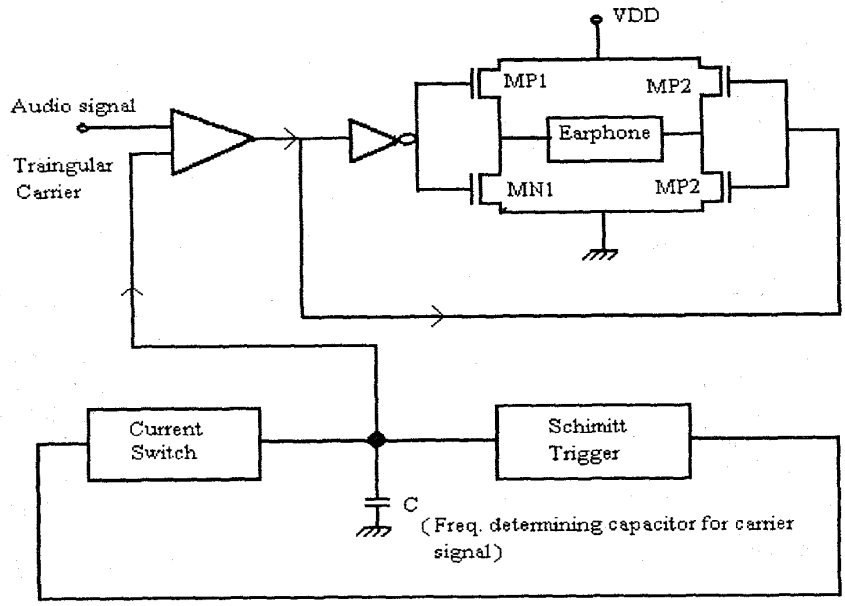


**Fig. 4 Block diagram of class D amplifier**

general difficulties encountered while attempting system level simulation of the complete hearing aid. The difficulties are :

(a) Because of large device count and operation of the individual blocks in mixed subthreshold - strong threshold region of operation there was serious convergence problem.

(b) Both electroacoustic transducers at the input and output stage, namely , the microphone and the earphone, are not directly compatible to SPICE level simulation [3].

The problems were circumvented by adopting behavioral level simulation of the building blocks and developing appropriate RLC equivalent circuit of the electroacoustic transducers [1].

It was possible to simulate the entire hearing aid system on PSPICE including microphone , preamplifier, automatic gain control and output stage including earphone. The simulation provides the design guidelines for the optimised performance of the system such as setting for gain control, linearity, output power level etc. and shaping of frequency response of the hearing aid. In other words, with the basic CMOS building blocks a computer aided hearing aid system could be realised at the simulation level.

Table I provides some information on the complexity of the building blocks of hearing aid system and power consumption of various blocks.

## CONCLUSIONS :

A micropower general purpose hearing aid circuit is reported which has the following novel features.

(a) A low voltage digital CMOS process has been used to realise a micropower hearing aid with several of MOS transistors operating in the subthreshold region. The design was first simulated within the process corners which demanded critical optimisation of device sizing.

(b) The novel feature of the critical block - variable gain stage - lies in using an adaptive biasing to realise higher degree of input linearity wtihout the use of large value of resistor resulting in integration of degenerating linearising resistor on silicon. Adaptive biasing of MTL loop provides additional bonus in economising budget of power consumption.

(c) The class - D amplifier uses an integrated sawtooth generating circuit and a comparator which eliminate the use of passive components and yet provides a compact structure for pulse width modulation.

(d) The building blocks are generic to be useful for the development of digitally programmable analog hearing aids.

(e) The hearing aid has been found to perform satisfactorily under a supply voltage degradation from 1.5 to 1.1 volts.

## TABLE -I

| | BLOCKS | DEVICE COUNT | POWER CONSUMPTION ( μW ) |
|---|---|---|---|
| 1. | Preamplifier | 12 | 80 |
| 2. | Variable gain amplifier with MTL loops | 59 | 20 |
| 3. | Buffer amplifier | 19 | 200 |
| 4. | Operational transconductance rectifier | 20 | 10 |
| 6. | Class-D amplifier | 41 | 170 |
| 7. | Voltage doubler | 14 | 250 |

(f) The successful performance of the micropower CMOS building blocks leading to two-chip hearing aid is now being configured for a single chip version in the near future.
(g) Some of the blocks developed are attractive for applications in other biomedical electronic systems and portable/pocket micropower electronics.

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