OPCODE	u-ins	STEPS
NOP	NOP	no operation
FETCH	FETCH_1	AR <- PC , Read
	FETCH_2	DR <- M , PC <- PC + 1
	FETCH_3	IR <- DR , AR <- PC , Read
LDAC	LDAC_1	DR <- M , PC <- PC + 1
	LDAC_2	TR <- DR , AR <- PC , Read
	LDAC_3	DR <- M , PC <- PC + 1
	LDAC_4	AR <- DRTR , Read
	LDAC_5	DR <- M
	LDAC_6	AC <- DR
STAC	STAC_1	DR <- M , PC <- PC + 1
	STAC_2	TR <- DR , AR <- PC , Read
	STAC_3	DR <- M , PC <- PC + 1
	STAC_4	AR <- DRTR , Read
	STAC_5	DRTR <- AC , Write
	STAC_6	AR <- AR +1
	STAC_7	DR <- TR , Write
CLAC	CLAC	AC <- 0, Z <- 0
JUMP	JUMP_1	DR <- M , PC <- PC + 1
	JUMP_2	TR <- DR , AR <- PC , Read
	JUMP_3	DR <- M , PC <- PC + 1

	JUMP_4	PC <- DRTR , Read
JUMPZ	JUMPZY_1 JUMPZY_2 JUMPZY_3 JUMPZY_4 JUMPZN_1 JUMPZN_2	DR <- M , PC <- PC + 1 TR <- DR , AR <- PC , Read DR <- M , PC <- PC + 1 PC <- DRTR , Read PC <- PC + 1 PC <- PC + 1
MULTWO	MULTWO_1 MULTWO_2	ALU_op <- 110 AC <- AC * 2
INC	INC_1 INC_2	DR <- M , PC <- PC + 1 INC_sel <- DR[3:0] R[R1] <- R[R1] + 1
ADD	ADD_1 ADD_2 ADD_3	DR <- M ; PC <- PC + 1 WTA_sel <- DR[4:0] AC <- AC + R[R1]
MUL	MUL_1 MUL_2 MUL_3	DR <- M ; PC <- PC + 1 WTA_sel <- DR[4:0] AC <- AC * R[R1]
XOR	XOR_1 XOR_2 XOR_3	DR <- M ; PC <- PC + 1 WTA_sel <- DR[4:0] AC <- AC (+) R[R1], if AC=0 set Z=1
MOVEAC	MOVEAC_1 MOVEAC_2	DR <- M ; PC <- PC + 1 WTR_sel <- DR[4:0] , A bus <- AC

MOVETOAC	MOVETOAC_1 MOVETOAC_2	DR <- M ; PC <- PC + 1 WTA_sel <- DR[4:0] , AC <- R[R1]
RESET	RESET_1 RESET_2	DR <- M , PC <- PC + 1 RESET_sel <- DR[3:0] R[R1] <- 0
DIV	DIV_1 DIV_2 DIV_3	DR <- M ; PC <- PC + 1 WTA_sel <- DR[4:0] AC <- AC / R[R1], if AC=0 set Z=1
MOD	MOD_1 MOD_2 MOD_3	DR <- M ; PC <- PC + 1 WTA_sel <- DR[4:0] AC <- AC % R[R1]