

RISC-V: A Didactic Platform

Documentation

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1 Introduction

This document describes the RV32IM processor and its architecture. I've tried to make it as clear as possible such that everyone with a basic knowledge of computer architecture can understand it. It will describe each significant module of the processor, what it does and what are the different inputs and outputs with an image of the module. It is recommended to follow this document with the source code of the processor, which is available in the Verilog folder of the project. Don't hesitate to use the table of contents to navigate through the different parts of the document. If you see any mistake or are confused by something don't hesitate to contact me at the mail address jules.perrin@epfl.ch.

2 Fetch

2.1 IF Stage

The IF stage is responsible for fetching the next instruction from the ROM and passing it to the ID stage. The IF stage contains two different modules: the PC and the branch predictor.