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Bachelor Project
Summer 2023

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

RISC-V : A Didactic Platform

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Introduction

This project, RISC-V: A Didactic Platform, embarks on the pursuit of simplifying complex computer architecture concepts, targeting both an academic audience who is striving to comprehend the intricate world of processor design. It specifically focuses on the creation of a RV32I processor in Verilog, based on the RISC-V instruction set architecture.

Goals

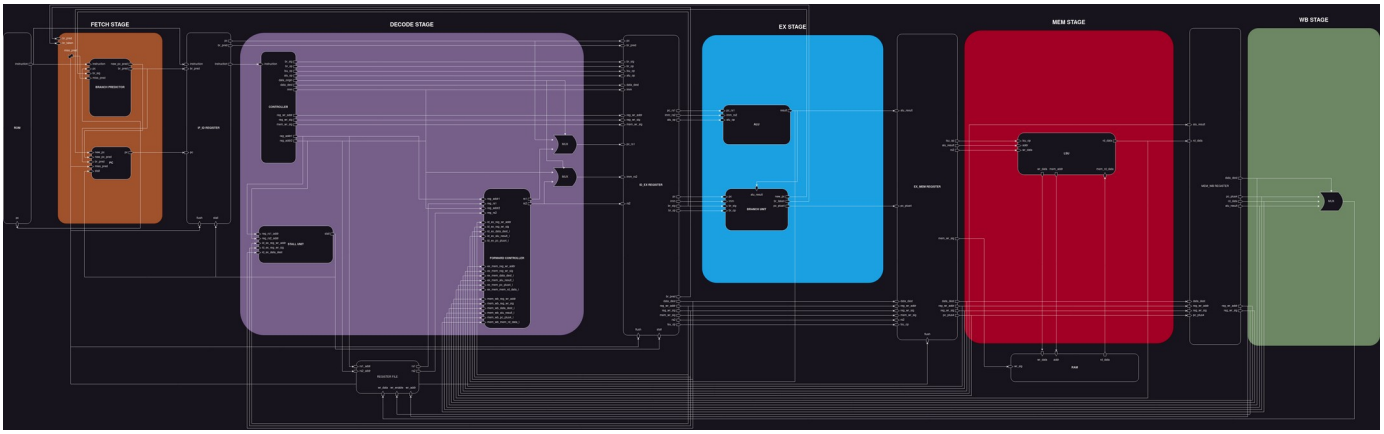
- Creating a RV32I unpipelined CPU
- Creating a RV32I pipelined in 5 stages CPU
- Chose how to resolve the different issues due to pipelining the processor, mainly data dependency and branch prediction.
- The CPU should work on Icarus Verilog.
- Add extensive testing to the main modules of the processor.
- Add an easy way for the user to use and create programs for the finished processors.
- Document everything such that the project could be use in an academic way and also such that someone could easily add things on it.

Add some extensions to the architecture, mainly the M extension.

Summary

Everything has be done, the main focus of course has been made on the pipelined version of the CPU.
So to enumerate on everything that has been done:

- *Unpipelined version of a RV32IM CPU, untouched since half of the project so may contains some errors*
- *A Pipelined version of a RV32IM CPU*
- *Chose to go with forwarding path and branch prediction algorithm to resolve the issues introduce by pipelining the processor.*
- *The CPU is working on Icarus Verilog and Quartus Modelsim in any mode.*
- *Tested most of the important modules*
- *Added a way to compile C programs into a .hex file that can be used to put inside the ROM and also to see what the assembly program looks like to better understand how RISC-V assembly works.*
- *Creating a pretty detail documentation document, telling the user what are the different input/output and what they do and the general purpose of the different modules and stages.*



Future considerations

Here are the different ways the project could be even better :

- *Add more extensions from the RV32I specs to the processor*
- *Add more tests to the existing RV32IM pipelined processor since I think I could have tested more corner cases or things like that*
- *Maybe implement caches*
- *Implement a multi-processor architecture*
- *Implement instruction reordering*
- *Create a simple program to execute on the FPGA board for maybe a more interactive experience.*