

RISC-V: A Didactic Platform

Documentation

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1 Introduction

This document describes the RV32IM processor and its architecture. I've tried to make it as clear as possible such that everyone with a basic knowledge of computer architecture can understand it. It will describe each significant module of the processor, what it does and what are the different inputs and outputs with an image of the module. To avoid repeating too much the signal, I will only list the signals directly linked to the module, that's why most of the stages don't have any signals listed because it's their inside modules that are using them and will be listed here instead.

It is recommended to follow this document with the source code of the processor, which is available in the Verilog folder of the project. Don't hesitate to use the table of contents to navigate through the different parts of the document. If you see any mistake or are confused by something don't hesitate to contact me at the mail address jules.perrin@epfl.ch.

2 Fetch

2.1 IF Stage

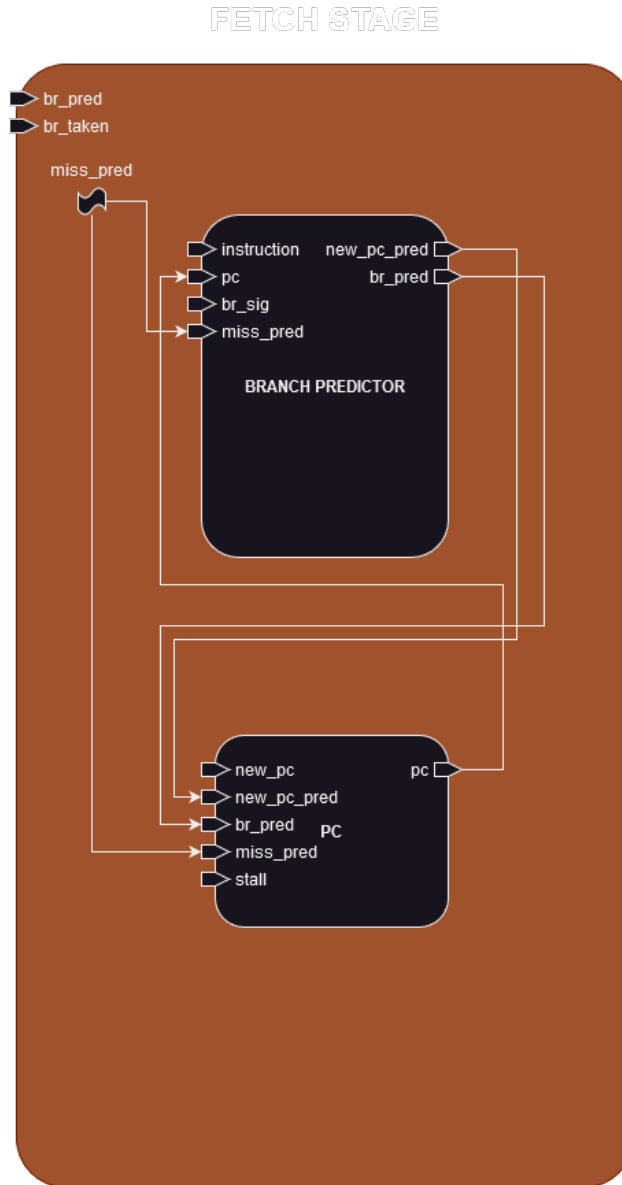


Figure 1: Diagram of the IF Stage

The IF stage is responsible for fetching the next instruction from the ROM and passing it to the ID stage. The IF stage contains two different modules: the PC and the branch predictor. The IF stage is the only stage that computes a value outside of a value, it uses the *br_pred* signal and the *br_taken* signal to compute if there is a miss prediction such that the PC and the branch predictor can be updated accordingly.

Signals:

1. Input: *br_pred*, This signal is representing the state of the prediction made by the branch predictor in the EX stage.
2. Input: *br_taken*, This signal is representing the state of the branch in the EX stage.
3. Output: *miss_pred*, This signal is representing if there is a miss prediction or not.

2.2 Branch Predictor

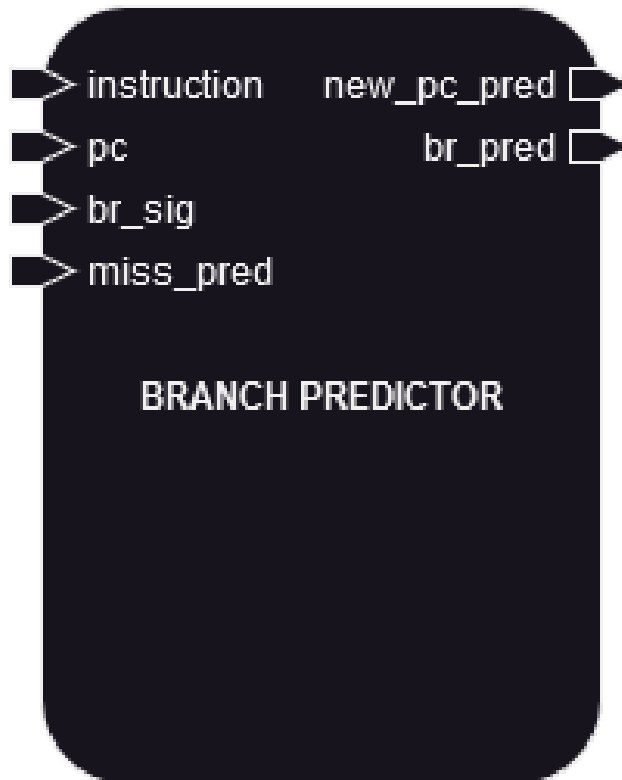


Figure 2: Diagram of the Branch Predictor

The branch predictor as its name suggests is responsible for predicting if the branch will be taken or not. The algorithm that is being used is the two-level adaptive branch predictor, which I will not describe in detail but reuse the idea of a 2-bit saturating counter but apply a bit of the notion of locality and pattern recognition. Of course, the algorithm could be improved or replaced by any other algorithm and it is up to the user to do it if he wants to. It works at the beginning by doing a simple matching on the current instruction to see if it is a branch instruction. If that's the case we look if it is a conditional branch or not, if it is not we simply predict that the branch will be taken for the JAL instruction, but the JALR one will be always predicted as not taken for data dependency reasons. If it is a conditional branch we simply use the algorithm described above to predict if the branch will be taken or not. The algorithm updates the prediction depending on the actual result of the branch

that is represented by the *miss_pred* signal. If the prediction is taken, we compute the next PC

Signals:

1. Input: *instruction*, This signal is representing the current instruction that is being fetched.
2. Input: *pc*, This signal is representing the current PC.
3. Input: *br_sig* This signal is representing the state of the current instruction in the EX stage. It is used to know if the instruction is a branch or not. such that it updates only the algorithm when it is a branch instruction.
4. Input: *miss_pred*, This signal is representing the state of the prediction made by the branch predictor in the EX stage.
5. Output: *new_pc_pred*, This signal is representing the next PC that will be used if the prediction is taken.
6. Output: *br_pred*, This signal is indicating if the branch is predicted as taken or not.

2.3 PC

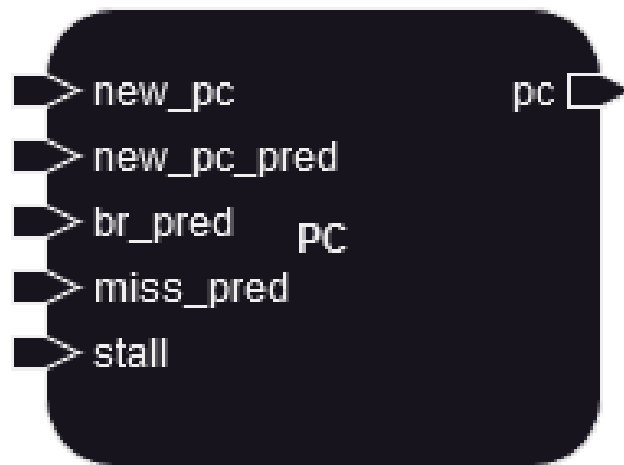


Figure 3: Diagram of the PC

The PC is responsible for computing the next PC. It uses the different input signals to know which PC to compute. for example, if it is a branch, the branch predictor will tell him what to do, and if the branch predictor is wrong it will be updated accordingly. If it is a more classic instruction such as an ADD, it will simply increment the PC by 4 etc.

Signals:

1. Input: *new_pc*, This signal represent the next PC given by the branch unit in the EX stage.
2. Input: *new_pc_pred*, This signal represent the next PC given by the branch predictor.
3. Input: *br_pred*, This signal is representing the state of the prediction made by the branch predictor in the EX stage.
4. Input: *miss_pred*, This signal is representing if there is a miss prediction or not.
5. Input: *stall*, This signal is representing if the pipeline is stalled or not due to a data dependency in the ID stage.
6. Output: *pc*, This signal is representing the current PC.

3 Decode

3.1 ID Stage

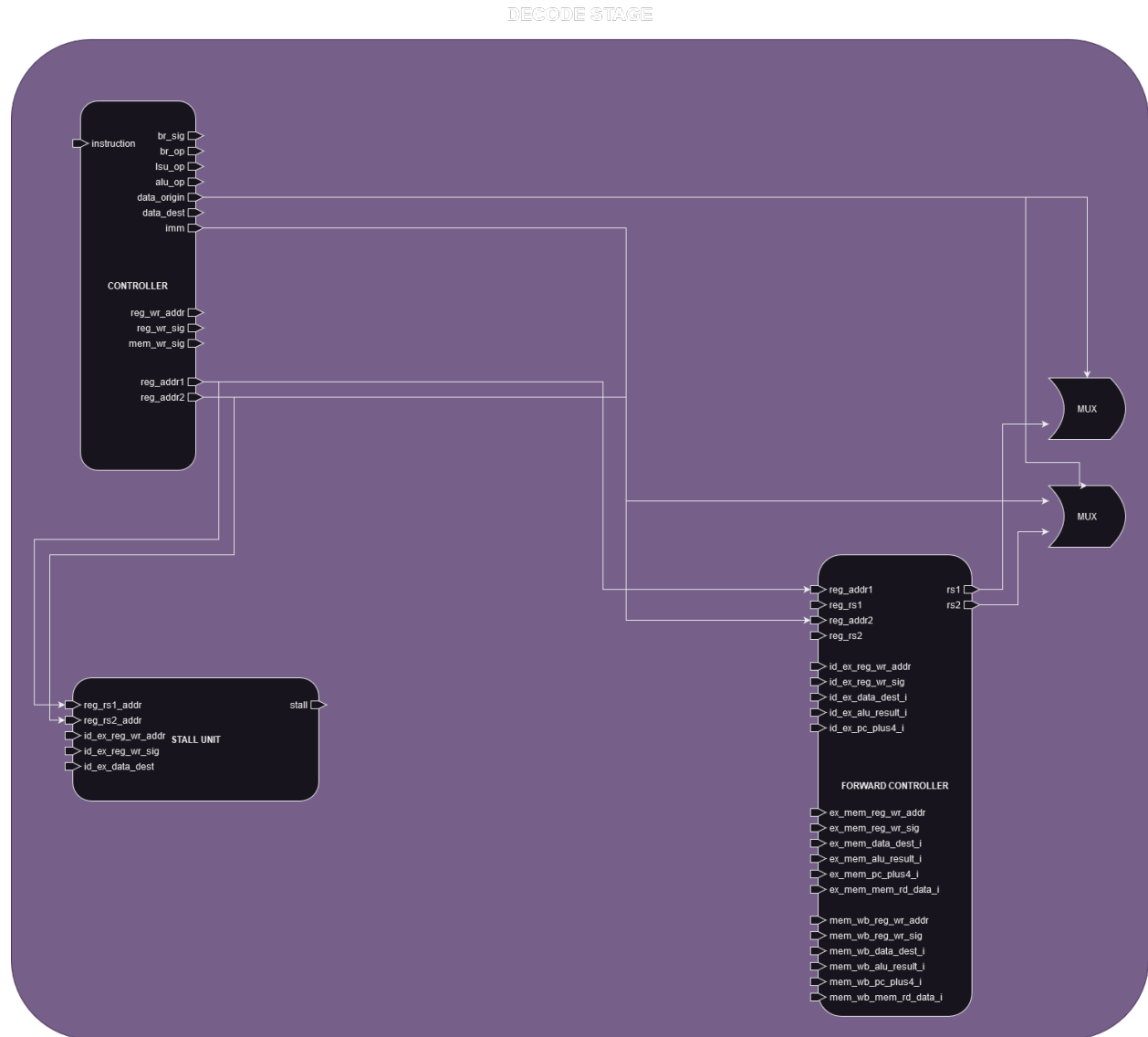


Figure 4: Diagram of the ID stage

The ID stage is the second stage of the pipeline. It is responsible for decoding the instruction and forwarding the data to the next stage. It is composed of the following modules: the controller which is the main module of the stage, the stall unit, the forward controller and 2 smaller modules which are 2 muxes used to select between the different registers and the immediate value or the pc.

3.2 Controller

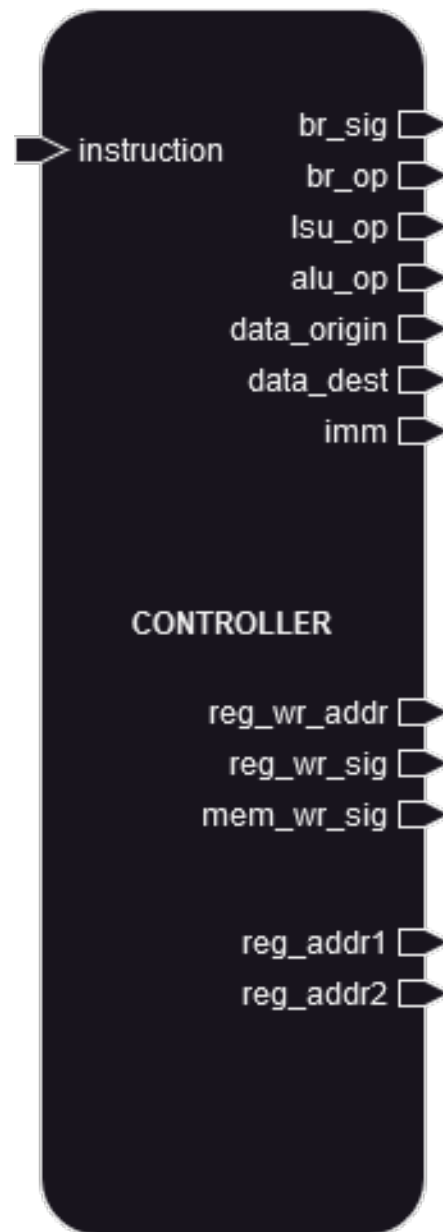


Figure 5: Diagram of the Controller

The controller is the main module of the ID stage. It is responsible for decoding the current instruction which is the action of extracting the different fields of the instruction and forwarding them to the next stage. For more information about the different types of instruction and how the data is encoded in the instruction, please refer to the RISC-V manual [?].

Signals:

1. Input: *instruction*, This signal is representing the current instruction that is being decoded.
2. Output: *br_sig*, This signal is representing the state of the current instruction. It is used to know if the instruction is a branch or not.
3. Output: *br_op*, This signal is representing the type of branch that is being executed.
4. Output: *lsu_op*, This signal is representing the type of load or store that is being executed.
5. Output: *alu_op*, This signal is representing the type of ALU operation that is being executed.
6. Output: *data_origin*, This signal is representing the origin of the data that is being used by the ALU. That could be the registers, or one register and an immediate or one register and the PC.
7. Output: *data_dest*, This signal will be useful in the write-back stage to know which data to write back, so either the ALU result or the data from the memory or the next PC (so the PC+4).
8. Output: *imm*, This signal is representing the immediate value that is being used by the ALU.
9. Output: *reg_wr_addr*, This signal is representing the register address that will be written back.
10. Output: *reg_wr_sig*, This signal is representing if we want to write to the register file or not.
11. Output: *mem_wr_sig*, This signal is representing if we want to write to the memory or not.
12. Output: *reg_addr1*, This signal is representing the first register address that has been extracted from the instruction.
13. Output: *reg_addr2*, This signal is representing the second register address that has been extracted from the instruction.