RISC-V: A Didactic Platform
Report

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June 12, 2023

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1 Introduction

1.1 Motivation

This project, RISC-V: A Didactic Platform, embarks on the pursuit of simplifying complex computer architecture concepts, targeting an academic audience who is striving to comprehend the intricate world of processor design. It specifically focuses on the creation of a RV32I processor, based on the RISC-V instruction set architecture.

RISC-V, an open standard instruction set architecture (ISA), has increasingly gained popularity due to its simplified design and flexibility for customization. While its usage has been witnessed across a multitude of applications, its potential as an educational tool remains largely unexplored. The objective of this project is to bridge this gap by providing a detailed, comprehensible, and implementable design of an RV32IM processor, leveraging the RISC-V architecture.

This project not only contributes to the existing body of knowledge around RISC-V and processor design but also aims to democratize access to information on complex computing architectures. Through this platform, users will not only learn the theory behind processor design but will also gain valuable hands-on experience with the actual implementation, enabling them to better understand the interplay between hardware and software in a computing system.

In an era where the understanding of computer architecture is pivotal for both hardware and software development, a project like RISC-V: A Didactic Platform can serve as a crucial resource. By harnessing the power of the RISC-V architecture and presenting it through

a user-friendly and accessible platform, we hope to elevate the understanding of processor design to new heights.

1.2 Project Scope

Here are the different main focus points of the project:

- Openess: It is an important point for the project to use as much as possible open source software and also for the project to be as open as possible such that people can work on it with the less possible restrictions.
- Comprehensive: Since the project needs to be open source and be used by academic people to understand but also add things on top of it, the project needs to focus on being as comprehensive as possible.
- Simplicity: This point is linked a bit with the last one, but the project doesn't aim as performance first, but more as ease of understanding, so if a solution can be easier but degrade a bit the performance, it should be taken except if it adds an educational value to do it

1.3 Project Objectives

Overall, the project aims to give a very basic implementation of an RV32IM processor such that it can be used as an academic tool to teach and explain how a RISC processor works and how to build one using HDL languages such as Verilog. Here are the main objectives that has been set for the project:

- First create an unpipelined version of the RV32IM processor as a proof of concept
- Pipeline the existing unpipelined version of the processor
- Fix the different issues caused by the pipelining of the processor, mainly the data dependency but also the branch prediction problem by either stall or implementing some forwarding paths and branch predictor and mechanisms to make everything work correctly
- The simulation should works on Icarus Verilog to make the whole process more open instead of relying on proprietary software such as Questa Modelsim.
- Add extensive testing of the different main modules to make the processor as reliable as possible.
- Add an easy way for users to create programs and load them into the ROM memory.
- Document everything such that users can easily understand how things work and can work on it easily.

2 Background Research and Knowledge