

Switched Capacitor A/D Converter Input Buffer

Julia Arnold

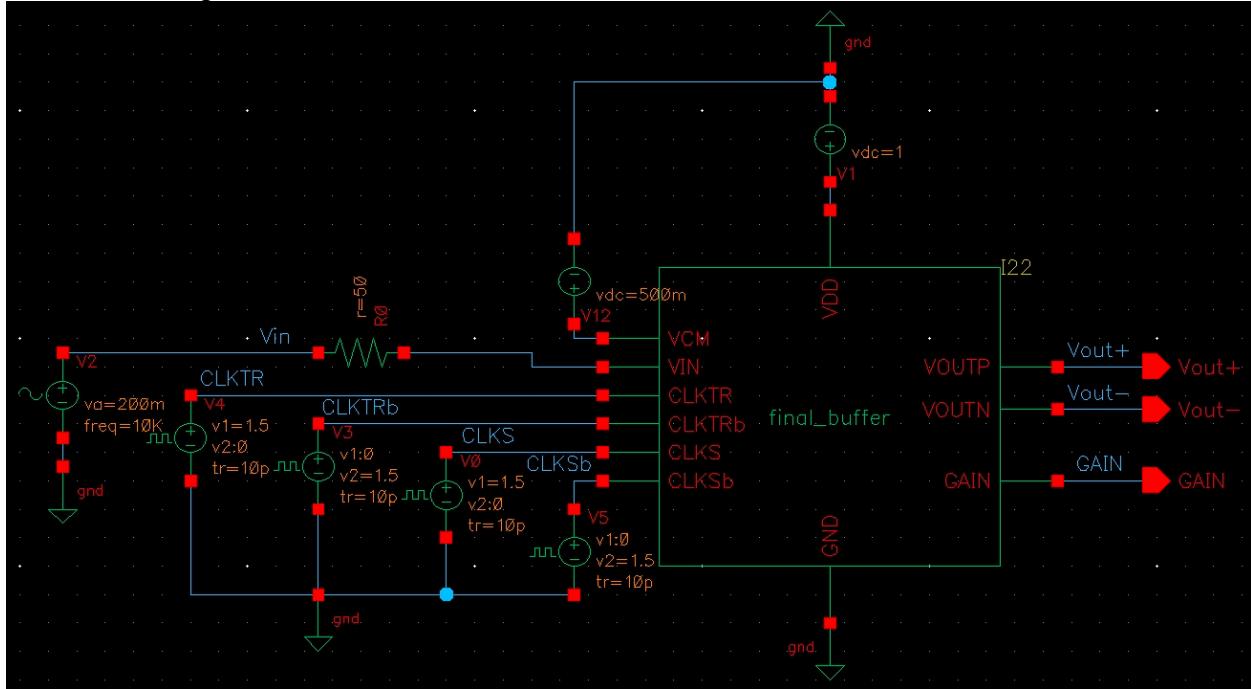
6.775 Final Project

19 May 2021

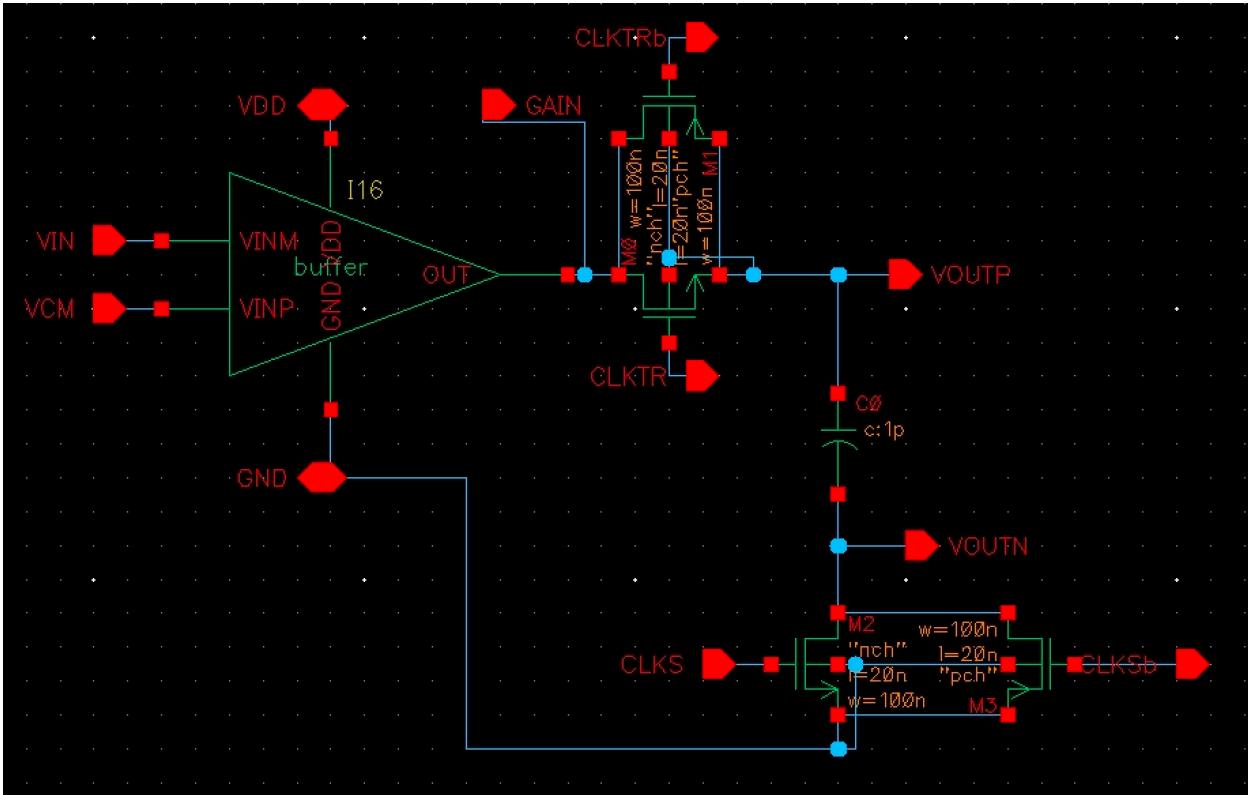
	Requirement	Measurement
AC Gain	1 or $-1 \pm 1\%$	-1.0028
Input/output signal swing	$\pm 200\text{mV}$	300.493mV to 699.444mV for 200mV amplitude input 13.7419mV to 984.817mV for 500mV amplitude input
Input impedance (DC)	not lower than 10 kW	20.4k Ω
Load	1pF load	1 pF
Switching Frequency	50MHz	50 MHz
-3dB bandwidth	20MHz with the 1pF load	41.372MHz
Maximum Power Consumption	3mW	1.315mW
Total thermal/shot noise	< 400 μV rms, output referred, 0-200MHz	176.1uV
Total harmonic distortion at 1MHz	better than -50dB	-65.699dB

Circuit Schematic

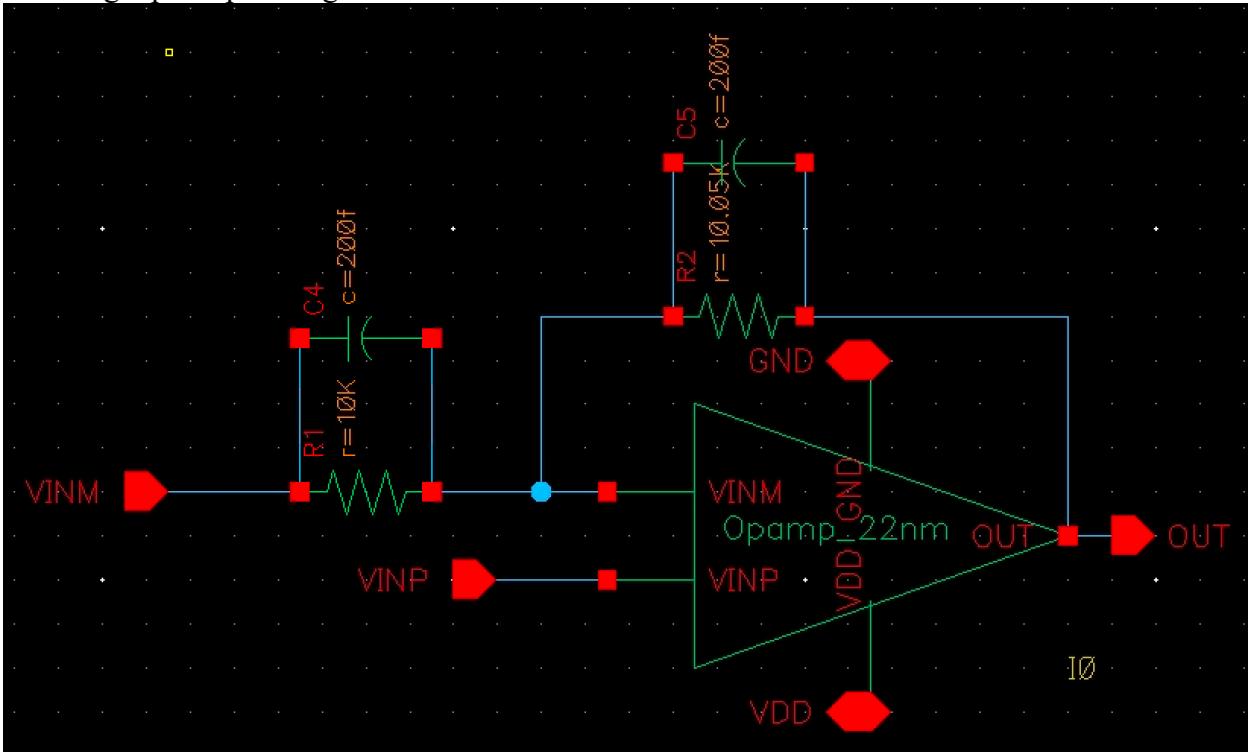
Testbench Setup



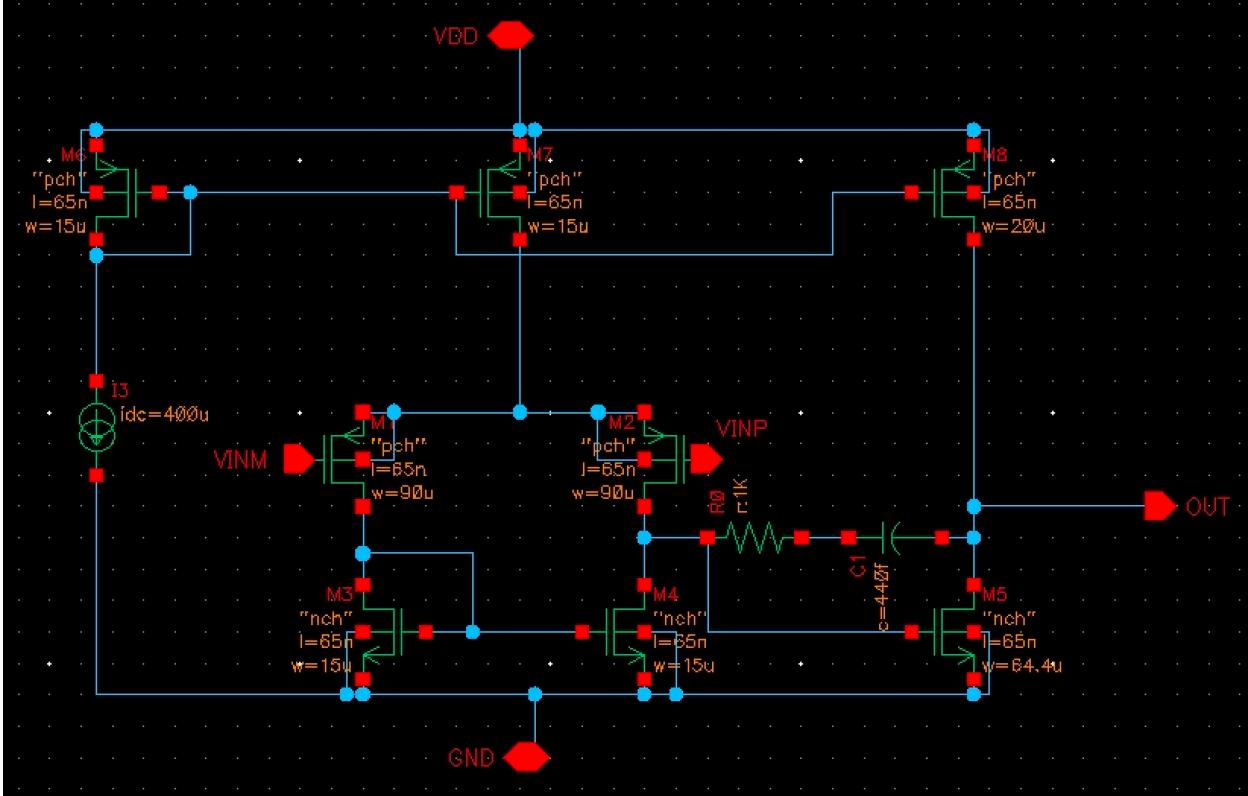
Track and Hold Circuit



Inverting Op-Amp Configuration



Op-Amp



Description of Operation

This circuit is a basic track and hold circuit comprised of an op-amp and two switches. To calculate the R_{on} of the switch we have

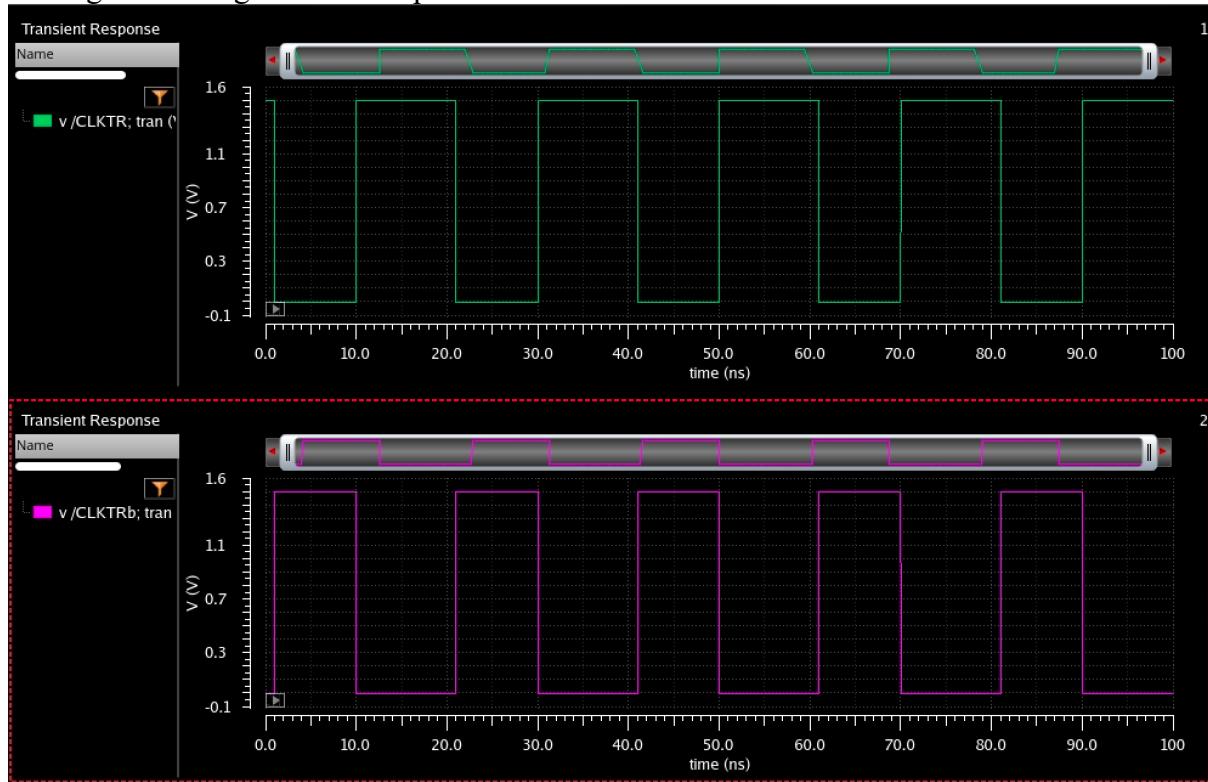
$$R_{on} = \frac{1}{\mu C_{ox} W / L (V_H - V_{in} - V_T)}$$

Where we can change W and L. To make R_{on} as small as possible we want large W and small L. Thus I chose L as small as possible at 20nm and made W to be 100nm. As I made W larger, I saw more noise when the switch opened and closed, so I chose to make W relatively small.

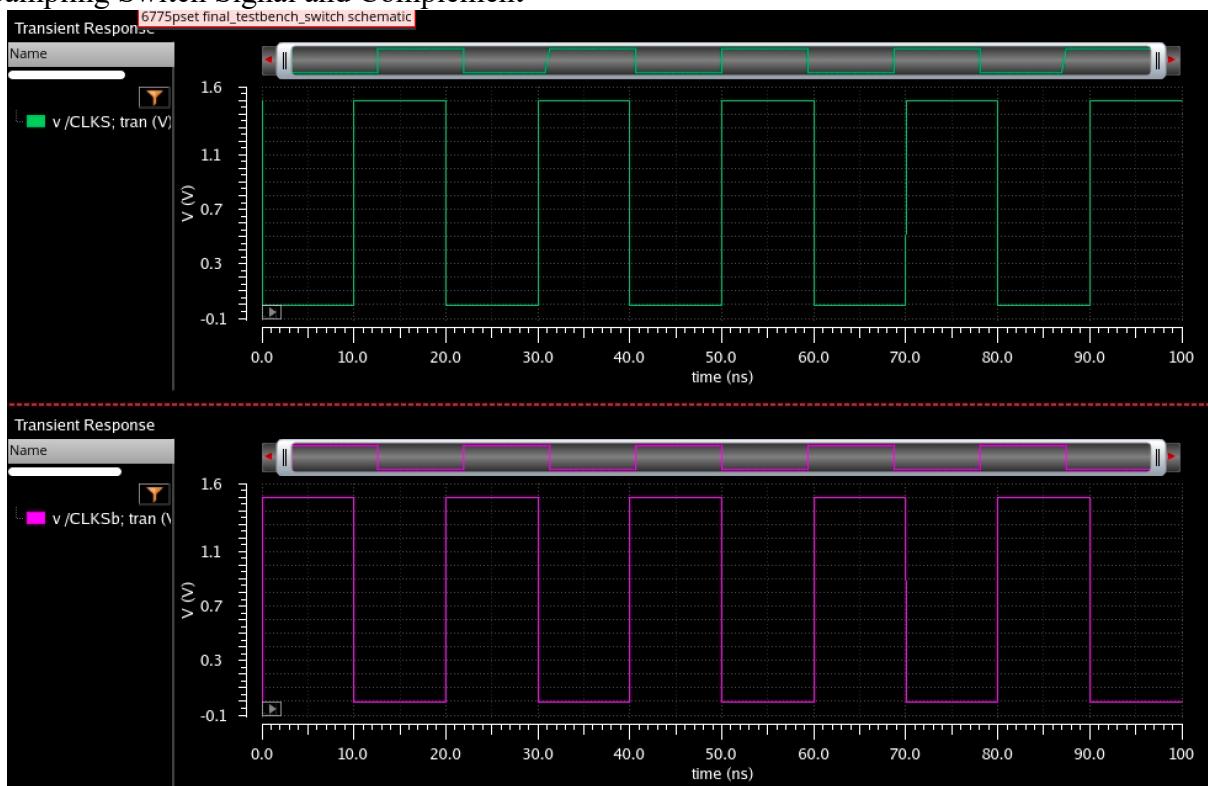
I also chose to implement a complementary switch to decrease total harmonic distortion.

Shape of Clock Signals

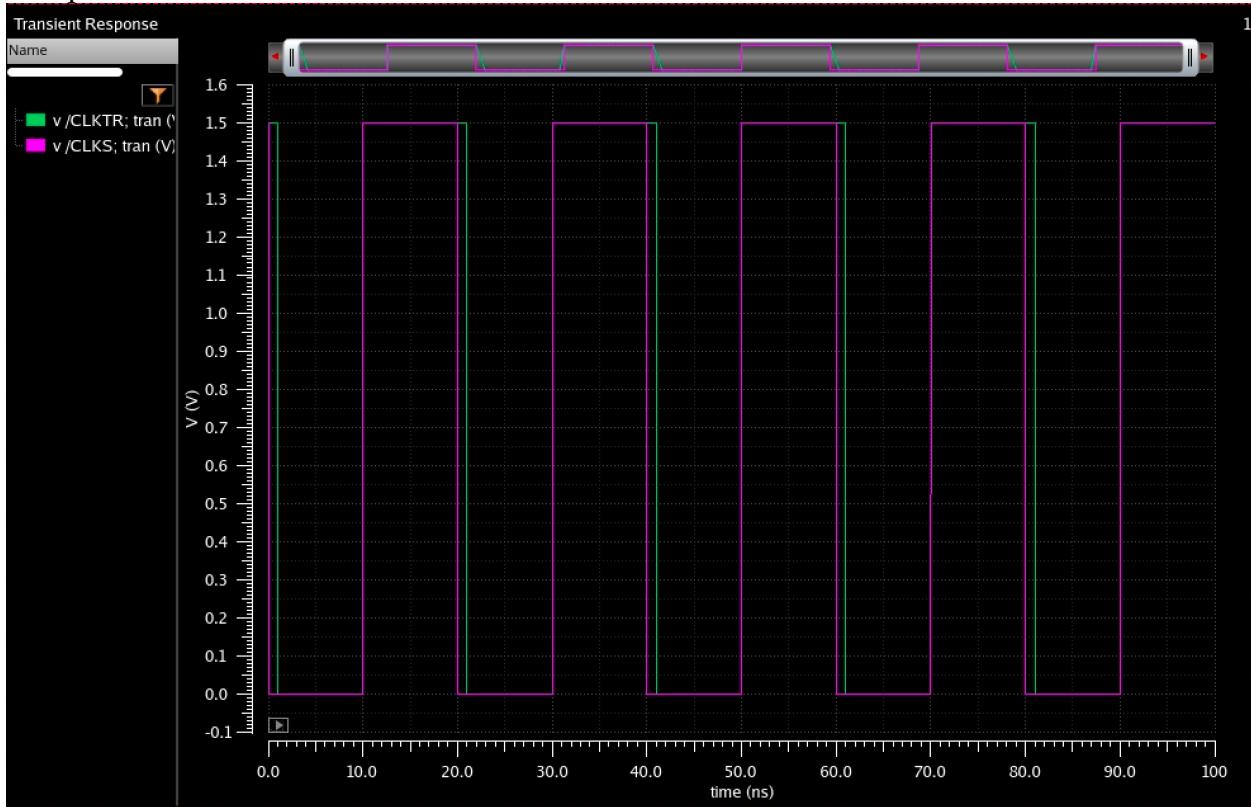
Tracking Switch Signal and Complement



Sampling Switch Signal and Complement



Comparison



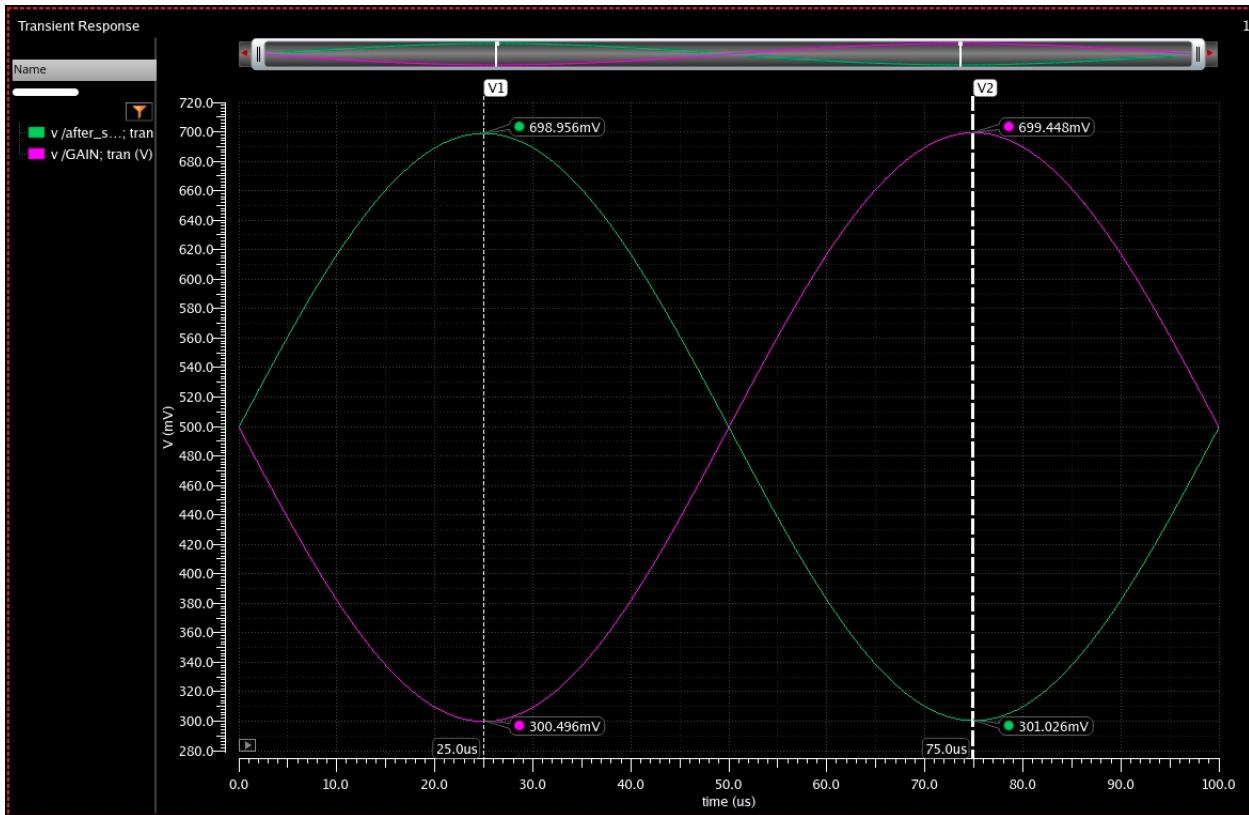
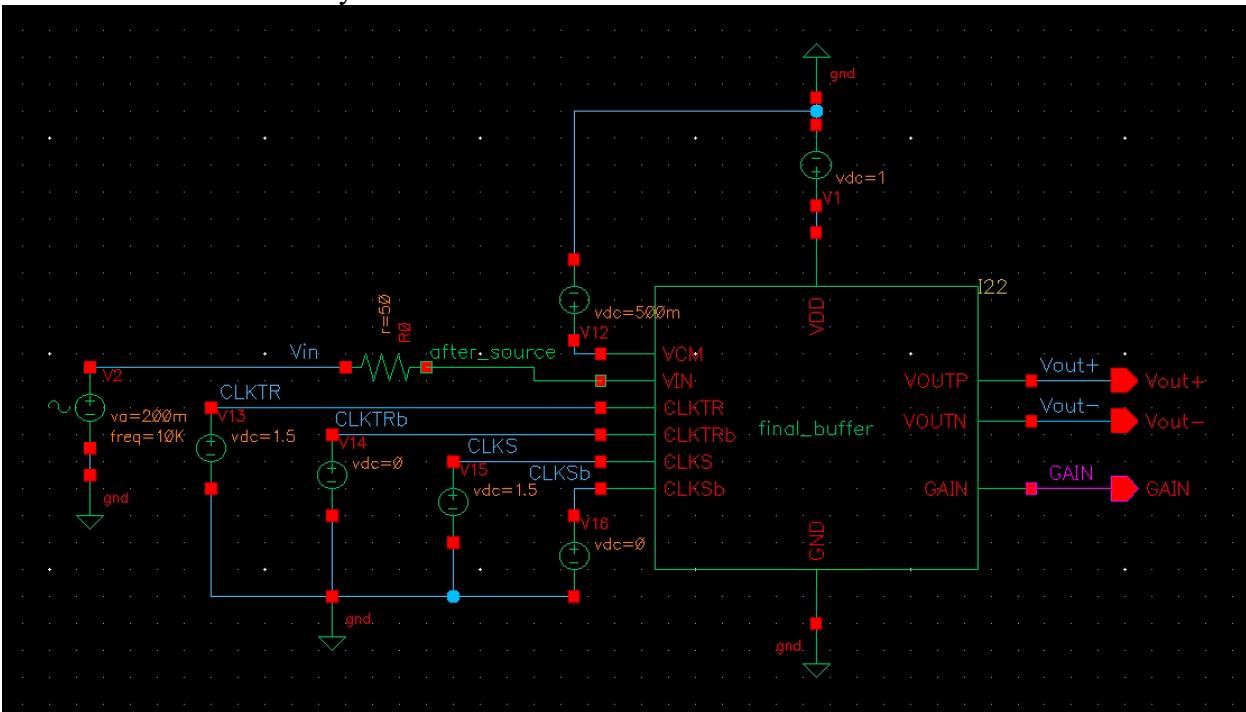
Testbenches and Simulation Outputs

1. Gain: 1 or $-1 \pm 1\%$ Measured as the buffer output amplitude divided by the buffer input amplitude (after the 50W source resistor) during the track mode with a full-scale sinusoid (200mV amplitude) input at 10kHz. For this measurement, you may put the circuit in a continuous track mode, and use transient simulation.

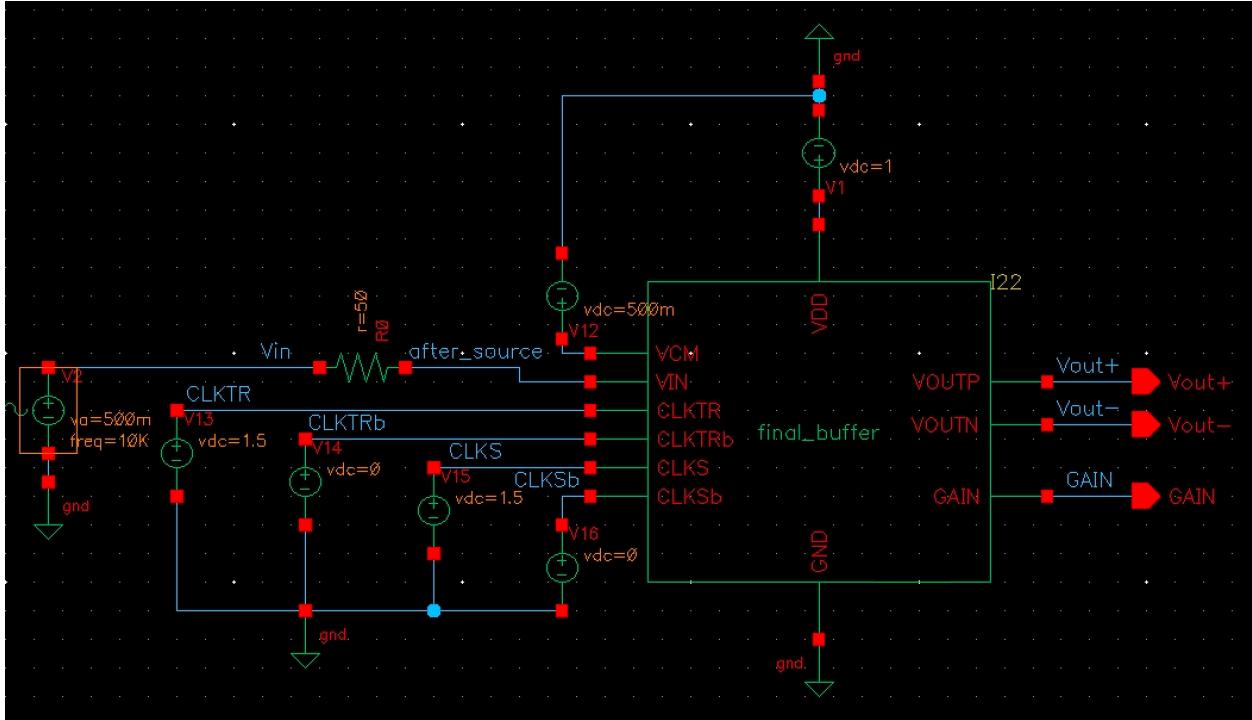
$$\frac{V_{out}}{V_{in}} = \frac{699.448mV - 500mV}{301.026mV - 500mV} = -1.0024$$

$$\frac{V_{out}}{V_{in}} = \frac{300.496mV - 500mV}{698.956mV - 500mV} = -1.0028$$

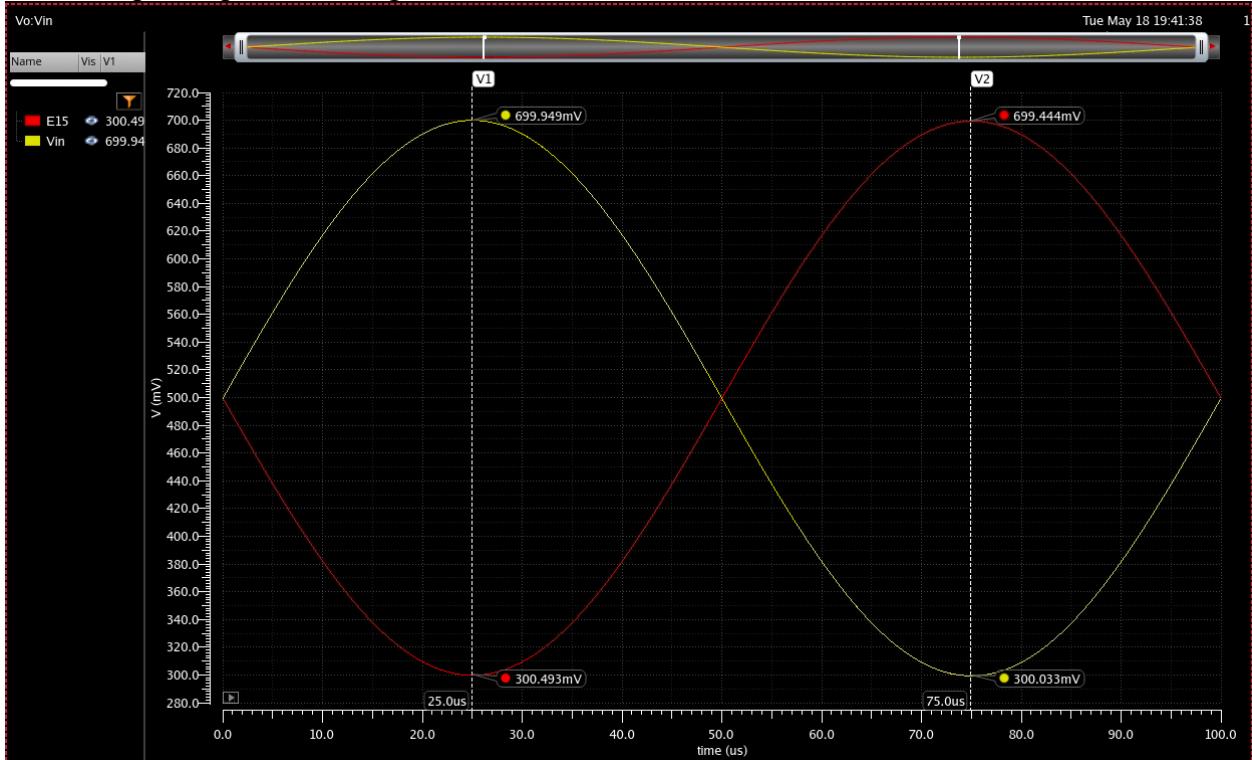
GAIN is connected directly after the internal buffer



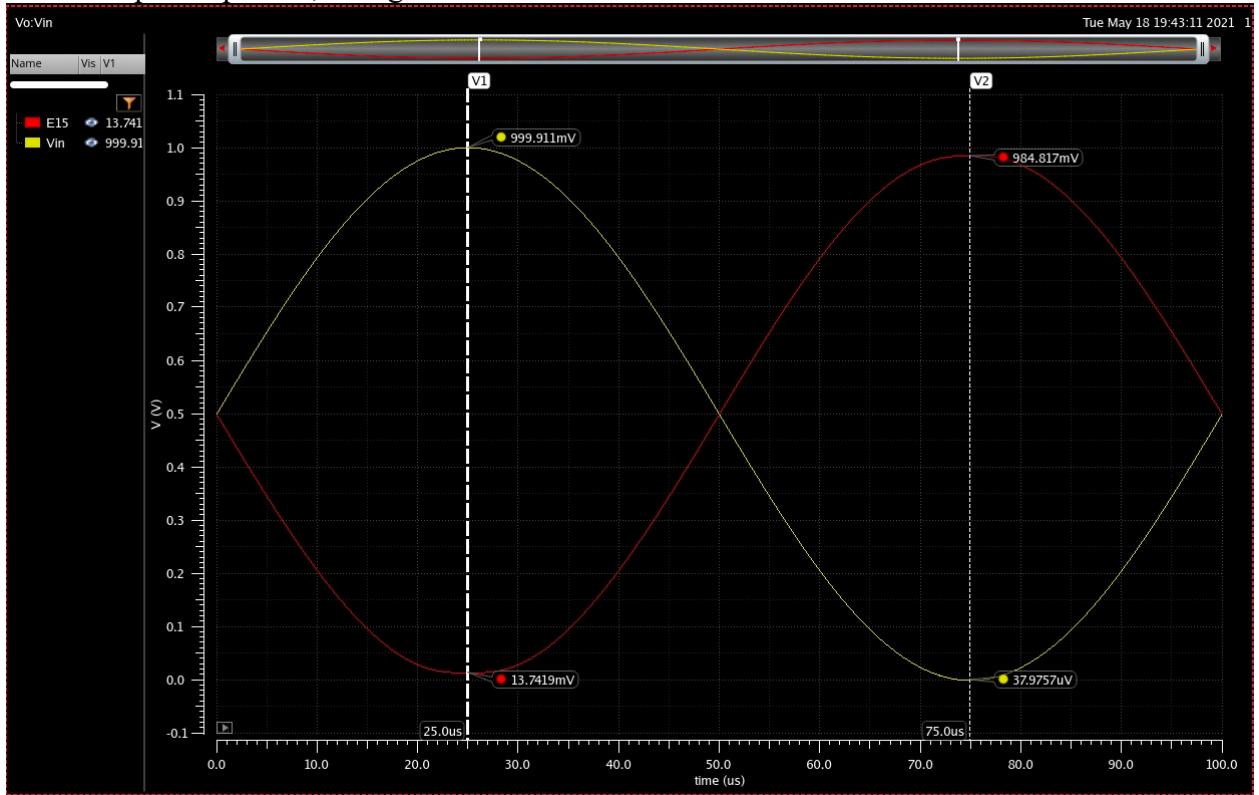
2. Signal swing: $\pm 200\text{mV}$ around the common-mode voltage of your choice, continuous track mode



E15 is V_o , the differential voltage over the load capacitor
 200mV input amplitude, swing: 300.493mV to 699.444mV



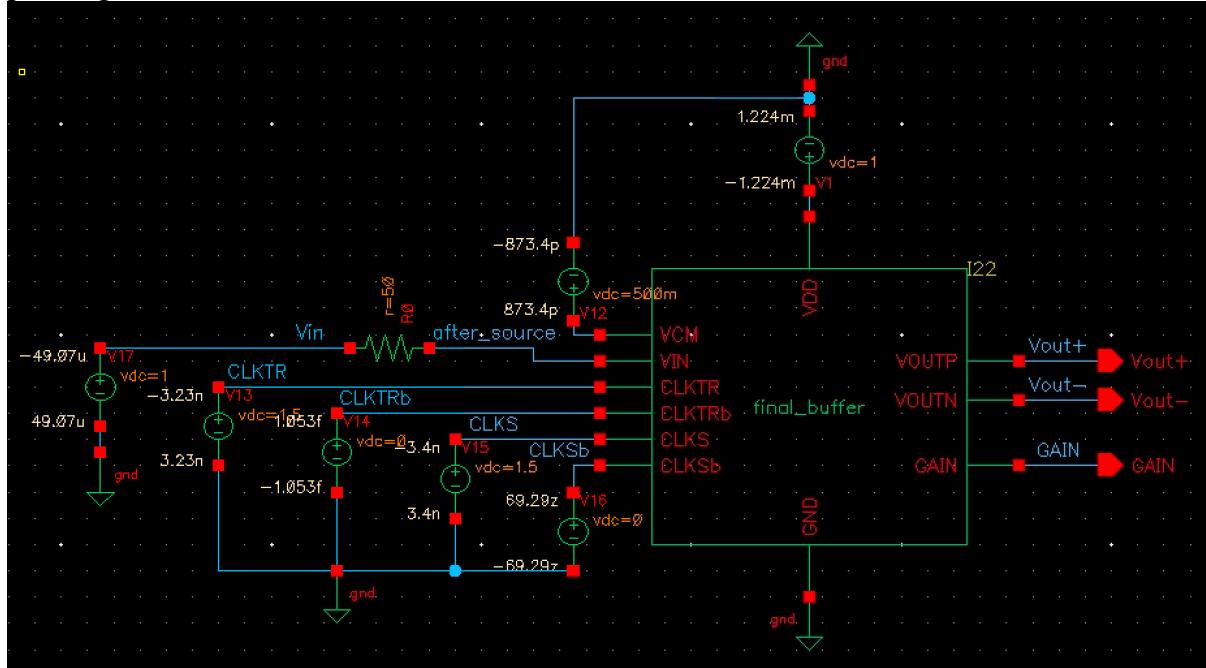
500mV input amplitude, swing: 13.7419mV to 984.817mV



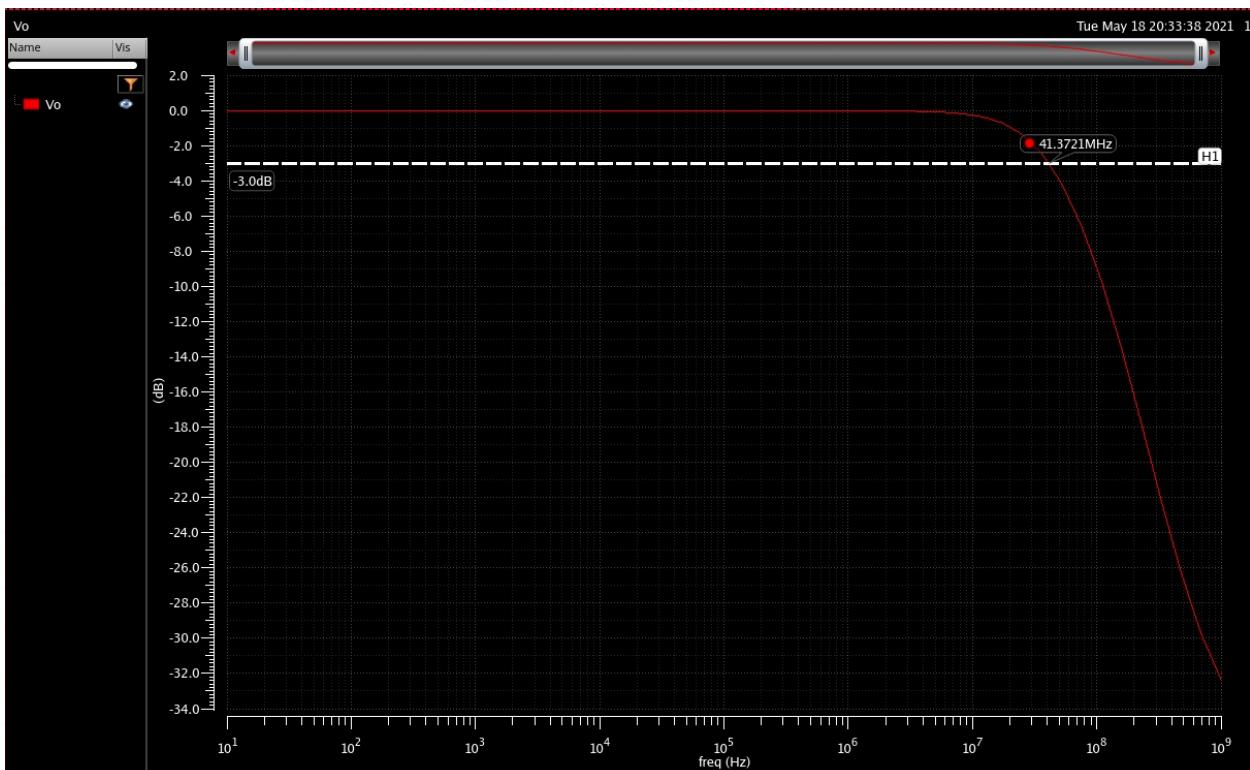
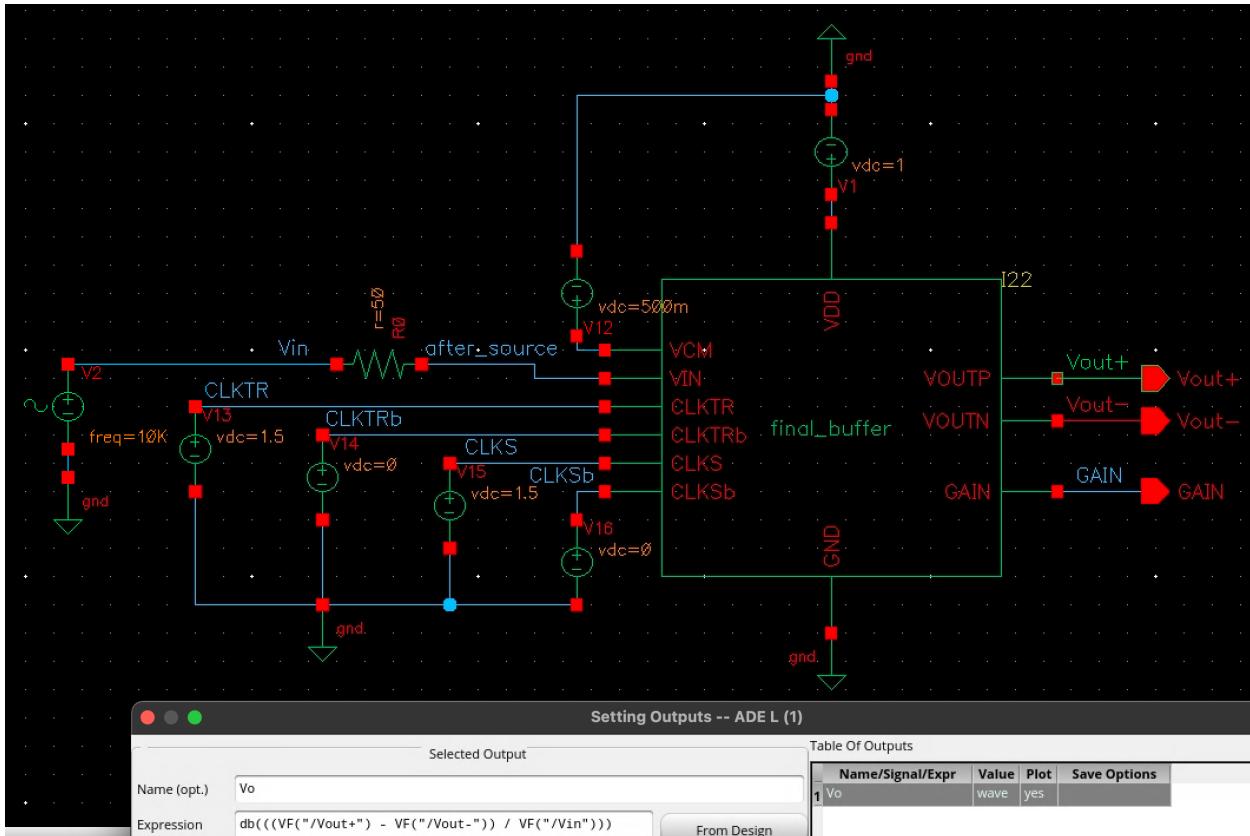
3. Input impedance (DC): not lower than 10 kW in parallel with 1 pF, non-switched, AC simulation

$$\frac{V}{I} = \frac{1V}{49.07\mu A} = 20.4k\Omega$$

Operating Currents

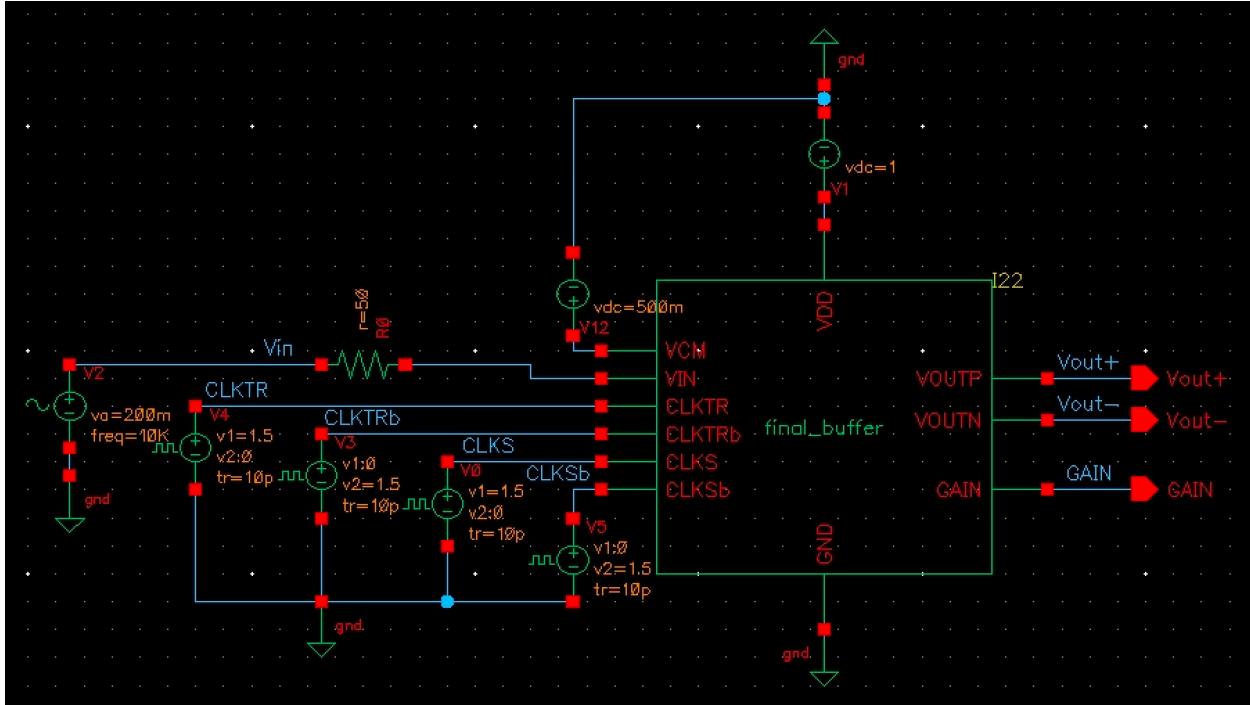


6. Track mode -3dB bandwidth: 20MHz with the 1pF load CL switched on.
 Bandwidth: 41.372MHz

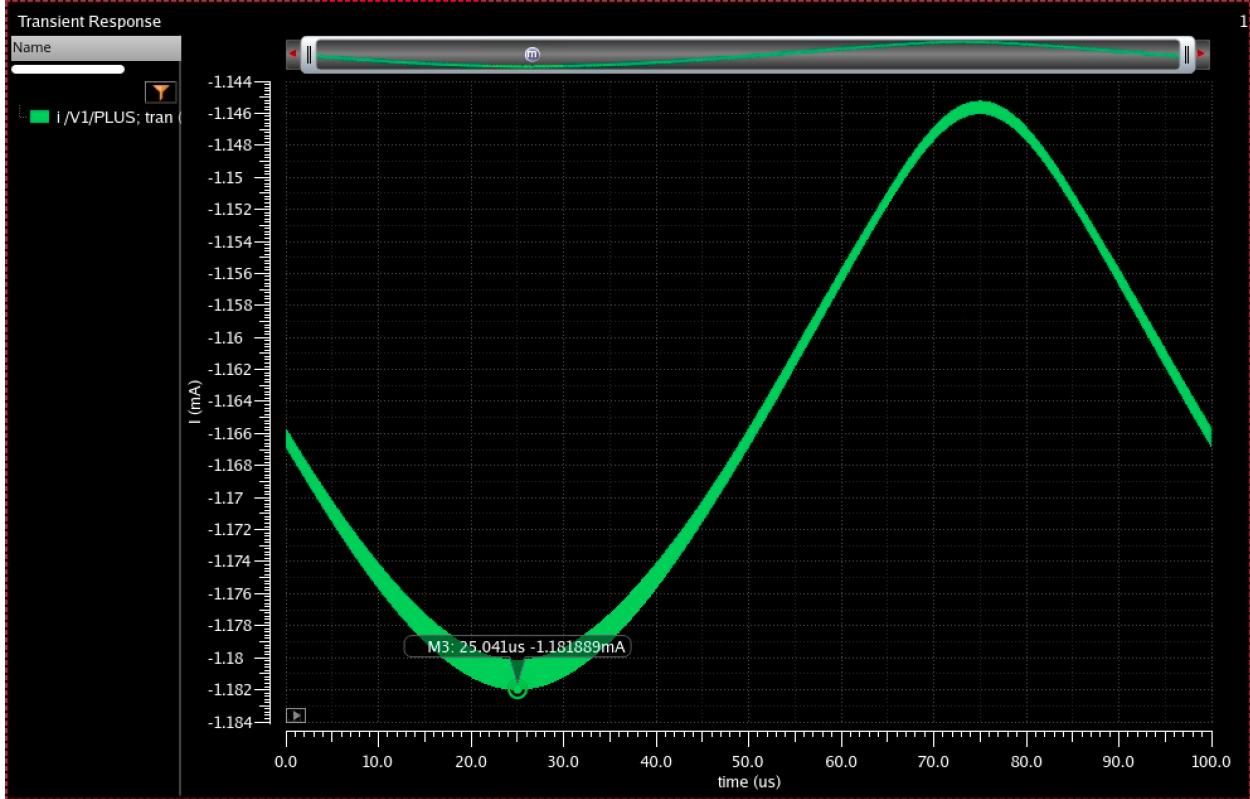


7. Maximum Power Consumption: 3mW. Includes power from the 1.0 supply and the ideal current source. switching

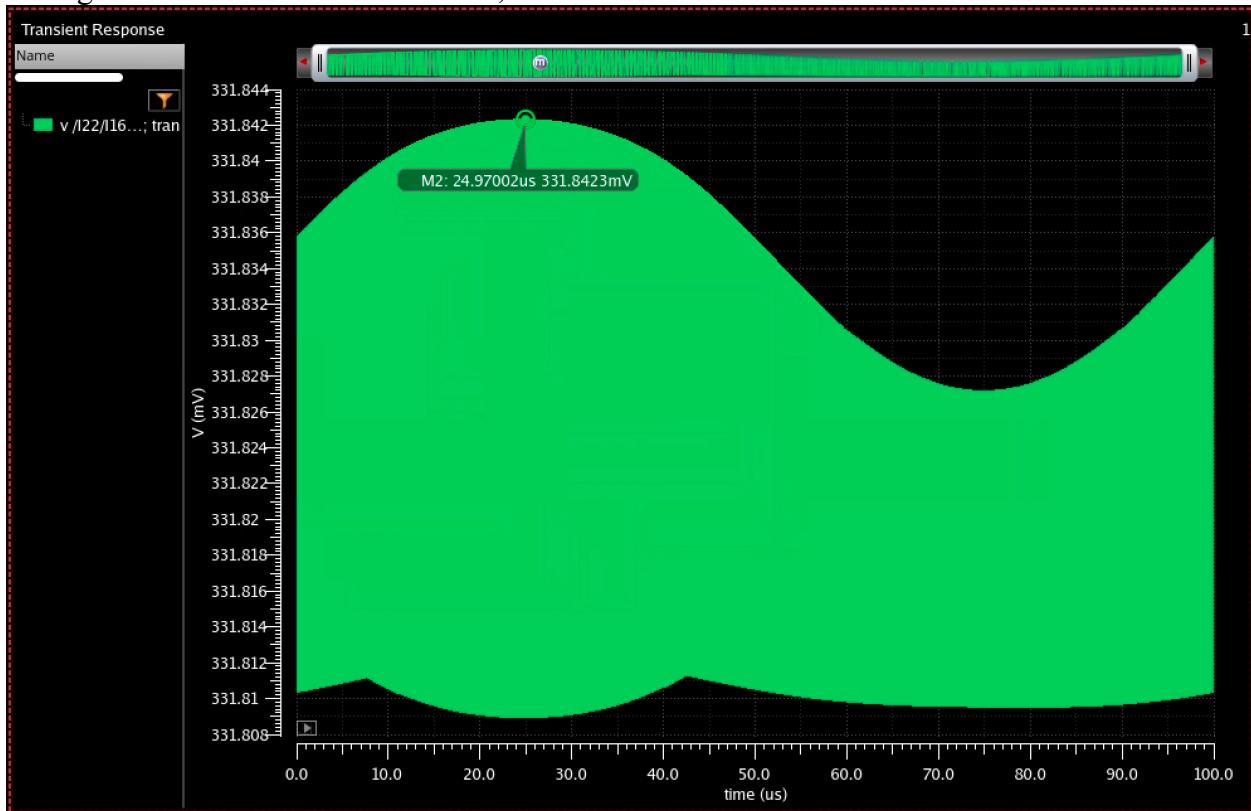
$$Power = 1.182mA * 1V + 400\mu A * 331.8mV = 1.315mW$$



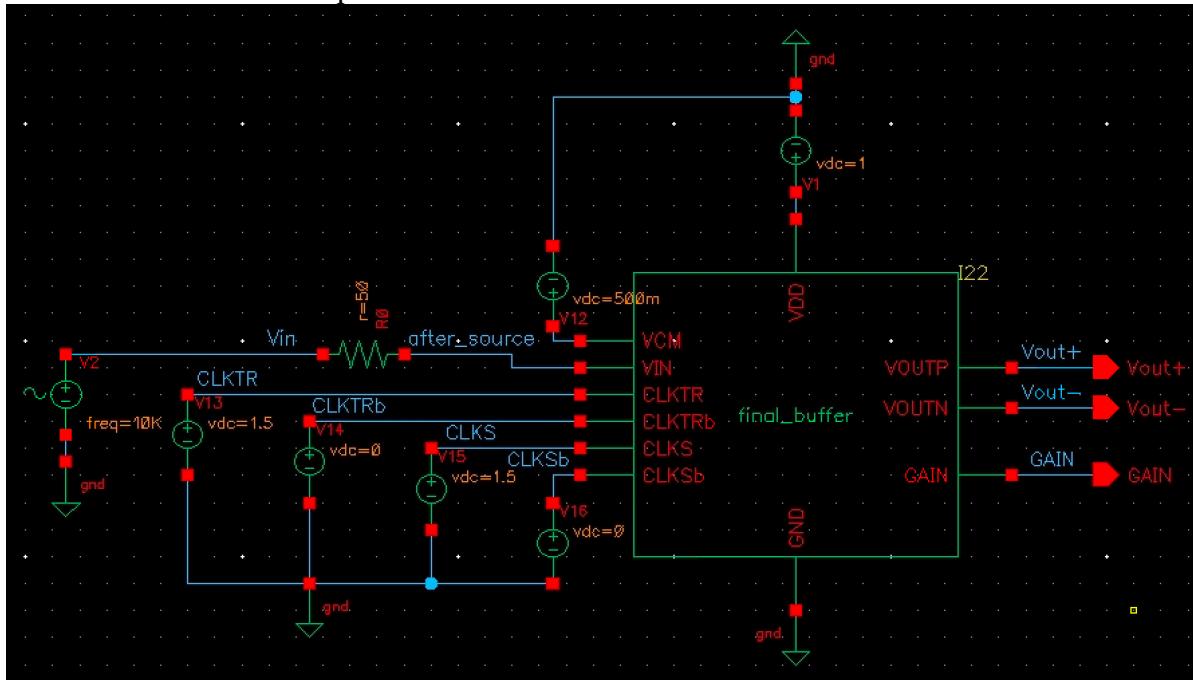
Current from 1V supply, max 1.182mA

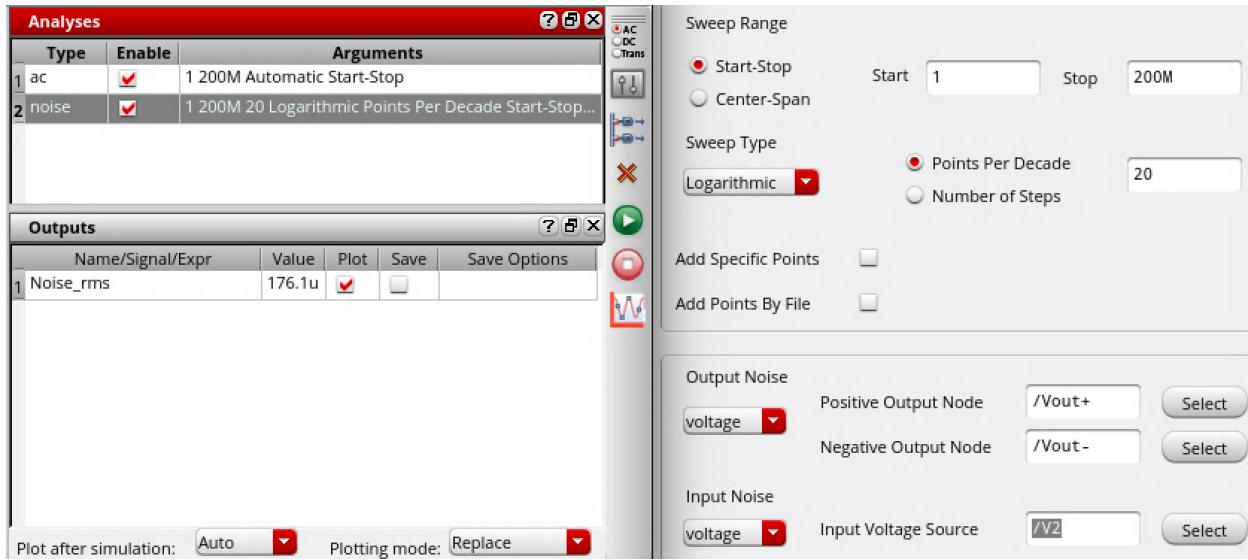


Voltage of ideal 400uA current source, max 331.8mV

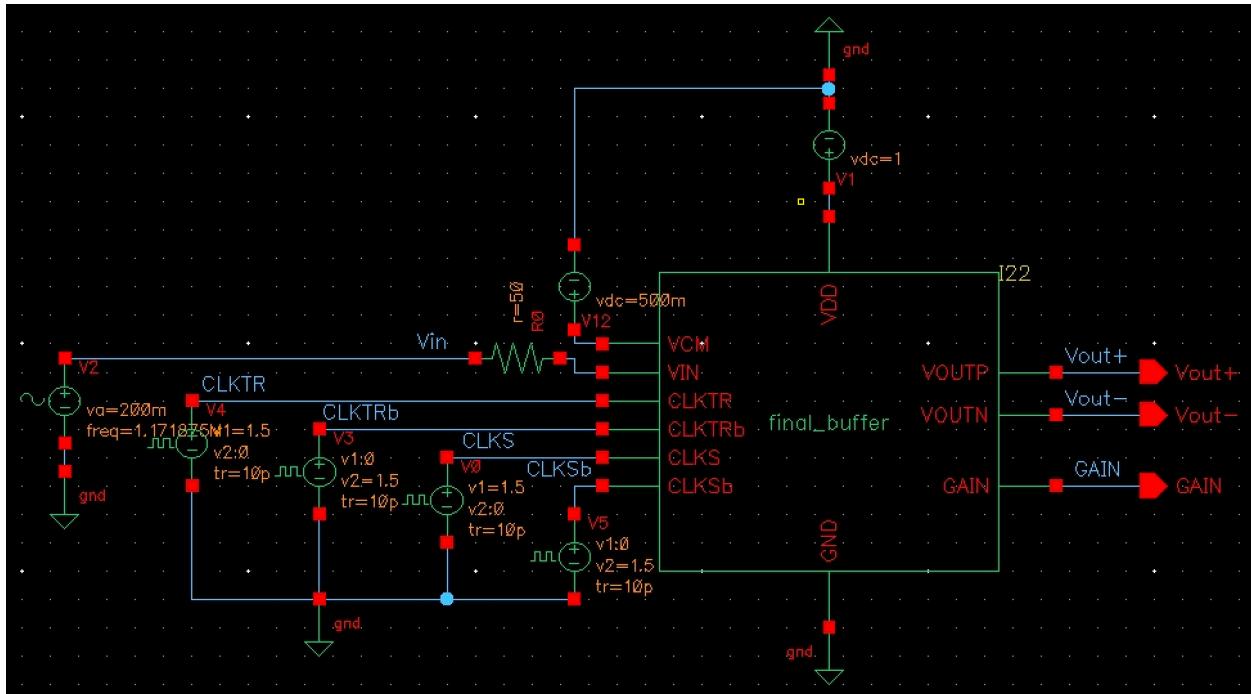


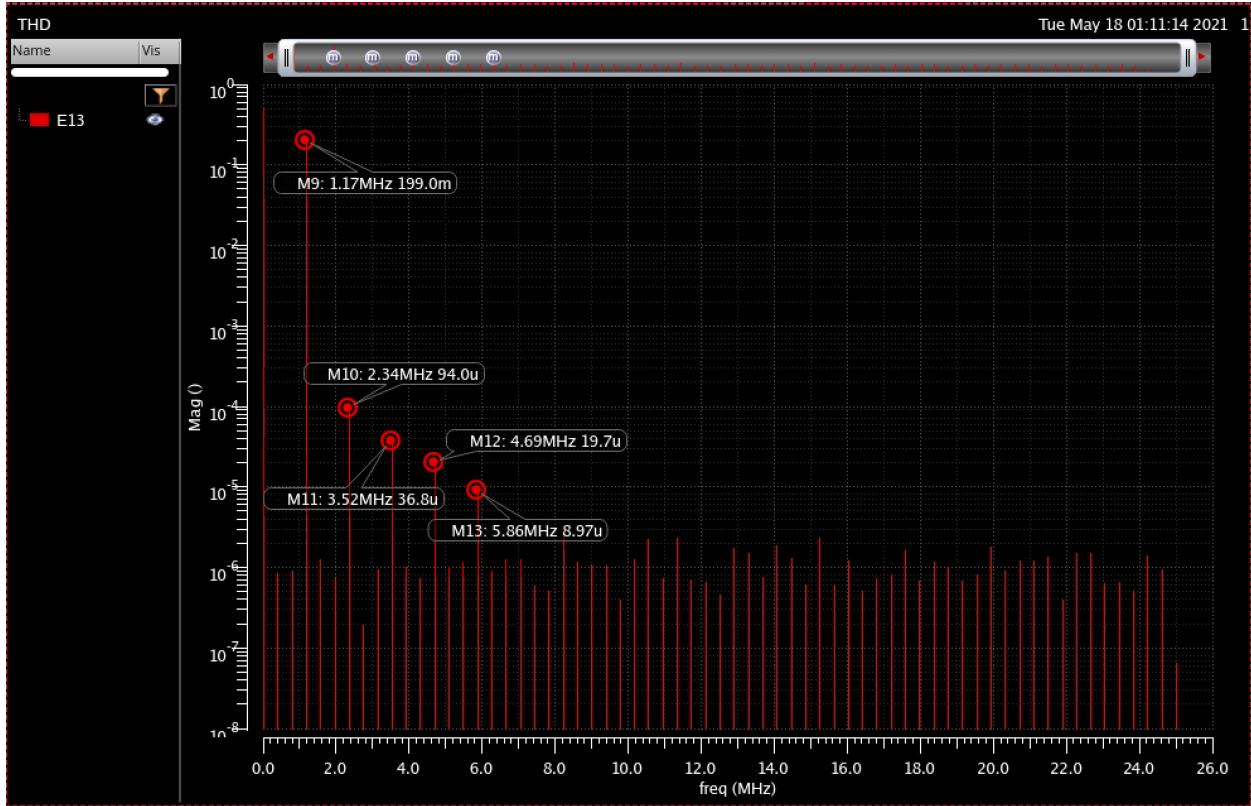
8. Total thermal noise: < 400 μ V rms, **output referred**, 0-200MHz, on the 1pF load capacitance, measured during the track mode (i.e. with the 1pF load capacitance CL switched on). You may use AC simulation for this specification.





9. Total harmonic distortion: better than -50dB





$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_s} = \frac{\sqrt{94u^2 + 36.8u^2 + 19.7u^2 + 8.97u^2}}{199.0m} = .0005188011 = -65.699\text{dB}$$

Discussion of Circuit Performance

Overall, this design could be executed as expected. The most time was spent adjusting the transistor sizing to minimize R_{on} but avoid noise at the transitions between off and on. The length of the transistors was minimized as much as possible. Increasing the width would decrease R_{on} but introduced more noise at the switch transitions, so the final width is a compromise of these two factors.

I also chose to incorporate complementary switches to accompany the original ones. This helped bring down the THD but requires extra signals to be created and could create extra delay in a physical implementation.