EXPERIMENT 7

Operation Amplifier Characterization

7.1 Application

Operational amplifiers are available in nearly unlimited varieties from countless vendors. In order to understand how to pick the correct op amp for a specific circuit, it is necessary to understand what all of the parameters on an op amp datasheet mean. A thorough understanding of op amp characteristics is invaluable to the analog circuit designer. The measurable parameters of an op amp can be used to predict how well the surrounding circuit will perform and allow for verifying that the inputs and outputs of the circuit will behave as expected.

7.2 The real op amp

So far, we have used the op amp in circuits assuming it is ideal. That is, we used the ideal virtual short circuit analysis that effectively assumes all op amps have

1. infinite input resistance,
2. zero input current,
3. infinite gain, and
4. zero output resistance.

However, the op amp we just built does not satisfy all of these assumptions. Many nonidealities exist for op amps. In order to compare our op amp to others, we must study how the non-ideal characteristics manifest, the relevant datasheet metrics, and finally the impacts on a given circuit topology.

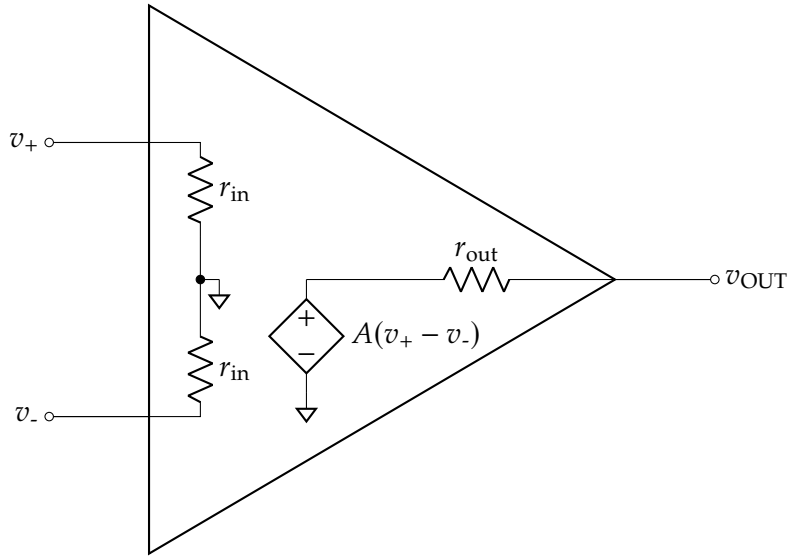

Figure 7.1: A model that better reflects real op amps, where r_{in} is the common mode input resistance, A is the op amp gain, and r_{out} is the output resistance.

Figure 7.1 is a simple op amp circuit model updated to reflect the real nature of both the inputs and the output. This model is still a simplification – there are other biasing requirements, e.g., input bias current, common mode voltage, etc., that need to be guaranteed for this simplified circuit model to hold. The additional requirements can be derived by thoroughly analyzing the input and output stages.

7.2.1 Op amp characteristics

The many non-idealities of real op amps will be explored through the next few sections. Overall, these characteristics can be used to explain why an op amp acts the way it does in a wider variety of applications than the ideal model can describe.

Finite gain and bandwidth

The gain of an op amp, known as the *open loop gain*, is very large. Ideally, we consider it to be infinite; however, commercial op amps typically have a gain of $\gg 80\,\text{dB V}$. An op amp will act like a low-pass filter due to the added capacitor and transistor parasitics. Therefore, one can not expect an op amp to perform correctly at high frequency. Thankfully, the gain-bandwidth product helps simplify the issue.

Gain-bandwidth product (GBW)

The gain-bandwidth product, GBW, as its name implies, is simply equal to $GBW = \text{gain} \times \text{bandwidth}$. The surprising thing is that the product is a constant! In other words, if you know the GBW value from an op amps datasheet, then one can compute the maximum bandwidth in which the op amp will function for a certain gain and vice versa.

For example, if an op amp circuit is built to have a gain of 10, and the gain bandwidth is 1 MHz, then the maximum bandwidth of the entire op amp circuit will be $\frac{1\,\text{MHz}}{10} = 100\,\text{kHz}$. Going in the other direction, if we need to build an op amp circuit with a bandwidth of 50 kHz and the op amp has a gain bandwidth of 1 MHz, then the maximum gain we can get from the op amp circuit is $\frac{1\,\text{MHz}}{50\,\text{kHz}} = 20$.

The definition of bandwidth is not important as long as you are consistent. Most datasheets cite the product using the $-3\,\text{dB}$ point, however, one can find the product under the $-0.1\,\text{dB}$ definition(1) and use it like normal.

(1) or any other for that matter

Finite input impedance

Ideally an op amp will have an infinite input resistance but practically there is a limit. The good thing is that modern FET based op amps like the one we built can realize such large impedances ($> 10^{10}\,\Omega$) that they are effectively infinite. Even BJT based designs should have input impedances of greater than $2\,\text{M}\Omega$.

Input bias current

The input bias current is ideally zero. A bipolar junction transistor (BJT) based op amp can not be perfectly zero because the internal differential amplifier must draw some amount of current to bias itself. For a complementary metal–oxide–semiconductor (CMOS) op amp, the bias current will still be present in most op amps due to leakage through ESD protection circuits that are present in almost all integrated circuits (ICs). The bias current is approximately DC and, while extremely small in modern op amps (nano to pico amps), can not always be treated as zero.

For example, if the input of a non-inverting amplifier is capacitively coupled, then the input bias current from the non-inverting terminal will slowly charge the coupling capacitor until it charges to nearly the supply, in turn causing the op amp output to saturate. In this case, the input resistance of the non-inverting amplifier can be sacrificed by placing a resistor to ground at the non-inverting amplifier, thereby giving the input bias current a DC path to ground to flow through.

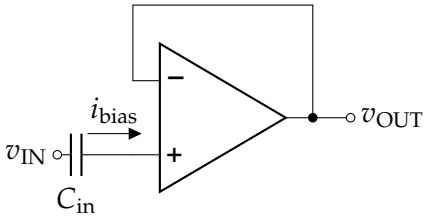

Figure 7.2: Capacitively coupled op amp input – don't do this!

Input offset voltage

The input offset voltage is the voltage that must be externally applied across the device's inputs[2] to give a zero volt output. By design the offset voltage should be zero; however, in practice the input stage of an op amp is slightly unbalanced. This small imbalance appears as parasitic input to the op amp in addition to the feedback voltage. An example of input offset is shown in figure 7.3. The output of the circuit should be much greater than 0, but the input offset cancels out the 1 mV from the positive input. In effect, the dependent source in figure 7.1 actually follows the equation:

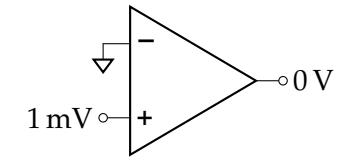

Figure 7.3: Behavior of input offset voltage

$$A(v_+ - v_- \pm v_{\text{off}})$$

Where v_{off} is the input offset voltage. The datasheet for an op amp will usually report the worst case input offset voltage *magnitude*, so the sign can be positive or negative.

Input offset current

The input offset current is the amount of mismatch between the input bias current at the each input terminal. That is, it is $i_+ - i_-$. This can cause a mismatch in the voltage at the input terminal via the surrounding resistor network and result in a DC error on the output. In modern op amps this mismatch is typically so small that it can normally be ignored.[3]

[2] That is, the voltage at each input is slightly different.

[3] If the feedback network is high impedance, then the input offset current will affect the circuit.

Slew rate

Slew rate is defined as the change of electrical quantity per unit of time. In the context of op amps, it is defined as the maximum rate of change of voltage at the output. The rate is usually defined as volts per microsecond.

The slew rate of an op amp is typically measured with the op amp configured as a voltage follower with a sqare wave input. A common definition[4] for slew rate is the average slope of the output between 10% and 90% of the output swing.

[4] Always read the datasheet for an op amp to figure out how the manufacturer defines slew rate. It is not always the same.

Input common-mode voltage

In order to keep the input transistors biased in saturation, the DC bias voltage at the gate must be limited to a certain range. The op amp we designed initially assumed that the common mode voltage is 0 V; however, the input transistors will continue to function if the DC input changes. The upper limit is set by the active load PMOS transistors and the lower limit is set by the current mirror.

Common-mode gain (common-mode rejection ratio)

The differential input stage of the op amp does not amplify common mode signals well, as we saw in experiment 5. Datasheets typically cite a common-mode rejection ratio. The rejection ratio is the ratio between the input and output common-mode voltages.

The differential to single ended conversion done by the active load differential amplifier circuit will cause the common-mode rejection ratio to decrease from what was measured in experiment 5.

Power supply rejection

The power supply rejection ratio (PSRR) is the ratio between the change in the supply voltage of the op-amp to the change in output voltage.

$$PSRR = \frac{\text{change in } V_{CC}}{\text{change in } v_{OUT}}$$

7.3 Prelab

Task 7.3.1: Prelab Questions

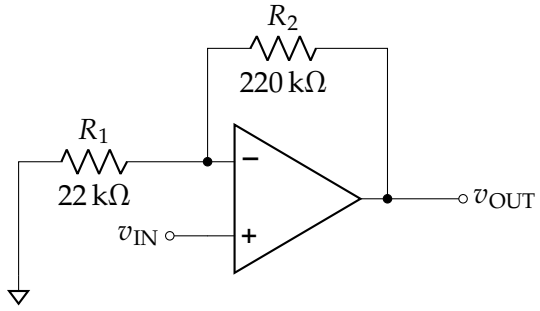

Figure 7.4: A non-inverting amplifier circuit.

Consider the op amp circuit in figure 7.4 for the following:

1. If the op amp has a gain bandwidth of 220 kHz, what will the bandwidth of the whole amplifier circuit be?
2. If the open loop gain of the op amp is 30 dB V[a], $r_{out} = 1\,k\Omega$, and $r_{in} = \infty$, what will the actual gain of the circuit be? Replace the op amp with the circuit in figure 7.1 then solve for the relationship between v_{OUT} and v_{IN} to calculate this.

[a] Recall that voltage gain in dB V is $20\log(A_V)$

7.4 Tasks

Task 7.4.1: Op amp construction

1. Construct the op amp circuit in figure 7.5. This is the same circuit built in experiment 6. $Q_{2,3}$, Q_7 and Q_8 are still made with two transistors in parallel.

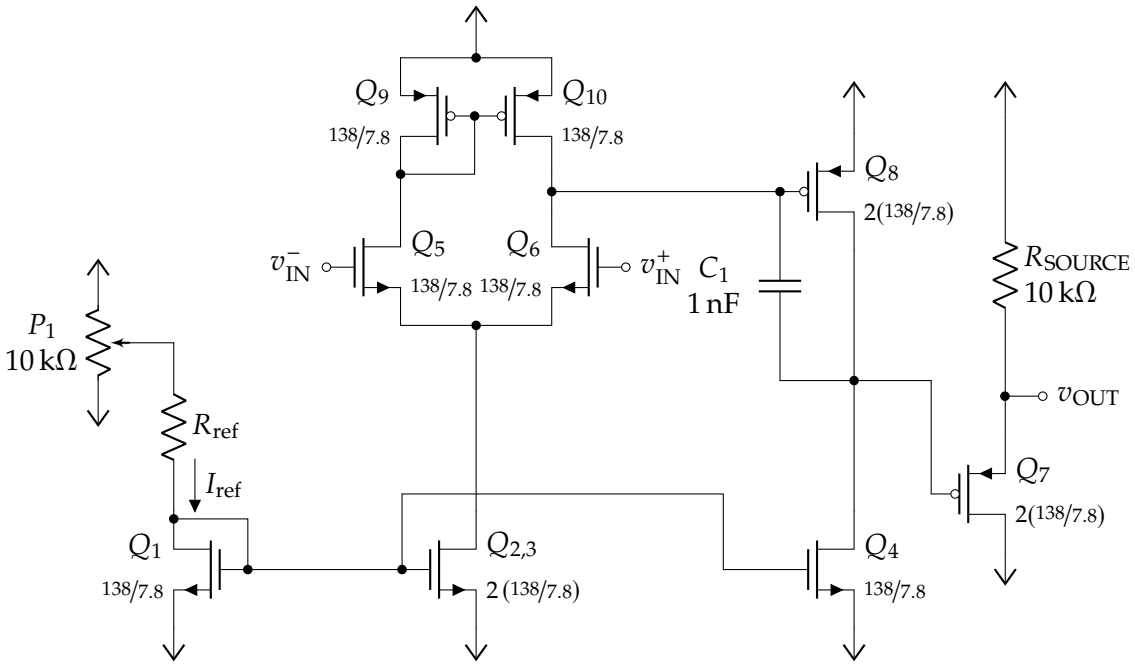

Figure 7.5: Op amp schematic.

2. *Set* I_{REF} to 200 µA
3. *Build* the circuit in figure 7.6 using the op amp.
4. *Apply* a 500 Hz 1 V_{p-p} sine wave signal to v_{IN} and capture and oscilloscope screenshot showing v_{IN} and v_{OUT}. Does this circuit behave like it would with an ideal opamp?

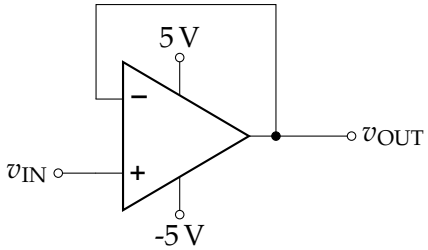

Figure 7.6: Op amp buffer circuit.

Task 7.4.2: Slew rate

For this task, continue using the buffer circuit from figure 7.6.

1. *Apply* an input 5 V_{p-p} square wave at 1 kHz
2. Does the output look like you expect for a buffer circuit?
3. Zoom into the transition on the output and obtain a printout of v_{IN} and v_{OUT} for both a rising edge and falling edge.
4. *Measure* the rising edge and falling edge slew rate of the output using the cursors on the oscilloscope.

Task 7.4.3: Op amp open loop gain and phase measurement

1. *Construct* the circuit in figure 7.7

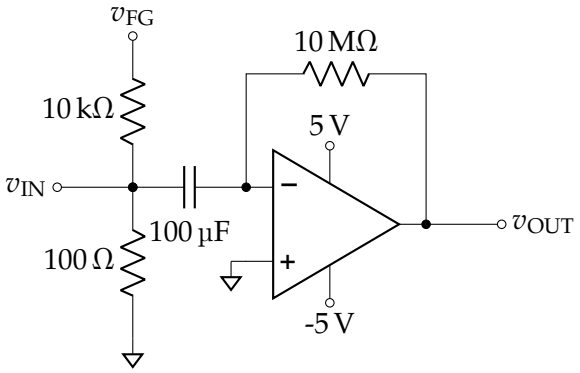

Figure 7.7: Open loop measurement circuit.

2. *Configure* the oscilloscope trigger to sync with the function generator.
3. *Apply* a 100 Hz 0.1 V_{p-p} sine wave to v_{FG}.
4. Obtain a printout showing v_{IN} and v_{OUT}.
5. Measure and *Plot* the gain and phase response from 10 Hz to 500 kHz.[a]
6. Measure the −3 dB points.
7. Measure or Estimate the unity gain bandwidth[b] What is the phase at this point?

[a] Ensure that the amplitude of the output is large enough to reliably measure the peak to peak value. You may need to increase the input amplitude at higher frequencies.
[b] This is the frequency when $|v_{OUT}| = |v_{IN}|$.

Task 7.4.4: Op-amp gain bandwidth measurement

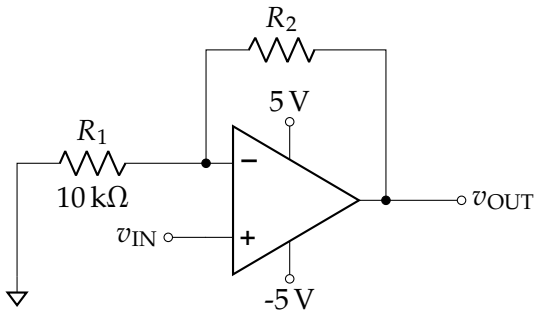

Figure 7.8: A non-inverting amplifier circuit.

1. Complete the following steps using $R_2 = 100\,\text{k}\Omega, 150\,\text{k}\Omega,$ and $220\,\text{k}\Omega$:
   a) *Determine* the expected gain of the amplifier.
   b) Using a sinusoid as v_{IN}, *select* an amplitude that produces a non-distorted output.
   c) Measure and *Plot* the gain versus frequency from 10 Hz to 1 MHz.
   d) From the gain plot, estimate the −3 dB point. Use the measured gain at low frequency as your reference gain.[a]
   e) Measure the phase at the −3 dB points.
2. What is the relationship of the gain bandwidth products over the different gains?

[a] For example, if you calculate that the gain should be 18 but the gain at 10 Hz is only 17.5, then your −3 dB point is when the gain is $0.707 \cdot 17.5$.