EXPERIMENT 10

Switching circuits: DC voltage regulation

10.1 Application

The simple RLC circuit is used in almost every power supply and electronic device sold today. With the addition of a couple of switches, an RLC circuit can be used to efficiently regulate voltages to different levels. While the circuits in actual devices contain more sophisticated control logic, the core method for efficiently regulating voltage is the RLC circuit.

Switching voltage converters are used to allow ultra lower power devices get usable voltages to run their circuitry as well as step high voltage and high power supplies down to low voltages very efficiently. They are essential to any modern circuit or system design.

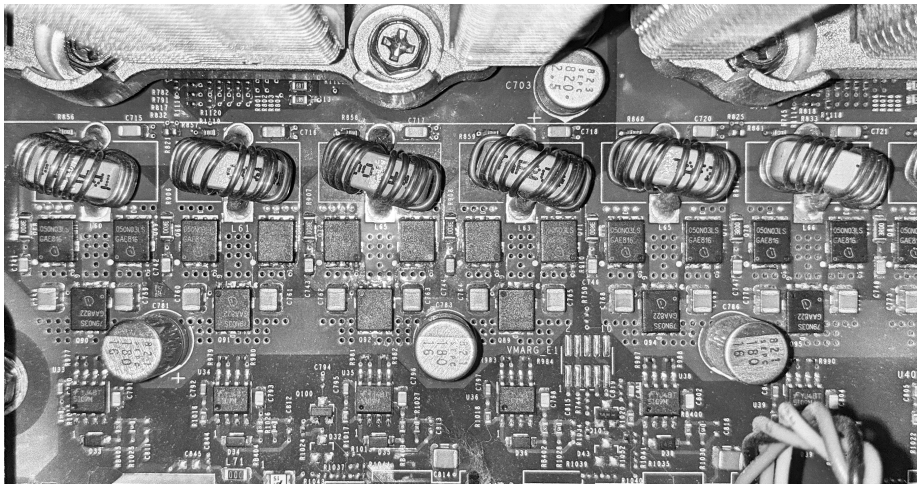
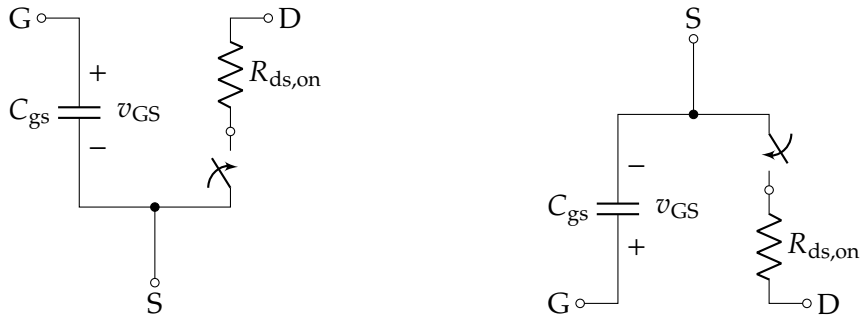


Figure 10.1: An array of switching voltage regulators on a motherboard. Multiple regulators are necessary as some processors can continuously draw over 100 A!

10.2 Semiconductor switches

In order to simplify the analysis of circuits with metal-oxide-semiconductor field-effect transistors (MOSFETs) and diodes used as switches, we will use an easy to apply model of each as a near ideal voltage controlled switch.

10.2.1 Simple MOSFETs switch model



(a) NMOS (b) PMOS

Figure 10.2: MOSFET switch models

When used in a switching application, a simpler model of the MOSFET can be used. The core requirement for using this model is that the transistor will always be in either linear/triode or cutoff operation. Electrically, this means that $V_{GS} \gg V_{th}$ for NMOS or $V_{GS} \ll V_{th}$ for PMOS. If this condition is not satisfied, then the transistor may enter saturation which leads to a large amount of power dissipation in the switch.

There are two dominant parasitics in the MOSFET switch. The first, resistance from drain to source ($R_{DS(on)}$), is the effective resistance of the channel when the transistor is on. It causes a voltage drop across the device and sets an upper limit on the amount of current that can flow through the device. Ideally, $R_{DS(on)}$ is as close to zero as possible. The N-Channel logic level power MOSFET (RFD3055LE) [1] we will use in this lab has a $R_{DS(on)}$ of $0.15\,\Omega$ as its maximum current of 12 A. While $0.15\,\Omega$ may not seem like much, this means that there will be a 1.8 V across the transistor at maximum load!

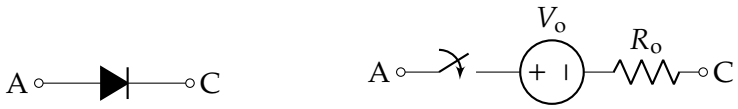
The second major parasitic of power MOSFETs is gate capacitance. As we saw in experiment 2, we can use a varying duty cycle square wave to control a power MOSFET. This means that we must fully charge and discharge the gate of the MOSFET every switching cycle. The large gate capacitance of power MOSFETs means that a large amount of current is needed to change the gate voltage quickly. The gate capac-

itance sets an overall limit on the switching frequency of a MOSFET for a given driver circuit[1]. The datasheet for a power MOSFET typically specifies input, output, and reverse transfer capacitance. C_{gs} can be estimated as $C_{gs} = C_{iss} - C_{rss}$.

[1] It is not uncommon to see transistor gate driver circuits in order to amplify a signal to drive a large power MOSFET from a weaker signal source. The driver circuit is able to drive the large capacitance and may use larger voltages to ensure the transistor fully turns on

10.2.2 Diodes

The switch model of a diode is shown in figure 10.3. The diode acts like a switch that is only closed when $V_A - V_C > V_o$. The diode linear model voltage (V_o) and diode linear model resistance (R_o) model the fact that a diode does not conduct a significant amount of current until the forward voltage is high enough. Ideally, the voltage and resistance are as close to zero as possible. This is why Schottky diodes are used in power electronics as they are the most widely available diodes with a low turn on voltage.



(a) Circuit Symbol (b) Model

Figure 10.3: The Diode Switch Model

The voltage dropped across a diode is a major source of loss of efficiency in switching power circuits, especially when working at low voltages. In order to further simplify analysis, we will assume that the transistor switches and diodes are fully ideal in this experiment; however, this will lead to error in the constructed circuits. It is for this reason that the ideal voltage conversion switching circuits are not used without additional control circuitry to automatically compensate for the losses.

10.3 Switched RLC circuits

In this experiment, we will analyze three different switched RLC circuits. Each circuit uses two switches in order to control the circuit behavior. We will be using a function generator to control the MOSFET switches, but in actual designs there are dedicated integrated circuits (ICs) that would generate the correct frequency and duty cycle square waves to control the switches.

10.3.1 Buck converter

The buck converter is an application of an RLC circuit that takes a large input voltage and efficiently produces a smaller

output voltage. The circuit for a buck converter is shown in figure 10.4. The buck converter has three stages:

1. S_1 is closed and S_2 is open. The circuit is a driven RLC circuit.
2. S_1 is open and S_2 is closed. The circuit is an undriven RLC circuit.
3. Both switches are open. The circuit is a first order RC circuit.

The duration of the first stage is set by a control signal. The control signal is a square wave with period T and duty cycle D. The second stage allows the inductor to fully discharge into the circuit. As soon as $i_L(t) = 0$, the circuit will move into the third stage with both switches open. Depending on the values of the components and switching frequency, the circuit may never enter the third stage.

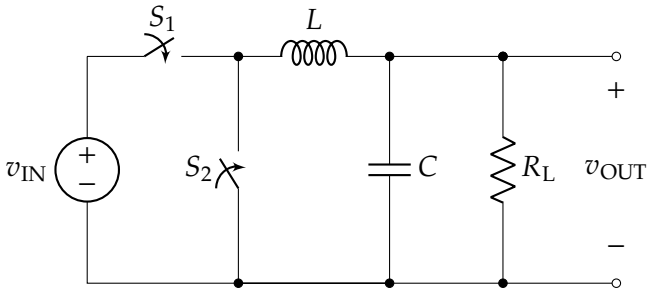


Figure 10.4: A buck converter circuit.

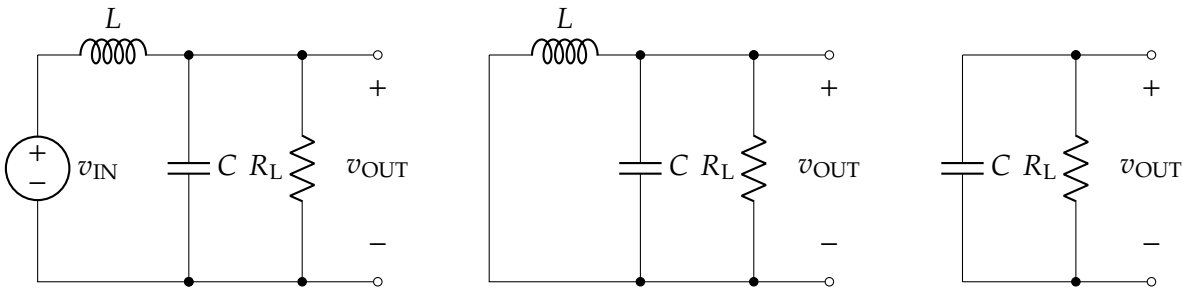
In order to understand how this circuit works, we must find the equilibrium response. The circuit is at equilibrium when the voltage and current at the beginning and the end of a period are equal. As long as the load stays the same, every period will have the same behavior. We can apply the equilibrium conditions to find equation (10.1) and equation (10.2).

$$\begin{aligned} i_L(T) &= i_L(0) \\ i_L(T) - i_L(0) &= 0 \\ \frac{1}{L}\int_0^T v_L(t)\,\mathrm{d}t &= 0 \end{aligned} \tag{10.1}$$

$$
\begin{aligned}
v_C(T) &= v_C(0) \\
v_C(T) - v_C(0) &= 0 \\
\frac{1}{C}\int_0^T i_C(t)\,\mathrm{d}t &= 0 \qquad (10.2)
\end{aligned}
$$

A full analysis of the RLC circuits can be performed to predict the response of the converter; however, finding the equilibrium point without any assumptions is difficult.(2) The key assumption needed is that the output voltage has negligible ripple. This assumption can be made as long as the time constant for the circuit $\tau = RC$ is much larger than the switching period T. This typically involves picking a sufficiently large capacitor or increasing the switching frequency. With this assumption, we can treat the output as a DC voltage.

(2) As part of the design process for a converter, it is useful to make a first order estimate with assumptions then simulate the response using SPICE.



(a) S1 on, S2 off (b) S1 off, S2 on (c) S1 off, S2 off

Figure 10.5: Buck converter operation

Finding $i_L(t)$ In section 10.3.1, we can use the assumption that the output voltage is effectively constant to say that $v_L(t) = v_{IN} - v_{OUT}$. After DT seconds pass, S_1 opens and S_2 closes, yielding the circuit in section 10.3.1. In this stage, $v_L(t) = -v_{OUT}$. Once the current in the inductor drops to 0, S_2 opens, and the circuit becomes section 10.3.1. In this stage, $v_L(t) = 0$. When all three stages occur, $i_L(T) = i_L(0) = 0$, so the equilibrium condition is satisfied.

These can be plugged into equation (10.1) to find the inductor current.

$$
i_L(t) = \begin{cases}
\frac{1}{L}\int_0^t v_{IN} - v_{OUT}\,\mathrm{d}s = \frac{t}{L}(v_{IN} - v_{OUT}) & 0 < t \le DT \\
i_L(DT) + \frac{1}{L}\int_{DT}^t -v_{OUT}\,\mathrm{d}s = \frac{DT}{L}(v_{IN} - v_{OUT}) - \frac{t-DT}{L}v_{OUT} & DT < t \le DT\frac{v_{IN}}{v_{OUT}} \\
0 & DT\frac{v_{IN}}{v_{OUT}} < t \le T
\end{cases}
$$

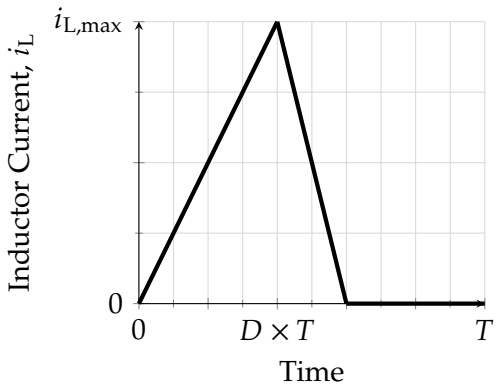


Figure 10.6: Buck converter inductor current

A plot of the inductor current is shown in figure 10.6

Because the circuit is in equilibrium, all of the energy that enters the circuit must be dissipated by the load in the same period. The net result of this is that the average current through the inductor must be the same as the average current through the load.

Current is a measure of coulombs per second, so the average current over a period can be used to measure the total amount of charge that enters a circuit. When the circuit is in equilibrium, the same amount of charge must enter in a single period that leaves in a single period; therefore, the average current in needs to be the same as the average current out. Since $i_L(t)$ is triangular, we can easily evaluate its intergral using $A = \frac{1}{2}BH$, where A is the area of a triangle, B is the length of the base, and H is the height.

$$\frac{1}{T}\int_0^T i_L(t)\,\mathrm{d}t = \frac{v_{\mathrm{OUT}}}{R}$$

$$\frac{1}{2T}DT\frac{v_{\mathrm{IN}}}{v_{\mathrm{OUT}}}\frac{DT}{L}(v_{\mathrm{IN}} - v_{\mathrm{OUT}}) = \frac{v_{\mathrm{OUT}}}{R}$$

$$v_{\mathrm{OUT}} = Dv_{\mathrm{IN}}\frac{\sqrt{8RLT + D^2R^2T^2} - DRT}{4L} \tag{10.3}$$

If the desired input and output voltages are known, the duty cycle D can be calculated by solving equation (10.3):

$$D = \frac{\sqrt{2v_{\mathrm{OUT}}}}{\sqrt{\frac{RTv_{\mathrm{IN}}}{L}\left(\frac{v_{\mathrm{IN}}}{v_{\mathrm{OUT}}} - 1\right)}} \tag{10.4}$$

Notice that the capacitance does not factor into this equation. That is due to the small ripple assumption. As long as the

capacitor is big enough, we can use this solution to solve for the duty cycle needed.

The analysis of the converter is much simpler if the inductor current never reaches zero, as switch S_2 never reopens.

$$i_L(t) = \begin{cases} i_L(0) + \frac{t}{L}(v_{\text{IN}} - v_{\text{OUT}}) & 0 < t \leq DT \\ i_L(0) + \frac{DT}{L}(v_{\text{IN}} - v_{\text{OUT}}) - \frac{t-DT}{L} v_{\text{OUT}} & DT < t \leq T \end{cases}$$

In order to solve for the equilibrium case, we set $i_L(T) = i_L(0)$:

$$\begin{aligned} i_L(0) = i_L(0) + \frac{DT}{L}(v_{\text{IN}} - v_{\text{OUT}}) - \frac{T - DT}{L} v_{\text{OUT}} \\ v_{\text{OUT}} = D v_{\text{IN}} \end{aligned} \tag{10.5}$$

Equation (10.5) is only valid when

$$D > 1 - \frac{2L}{RT} \tag{10.6}$$

If this condition is not satisfied, then the current will go to 0 and equation (10.3) must be used.

10.3.2 Boost converter

Many devices need a larger voltage than supplied by the power source. In order to generate the higher voltages, a boost converter is used. The schematic for a boost converter is shown in figure 10.7

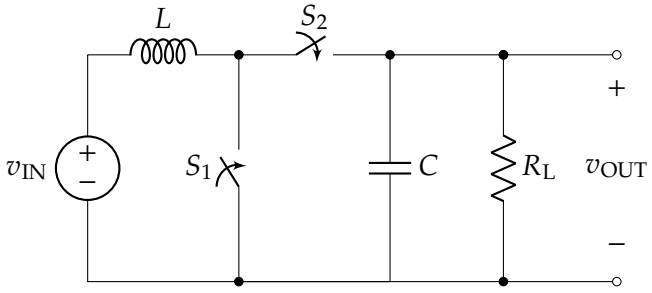


Figure 10.7: A boost converter circuit.

The three stages of operation are:

1. S_1 is closed and S_2 is open. The circuit is an L circuit and an RC circuit.
2. S_1 is open and S_2 is closed. The circuit is a driven RLC circuit.

3. Both switches are open. The circuit is a first order RC circuit.

The time that S_1 stays closed is once again set by the duty cycle D. Then, S_2 remains closed until $i_L(t)$ reaches zero. Just like the buck converter, it is possible that the third state does not occur if the inductor current never reaches zero.

The boost converter is solved using the same procedure as the buck converter. First, the inductor current is found in all three stages.

$$i_L(t) = \begin{cases} \frac{1}{L}\int_0^t v_{\text{IN}}\,\mathrm{d}s = \frac{t}{L}v_{\text{IN}} & 0 < t \leq DT \\ i_L(DT) + \frac{1}{L}\int_{DT}^t (v_{\text{IN}} - v_{\text{OUT}})\,\mathrm{d}s = \frac{DT}{L}v_{\text{IN}} + \frac{t-DT}{L}(v_{\text{IN}} - v_{\text{OUT}}) & DT < t \leq DT\frac{v_{\text{OUT}}}{v_{\text{OUT}}-v_{\text{IN}}} \\ 0 & DT\frac{v_{\text{OUT}}}{v_{\text{OUT}}-v_{\text{IN}}} < t \leq T \end{cases}$$

By setting the average inductor current equal to the average load current, the relationship for input and output can be determined.

$$\frac{D^2 T v_{\text{IN}} v_{\text{OUT}}}{2L(v_{\text{OUT}} - v_{\text{IN}})} = \frac{v_{\text{OUT}}}{R_{\text{L}}}$$

$$v_{\text{OUT}} = v_{\text{IN}}\left(1 + \frac{D^2 RT}{2L}\right) \tag{10.7}$$

$$D = \sqrt{\frac{2L(v_{\text{OUT}} - v_{\text{IN}})}{RT v_{\text{IN}}}} \tag{10.8}$$

In the case where the inductor never fully discharges, the equation for v_{OUT} simplifies:

$$v_{\text{OUT}} = \frac{v_{\text{IN}}}{1 - D} \tag{10.9}$$

Equation (10.9) is only valid when

$$D(1 - D) < \frac{2L}{RT} \tag{10.10}$$

If equation (10.10) is not satisfied, then equation (10.7) must be used.

10.3.3 Inverting boost converter

Some devices need a negative supply voltage generated from only one DC source. In order to generate the negative voltages,

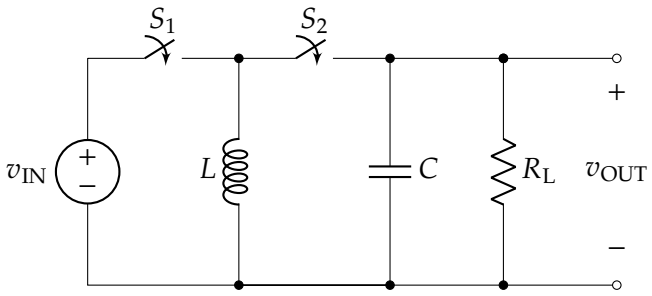


Figure 10.8: An inverting boost converter circuit.

an inverting boost converter is used. The schematic for an inverting boost converter is shown in figure 10.8

The three stages of operation are:

1. S_1 is closed and S_2 is open. The circuit is an L circuit and a RC circuit.
2. S_1 is open and S_2 is closed. The circuit is an undriven RLC circuit.
3. Both switches are open. The circuit is a first order RC circuit.

We once again start from the inductor current. v_{OUT} will be negative, so keep that in mind when reading the equations.

$$i_L(t) = \begin{cases} \frac{1}{L}\int_0^t v_{IN}\,ds = \frac{t}{L}v_{IN} & 0 < t \le DT \\ i_L(DT) + \frac{1}{L}\int_{DT}^t v_{OUT}\,ds = \frac{DT}{L}v_{IN} + \frac{t-DT}{L}v_{OUT} & DT < t \le DT\frac{v_{OUT}-v_{IN}}{v_{OUT}} \\ 0 & DT\frac{v_{OUT}-v_{IN}}{v_{OUT}} < t \le T \end{cases}$$

The relationship between input and output can be determined by setting the average load current equal to the average inductor current.

$$\frac{D^2 T v_{IN}(v_{OUT} - v_{IN})}{2Lv_{OUT}} = -\frac{v_{OUT}}{R_L}$$

$$v_{OUT} = -\frac{Dv_{IN}}{4L}\left(RDT + \sqrt{R^2D^2T^2 + 8RTL}\right) \qquad (10.11)$$

$$D = \sqrt{\frac{2Lv_{OUT}^2}{RTv_{IN}(v_{IN} - v_{OUT})}} \qquad (10.12)$$

v_{OUT} again simplifies when $i_L(t)$ never reaches zero:

$$v_{\text{OUT}} = -v_{\text{IN}} \frac{D}{1-D} \tag{10.13}$$

Equation (10.13) is only valid when

$$D > 1 - \frac{2L}{RT} \tag{10.14}$$

otherwise, the current will reach 0 A and equation (10.11) must be used.

10.4 Prelab

Task 10.4.1: Prelab questions

1. *Calculate* the gate capacitance C_{gs} for the RFD3055LE and P-Channel QFET® power MOSFET (FQU17P06) [2] using the C_{iss} and C_{rss} values in the datasheets.
2. How long will it take a function generator with 50 Ω output resistance to charge the gate of the RFD3055LE from 0 V to the maximum V_{th} in the datasheet using a 5 V input?
3. What is the fastest frequency that the FQU17P06 gate can be switched from 0.1 V to 4.9 V and back to 0.1 V from a function generator with 50 Ω output impedance switching from 0 V to 5 V?
4. For the following prelab tasks, use $L = 1$ mH and $C = 10$ µF. Hint: A resistor can be used as a primitive model of a load with a known voltage and current draw using $R = {}^{V_{out}}/_{I_{load}}$. Assume the potentiometer is set such that $v_{IN} = 0$ V
   a) *Design* the 10 V supply needed in task 10.5.4 by *Selecting* D and T. Use $0.3 < D < 0.7$ and $25\,\text{kHz} < \frac{1}{T} < 100\,\text{kHz}$. You will need to use equation (10.7) or equation (10.9).
   b) *Design* the −10 V supply needed in task 10.5.4 by *Selecting* D and T. Use $0.3 < D < 0.7$ and $25\,\text{kHz} < \frac{1}{T} < 100\,\text{kHz}$. You will need to use equation (10.11) or equation (10.13).
   c) *Draw* the overall circuit showing how the boost, inverting boost, and opamp are connected.

10.5 Tasks

Task 10.5.1: Buck converter

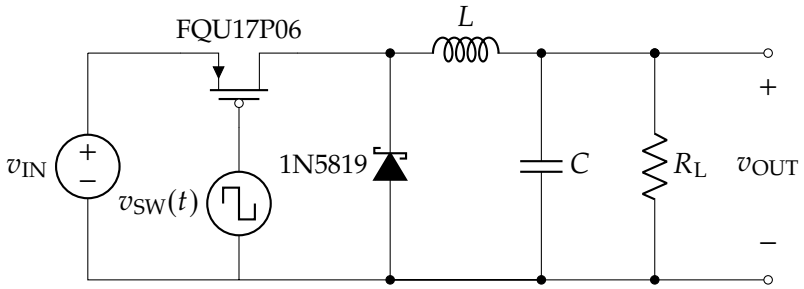


Figure 10.9: A buck converter circuit.

1. *Compute* the theoretical $v_{OUT,avg}$ given $L = 1\,\text{mH}$, $C = 10\,\mu\text{F}$, $R_L = 330\,\Omega$, $v_{IN} = 5\,\text{V}$, and $v_{SW}(t)$ is a $-5\,\text{V}$ to $5\,\text{V}$ 100 kHz square wave with duty cycle $D = 50\%$.
2. *Construct* the circuit in figure 10.9 with the above values.
3. *Measure* the v_{pp} and $v_{OUT,avg}$ with the oscilloscope set to a vertical scale of 100 mV/div. *Calculate* the error for $v_{OUT,avg}$.
4. *Capture* two screenshots of output $v_{OUT}(t)$: One with a vertical scale of 100 mV/div and one with a vertical scale of 1V/div.
5. *Measure* the efficiency of the conversion P_{out}/P_{in}.[a]
6. *Measure* and *plot* $v_{OUT,avg}$ vs. duty cycle of the switch. For this circuit, the duty cycle of the switch is not the duty cycle of the function generator. Instead, $D_{SW} = 1 - D_{FG}$.

[a] Assume that P_{in} can be calculated from the voltage and current reading on the power supply unit. If your power supply unit does not indicate the output current, you should use a multimeter to measure current.

Task 10.5.2: Boost converter

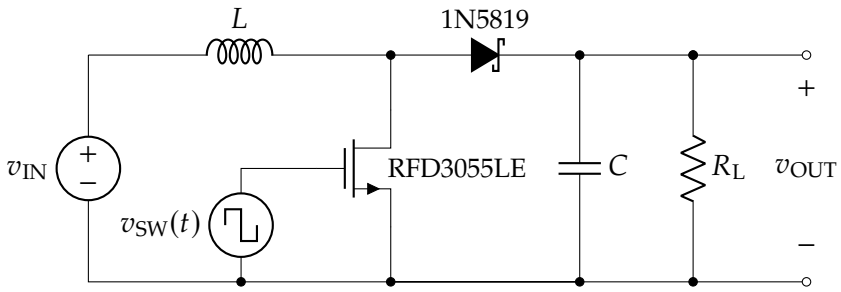


Figure 10.10: A boost converter circuit.

1. *Compute* the duty cycle of the switch needed for $v_{OUT} = 10\,V$ given $L = 1\,mH$, $C = 10\,\mu F$, $R_L = 680\,\Omega$, $v_{IN} = 5\,V$, and $v_{SW}(t)$ is a 0 V to 5 V 100 kHz square wave.
2. *Construct* the circuit in figure 10.10 using the above values.
3. *Measure* the v_{pp} and $v_{OUT,avg}$ with the oscilloscope set to a vertical scale of 200 mV/div. *Calculate* the error for $v_{OUT,avg}$.
4. *Capture* two screenshots of output $v_{OUT}(t)$: One with a vertical scale of 200 mV/div and one with a vertical scale of 1 V/div.
5. *Measure* the efficiency of the conversion P_{out}/P_{in}.[a]

[a] Assume that P_{in} can be calculated from the voltage and current reading on the power supply unit. If your power supply unit does not indicate the output current, you should use a multimeter to measure current.

Task 10.5.3: Inverted boost converter

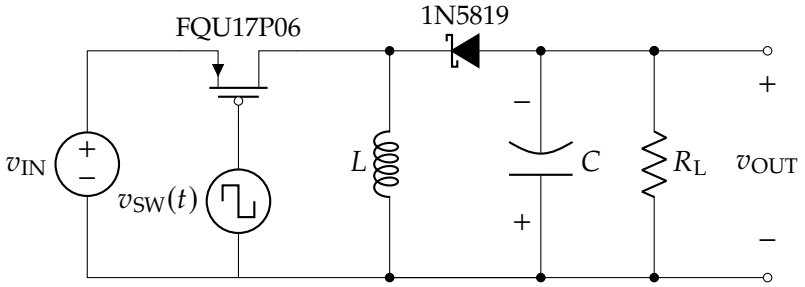


Figure 10.11: An inverted boost converter circuit.

1. *Compute* the duty cycle of the switch needed for $v_{OUT} = -10\,V$ given $L = 1\,mH$, $C = 10\,\mu F$, $R_L = 680\,\Omega$, $v_{IN} = 5\,V$, and $v_{SW}(t)$ is a −5 V to 5 V 100 kHz square wave.
2. *Construct* the circuit in figure 10.11 using the above values. *Recall* that for the PMOS switch, $D_{SW} = 1 - D_{FG}$. Also *ensure* that any electrolytic capacitors are installed in

the correct polarity, as shown in figure 10.11.

3. *Measure* the v_{pp} and $v_{OUT,avg}$ with the oscilloscope set to a vertical scale of 200 mV/div. *Calculate* the error for $v_{OUT,avg}$.

4. *Capture* two screenshots of output $v_{OUT}(t)$: One with a vertical scale of 200 mV/div and one with a vertical scale of 1 V/div.

5. *Measure* the efficiency of the conversion P_{out}/P_{in}.[a]

[a] Assume that P_{in} can be calculated from the voltage and current reading on the power supply unit. If your power supply unit does not indicate the output current, you should use a multimeter to measure current.

Task 10.5.4: Dual rail power supply design

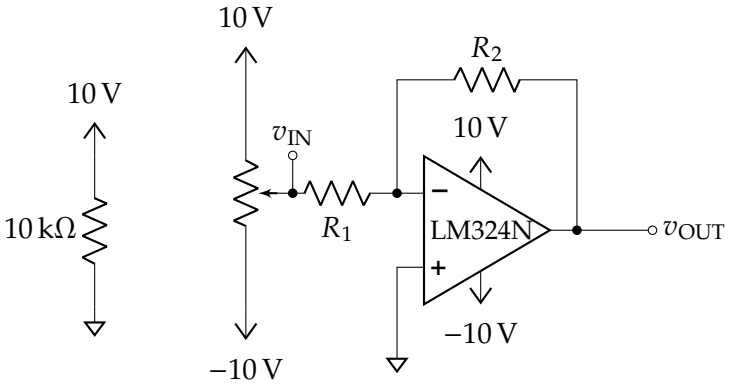


Figure 10.12: An inverting amplifier circuit.

In this task, you will design your own dual rail power supply to drive the operational amplifier in the inverting amplifier circuit from a 5 V USB power supply.

1. *Design* a dual rail power supply that outputs both 10 V and −10 V. The Low-Power Quad-Operational Amplifiers (LM324N) [3] draws approximately 4 mA. You will need both outputs of the function generator.

2. *Pick* an appropriate R_1 and R_2 so that the op-amp has a gain of −4.7. Pick R_1 and R_2 to both be greater than 10 kΩ.

3. *Construct* the designed circuit with the op amp connected. **Do not turn on the circuit without the opamp connected to the positive supply or the voltage will increase without bound!**

4. *Adjust* the duty cycles[a] on the function generator to fine tune the output voltages to the designed ±10 V.

5. *Measure* v_{IN} and v_{OUT} while varying the potentiometer. *Plot* v_{OUT} vs. v_{IN}.

[a] In a real switching power supply, there are circuits that automatically adjust the duty cycle based on a feedback system.

10.6 References

[1] *RFD3055LE, RFD3055LESM n-channel log level power MOSFET*, RFD3055LE, Rev C0, Fairchild Semiconductor, Sep. 2013. [Online]. Available: `https://www.onsemi.com/pub/Collateral/RFD3055LESM-D.pdf`.

[2] *FQD17P06 / FQU17P06 p-channel QFET® MOSFET*, FQU17P06, Rev C3, Fairchild Semiconductor, Apr. 2014. [Online]. Available: `https://www.onsemi.com/pub/Collateral/FQU17P06-D.pdf`.

[3] *LMx24-N, LM2902-N low-power, quad-operational amplifiers*, LM324N, SNOSC16D, Texas Instruments Inc., Jan. 2015. [Online]. Available: `http://www.ti.com/lit/ds/symlink/lm324-n.pdf`.