EXPERIMENT 5

MOSFET Differential Amplifier with Current Mirror

5.1 Application

In practical terms one of the many useful applications of a differential amplifier is in noise resistant circuits. Consider that all electrical circuits require two conduction paths—an outgoing (a) and return (b) path. The signal (y) is the voltage difference between them, thus

$$y = a - b$$

If a noise signal (N) couples onto those conductors, it will produce a similar change on both:

$$y = (a + N) - (b + N)$$

If the receiver design is based on a differential amplifier, it will amplify the difference while rejecting the noise, which allows for reconstructing the original signal:

$$\begin{aligned} y &= (a + N) - (b + N) \\ y &= a + N - b - N \\ y &= a - b \end{aligned}$$

Most modern digital communication systems use differential amplifiers in their receivers: memory, CPU to CPU, and PCIe buses, HDMI, USB, Thunderbolt, Ethernet, and many more. Differential amplifiers also serve as the input stage to operational amplifiers (op amps), which form the basis of most modern analog circuits.

Figure 5.1: Four twisted pairs are used in CAT6 ethernet cable to carry differential signals. This allows for sending data long distances through potentially electrically noisy environments.

5.2 Background

If we consider the two-port circuits we have studied so far, they have a significant limitation: their output depends on a single input. In mathematics, any operation that acts on only one variable is called a *unary* operator, e.g., $\sin(x)$. To create useful systems, *binary* operators that act on two inputs are essential.

In case you have not realized it yet, $y = a + b$ and $y = a - b$ are examples of binary operators. Without a binary circuit a designer cannot add, subtract, multiply, etc.

This lab focuses on the basic building block of the majority of real-world amplifiers and signal processing systems, the differential amplifier.(1)

(1) The simplest useful differential amplifier circuits are called the "differential pair" when built from bipolar junction transistors (BJTs) or the "source-coupled differential pair" when built from metal-oxide-semiconductor field-effect transistors (MOSFETs), however, both are very similar.

Differential amplifiers are widely used in modern analog and digital design. For example, they are typically the first stage of the ubiquitous op amp device. In fact, the MOSFET differential amplifier will be developed into a two-stage op amp in experiment 6.

This experiment investigates the MOSFET based differential amplifier with current source biasing. The entire circuit can be found in figure 5.9.

5.3 The differential amplifier

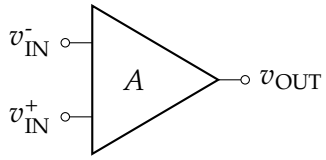

Figure 5.2: Schematic symbol for a differential amplifier.

As seen in figure 5.2, the differential amplifier is a three-terminal device. Terminals v_{IN}^- and v_{IN}^+ are inputs and v_{OUT} is the amplifier's output.

The first-order function of the ideal differential amplifier is to sense the voltage at each input, subtract them and multiply the result by a gain. In other words, the input-output characteristic is given by the following:

A differential amplifier can easily be confused with an op amp; however, there are noteworthy differences. Experiment 6 explores MOSFET op amps in depth, so for now note that differential amplifiers are only the first stage of most modern op amps.

$$v_{\text{OUT}} = A_{\text{d}} \left(v_{\text{IN}}^+ - v_{\text{IN}}^- \right) \tag{5.1}$$

5.3.1 Differential versus common mode input

Unfortunately, real differential amplifiers are non-ideal. To study the non-idealities it is helpful to break the input signal into two separate parts: the so-called differential and common mode components. We then use superposition to analyze the system's response to each part separately.

The differential input, v_d

We have already seen the differential input v_d. It is simply the difference between the two inputs v_{IN}^+ and v_{IN}^-; that is,

$$v_d = v_{IN}^+ - v_{IN}^- \tag{5.2}$$

The common mode input, v_{cm}

The common mode input v_{cm} is the average of the input signals v_{IN}^+ and v_{IN}^-; that is:

$$v_{cm} = \frac{1}{2}\left(v_{IN}^+ + v_{IN}^-\right) \tag{5.3}$$

In other words, the common mode input is the shared voltage between the two signals. By virtue of the subtraction in equation (5.1), this is the portion of the input that differential amplifier will reject, or, in other words, cancel out and not amplify.

It is sometimes useful to define v_{IN}^+ and v_{IN}^- in terms of their differential and common mode parts. The definition is as follows:

$$v_{IN}^- = v_{cm} - \frac{v_d}{2}$$
$$v_{IN}^+ = v_{cm} + \frac{v_d}{2}$$

5.3.2 The non-ideal differential amplifier

Reformulating equation (5.1) by splitting the input and gain terms into their differential (v_d, A_d) and common mode (v_{cm}, A_{cm}) forms results in the following input-output relationship:

$$v_{OUT} = A_d v_d + A_{cm} v_{cm} \tag{5.4}$$

An ideal differential amplifier has $A_{cm} = 0$ so equation (5.4) reduces to equation (5.1)

$$v_{OUT} = A_d v_d.$$

Reasonably well-designed differential amplifiers will have an A_{cm} that is many orders of magnitude smaller than A_d. None the less, we include the common mode term to ensure a thorough analysis. In practice, non-zero common mode gain can result from mismatches in the transistors and other circuit components.[2]

[2] Advancements in analog integrated circuit (IC) fabrication such as laser trimming and fuse arrays have significantly improved common mode rejection in many off the shelf amplifiers.

5.3.3 Measuring the performance of a differential amplifier: Common mode rejection ratio

The main figure of merit for measuring the quality of a differential amplifier is to compare the magnitude of the differential and common mode gains. To do so, one can use the common mode rejection ration (CMRR) metric. That is, the ratio of the differential gain to common-mode gain:

$$\text{CMRR} \equiv \frac{|A_d|}{|A_{cm}|}$$

Because well-designed differential amplifiers will have very large common mode rejection ratios, it is often expressed in decibels of power[3]

[3] Conversion from voltage gain to power gain is done assuming the input resistance is the same as the load resistance. Thus,

$$\frac{P_{out}}{P_{in}} = \frac{v_{out}^2/R_{load}}{v_{in}^2/R_{in}}$$
$$\frac{P_{out}}{P_{in}} = \frac{v_{out}^2}{v_{in}^2}$$
$$\frac{P_{out}}{P_{in}} = \left(\frac{v_{out}}{v_{in}}\right)^2 = A_V^2$$

Note that this makes the unit of measurement watts, not volts!

$$\text{CMRR (dB)} \equiv 20 \log \frac{|A_\text{d}|}{|A_\text{cm}|} \tag{5.5}$$

The INA226 [1], a current and power monitor IC from Texas Instruments, has a minimum CMRR of 166 dB. Even the LM358 [2] op amp released in 1976 has a CMRR of 80 dB.

5.4 Differential amplifier

Now that we have introduced the basic concepts of a differential amplifier, let us take a turn to the practical side and consider the actual design in figure 5.3. At the core of the circuit structure is a MOSFET matched pair[(4)] made from Q_1 and Q_2 biased by a constant current source. As was done in experiment 4, we will use a current mirror to realize the current source. For the moment, we will assume the current mirror has a nearly infinite output impedance. Finally, the amplifier is loaded with equal resistors R_D.

[(4)] By a matched pair we mean the two transistors with nearly equal parameters (k', $\frac{W}{L}$, and V_th)

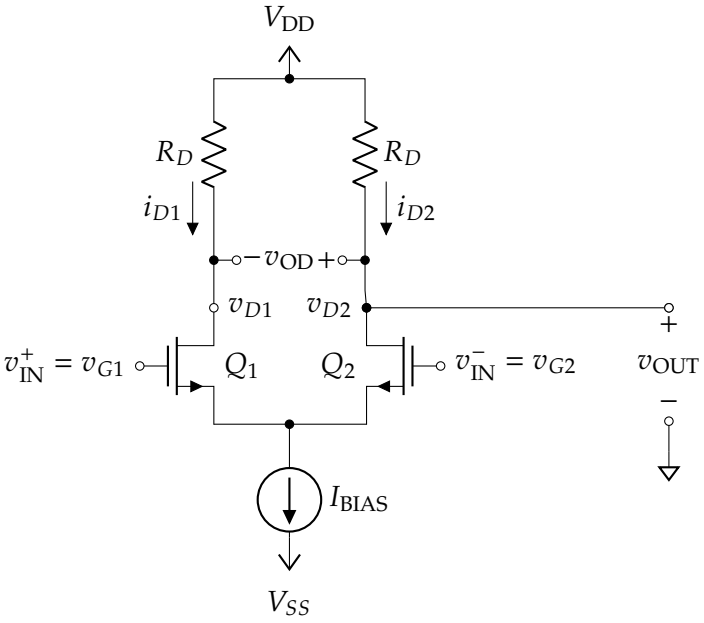

Figure 5.3: N-channel MOSFET (NMOS) differential amplifier with current source bias.

5.4.1 Large signal analysis

We begin by reminding ourselves that, when in the saturation region, the current through the drains of the two MOSFETs in figure 5.3 are equal to

$$i_{D1} = \frac{1}{2} k' \frac{W}{L} (v_{GS1} - V_\text{th})^2 \tag{5.6}$$

and

$$i_{D2} = \frac{1}{2} k' \frac{W}{L} (v_{GS2} - V_\text{th})^2 \tag{5.7}$$

It it worth noting that the analysis in this section applies to both AC and DC inputs and does not require any assumptions of small signal. However, we are using the equations of a MOSFET in saturation, so we do have to be careful to ensure they are all operating somewhere in that region.

Next, we apply Kirchoff's current law at the source network of Q_1 and Q_2 and arrive at the equation we will use to calculate the operation of the differential amplifier

$$i_{D1} + i_{D2} = I_{\text{BIAS}} \tag{5.8}$$

This relationship says that under all circumstances the current I_{BIAS} must split itself between the two branches of the differential pair.

Amplifier output due to common mode input

To get started, we consider how the circuit responds to a common mode input. First, we note that a signal composed entirely of common mode voltage results in $v_{G1} = v_{G2}$. Therefore, because Q_1 and Q_2 are matched, we will find that equation (5.6) and equation (5.7) evaluate to the same current, so

$i_{D1} = i_{D2}$. Combining this result with equation (5.8) leads to:

$$i_{D1} = i_{D2} = \frac{I_{\text{BIAS}}}{2}$$

Finally, we solve for v_{OUT} and find that:

$$v_{\text{OUT}} = V_{\text{DD}} - i_{\text{D2}} R_{\text{D}} = V_{\text{DD}} - \frac{I_{\text{BIAS}}}{2} R_{\text{D}} \tag{5.9}$$

Equation (5.9) shows that v_{OUT} is not affected by common mode inputs, as desired for an ideal differential amplifier.

As v_{GS} changes, i_D also changes; however, equation (5.9) shows the output is insensitive to common mode v_{GS}. This is a result of the current source I_{BIAS}. I_{BIAS} actively maintains a constant total current in the pair by adjusting the voltage dropped across itself. If a common mode increase in each transistor's gate voltages occurs, the current source will increase the voltage across it to ensure that v_{GS} never changes from its original value. This ensures that the original set current I_{BIAS} flows through the current source. This is one reason why a good current source is critical for quality common mode rejection.

Current steering

From equation (5.8) we know that I_{BIAS} splits between the two drain currents and that common mode input results in an even split. Now we consider what happens when a differential voltage is applied.

Consider the case when $v_{GS1} > v_{GS2}$. From equation (5.6) and equation (5.7) we deduce that $i_{D1} > i_{D2}$ because the transistors

If the parameters of a MOSFET are not matched, then an equal change in gate voltage can cause an unequal change in current while still satisfying equation (5.8). This results in a non-zero CMRR because some common mode input may "leak" into the output by virtue of the I_{BIAS} not perfecting splitting between the differential pair.

are matched. However, the sum of the drain currents must still equal I_{BIAS}, so $i_{D2} = I_{\text{BIAS}} - i_{D1}$.

By symmetry, $i_{D2} > i_{D1}$ when $v_{GS2} > v_{GS1}$. The relative values of the gate-source voltage "steer" a proportional amount of current through the associated drain. As a result, the current flowing through each R_{D} changes which leads to a corresponding change in v_{OUT}.

Similar to the common mode case, the current source enforces a constant current by adjusting the voltage drop across its own leads. This adjustment is common to both transistors' v_{GS} which allows I_{BIAS} to remain constant even though the gate voltages may change.

Small signal analysis: Voltage gain

As we continue our analysis of the differential amplifier, we need to find out how much it actually amplifies! We have seen that changing v_{GS1} and v_{GS2} relative to each other changes the current in each branch and therefore v_{OUT}. To completely understand the relationship, we convert figure 5.3 to its small signal equivalent, figure 5.4. Here, we assume that r_{o} is large enough that it can be safely ignored.[5]

[5] An assumption that should always be verified for a particular design.

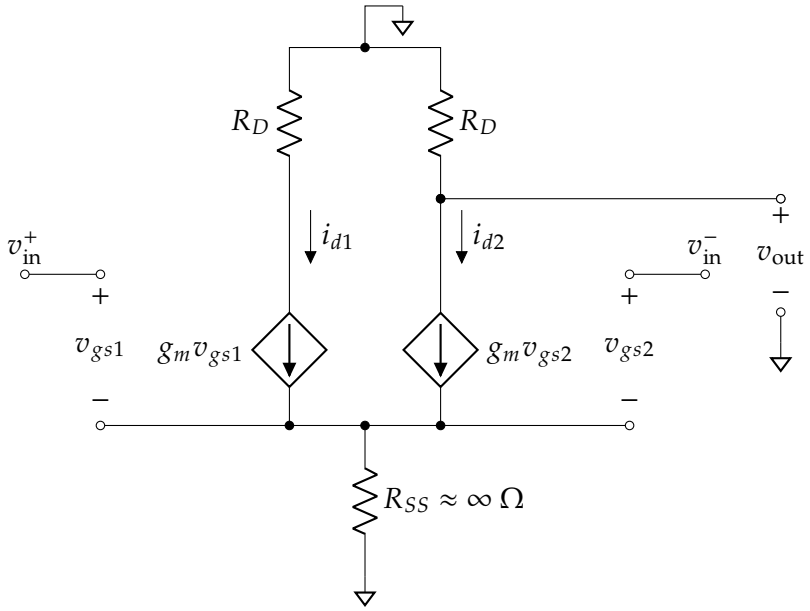

Figure 5.4: Small signal model of the differential amplifier in figure 5.3, assuming $r_o \gg R_{\text{D}}$

We proceed by leveraging superposition to simplify solving the circuit.[6] First, we look for a relationship between v_{out} and i_{d1} because we possess many tools to compute i_{d1}. We can use Ohm's law to find v_{out}:

$$v_{\text{out}} = -i_{d2} R_{\text{D}} = -g_m v_{gs2} R_{\text{D}} \tag{5.10}$$

Therefore, we must find an equation relating v_{gs2} and v_{in}^+ so that it can be substituted into equation (5.10) and ultimately

[6] This is only possible because the small signal models of a MOSFET are composed of only linear circuit elements. These calculations will not hold if the MOSFET DC bias changes significantly.

worked into formula for gain, that is, the ratio $v_{\text{out}}/v_{\text{in}}^{+}$.

We start the super position argument by selecting v_{in}^{+} to be the input signal and grounding v_{in}^{-}, that is $v_{\text{in}}^{-} = 0\,\text{V}$. The following facts resulting from these choices will be helpful as we continue the analysis

$$v_{gs2} = v_{g2} - v_s = -v_s \tag{5.11}$$

$$v_{gs1} = v_{g1} - v_s = v_{\text{in}}^{+} - v_s \tag{5.12}$$

Now we apply KCL by summing the currents feeding the source network, set them equal to zero, and simplify:

$$g_m v_{gs1} + g_m v_{gs2} = 0$$

$$v_{gs1} = -v_{gs2}$$

Using the observations from equation (5.11) and equation (5.12), we rewrite the last equation as:

$$v_{\text{in}}^{+} - v_s = v_s$$

$$v_s = \frac{v_{\text{in}}^{+}}{2}$$

We recall that we are ultimately after an equation for v_{gs2} in terms of v_{IN}^{+} and so return to equation (5.11) and arrive at

$$v_{gs2} = -\frac{v_{\text{in}}^{+}}{2}$$

Finally, we take equation (5.10) and replace v_{gs2} with the above result:

$$v_{\text{out,+}} = \frac{1}{2} g_m R_{\text{D}} v_{\text{in}}^{+} \tag{5.13}$$

One can work through a similar procedure to find v_{out} in terms of v_{in}^{-} when v_{in}^{+} is grounded. For the sake of brevity, we skip that derivation and jump directly to the final result, which is

$$v_{\text{out,-}} = -\frac{1}{2} g_m R_{\text{D}} v_{\text{in}}^{-} \tag{5.14}$$

Now, we complete the superposition argument by adding each calculated v_{out}:

$$\begin{aligned}
v_{\text{out}} &= v_{\text{out,+}} + v_{\text{out,-}} \\
v_{\text{out}} &= \frac{1}{2} g_m R_{\text{D}} v_{\text{in}}^{+} - \frac{1}{2} g_m R_{\text{D}} v_{\text{in}}^{-} \\
v_{\text{out}} &= \frac{1}{2} g_m R_{\text{D}} \left(v_{\text{in}}^{+} - v_{\text{in}}^{-} \right) = \frac{1}{2} g_m R_D v_{\text{d}}
\end{aligned}$$

Single-ended output gain

"Single ended output gain" refers to the gain when measuring only one of the differential amplifier outputs with respect to ground, which is just the value of v_{out} in **??**. We can compute the single-ended output gain as:

$$A_{\text{v}} = \frac{v_{\text{out}}}{v_{\text{d}}} = \frac{1}{2} g_m R_{\text{D}} \tag{5.15}$$

Differential output gain

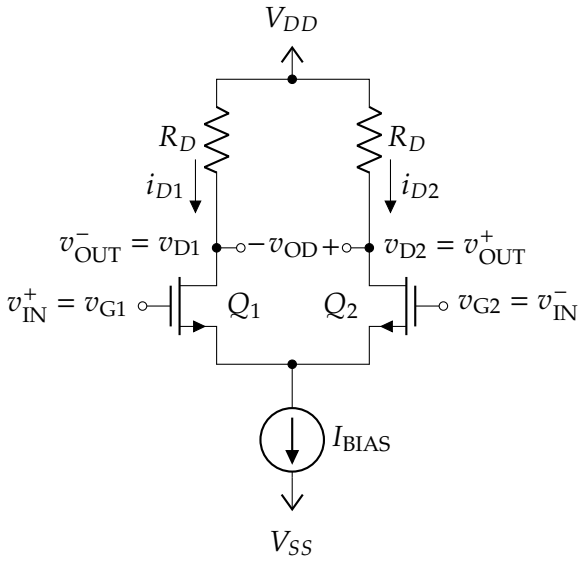

Figure 5.5: n-channel MOSFET (NMOS) differential amplifier with a differential output.

The output of a differential amplifier is defined as

$$v_{\text{OD}} = v_{\text{out}}^+ - v_{\text{out}}^- \tag{5.16}$$

For the amplifier in figure 5.5, it can be derived that the single-ended small signal gain observed at node v_{out}^- is just the negative of the gain observed at the node v_{out}^+.

$$\frac{v_{\text{out}}^-}{v_{\text{in}}^+ - v_{\text{in}}^-} = -\frac{v_{\text{out}}^+}{v_{\text{in}}^+ - v_{\text{in}}^-} = -\frac{1}{2} g_m R_{\text{D}} \tag{5.17}$$

Therefore, if the output is calculated using equation (5.16)

$$\begin{aligned} v_{\text{od}} &= v_{\text{out}}^+ - v_{\text{out}}^- \\ v_{\text{od}} &= \frac{1}{2} g_m R_{\text{D}} v_{\text{d}} - \left(-\frac{1}{2} g_m R_{\text{D}} v_{\text{d}} \right) \\ v_{\text{od}} &= g_m R_{\text{D}} v_{\text{d}} \end{aligned}$$

and, therefore,

$$A_{\mathrm{d}} = \frac{v_{od}}{v_{\mathrm{d}}} = g_m R_{\mathrm{D}} \tag{5.18}$$

5.4.2 The active load

For a fixed supply voltage, there is an inherent limit on the maximum $g_{\mathrm{m}} R_{\mathrm{D}}$ that can be built. Increasing g_{m} causes the output DC voltage to decrease and eventually the transistor will no longer be in saturation. Increasing R_{D} has the same effect, which requires the drain current (I_{D}) to be reduced to have the circuit function correctly. A common solution to this predicament is called an active load circuit, which is a structure that is very similar to a current mirror.[7] In section 5.4.1, the resistance r_{o} was assumed to be very large to simplify the analysis. Here, we consider what happens when, instead of ignoring it, the very large r_{o} of an active load's PMOS replaces R_{D} in the original differential amplifier design.

[7] Recall an ideal current source has infinite impedance.

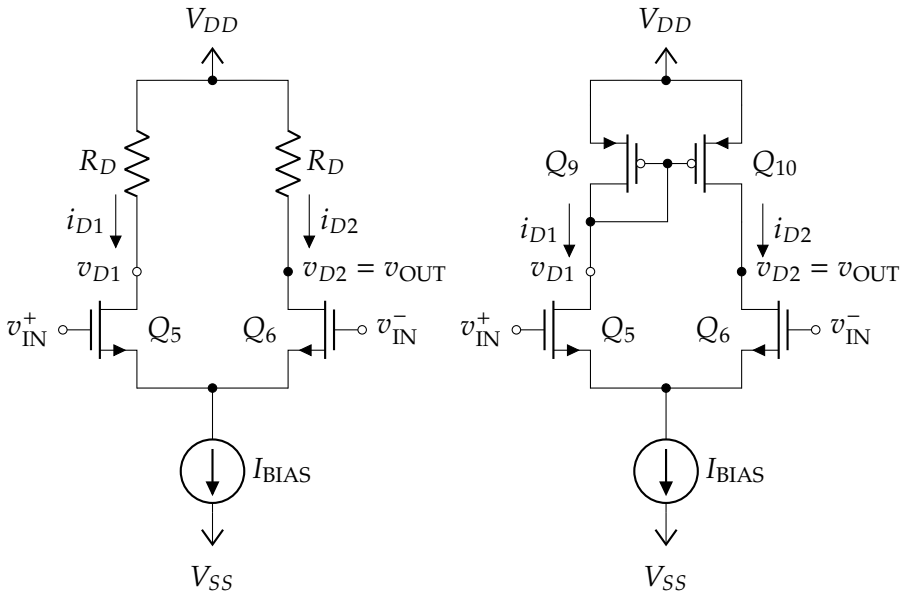

Figure 5.6: Comparison of resistive and active loads.

To analyze the active load in figure 5.6, we need to analyze the small signal model again. Unlike the resistively loaded differential amplifier, it is necessary to include the r_{o} values for both the NMOS ($r_{\mathrm{o,n}}$) and PMOS ($r_{\mathrm{o,p}}$) transistors. The value of r_{o} is calculated by finding the small signal resistance at the operating point of the transistors. This must be done

using the MOSFET equation with channel length modulation:

$$i_\mathrm{d} = \frac{1}{2}k'\frac{W}{L}(v_\mathrm{GS} - V_\mathrm{th})^2\,(1 + \lambda v_\mathrm{DS})$$

We want the small signal resistance, so we take the derivative. As $\lambda \ll 1$, i_d can be substituted in as an approximation.

$$\frac{1}{r_\mathrm{o}} = \frac{\partial i_\mathrm{D}}{\partial v_\mathrm{DS}} = \frac{1}{2}\lambda k'\frac{W}{L}(v_\mathrm{GS} - V_\mathrm{th})^2 \approx \lambda i_\mathrm{D} \Rightarrow r_\mathrm{o} \approx \frac{1}{\lambda i_\mathrm{D}}$$

Now that we know all the parameters, it is possible to analyze the small signal circuit using similar techniques used in the previous experiments. Because the NMOS transistors are identical and biased at the same current, they both have the same $g_\mathrm{m,n}$ and $r_\mathrm{o,n}$. Similarly, it is also true for the PMOS transistors' $g_\mathrm{m,p}$ and $r_\mathrm{o,p}$ — this will help simplify our analysis.

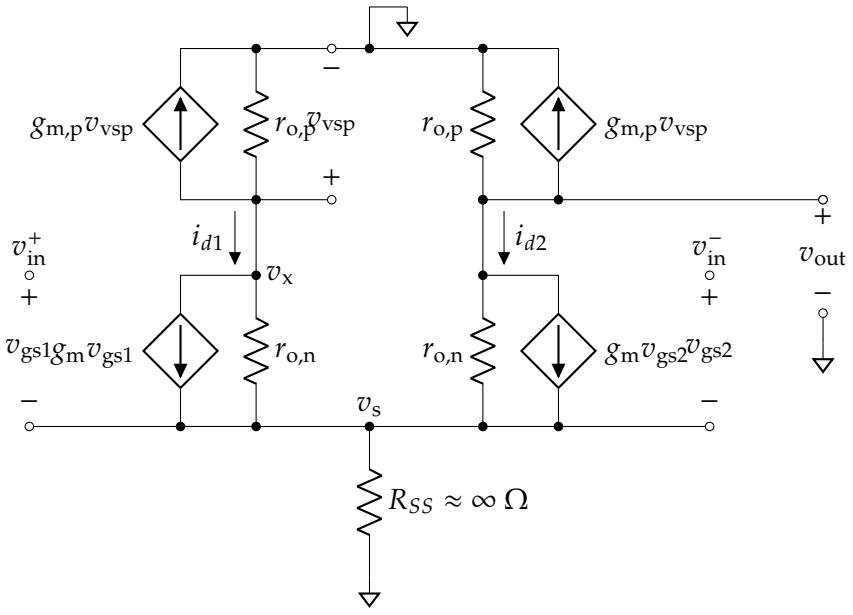

Figure 5.7: Small signal model of a differential amplifier with an active load.

Adding the resistances adds a lot of complexity to our circuit equations, but a careful application of nodal analysis and superposition can be used to solve the circuit. First, we assume $v_\mathrm{in}^- = 0$. This results in the following nodal equations:

$$\frac{v_\mathrm{x} - v_\mathrm{s}}{r_\mathrm{o,n}} + \frac{v_\mathrm{out} - v_\mathrm{s}}{r_\mathrm{o,n}} + g_\mathrm{m,n}\left(v_\mathrm{in}^+ - v_\mathrm{s}\right) + g_\mathrm{m,n}(-v_\mathrm{s}) = 0$$

$$\frac{v_\mathrm{x}}{r_\mathrm{o,p}} + g_\mathrm{m,p}v_\mathrm{x} + \frac{v_\mathrm{x} - v_\mathrm{s}}{r_\mathrm{o,n}} + g_\mathrm{m,n}\left(v_\mathrm{in}^+ - v_\mathrm{s}\right) = 0$$

$$\frac{v_\mathrm{out}}{r_\mathrm{o,p}} + g_\mathrm{m,p}v_\mathrm{x} + \frac{v_\mathrm{out} - v_\mathrm{s}}{r_\mathrm{o,n}} + g_\mathrm{m,n}\left(-v_\mathrm{s}\right) = 0$$

Those equations certainly do not look fun! The equations can be solved[8] for v_x, v_s, and v_{out} in terms of all the parameters that can be calculated from the DC bias. The equation for v_{out} can be used to find the gain of the circuit

[8] We recommend using an equation solver, but you could do it by hand.

$$v_{out} = \frac{g_{m,n} r_{o,n} r_{o,p} \left(1 + 2 g_{m,p} r_{o,p}\right)}{2 \left(r_{o,n} + r_{o,p}\right) \left(1 + g_{m,p} r_{o,p}\right)} v_{in}^{+}$$

Typically, $g_{m,p} r_{o,p} \gg 1$, so we can then simplify by taking the limit:

$$\frac{\left(1 + 2 g_{m,p} r_{o,p}\right)}{2 \left(1 + g_{m,p} r_{o,p}\right)} \approx 1$$

This simplifies the formula for v_{out} to:

$$v_{out} = g_{m,n} \frac{r_{o,n} r_{o,p}}{r_{o,n} + r_{o,p}} = g_{m.n} \left(r_{o,n} \parallel r_{o,p}\right) v_{in}^{+}$$

The v_{out} due to v_{in}^{-} is calculated using a similar procedure, which ultimately results in the final equation for v_{out}. The r_o's are significantly larger than the discrete resistors used in the original differential amplifier, so we can expect a huge increase in gain for this circuit. Amazingly, we can get this large increase in gain without increasing power consumption! Unfortunately, it is not all improvements. This method has negative effects on the maximum output swing and linearity.

$$v_{out} = g_{m,n} \left(r_{o,n} \parallel r_{o,p}\right) \left(v_{in}^{+} - v_{in}^{-}\right) = g_{m,n} \left(r_{o,n} \parallel r_{o,p}\right) v_d$$

5.5 Ratioed current mirror

In experiment 4, the current mirror was explored. To use less bias current and design multiple stage circuits, we need a current mirror that can have different output currents than input currents. The easiest parameter to control is W/L. When designing ICs, it is easy to adjust transistor width. Unfortunately, that cannot be done with discrete design; however, it is possible to design current mirrors that have integer multiples of the bias current.

5.6 Mirror analysis

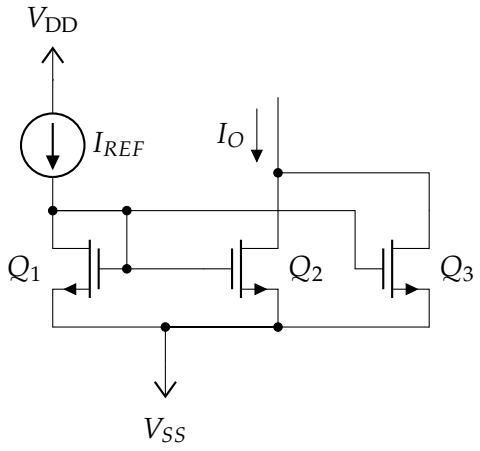

Figure 5.8: Basic MOSFET current mirror.

If Q_1, Q_2, and Q_3 are all the same size of MOSFET, then they will all have the same gate to source voltage (V_{GS}) and I_D. In this case, a simple application of Kirchoff's current law at the drains of Q_2 and Q_3 can be used to determine I_O:

$$I_O = I_{D,2} + I_{D,3} = 2I_{D,1}$$

5.7 Complete differential amplifier circuit

Now that we have both the differential amplifier and the current mirror building blocks, we can put them together to create a working differential amplifier. Taking the amplifier structure of figure 5.3, the ideal current source is replaced with a current mirror. A complete, and realizable, differential amplifier circuit is given in figure 5.9. As we will see in future experiments, this basic circuit structure is used as the front end in a large amount of modern analog circuity.

Symmetric output swing One common starting point when designing a differential amplifier is to aim for maximum symmetric output swing. One method of approximately achieving this requirement is to bias the amplifier such that its output voltage is roughly in the middle of V_{DD} and $V_G - V_{th}$ when $v_d = 0\,V$.

$$V_{out,DC} = \frac{V_{DD} + (V_G - V_{th})}{2} \tag{5.19}$$

V_G is the common mode voltage of the input signals. For this experiment, we will use $V_G = v_{CM} = 0\,V$. Biasing for maximum symmetric swing is not always the best choice. There are many trade offs that require consideration when designing a biasing scheme.

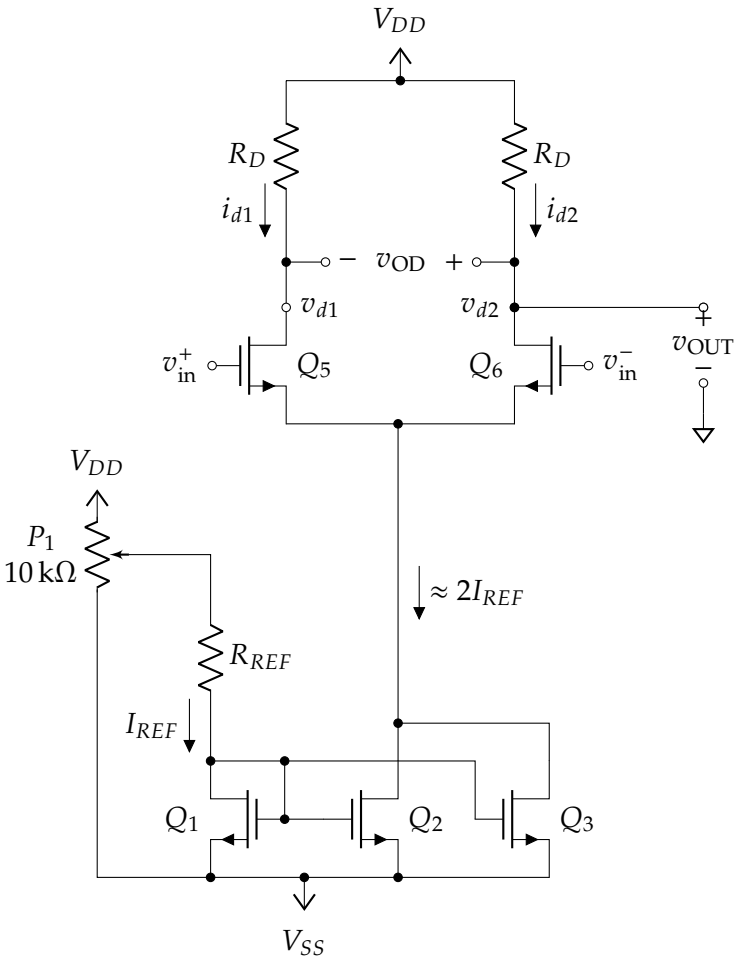

Figure 5.9: A MOSFET differential amplifier with current mirror biasing. Note $Q_{2,3}$ is a "ratioed current mirror" using both Q_2 and Q_3.

5.8 Prelab

Task 5.8.1: Prelab Questions

1. *Calculate* $v_{\text{out}}/v_{\text{in}}^-$ when v_{IN}^+ is grounded for the circuit in figure 5.4. The procedure is very similar to how $v_{\text{out}}/v_{\text{in}}^+$ was calculated.
2. *Select* an R_{D} and I_{REF} for the circuit in figure 5.9 that results in a single ended gain gain $A_v = 4$ and maximum symmetric output swing according to equation (5.19). R_{D} should be a standard value that is available to you. What is the expected value of I_{D} for each transistor?
3. *Calculate* the expected gain of the active load differential amplifier in figure 5.6 assuming the NMOS transistors are biased to the same I_{D} values from step 2.

5.9 Tasks

Please complete the following tasks assuming $V_{\text{DD}} = 5\,\text{V}$ and $V_{\text{SS}} = -5\,\text{V}$. Use $V_{\text{TN}} = 0.7\,\text{V}$, $k'_{\text{n}} = 32\,\mu\text{A}\,\text{V}^{-2}$, $V_{\text{TP}} = -0.7\,\text{V}$, $k'_{\text{p}} = 11\,\mu\text{A}\,\text{V}^{-2}$, $\frac{W}{L} = \frac{138}{7.8}$, $\lambda_n = 0.009$, and $\lambda_p = 0.008$. Use the ALD1106 for Q_1, Q_2, and Q_3. Use the ALD1105 for Q_5 and Q_6.

Also recall that g_{m} can be computed in terms of I_{D} and k' using the following relationship:

$$g_m = \sqrt{2\frac{W}{L}k' i_{\text{D}}}$$

Task 5.9.1: Build and test the ratioed current mirror

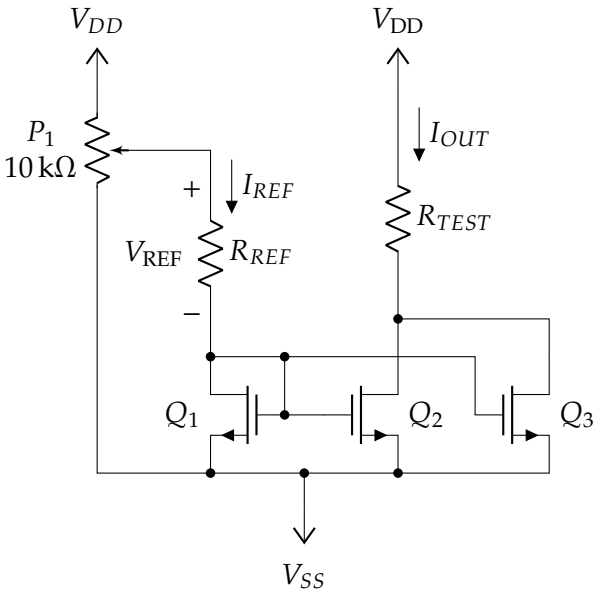

Figure 5.10: NMOS current mirror with test load.

For this task, use $V_{DD} = 5\,V$ and $V_{SS} = -5\,V$, and use the ALD1106 for the three MOSFETs.

1. *Select* R_{REF} and R_{TEST} so that all transistors stay in saturation over the test range of $0.1\,mA \leq I_{OUT} \leq 5\,mA$.
2. *Construct*[a] the current mirror in figure 5.10 using both Q_2 and Q_3 to create a current doubler.
3. *Measure* I_{REF} and I_{OUT} over the range $0.1\,mA < I_{OUT} < 5\,mA$.
4. *Plot* I_{OUT} versus I_{REF} over the test range.
5. *Compare* the expected and experimental results. Why is the result not a perfect doubler?

[a] You will use this exact current mirror when building the differential amplifier in the next part.

Task 5.9.2: Build and test the differential pair

1. *Design* the circuit from figure 5.11 to achieve a single ended gain of $A_v = 4$ and approximately symmetric output swing.
2. *Construct* the circuit from figure 5.11 using the current mirror developed in task 5.9.1 as the current source. Make sure to remove R_{TEST}. Use the two NMOS transistors in the ALD1105 for Q_5 and Q_6, and set $V_{DD} = 5\,V$ and $V_{SS} = -5\,V$.

3. *Ground* both the v_{IN}^{+} and v_{IN}^{-} inputs and adjust the bias current until v_{OUT} is at the expected DC value.

4. *Measure* and *record* the voltage at V_{D5} and V_{D6}. Should they be equal to each other? If they are not as expected, what could be a possible cause of the error?

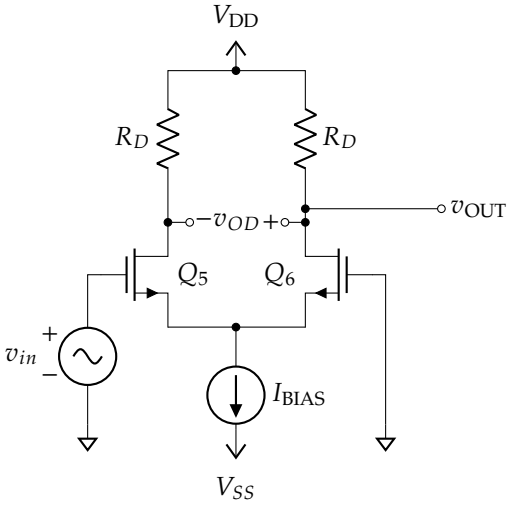

Figure 5.11: Differential amplifier connected with a single-ended input.

5. *Configure* the function generator to supply a 1 kHz sin wave with zero offset and *connect* it to v_{IN}^{+} input. Ground the v_{IN}^{-} input. *Adjust* the amplitude of the v_{IN}^{+} input until the output v_{OD} is 250 mV peak-to-peak. This represents a "single-ended" input and is demonstrated in figure 5.11. v_{OD} can be measured by using the subtraction feature of your oscilloscope.

   a) *Measure* and *plot* the single-ended output v_{OUT} and calculate the single ended gain A_v. *Compare* with the expected value.

   b) *Measure* and *plot* the differential output v_{OD} and calculate the differential gain A_{d}. *Compare* with the single-ended value.

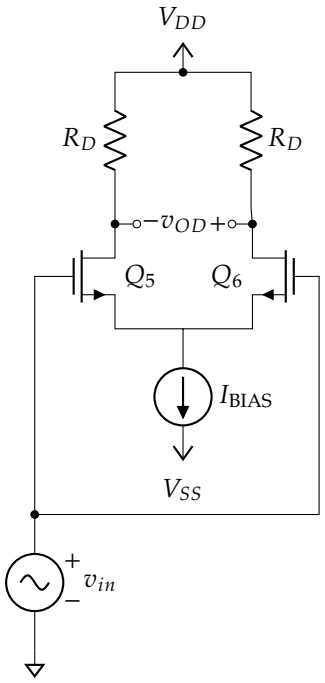

Figure 5.12: Differential amplifier connected with a common mode input.

6. *Configure* the function generator to have zero offset and $v_{\text{in}} = 250\,\text{mV}$ peak-to-peak amplitude, then *connect* it to the v_{IN}^{+} input. Short the v_{IN}^{+} and v_{IN}^{-} pins together. This is to ensure that all the applied voltage is common mode and is demonstrated in figure 5.12.
   a) *Compare* the nonideal diffamp behavior in equation (5.4) to the ideal behavior in equation (5.18). What is the expected gain of the circuit in figure 5.12 due to a common mode input?
   b) What do you actually observe?
   c) Use your observations to *compute* the common mode gain, $A_{\text{cm}} = \frac{v_{\text{OD}}}{v_{\text{CM}}}$.
7. Use your measured values of A_{d} and A_{cm} to *compute* the amplifiers CMRR in decibels.

Task 5.9.3: The active load differential amplifier

1. Remove both R_{D} resistors from the differential amplifier and replace them with the PMOS active load wired as shown in figure 5.6. Use the two PMOS transistors in the ALD1105.
2. *Measure* and *plot* the single-ended input, singled ended output small signal gain.
3. *Compare* the gain of the active load with the gain of the resistive load.

5.10 References

[1] *INA226 hide-side or low-side measurement, bi-directional current and power monitor with I2C compatible interface*, INA226, SBOS547A, Texas Instruments, Aug. 2015. [Online]. Available: `http://www.ti.com/lit/ds/symlink/ina226.pdf`.

[2] *LMx58-N low-power, dual-operational amplifiers*, LM258, SNOSBT3I, Texas Instruments, Dec. 2014. [Online]. Available: `http://www.ti.com/lit/ds/symlink/lm158-n.pdf`.