Lab 4 – Notes

Spring 2024

JOHN GERGUIS

General Notes

- Make sure to use your ESD wristband at all times when using the ALD chips.

Task 1

Task 4.8.1: Build and test the current mirror

1. *Build* the circuit shown in figure 4.10 using the ALD1106 with $R_{REF} = R_{TEST} = 1\,k\Omega$.

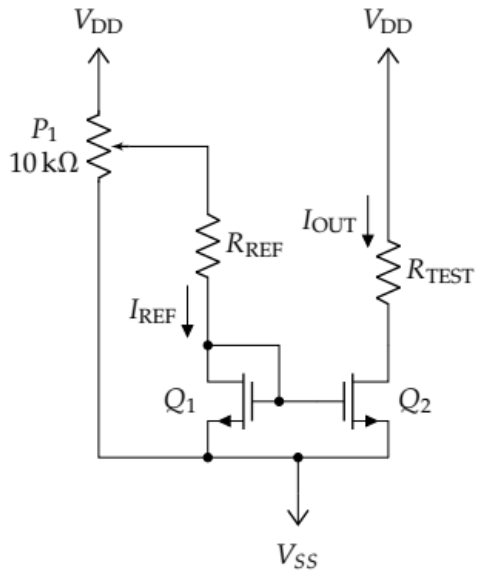


Figure 4.10: Circuit for testing a current mirror.

2. *Plot* the output current I_{OUT} versus the input current I_{REF} over the range 0.1 mA to 2.5 mA. The current can be measured by finding the voltage across R_{TEST} and R_{REF} at each point.

3. Set the reference current to the designed current for the amplifier that you calculated in prelab task 4.7.1 question 2. *Measure* the gate to source voltage, v_{GS}, and the drain to source voltage, v_{DS}, for each transistor.

2.

- Tune the potentiometer to change the currents.
- Take at least 10-15 points to be able to plot Iout vs Iref.
- To measure the currents, we usually measure the voltage across a known resistance and then divide the voltage by the resistance to get the current:
  - Using the AD2? Connect ch1 across Rref and Ch2 across Rtest, then measure the voltages on the voltmeter tool.
  - Using the benchtop equip.? You cannot connect ch 1 and ch2 simultaneously, instead you can use ch1 of the scope to measure V across Rref (or Rtest) and use the DMM to measure V across the other branch.

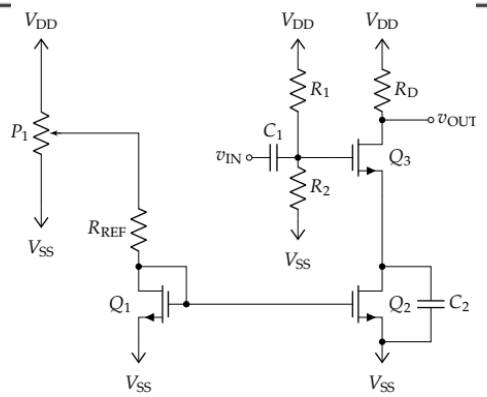
3.

- Check the value of the current with your TA before proceeding.
- Set Iref to the value that you have calculated (again by measuring the voltage across Rref).
- Measure $V_{GS_1}, V_{GS_2}, V_{DS_1}, V_{DS_2}$.

Task 2

Task 4.8.2: Build and test the amplifier

1. *Calculate* the values of C_1 and C_2 necessary to make each filter have a 3dB point lower than 30 Hz using equations (4.12) and (4.13).
2. *Build* the circuit in figure 4.7 using the values calculated in the prelab. Use the ALD1106 for all 3 transistors.
3. *Set* v_{IN} to 0 V and measure the DC value of v_{OUT}. Adjust the potentiometer until the DC value of v_{OUT} is the design target of 1 V. This ensures that the bias current is correct.
4. *Set* v_{IN} to be a 200 mV_{p-p} sine wave at 500 Hz.
5. *Capture* an oscilloscope screenshot showing v_{IN} and v_{OUT}
6. *Calculate* the small signal gain $A_V = \frac{V_{out,p-p}}{V_{in,p-p}}$.
7. *Plot* $|A_v|$ versus frequency for 1 Hz < f < 500 kHz.
8. *Change* v_{IN} to be a 1 V_{p-p} 5 kHz triangle wave.
9. Slowly *increase* the amplitude of v_{IN} to find the largest signal that does not cause significant distortion at the output.
10. *Capture* a screenshot showing the maximum amplitude input and output triangle wave using the oscilloscope.



1. Calculate the values of the capacitors from the relations, then round them to the next higher values available in your kit ($Capacitance\ \alpha\ \frac{1}{f}$).
2. Check the values with a TA before building the circuit.
3. This step is to set the bias current, you need to adjust the potentiometer till Vout becomes 1v (measure Vout w.r.t. ground, e.g. 1+ connected to Vout and 1- to gnd).

4-6. The output should be inverted (the gain is -ve), and the gain should be very close to the designed value.

7. Use the frequency response tool in the AD2 or the benchtop scope.

- Connect ch1 (and the wavegen) to the input and ch2 to the output. You must use the same wavegen of the device that you are using, e.g. if you are using the benchtip scope, then you must use the wavegen inside that scope. The same if you are using the AD2, you must use W1 of the AD2.
- Whenever you run the frequency response, you have to make sure to choose an input voltage which is small enough such that the output is not distorted/clipped (try to limit the output to be around 1v or so). Otherwise, you will get a frequency response, but it will be wrong. This is specially very important in the next labs when the gains are high.

8-10. Check the max Vin amplitude after which the output begins to be distorted.