Lab 5 – Notes

Spring 2024

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General Notes

- Make sure to use your ESD wristband at all times when using the ALD chips.

Task 1

Task 5.9.1: Build and test the ratioed current mirror

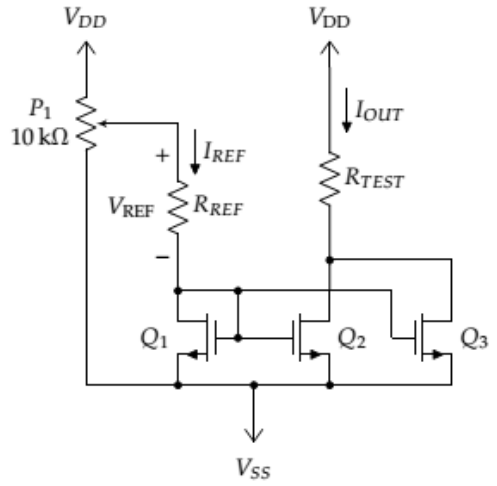


Figure 5.10: NMOS current mirror with test load.

For this task, use $V_{DD} = 5\,V$ and $V_{SS} = -5\,V$, and use the ALD1106 for the three MOSFETs.

1. *Select* R_{REF} and R_{TEST} so that all transistors stay in saturation over the test range of $0.1\,mA \le I_{OUT} \le 5\,mA$.
2. *Construct*[a] the current mirror in figure 5.10 using both Q_2 and Q_3 to create a current doubler.
3. *Measure* I_{REF} and I_{OUT} over the range $0.1\,mA < I_{OUT} < 5\,mA$.
4. *Plot* I_{OUT} versus I_{REF} over the test range.
5. *Compare* the expected and experimental results. Why is the result not a perfect doubler?

[a] You will use this exact current mirror when building the differential amplifier in the next part.

*Leave this circuit built for tasks 2 and 3

1. You need to pick Rref and Rtest such that at the max current (5mA) the transistors are still in saturation.

(Hint: You can use values $R_{Ref} = R_{Out} = 1k\Omega$, verify that by calculations).

3. To measure the current, measure the voltage across the resistor then divide by its value, e.g. Measure the voltage across Rref, then $I_{Ref} = \frac{V_{Ref}}{R_{Ref}}$.

- Using the AD2? You can use the 2 channels and the voltmeter tool or the Logger tool in the AD2 to measure I_{Ref} and I_{Out} simultaneously.
- Using the benchtop equipment? You CANNOT use the ch1 and ch2 of the scope simultaneously, instead, use one channel of the scope and the DMM.

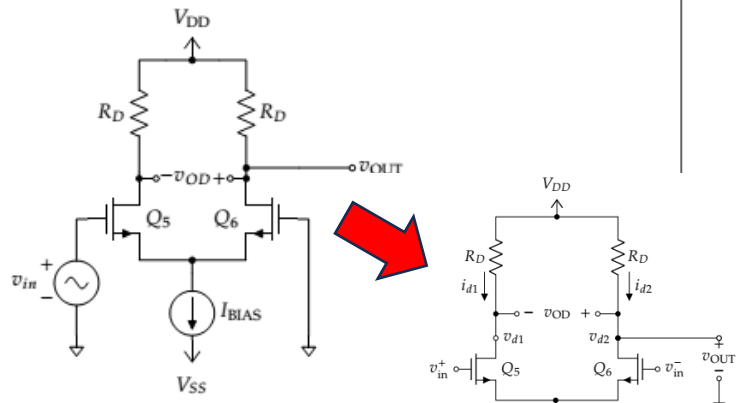
Take at least 10 points for Iref and Iout (0.1mA<Iout<5mA) to plot the curve.

5. $\frac{I_{out}}{I_{Ref}}$ will not be equal 2 across the whole range, why ?! Comment on that.

Task 2

Task 5.9.2: Build and test the differential pair

1. *Design* the circuit from figure 5.11 to achieve a single ended gain of $A_v = 4$ and approximately symmetric output swing.
2. *Construct* the circuit from figure 5.11 using the current mirror developed in task 5.9.1 as the current source. Make sure to remove R_{TEST}. Use the two NMOS transistors in the ALD1105 for Q_5 and Q_6, and set $V_{DD} = 5\,V$ and $V_{SS} = -5\,V$.
3. *Ground* both the v_{IN}^+ and v_{IN}^- inputs and adjust the bias current until v_{OUT} is at the expected DC value.
4. *Measure* and *record* the voltage at V_{D5} and V_{D6}. Should they be equal to each other? If they are not as expected, what could be a possible cause of the error?



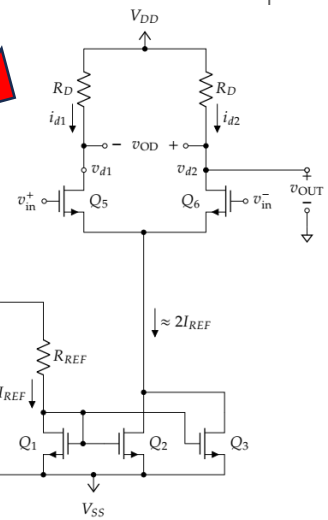


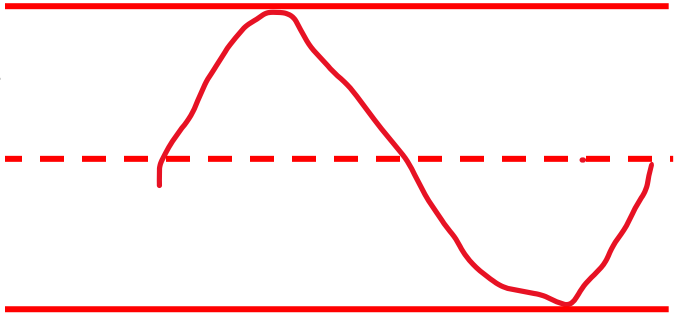
Figure 5.11: Differential amplifier connected wi

* Use the ALD 1106 for the current mirror and ALD 1105 for the DiffAmp.

1. Check with a TA the values of the RD and bias current that you computed in the prelab before building the circuit.

3. Ground both Vin+ and Vin-, then measure Vout w.r.t. ground using the voltmeter tool (e.g. connect 1+ to Vout and 1- connected to Gnd).

Adjust the potentiometer till you get the required voltage of Vout,DC



$$V_{\max} = 5v$$

$$V_{out,DC} = \frac{V_{max} + v_{min}}{2}$$

$$V_{min} = V_g - V_{th} \cong 0 - 0.7$$

Task 2 (Cont'd)

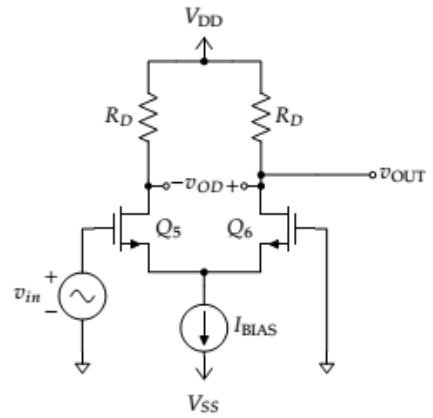


Figure 5.11: Differential amplifier connected with a single-ended input.

5. *Configure* the function generator to supply a 1 kHz sin wave with zero offset and *connect* it to v_{IN}^{+} input. Ground the v_{IN}^{-} input. *Adjust* the amplitude of the v_{IN}^{+} input until the output v_{OD} is 250 mV peak-to-peak. This represents a "single-ended" input and is demonstrated in figure 5.11. v_{OD} can be measured by using the subtraction feature of your oscilloscope.

   a) *Measure* and *plot* the single-ended output v_{OUT} and calculate the single ended gain A_v. *Compare* with the expected value.

   b) *Measure* and *plot* the differential output v_{OD} and calculate the differential gain A_d. *Compare* with the single-ended value.

5. **Measuring the differential gains.** This step is single-ended input (the input is connected to Vin+ while Vin- is grounded)

- First, measure the differential output:
  - Using the AD2? connect 2+ to Vd6 and 2- to Vd5 while channel 1 is measuring the input (1+ to Vin+ and 1- is Gnd).
  - Using the benchtop equipment? To measure the output use ch2 (connected across Vd5 & gnd) and ch3 (connected across Vd6 & gdn) and do subtraction (ch3 – ch2) from the math tool to get the output.
- Change the amplitude of the input signal (@ Vin+) till you get the measured output to be 250 mV peak-to-peak.

b) Measure the differential gain: Divide the peak-to-peak of the output (250mV) by the peak-to-peak of the input signal. This the differential gain (It should be ~ double the value that you have designed for).

a) Measure the single-ended gain: Remove 2- and connect it to Gnd, you should now be measuring the peak-to-peak of the output to be almost the half (~125mV). Divide the output by the peak-to-peak of the input signal. This the single-ended gain (It should be ~ the value that you have designed for).

Task 2 (Cont'd)

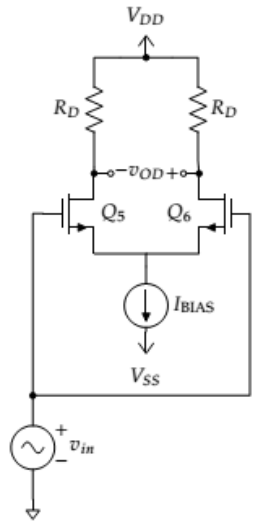


Figure 5.12: Differential amplifier connected with a common mode input.

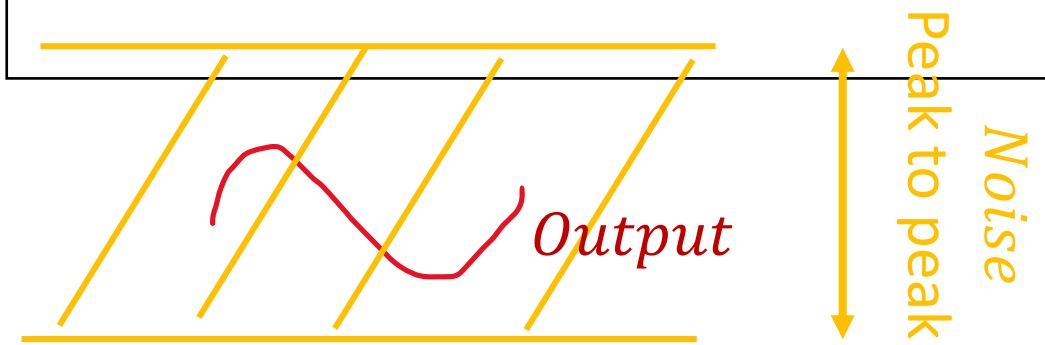
6. *Configure* the function generator to have zero offset and v_{in} = 250 mV peak-to-peak amplitude, then *connect* it to the v_{IN}^{+} input. Short the v_{IN}^{+} and v_{IN}^{-} pins together. This is to ensure that all the applied voltage is common mode and is demonstrated in figure 5.12.
   a) *Compare* the nonideal diffamp behavior in equation (5.4) to the ideal behavior in equation (5.18). What is the expected gain of the circuit in figure 5.12 due to a common mode input?
   b) What do you actually observe?
   c) Use your observations to *compute* the common mode gain, $A_{cm} = \frac{v_{OD}}{v_{CM}}$.
7. Use your measured values of A_d and A_{cm} to *compute* the amplifiers CMRR in decibels.

6. **Measuring the common-mode gain and CMRR.**

- Connect Vin+ to Vin- to the source, and set Vin = 250 mV peak to peak (Measure the input with channel 1).
- Measure the differential output with channel 2 (e.g. using the AD2? connect 2+ to Vd6 and 2- to Vd5).
- The output signal is very small (ideally should be zero), so it will be masked by the noise of the AD2 or the benchtop scope. We will measure the max $A_{CM} < \frac{V_{OD(peak-to-peak\ noise)}}{V_{CM\ (250mV)}}$.

7. We will compute the min CMRR:

$$CMRR > 20\log(\frac{A_d}{A_{CM}})$$



Task 3

Task 5.9.3: The active load differential amplifier

1. Remove both R_D resistors from the differential amplifier and replace them with the PMOS active load wired as shown in figure 5.6. Use the two PMOS transistors in the ALD1105.
2. *Measure* and *plot* the single-ended input, singled ended output small signal gain.
3. *Compare* the gain of the active load with the gain of the resistive load.

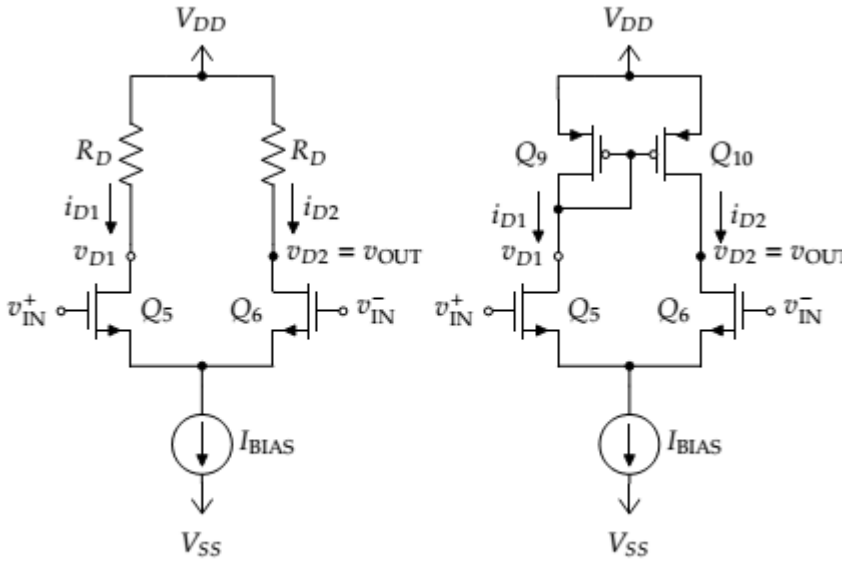


Figure 5.6: Comparison of resistive and active loads.

* This circuit is single-ended input and single-ended output.

- Use the same circuit as in task 2, but replace the resistive load DiffAmp(the schematic on the left) by the active load DiffAmp (the schematic on the right).
- Connect the wavegen to Vin+ (use a small Vinpp of 10 mV) and connect Vin- to Gnd. Measure the input using channel 1.
- Measure the output using channel 2 (Connect 2+ to Vd6 and 2- to Gnd)
- Compute the Gain $A_v = \frac{V_{out,P-P}}{V_{in,P-P}}$. It should be high.