EXPERIMENT 6

MOSFET Operational Amplifier

6.1 Application

The operational amplifier (op amp) is an incredibly versatile building block used in virtually all analog electronics. The behavior of an op amp circuit can be easily customized with only a few external components. The versatility of the op amp circuit enabled its use in analog computers used to solve differential equations prior to the prevalence of digital computers.

Op amps are utilized by designers to easily construct circuits that can provide gain, isolate signals, or perform other signal processing tasks. Almost any electronic system will have op amps somewhere inside to perform a task critical to the successful operation of the system as a whole, as they are critical to both analog and mixed signal circuits.

Figure 6.1: GAP/R SK2-P vacuum tube op amp.

6.2 Design of an operational amplifier

Initial op amps were created from vacuum tubes, like the one photographed in figure 6.1; however, the invention of transistors allowed for the development of solid-state op amps.

Most useful op amps have the following properties:

- **Differential inputs** allow for operating at a wide range of common mode inputs. The benefits of differential amplifiers were covered in experiment 5.
- **Very large open-loop gain**(1) allows for negative feedback networks to create amplification and filtering circuits independent of the particular op amp design.
- **Very large input impedance** prevents loading "high-impedance" outputs, so accuracy is not lost due to mismatch or current consumed at the op amps input.
- **Low output impedance** enables driving small impedance loads without loss of linearity or accuracy.
- **High bandwidth**(2) allows the amplification of high frequency signals.

(1) A system's open loop gain is the system's total gain when no feedback is in use.

(2) It is important to verify that the bandwidth is adequate for your application at the gain you are designing for. We will look at op amp bandwidth in experiment 7.

The combination of these features allows for creating a system where the critical design tasks lie outside of considering the abilities of the op amp. The negative feedback network outside of the op amp can be used to control the system's gain and bandwidth. The combination of high input impedance and low output impedance further simplifies design as circuits can be easily cascaded.

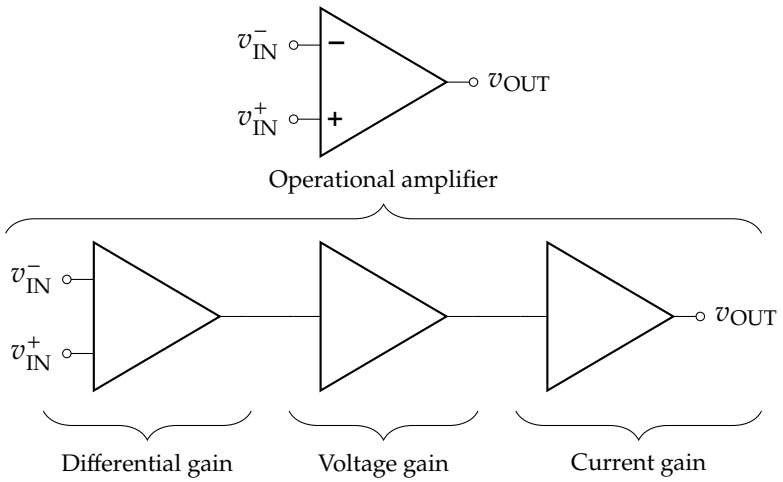

Figure 6.2: Model of an op amp.

In practice, building an op amp requires carefully designing a multiple stage amplifier that can meet the desired characteristics of the amplifier. Such an architecture can be seen in figure 6.2, where the large open-loop gain is provided by both the differential gain and voltage gain stages. The large input impedance is provided by the differential amplifier, and, finally, the low output impedance is provided by the current gain amplifier. Unfortunately, cascading stages together can reduce the bandwidth of the circuit. There are always trade-offs between the ideal op amp properties that arise during design.

Figure 6.3 shows a complete MOSFET based implementation of the architecture given in figure 6.2. We will spend the rest of the lab breaking it into pieces and analyzing it step-by-step. You may often need to refer back to this schematic while building the op amp.

6.3 Extending a differential amplifier to an operational amplifier

The op amp design starts by leveraging the same differential amplifier and current source biasing from experiment 5. This provides the op amp's differential inputs and large input impedance. Unfortunately, the differential amplifier's gain fails to adequately meet the high open-loop gain requirement of an op amp. To help remedy the situation, the active load version of the differential amplifier is used; however, that is still insufficient for a high-quality op amp. To further increase

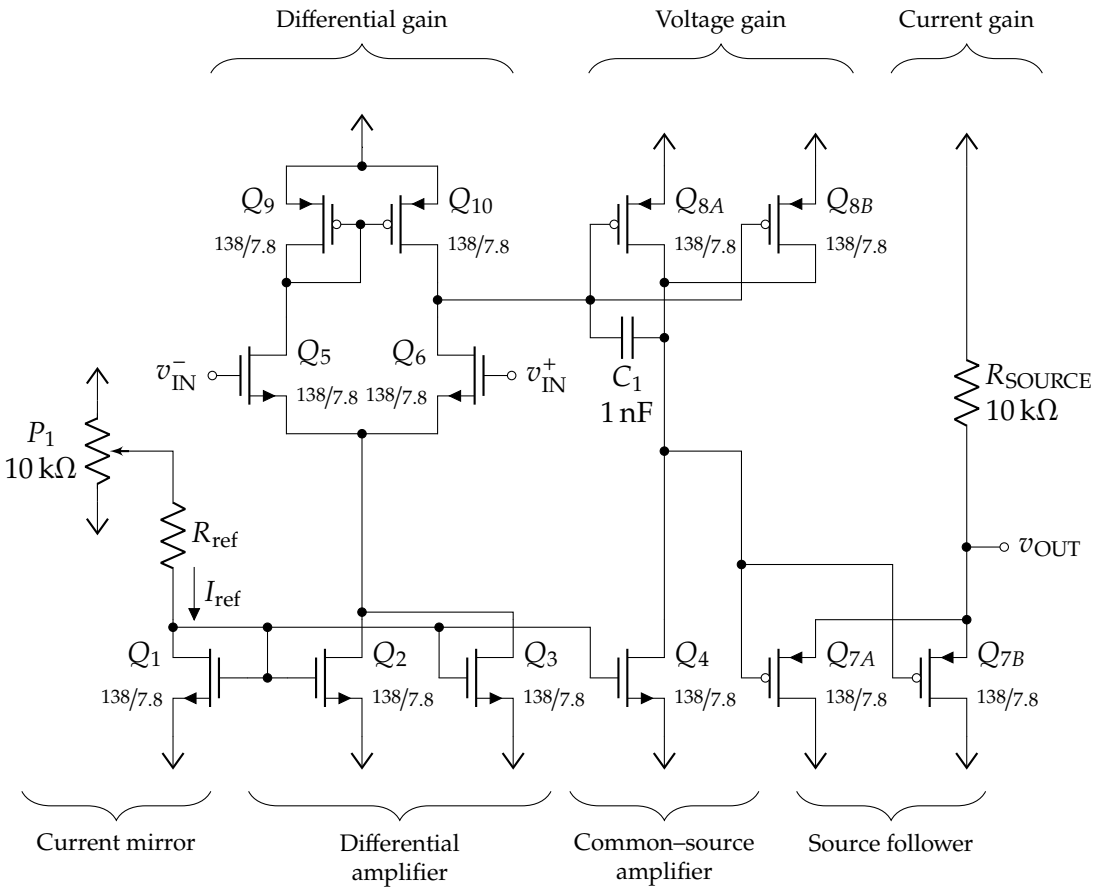

Figure 6.3: Complete op amp circuit. $Q_{1\text{-}4}$ are built with an ALD1106, $Q_{5,6,9,10}$ are built with an ALD1105, and $Q_{7,8}$ are each two PMOS in parallel on the ALD1107.

the gain, a common source amplifier is used as the second stage.

6.3.1 More gain: common source amplifier

An ideal op amp has infinite open-loop gain. Although that is not practically attainable, we can effectively achieve very large gains by chaining voltage amplifier stages together. The resulting overall system gain can be found by multiplying the gains of all of the stages together.[3] The op amp design from figure 6.3 uses a common source amplifier as a second voltage gain stage.

[3] If any stages load the previous stage, the product will overestimate the total gain.

We first explored the gain of a common source amplifier in experiment 4. PMOS and NMOS transistors have the same small signal models, so the gain of the common source amplifier stage in figure 6.4 is

$$A_v = g_{m8}\,(r_{o8} \parallel r_{o4})$$

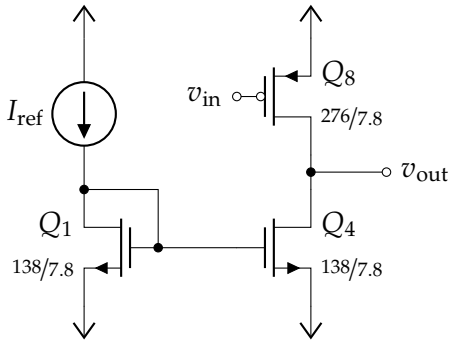

Figure 6.4: Common source voltage gain portion of figure 6.3.

Additionally, we can compute the output impedance of this stage using the small signal model.

$$r_{\text{out}} = r_{o8} \parallel r_{o4}$$

6.3.2 Lowering the output impedance: Source follower

For many realistic loads the output impedance of the common source stage would be too large and does not satisfy the "low output impedance" property from section 6.2. Imagine for a moment that the op amp has an output impedance of around 50 kΩ and is driving a load on the order of 100 kΩ. Then, only about 66% of the output voltage will actually be delivered because the load and amplifier will effectively form a voltage divider.[4]

To lower the output impedance, we add a source follower[5] as a third gain stage. This will provide the amplifier with current gain, or in other words will reduce the output impedance so that the amplifier can deliver more current with less voltage drop.[6]

A resistively loaded PMOS source follower can be found in figure 6.5. Considering the large signal behavior of Q_7, we can solve for the output voltage assuming Q_7 is in saturation

$$v_S = v_{IN} + v_{SG} = v_{IN} + \sqrt{\frac{i_D}{\frac{W}{2L}k'} + |V_{th}|}$$

That is, the source terminal of Q_7 tracks the input voltage with a nearly constant offset of V_{th}.[7] The name "source follower" derives from the fact that the source voltage "follows" the input voltage.

[4]
$$\frac{v_{\text{load}}}{v_{\text{out}}} = \frac{R_{\text{LOAD}}}{R_{\text{LOAD}} + r_{\text{out}}}$$
$$\frac{v_{\text{load}}}{v_{\text{out}}} = \frac{100\,\text{k}\Omega}{100\,\text{k}\Omega + 50\,\text{k}\Omega} \approx .66$$

[5] Also known as a common drain amplifier.

[6] If the load is of very high impedance, such as the gate of another MOSFET (which is often the case in analog IC design) this current gain stage is sometimes omitted in order to save on power consumption and increase bandwidth.

[7] As long as v_{IN} is relatively small the changes in i_D will be small. Therefore, changes in v_{SG} will be negligible.

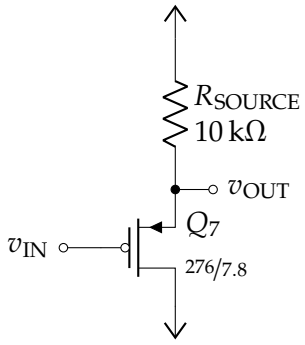

Figure 6.5: Source follower current amplifier from figure 6.3.

Source follower small signal analysis

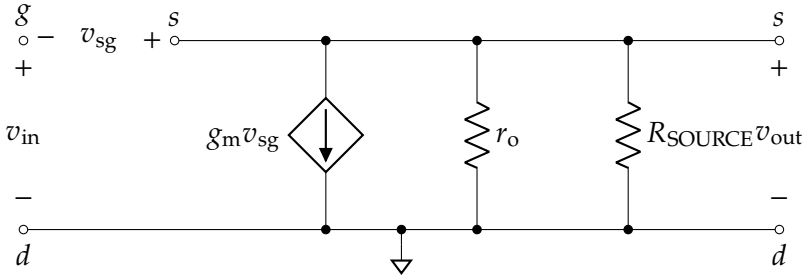

Figure 6.6: Small signal version of the source follower current amplifier from figure 6.3.

Computing the small signal gain of figure 6.5 is straightforward. First, we redraw the circuit in its small signal equivalent form as seen in figure 6.6. Next, we define $v_{in} = v_{gd}$ and $v_{out} = v_{sd}$. Note that with these definitions $v_{in} = v_{out} - v_{sg}$.

We can solve for $A_v = {}^{v_{out}}/_{v_{in}}$:

$$\begin{aligned} v_{out} &= -g_m v_{sg}(r_o \parallel R_{source}) \\ v_{out} &= -g_m(v_{out} - v_{in})(r_o \parallel R_{SOURCE}) \\ v_{out}[1 + g_m(r_o \parallel R_{SOURCE})] &= g_m(r_o \parallel R_{SOURCE})v_{in} \\ A_v = \frac{v_{out}}{v_{in}} &= \frac{g_m(r_o \parallel R_{SOURCE})}{1 + g_m(r_o \parallel R_{SOURCE})} \end{aligned}$$

As long as $g_m(r_o \parallel R_{SOURCE}) \gg 1$, then the gain of this circuit will be approximately $A_v = 1$. This assumption can be made as long as the transistor remains in saturation and has an adequately high k'.

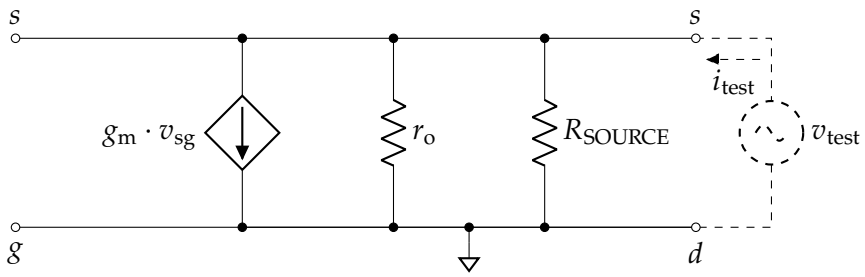

Figure 6.7: Small signal version of the source follower current amplifier from figure 6.3 with test input to measure r_{out}.

Source follower: Output resistance

Computing the small signal output resistance is not much harder. Again, we turn to the small signal equivalent circuit. However, this time we set the input to 0 and apply a test voltage v_{test} across the output, as seen in figure 6.7. By computing the resulting test current i_{test}, we can compute r_{out} using Ohm's law

$$r_{out} = \frac{v_{test}}{i_{test}}$$

We begin by observing that $v_{sd} = v_{test} = v_{sg}$ because the v_{IN} source has become an AC ground which shorts the gate and the drain. Then,

$$i_x = g_m v_x + \frac{v_x}{r_o} + \frac{v_x}{R_{SOURCE}}$$

$$r_{out}^{-1} = \frac{i_x}{v_x} = g_m + \frac{1}{r_o} + \frac{1}{R_{SOURCE}}$$

$$r_{out} = \frac{1}{g_m + \frac{1}{r_o} + \frac{1}{R_{SOURCE}}} = \frac{1}{g_m} \parallel r_o \parallel R_{SOURCE}$$

In nearly all circumstances $\frac{1}{g_m}$ will be much smaller than r_o and R_{SOURCE}, so

$$r_{out} \approx \frac{1}{g_m} \tag{6.1}$$

Recall that

$$g_m = \sqrt{2k' \frac{W}{L} I_D}$$

and

$$r_o = \frac{1}{\lambda I_D}$$

which are both functions of I_D. Therefore, the approximation of r_{out} can easily be verified after a design is determined.

Final design: Operational amplifier

The design now satisfies all the basic requirements of an op amp from section 6.2. The input differential amplifier provides differential input, the overall gain should exceed 60 dB, the input resistances are nearly infinite, and, finally, the output impedance is reasonably low. One addition that has not been discussed is the 1 nF added between the input and output of the common source stage. This capacitor is called a compensation capacitor and is used to ensure that the op amp does not oscillate during normal operation.

6.4 Prelab

Task 6.4.1: Prelab Questions

1. Draw the small-signal model for the entire opamp. You can combine transistors in parallel (e.g. Q_2 and Q_3) into a single transistor for the small signal model.
2. Derive an equation for the open loop gain without the source-follower in terms of the transistor parameters and I_{ref}. You do not need to rederive the active load differential amplifier gain.
3. *Estimate* the output resistance of the common drain output amplifier in figure 6.3 assuming that $v_{\text{OUT}} = 0\,\text{V}$.[a]

[a] This value may not be as small as you might expect, but that is because the negative feedback in typical applications will further reduce the output impedance.

6.5 Tasks

Please complete the following tasks assuming $V_{\text{DD}} = 5\,\text{V}$ and $V_{\text{SS}} = -5\,\text{V}$. Use $V_{\text{TN}} = 0.7\,\text{V}$, $k'_{\text{n}} = 32\,\mu\text{A}\,\text{V}^{-2}$, $V_{\text{TP}} = -0.7\,\text{V}$, $k'_{\text{p}} = 11\,\mu\text{A}\,\text{V}^{-2}$, $\frac{W}{L} = \frac{138}{7.8}$, $\lambda_n = 0.009$, and $\lambda_p = 0.008$. Use the ALD1106 for Q_1, Q_2, Q_3, and Q_4. Use the ALD1105 for Q_5, Q_6, Q_9, Q_{10}. Use the ALD1107 for Q_7 and Q_8. Q_7 and Q_8 are two transistors in parallel built like shown in figure 6.8.

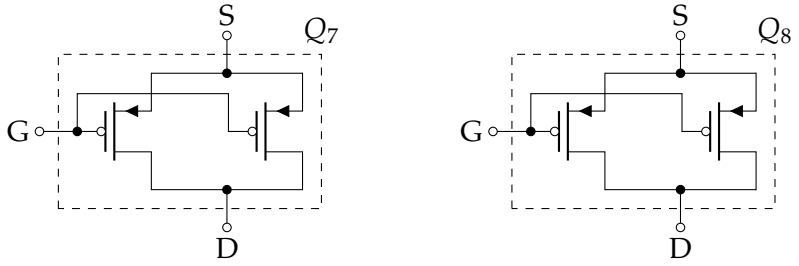

Figure 6.8: Parallel Transistor Configurations

Task 6.5.1: Multi-branch current mirror

You will need various current mirrors to build the circuit shown in figure 6.3. In this task, you will pre-construct those mirrors using temporary resistive loads. As you work through the experiment, you will replace each resistive load with a relevant amplifier.

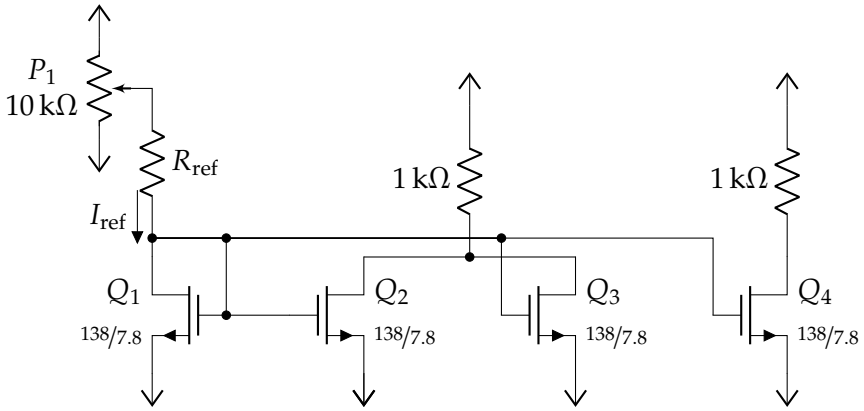

Figure 6.9: Multi-branch current mirror with 4 NMOS.

1. *Build* the current mirror shown in figure 6.9 and *set* the reference current to $I_{\text{REF}} = 200\,\mu\text{A}$ by adjusting P_1.
2. *Measure* the resulting current through the two branches. What are the percent errors?
3. What are the possible sources of error in the current mirrors?

Task 6.5.2: First stage: Active load differential amplifier

1. *Build* the differential amplifier with an p-channel MOSFET (PMOS) mirror active load from figure 6.3, using the 2 : 1 current mirror branch. Make sure to remove the temporary resistive load.
2. *Measure* the single ended gain using a $0.01\sin(2\pi 100t)$ signal applied to v_{IN}^{+} while connecting v_{IN}^{-} to ground.

Task 6.5.3: Second stage: Common source amplifier

1. *Estimate* the gain of the common source amplifier used as the second gain stage in figure 6.3 using the actual current measured in task 6.5.1.
2. *Estimate* the overall open-loop gain from the first two stages using the measured gain in task 6.5.2.
3. *Build* the common source amplifier from figure 6.3 using the 1 : 1 current mirror branch. Make sure to remove the temporary resistive load.

Previous techniques to measure amplifier's open-loop gain are now very difficult to apply. This is because the open-loop gain, A, is quite large, thus, even minute changes on the input produce large changes at the output. In practice this is not an issue because op amps are normally only used in circuits with negative feedback networks.

In lieu of measuring the open-loop gain, we will use the input stage of the op amp as a comparator. A comparator exploits the op amps large gain to output a constant voltage based on whether v_{IN}^{+} or v_{IN}^{-} is larger. It is important to note that if you need a comparator in a project, use an integrated circuit (IC) specifically designed as such.

3. *Apply* a DC threshold voltage of 0 V to v_{IN}^{-} by grounding it.
4. Using the function generator, apply a DC voltage between −2 V to 2 V[a]. *Adjust* the value and observe the output. *Explain* what the comparator circuit is doing.
5. *Record* the input and output for a positive input voltage.
6. *Record* the input and output for a negative input voltage.
7. *Change* the input voltage to be a $2\sin(2\pi 100t)$ V signal.
8. *Plot* the input and output. *Explain* the shape of the output.

[a] Be sure not to exceed −5 V to 5 V as you may permanently damage the transistors.

Task 6.5.4: Third stage: Source follower

1. *Build* the common drain amplifier from figure 6.3.
2. Connect v_{IN}^{-} to ground and v_{IN}^{+} to a $2\sin(2\pi 100t)$V signal.
3. *Plot* the input and output and compare to the result in task 6.5.3.

Task 6.5.5: Inverting Amplifier

As a final exercise, test your op amp by building the inverting amplifier shown in figure 6.10 using the complete op amp circuit you built in task 6.5.4.

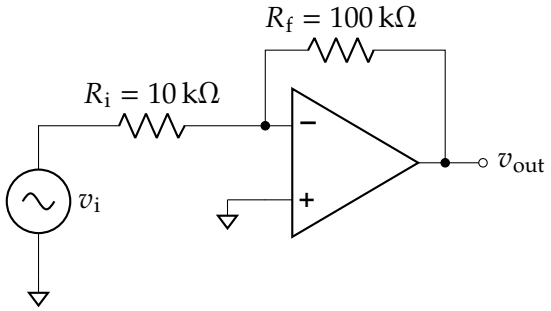

Figure 6.10: A gain −10 op amp based inverting amplifier.

1. *Build* inverting amplifier with gain 10 using the op amp from figure 6.3.
2. *Measure* the gain. What is the percent error?