EXPERIMENT 4

Common Source Amplifier

4.1 Application

The transistor is the fundamental building block for a number of analog and mixed signal circuits. Op amps, oscillators, and analog to digital converters are just a small selection of analog devices that are built from transistors. Generally, transistors can be used anywhere in a circuit that requires gain or control. There are several configurations of transistor amplifiers that can provide voltage or current gain. Metal-oxide-semiconductor field-effect transistor (MOSFET) amplifiers are the favorite choice for many new designs (as opposed to bipolar junction transistors (BJTs)), as they are easier to integrate at the nanoscale level and have a high input impedance due to the oxide layer between the gate and semiconductor. For the MOSFET, the three amplifier configurations are common source, common drain, and common gate. The common source amplifier provides high input impedance and high voltage gain, which makes it suitable for many analog signal processing tasks.

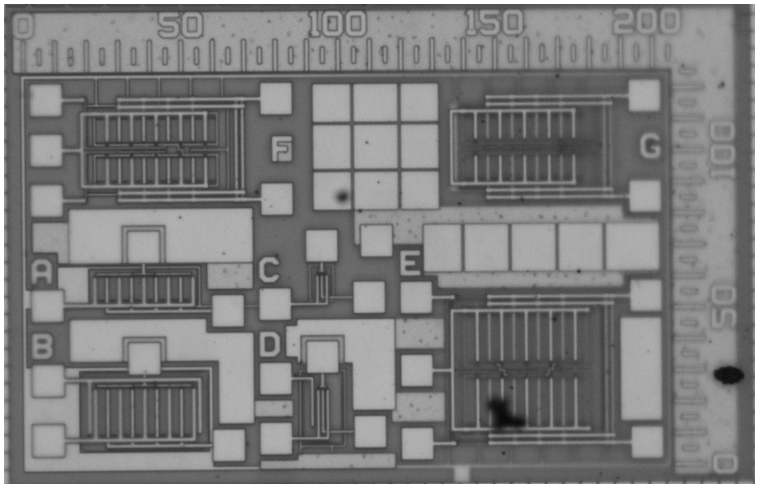

Figure 4.1: Silicon die photo showing a top down view of several transistors.

4.2 Small-signal analysis

Over the last few labs, we have explored the large-signal models of MOSFETs. The large-signal equations are useful in switching applications and for determining the DC operating conditions of a circuit. Unfortunately, analyzing an amplifier using the large-signal models is difficult and unintuitive. For that reason, we need a model that better represents the behavior of a transistor circuit when the input and output are sufficiently small. This method is called "small-signal analysis."

Small-signal analysis is a technique used to analyze nonlinear devices which have reasonably linear operating regions. When biased correctly, transistors act linearly over a fairly large range of operation. The small signal analysis of the transistor allows us to separately analyze the DC and AC behavior of a circuit.

Small signal analysis is essential for nearly all analog designs. Using nonlinear equations to design circuits would be incredibly time intensive, so small signal approximations are still used in the pen-and-paper calculation portion of the design process.

Small signal analysis assumes:

1. the device is biased to an operating point in a reasonably linear region of the current versus voltage (I–V) characteristic,
2. a small signal input is applied to the device,
3. a small signal output results,
4. the output signal is linearly related to the input signal.

How large is a small signal? There is no limit on how large a "small signal" can be. It is entirely dependent on the specific circuit and biasing point. In general, as long as the input and output of the circuit are linearly related, then the input and output signals can be considered "small signal." The region of small signal operation is dependent on the size of the approximately linear portion of the nonlinear system.

How can you tell if the input and output signals are linearly related? There are precise measurements of linearity,[1] but often times human observation can be used for a first order estimate when working in the lab.

1. If the input signal closely resembles and is proportional to the output signal, then we say that the network is linear for signals of that magnitude.[2] In this case, small signal analysis may be applied effectively.
2. If the magnitude of the input signal is increased until the output signal no longer resembles the input signal,

[1] Most linearity measurements revolve around determining how much of the output signal is not at the same frequency as the input signal. One common metric is total harmonic distortion, which measures the total amount of energy at the output that is at a different frequency than the input frequency.

[2] It can be difficult to visually observe distortion on a sine wave; however, looking for "bending" of a triangle wave at the output of a circuit is a strong indicator of distortion.

we say that the output signal is distorted and that input is not in the small signal region for the system.

4.3 MOSFET small signal model

The design and analysis of a MOSFET amplifier using only the large signal equations would be particularly difficult and time consuming. Instead, we will design a circuit that will stay in the small signal regime, so we can replace the MOSFET with a linear circuit equivalent. We will use the hybrid-π small signal model. The primary two parameters of the model are small signal transconductance (g_m) and small signal output resistance (r_o).[3] These two parameters are bias dependent because they change based on the current flowing through the MOSFET; however, if the small signal variation in current is significantly smaller than the bias current, it is possible to treat the parameters as constant.

[3] At high frequencies, we must also include three additional capacitors in the model: C_gs, C_gd, and C_{ds}.

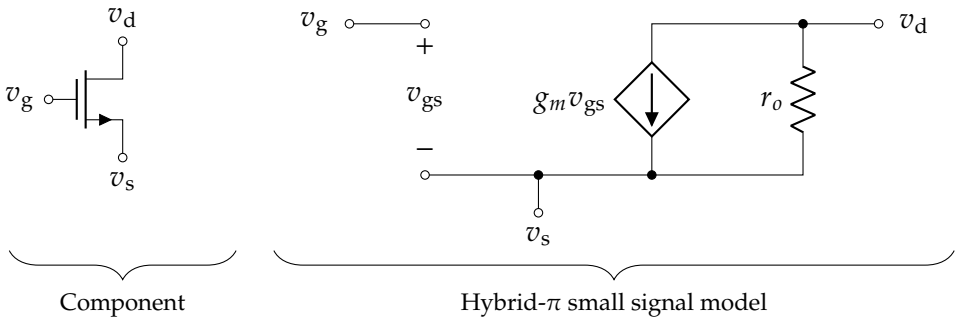

Figure 4.2: Hybrid-pi small signal model of a MOSFET.

4.3.1 Calculating g_m for a MOSFET

The transconductance g_m is found analytically by calculating $\partial i_\mathrm{D}/\partial v_\mathrm{GS}$ for a given bias point.[4] The bias point is found using the large signal MOSFET equation. For the circuits designed in this and the following labs, the transistor will always be biased in the saturation region, so the saturation equation for a MOSFET is used.

[4] Calculating g_m from the ideal square law equation is wildly innacurate for modern CMOS processes, as transistors are often biased close to the transition between the linear region and saturation region. Instead, designers will generate simulated tables and graphs of g_m values while sweeping bias current, drain-source voltage, and transistor size.

$$g_\mathrm{m} = \frac{\partial}{\partial v_\mathrm{GS}}\left(\frac{1}{2}k'\frac{W}{L}(v_\mathrm{GS} - V_\mathrm{th})^2\right) \tag{4.1}$$

$$g_\mathrm{m} = k'\frac{W}{L}(v_\mathrm{GS} - V_\mathrm{th}) \tag{4.2}$$

To find an equation for g_m in terms of i_D, the equation for i_D is solved for $(v_\mathrm{GS} - V_\mathrm{th})$ and inserted into equation (4.2). This yields:

$$g_m = \sqrt{2k'\frac{W}{L}i_D} \tag{4.3}$$

Using equation (4.3), we find that we need to either make the transistor bigger[5] (change W/L) or use more power (increase i_D) to increase g_m.

[5] In discrete design, W/L cannot be changed, but transistors in parallel effectively double W/L. For nanoscale integrated circuit (IC) design, the choices for L are limited, but W can be adjusted.

4.3.2 Channel length modulation

The r_o of an ideal MOSFET in saturation mode is infinite. For any real MOSFET, this is not true. The simple saturation mode equation for a MOSFET must be modified to reflect the fact that the current through a MOSFET is still weakly dependent on v_{DS} when in saturation. The new equation for the drain current is given in equation (4.4) where the channel width modulation factor (λ) determines the amount that the current is dependent on the drain voltage.

$$i_D = \frac{1}{2}k'\frac{W}{L}(v_{GS} - V_{th})^2(1 + \lambda v_{DS}) \tag{4.4}$$

The small signal parameter r_o can then be calculated by finding the relationship between v_{DS} and i_D at the bias point:

$$\frac{1}{r_o} = \frac{\partial i_D}{\partial v_{DS}} = \frac{1}{2}\lambda k'\frac{W}{L}(v_{GS} - V_{th})^2 = \frac{\lambda i_D}{1 + \lambda v_{DS}} \tag{4.5}$$

In general, λ is very small, so $(1 + \lambda v_{DS}) \approx 1$. Using this approximation, we can rewrite the equation for r_o as:

$$r_o \approx \frac{1}{\lambda i_D} \tag{4.6}$$

As current increases, the transistor becomes less ideal and r_o decreases. This puts an upper limit on the gain achievable in circuits using a transistor with channel length modulation.

4.4 Resistor biased common source amplifier

A simple common source amplifier can be built using three resistors. The required bias network is shown in figure 4.3. Using small signal analysis, we get the schematic shown in figure 4.4. For this circuit, r_o will be ignored because it is much greater than R_D.

Assuming that v_{in} is an ideal voltage source, R_1 and R_2 will not affect the gain of the circuit[6]. The two input resistors are

[6] The input resistors will affect the gain if the voltage source driving the circuit has a finite output resistance or if the DC blocking capacitor is too small. Fortunately, R_1 and R_2 can be chosen to be very large because no current flows into the transistor gate.

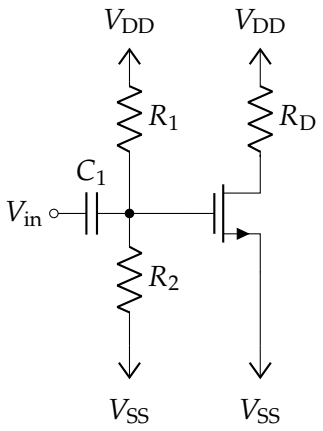

Figure 4.3: Resistor biased common source amplifier.

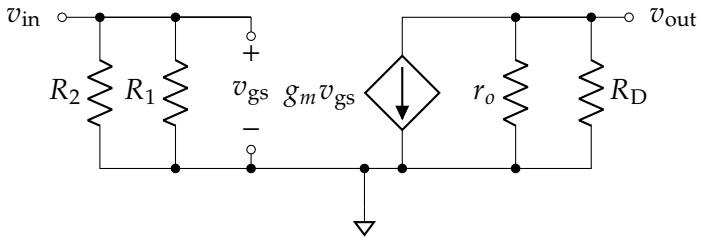

Figure 4.4: Common source amplifier small signal model.

only used to set the bias point of the transistor, so they can be ignored in small signal analysis. The gain can be calculated by writing the nodal equation at the output node:

$$\frac{v_{\text{out}}}{r_{\text{o}} \parallel R_{\text{D}}} + g_{\text{m}} v_{\text{gs}} = 0 \tag{4.7}$$

Using the assumption that v_{in} is ideal and that r_{o} is large, we can make the simplifications that $v_{\text{gs}} = v_{\text{in}}$ and $r_{\text{o}} \parallel R_{\text{D}} \approx R_{\text{D}}$. By plugging these assumptions into equation (4.7) and solving for $v_{\text{out}}/v_{\text{in}}$, we get the equation for gain:

$$\frac{v_{\text{out}}}{v_{\text{in}}} = -g_{\text{m}} R_{\text{D}} \tag{4.8}$$

This gives us two variables we can adjust to change gain. g_{m} is set by using equation (4.2), and R_{D} can be adjusted to the desired value. The issue with this circuit is that increasing g_{m} leads to a higher drain current, I_{D}, which reduces the DC output voltage. Eventually, the transistor will no longer be in the saturation mode and will cease to function as a good amplifier. In effect, this means that g_{m} and R_{D} cannot actually

Using discrete resistors is great in a lab environment as they can be easily changed, but the maximum gain of a circuit with a limited voltage supply and discrete resistors is often not enough for many applications. Instead of using discrete resistors, another transistor can be used to replace R_{D}. This approach will be used in experiment 5.

be set to any arbitrary value, but must be carefully selected to maximize gain.

4.5 Current mirrors

By using equation (4.3) and an ideal current source, it is possible to set g_m by adjusting the current through the source, as shown in figure 4.5. To build a circuit like this, we need to figure out how to build a controllable current source. Both BJT and MOSFET transistors can be operated in a region where the collector current, i_C, or drain current, i_D, is constant irrespective of the voltages v_{CE} or v_{DS}. The MOSFET, when used in saturation mode, is already close to an ideal current source. r_o is very high, and it pulls a constant current based on our control voltage, V_{GS}.

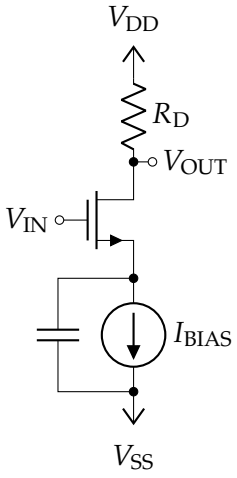

Figure 4.5: Current source biased transistor.

The major drawback to this design is that we still need to know many of the transistor parameters to accurately predict what the current will be. One of the most common solutions to this is the current mirror. It takes a reference current and can replicate the same current or a multiple of the current in different branches.

The current mirror is a critical circuit for creating practical constant-current biases. In the case of the differential amplifier, a constant current source is vital for the common mode performance of the circuit. The current mirror relies on two closely matched MOSFET transistors that have an identical V_{th}, k', and λ.[7]

[7] Transistor matching is achieved by using transistors on the same semiconductor wafer with the same length. Part to part variation or even variation across a single semiconductor chip are both common, so designers must be careful when precise current mirrors are needed.

4.5.1 Mirror analysis

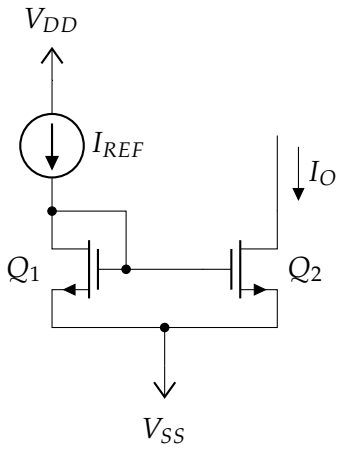

Figure 4.6: Basic MOSFET current mirror.

To analyze the circuit in figure 4.6, we begin by considering the drain current in Q_1. First, note we have connected V_{DS} to V_{GS} which forces[8] the transistor permanently into the saturation region. In saturation, current can be calculated as:

$$I_{REF} = I_{D1} = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_{th})^2$$

[8] Recall that the condition for saturation is $V_{GS} - V_{th} < V_{DS}$, which is always true when $V_{DS} = V_{GS}$ and $V_{GS} > V_{th}$.

The drain current, $I_D = I_{REF}$, is sourced from V_{DD}. This circuit still requires an ideal current source, but I_{REF} can be replaced with a resistor that is adjusted to set the current to the desired value.

The output current I_O is set by Q_2:

$$I_O = I_{D2} = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_{th})^2$$

Assuming Q_2 has the same V_{th}, k_n', and $\frac{W}{L}$ as Q_1 and using the fact that both transistors have the same V_{GS}, we can say:

$$I_O = I_{REF}$$

Note that we have disregarded λ in these calculations. In reality, this current mirror is slightly dependent on the output voltage based on how large λ is. We must also ensure that the output voltage across Q_2 is high enough to keep Q_2 in saturation.

4.6 Current mirror biased common source amplifier

The next step is to combine the current mirror with the common source amplifier. This will let us determine the values of g_m and R_D that achieve our desired gain, and, in some cases, it can allow us to remove the input bias resistors. The current mirror biased amplifier is shown in figure 4.7.

The combination of Q_2 and Q_1 forms a current mirror which is used to set the bias current. The bias current is adjusted by using P_1 and measured using the voltage across R_{REF}. For that reason, it is convenient to select R_{REF} to be a power of ten. The current mirror is able to keep the current through Q_3 constant by adjusting v_{DS2} to maintain a constant v_{GS3}. It is important to verify that the bias voltage v_{GS2} is not too high because Q_2 must remain in saturation mode for the current mirror to function.

4.6.1 Picking R_D and I_{BIAS}

The two primary design parameters needed for picking the bias current and drain resistor are gain and DC output voltage. The relevant equations for these are:

$$V_{OUT,DC} = V_{DD} - I_{BIAS}R_D \tag{4.9}$$

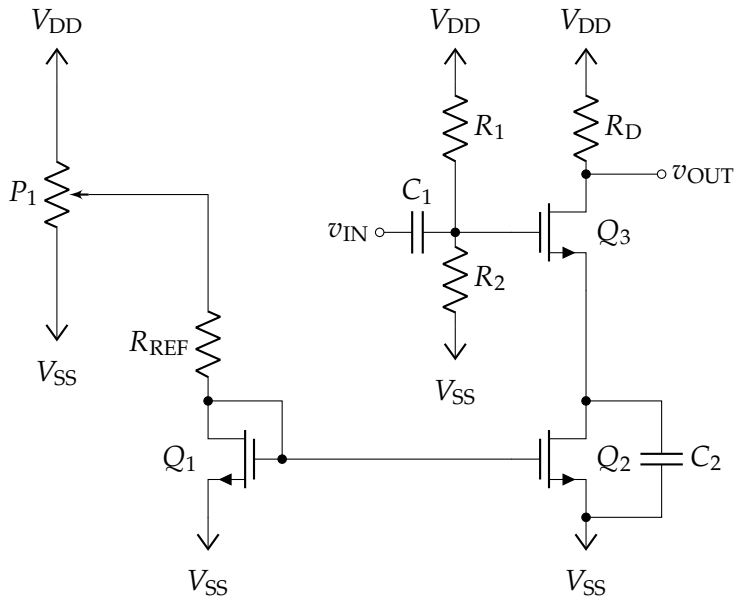

Figure 4.7: A current mirror biased common source amplifier.

$$A_v = -g_m R_D \tag{4.10}$$

g_m can be found using equation (4.3).

4.6.2 Picking R_1 and R_2

The input biasing resistors are needed if the desired output voltage swing risks pulling Q_3 out of saturation mode. Q_3 will go into linear mode if the output voltage swing causes v_{DS3} to drop below $v_{GS3} - V_{tn}$. An example of this is shown in figure 4.8. When the output voltage drops below $v_G - V_{TH}$, the transistor enters the linear region and the output is no longer linearly related to the input. If the minimum output voltage is $V_{OUT(min)}$ and $v_{GS,1}$ is solved for using the I_{BIAS} found previously, then we can solve for the $v_{G,3}$ required to maintain saturation. To remain in saturation, the following condition is required:

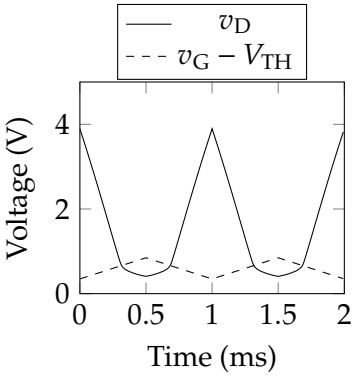

Figure 4.8: Transient signals showing distortion due to Q_3 entering the linear region

$$v_{GS} - V_{th} < v_{DS}$$

Rewritten for our scenario, this translates to:

$$v_{G,3} - v_{S,3} - V_{th} < V_{OUT(min)} - v_{S,3}$$

Solving for the gate voltage, we get:

$$v_{G,3} < V_{OUT(min)} + V_{th} \tag{4.11}$$

Therefore, we can pick R_1 and R_2 using the voltage divider equation and input impedance requirements. If $V_{\text{OUT(min)}} + V_{\text{th}} > V_{\text{IN}}$, then the input biasing resistors and capacitors can be removed completely.

4.6.3 Picking C_1 and C_2

The two capacitors in the circuit will set the low end of the frequency range that the amplifier can operate. C_1 forms a high pass circuit with the input biasing resistors of Q_3. The transfer function for the high pass circuit is given as:

$$|H(f)| = \frac{2\pi f C_1 (R_1 \parallel R_2)}{\sqrt{1 + (2\pi f C_1 (R_1 \parallel R_2))^2}}$$

Solving for when $|H(f)| = \frac{1}{\sqrt{2}}$ yields the $-3\,\text{dB}$ point:

$$f_{\text{-3 dB}} = \frac{1}{2\pi C_1 (R_1 \parallel R_2)} \tag{4.12}$$

Small signal analysis can be used to find the gain of the source degenerated amplifier.[9] This results in the gain relationship:

$$|A_{\text{v}}| = \frac{2\pi f R_{\text{D}} C_2}{\sqrt{1 + \left(2\pi f C_2 \frac{1}{g_{\text{m}}}\right)^2}}$$

[9] Source degenerated is a common term that means that the source does not have a direct connection to ground.

The 3dB point for this filter is at

$$f_{\text{-3 dB}} = \frac{g_{\text{m}}}{2\pi C_2} \tag{4.13}$$

In general, it is advantageous to choose a large capacitor for C_2 if low frequency amplification is needed.

Example 4.6.1: Common Source Amplifier Design Process

Design a common source amplifier with an inverting gain of 6, maximum peak to peak output voltage of $7\,\text{V}_{\text{p-p}}$, and $\pm 5\,\text{V}$ supplies using a transistor with $V_{\text{TN}} = 0.7\,\text{V}$, $k'_{\text{n}} = 32\,\mu\text{A V}^{-2}$, $\frac{W}{L} = \frac{138}{7.8}$, and $\lambda = 0$.

First, we need to find out $V_{\text{OUT,DC}}$. The maximum value this circuit can ever output is V_{DD}, so we need to make sure our output voltage never exceeds that. In this case, if we set

$$V_{\text{OUT,DC}} = V_{\text{DD}} - \frac{v_{\text{out,pp}}}{2} = 5\,\text{V} - 3.5\,\text{V} = 1.5$$

then we guarantee that the output will not go above V_{DD}. We will adjust R_1 and R_2 to make sure that the transistor stays in saturation at the bottom end of the range.

Next, we need to set up our system of equations to find g_m, I_{BIAS}, R_D using equations (4.3), (4.9) and (4.10).

$$\begin{aligned} g_m &= \sqrt{1.132 \times 10^{-}3 \cdot I_{BIAS}} \\ 1.5 &= 5 - I_{BIAS} R_D \\ -6 &= -g_m R_D \end{aligned}$$

When solved, we find

$$\begin{aligned} g_m &= 661\,\mu S \\ I_{BIAS} &= 385\,\mu A \\ R_D &= 9.08\,k\Omega \end{aligned}$$

Next, we need to find values for R_1 and R_2. $V_{OUT(min)}$ can be found using the peak to peak output voltage and DC output voltage:

$$V_{OUT(min)} = V_{OUT,DC} - \frac{v_{out,pp}}{2} = -2\,V$$

We can then take $V_{OUT(min)}$ and plug it in to equation (4.11) to find an upper bound on $V_{G,3}$:

$$\begin{aligned} v_{G,3} &< -2\,V + 0.7\,V \\ v_{G,3} &< -1.3\,V \end{aligned}$$

We will pick values as close to this bound as possible in order to give the current mirror transistor Q_2 ample headroom to stay in saturation. Using voltage division, we can now find a relationship between R_1 and R_2.

$$\begin{aligned} v_{G,3} = -1.3\,V &= -5\,V + (5\,V - (-5\,V))\frac{R_2}{R_1 + R_2} \\ R_2 &\approx 0.587 R_1 \end{aligned}$$

The last step is to pick a value for R_1 or R_2. You have effectively unlimited choices at this point, so you only need to find values available to you to actually build with as well as ensure the values are large enough to maintain the high input impedance. In this case, Picking $R_1 = 560\,k\Omega$ yields $R_2 = 329\,k\Omega$, which is incredible close to the E12 series value of $330\,k\Omega$, so it would be a good choice for this circuit.

You will also need to find an acceptable value of R_D that is available to you for prototyping. $9.1\,k\Omega$ is in the E24 series, so it is a common value, but you may need to round the calculated resistance to an available value then recalculate the bias current needed to get the correct gain. You will lose some peak to peak voltage using this approach, so ensure that the change to the output range is within your design tolerances.

4.7 Prelab

Task 4.7.1: Prelab Questions

Please complete the following tasks assuming $V_{DD} = 5\,V$ and $V_{SS} = -5\,V$. Use the V_{th} and k_n values you measured in experiment 3. For k_n, use the value for when $v_{GS} = 2.5\,V$. Assume $\lambda = 0$.

1. Refer to the circuit in figure 4.9 for the following questions.
   a) *Derive* an expression for v_{GS1} and v_{GS2} in terms of I_{REF}.
   b) *Derive* an expression for v_{DS2} in terms of I_{OUT}.
   c) *Calculate* the value of I_{REF} that causes $v_{GS2} - V_{TH} = v_{DS2}$.
   d) *Explain* what happens if I_{REF} is increased beyond the value found in step 1c.

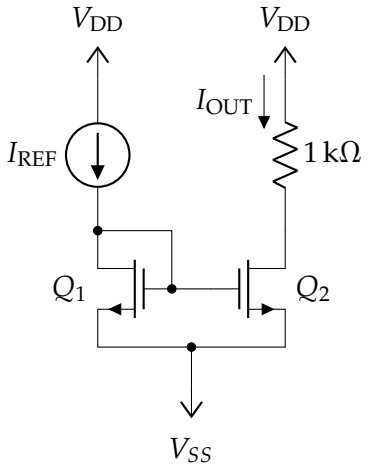

Figure 4.9: Simple current mirror with a load resistor.

2. Pick R_1, R_2, R_D, and I_{BIAS} in figure 4.7 on page 41 to achieve $A_v = -4$, $V_{out,dc} \approx 1\,V$ and $V_{out,min} \approx -1\,V$ using Q_1, Q_2, and Q_3. Pick R_1 and R_2 such that $R_1 \parallel R_2 > 100\,k\Omega$. This design can be done using equations (4.3) and (4.9) to (4.11).

4.8 Tasks

Task 4.8.1: Build and test the current mirror

1. *Build* the circuit shown in figure 4.10 using the ALD1106 with $R_{REF} = R_{TEST} = 1\,k\Omega$.

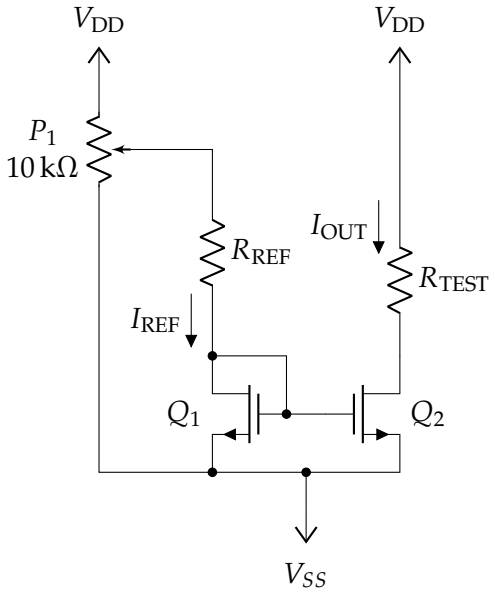

Figure 4.10: Circuit for testing a current mirror.

2. *Plot* the output current I_{OUT} versus the input current I_{REF} over the range 0.1 mA to 2.5 mA. The current can be measured by finding the voltage across R_{TEST} and R_{REF} at each point.

3. Set the reference current to the designed current for the amplifier that you calculated in prelab task 4.7.1 question 2. *Measure* the gate to source voltage, v_{GS}, and the drain to source voltage, v_{DS}, for each transistor.

Task 4.8.2: Build and test the amplifier

1. *Calculate* the values of C_1 and C_2 necessary to make each filter have a 3dB point lower than 30 Hz using equations (4.12) and (4.13).

2. *Build* the circuit in figure 4.7 using the values calculated in the prelab. Use the ALD1106 for all 3 transistors.

3. *Set* v_{IN} to 0 V and measure the DC value of v_{OUT}. Adjust the potentiometer until the DC value of v_{OUT} is the design target of 1 V. This ensures that the bias current is correct.

4. *Set* v_{IN} to be a 200 mV_{p-p} sine wave at 500 Hz.

5. *Capture* an oscilloscope screenshot showing v_{IN} and v_{OUT}
6. *Calculate* the small signal gain $A_{\text{V}} = \frac{V_{\text{out,p-p}}}{V_{\text{in,p-p}}}$.
7. *Plot* $|A_{\text{v}}|$ versus frequency for $1\,\text{Hz} < f < 500\,\text{kHz}$.
8. *Change* v_{IN} to be a $1\,\text{V}_{\text{p-p}}$ 5 kHz triangle wave.
9. Slowly *increase* the amplitude of v_{IN} to find the largest signal that does not cause significant distortion at the output.
10. *Capture* a screenshot showing the maximum amplitude input and output triangle wave using the oscilloscope.