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Section: 009

Lab: 05

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Abstract

The purpose of these experiments was to demonstrate how each of the building blocks of an opamp work. First, a current mirror was built using an ALD1106. Current values for I_{ref} and I_{test} were measured to verify the current mirror worked. Next, a differential amplifier using resistive loads was built (using an ALD1105) and attached to the current mirror. The common mode, differential, and single ended gains were found to verify the differential amplifier. The CMRR was also found in decibels. Finally, the resistive load in the differential amplifier was replaced by active loads using the same ALD1105. The experiment was important to understand how opamps work below the surface. All measurements were taken using an AD2, and all waveforms and power supplies were provided by the same AD2.

Task 1

Objective

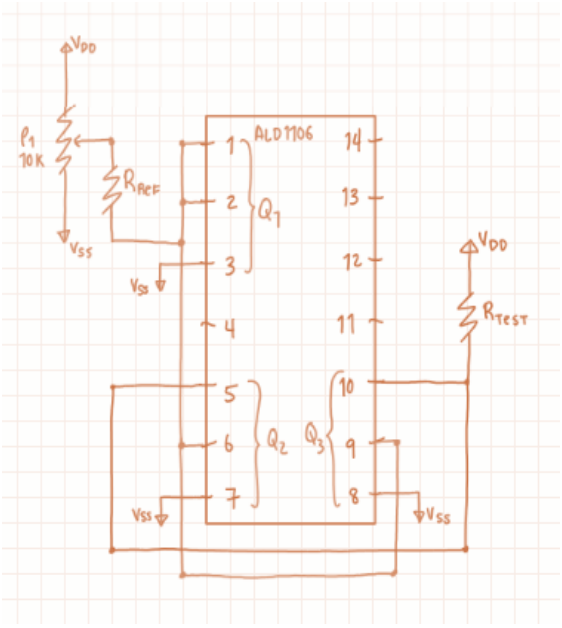
The objective of this task is to demonstrate how a current mirror is built and works.

Procedure

First, the R_{ref} and R_{test} were chosen so the MOSFETs in the circuit stay in saturation. The values for both were set to 1kΩ and then verified using equations below. Afterwards, the circuit was built. From the circuit I_{ref} and I_{out} were measured. I_{ref} vs I_{out} was plotted over .1ma – 5ma. The results were compared to the expected I_{ref} and I_{out} and analyzed on the differences.

Results

Circuit Diagram:



Equations used to verify R_{ref} and R_{test}:

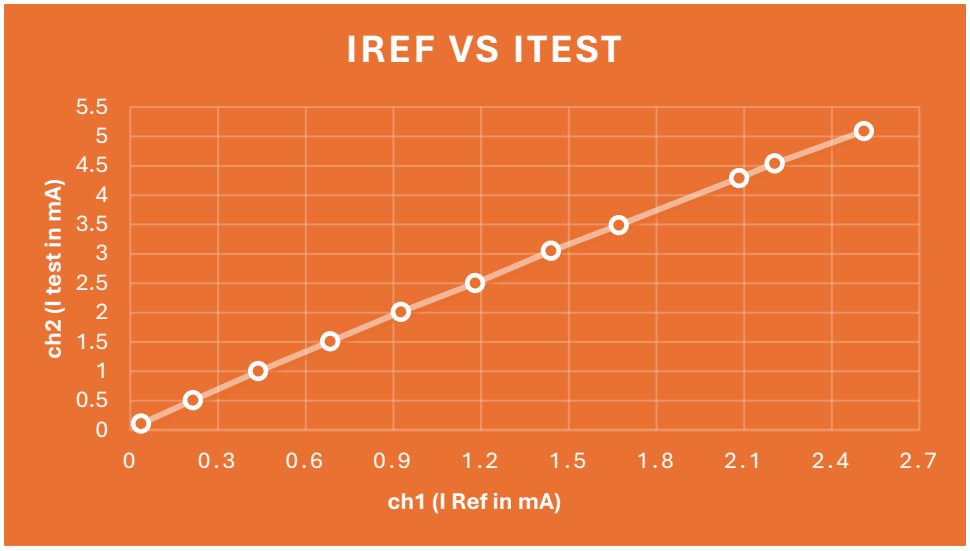
$$V_{GS} - V_T < V_{DS1} = V_{DD} - I_{REF}V_{REF} - V_T < V_{DD} - I_{REF}R_{REF}$$

$$V_{GS2} - V_T < V_{DS2} = I_{REF}R_{REF} - V_T < V_{DD} - I_{OUT}R_{TEST} = V_{DD} - I_{REF}R_{REF} < V_T - V_{DD} - 2I_{REF}R_{TEST}$$

I_{ref} and I_{out} measurements

Ref (mA)	Test (mA)
0.037676	0.10786
0.21402	0.5047
0.43812	1
0.68426	1.5077
0.926	2.011
1.1802	2.4997
1.44	3.05
1.672	3.49
2.083	4.29
2.2052	4.542
2.51	5.09

I_{ref} vs I_{out} plot



The graph shows a linear relationship in I_{ref} and I_{test}. It has a slope of approximately I_{test} = 2 I_{ref}. It is not perfect since we are not using perfectly ideal MOSFETs.

Conclusions

This task was successful because the current mirror was built, and the values of current were what was expected to be from the current mirror.

Task 2

Objective

The purpose of this task is to find the differential gain, the single ended gain, and the common mode gain and compute minimum the CMRR of the circuit. This task demonstrates how to find the different types of gain.

Procedure

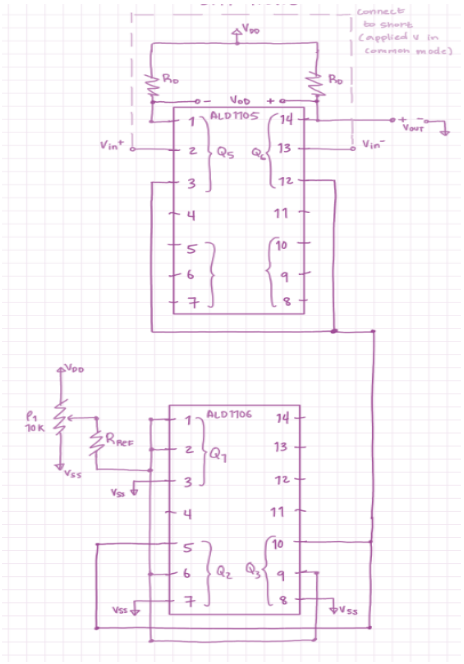
First, the circuit below was built using an ALD1106 and an ALD1105. The value for R_D from the prelab was used so that the gain in the circuit would be equal to 4. v_{in+} and v_{in-} were grounded. V_{D5} and V_{D6} were measured. Next, the function generator was configured to output a 1kHz sin wave. The signal was attached to v_{in+} and v_{in-} was left as ground. v_{OD} was measured with the oscilloscope.

Afterwards, the function generator amplitude was adjusted until v_{OD} was 250mV peak to peak. The single ended v_{OUT} was plotted and the single ended gain A_v was measured. The gain was compared to the expected value. v_{OD} was measured and plotted and the differential gain was calculated. This was also compared to the single ended value.

Next, the function generator amplitude was set to $250mV_{pp}$. v_{in+} and v_{in-} were shorted together. V_{D5} and V_{D6} measurements were taken and compared to nonideal differential amplifier behavior was compared. The common mode gain and CMRR was also calculated.

Results

Circuit diagram

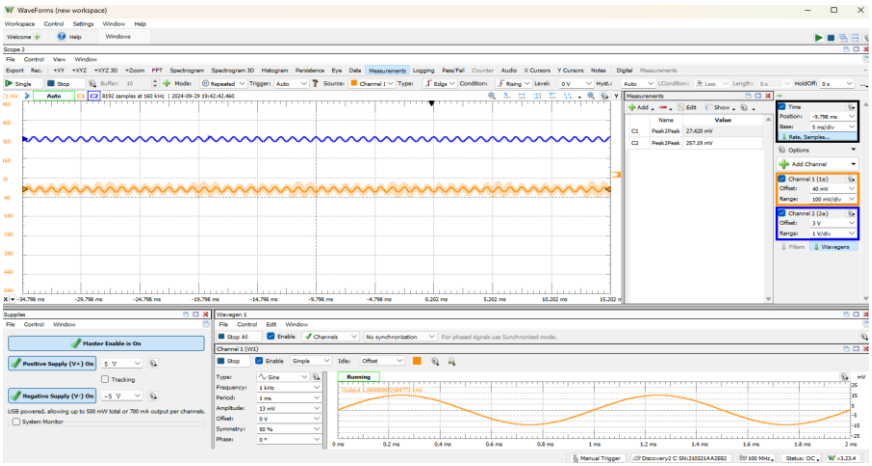


V_{D5} and V_{D6} voltages

	Voltage (V)
Vds5	2.41
Vds6	2.54

V_{D5} and V_{D6} should be equal. They are not exact since we do not have ideal MOSFETs.

v_{OD} and input plotted



Differential gain

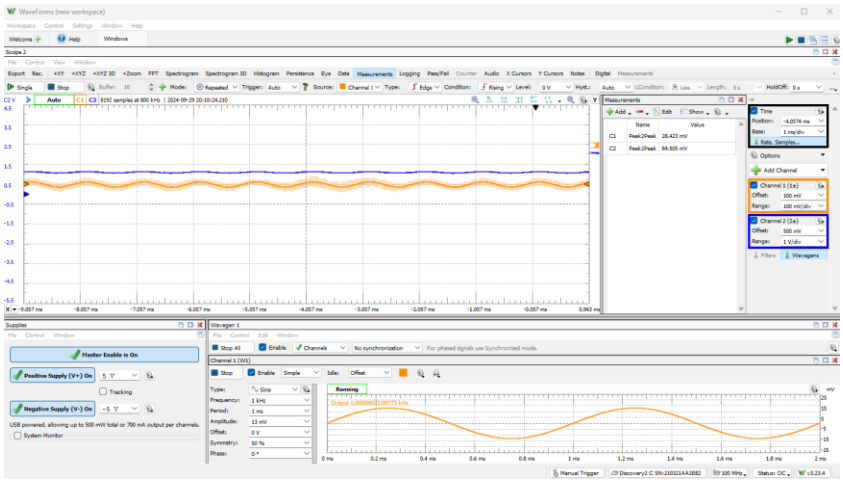
C1 = input = 27mv

C2 = v_{OD} = 254mv

$$A_d = \frac{V_{pp,out}}{V_{pp,in}} = \frac{254}{27} \approx 9.407$$

This gain is double the amount we designed for (4).

Input and Vd6 plotted



Single-ended gain

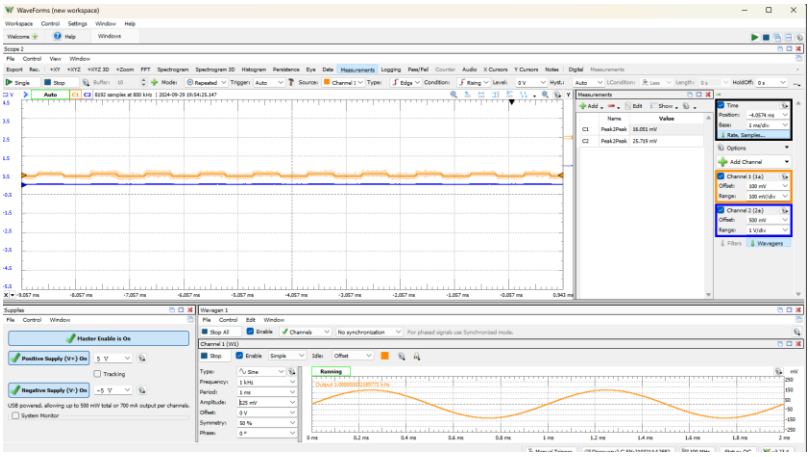
C1 = input = 28mV

C2 = vd6 to gnd = 84mV

$$A_v = \frac{V_{pp,out}}{V_{pp,in}} = \frac{84}{27} \approx 3$$

This gain is approximately the same as the gain we designed for (4). It is half of the differential gain.

v_{OD} and V_{out} plotted



	pp (mV)
c1 (vod)	16.051
c2 (vout)	25.719
Vcm	250

Minimum common mode gain:

$$A_{cm} < \frac{V_{od}}{V_{cm}\ (= 250mV)} = \frac{16}{250} \approx .064$$

Minimum CMRR (in decibels):

$$CMRR > 20\log\left(\frac{A_d}{A_{CM}}\right) = 20\log\left(\frac{9.4}{250}\right) = 43.34\ dB$$

Conclusions

This task was successfully completed because the differential gain, single ended gain, and common mode gain were all found. The minimum CMRR was also successfully found in this task.

Task 3

Objective

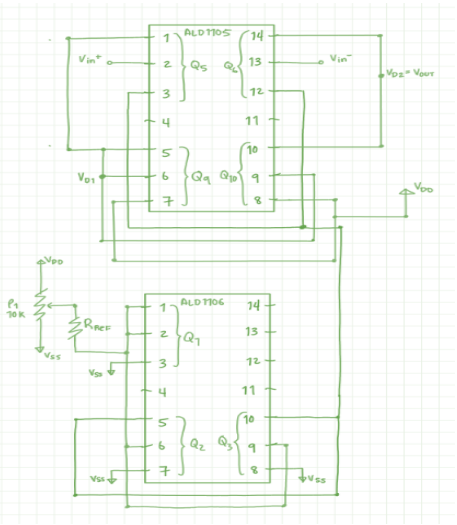
The objective of this task is to demonstrate the difference between active load and resistive loads. It shows how MOSFETs can be used to create active loads.

Procedure

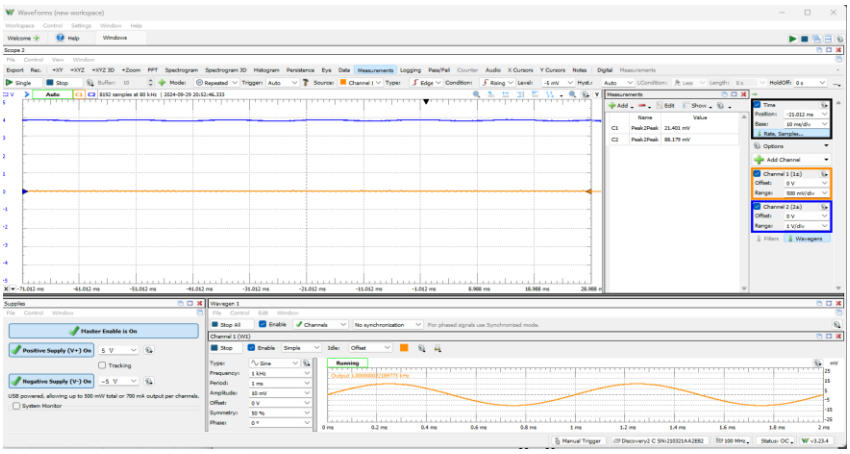
Using the same circuit but replacing the R_D resistors with active load MOSFETs on an ALD1105, the single ended input was measured and plotted. Next, the single ended output small signal gain was measured and plotted. The results of the active load were compared to that of the resistive load.

Results

Circuit



Single ended input and single ended output signals



C1 = $V_{in,pp}$ = 21.06 mV

C2 = $V_{out,pp}$ = 88 mV

$$A_v = \frac{V_{out,pp}}{V_{in,pp}} = \frac{88}{21.4} = 4.1$$

This gain is slightly higher than the resistive load A_v. This could be because I accidentally bumped into the potentiometer while updating the circuit or it could be the change in resistances. Also, after letting the circuit sit for a while, the $V_{out,pp}$ continued to rise slowly. This is likely since the potentiometer used was not the best.

Conclusions

This task was a success because the MOSFETs were successfully used as an active load in place of the resistors.