EXPERIMENT 1

CMOS Inverter

1.1 Application

The most common use of transistors worldwide is in digital logic gates. The Nvidia GTX 3090 Graphics Card has 28.3 billion transistors on the main graphics chip alone[1] where almost all of them are used as part of digital logic. In order to understand how to put transistors together to make such a complex system, we will start with the simplest logic gate: the inverter. The inverter takes a digital input (a '0' or '1') and outputs the opposite digital signal. Each CMOS inverter requires an NMOS and PMOS transistor to work in tandem to produce the desired result.

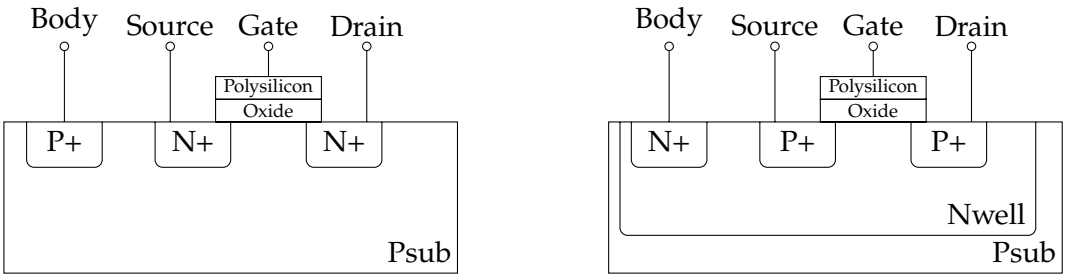

Figure 1.1: Structure of NMOS and PMOS transistors manufactured on a P doped substrate.

1.2 MOSFET structure

MOSFETs are four terminal, voltage-controlled, and high input impedance solid-state devices. They can operate in both depletion and enhancement mode. Enhancement mode MOSFETs are widely used as switches, amplifiers and in some cases as linear voltage regulators. On the other hand, there are fewer modern applications for depletion mode MOSFETs. Hence, for our experiments, we will only consider the characteristics and operations of an enhancement mode MOSFETs.

Figure 1.1 shows the overall structure of an NMOS and PMOS built in a conventional CMOS process. As you can see, each device has 4 terminals and is actually symmetric with regards to the source and drain. In fact, a MOSFET without a fixed connection between the source and body terminals can be used in either orientation. Most discrete MOSFETs are sold as a three terminal device, where the source is directly connected to the body terminal.

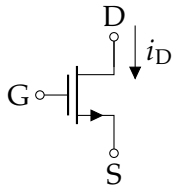

Figure 1.2: Three terminal NMOS circuit symbol

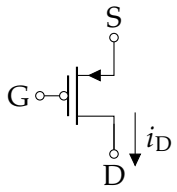

Figure 1.3: Three terminal PMOS circuit symbol

1.3 MOSFET large signal operation

Figure 1.4 shows the complete output characteristics of an n-channel MOSFET. This current versus voltage (I–V) plot shows the relationship between the current flowing through the MOSFET and the voltage between the drain and source of the MOSFET. This measurement is repeated for several values

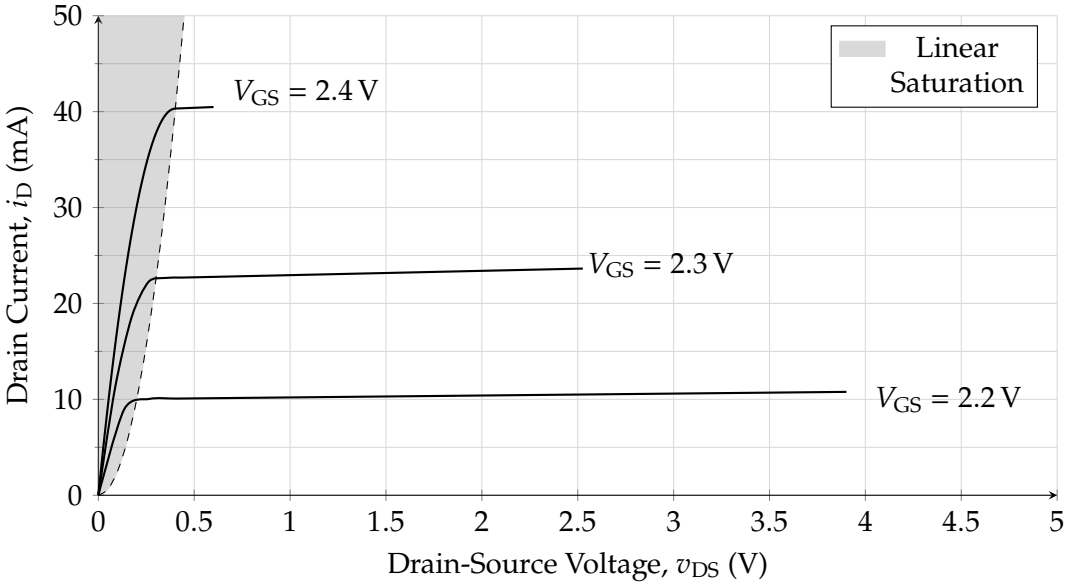

Figure 1.4: Output characteristics for an example n-channel enhancement mode MOSFET with $k_n = 0.5\,\text{A}\,\text{V}^{-2}$ and $V_{\text{th}} = 2\,\text{V}$.

of V_{GS} to generate what is called a "family of curves" for the MOSFET.

In order to understand the expected behavior of a MOSFET device, we need to look at its three modes of operation: cutoff, linear, and saturation.

1.3.1 Cutoff

Perhaps the simplest region to analyze, the cutoff region is when $v_{GS} < V_{th}$. In an ideal MOSFET, $i_D = 0$ when in the cutoff region. Real MOSFETs do have current flow in this subthreshold region, but the amount of current is insignificant compared to when the device is on.

1.3.2 Saturation

When $v_{GS} > v_{th}$ and $v_{DS} > v_{GS} - V_{th}$, the transistor is in saturation mode. While in saturation, the drain current is controlled only by the gate voltage and is only very weakly affected by the drain voltage. The drain current is proportional to the square of the gate-source voltage, as shown in equation (1.1).

While in the saturation region, the MOSFET acts like a voltage controlled current source, and when applied correctly, the device can be used to build a current source. The saturation region is also useful for building analog amplifiers. Both of these applications will be explored in future experiements.

$$i_D = \frac{k_n}{2}(v_{GS} - V_{th})^2 \tag{1.1}$$

1.3.3 Linear operation

The shaded portion of the I–V characteristic curve in Figure 1.4 shows the linear region of operation for MOSFETs; Within this region, MOSFETs act almost like resistors in which the current i_D is proportional to the voltage v_{DS} across the MOSFETs, as shown in equation (1.2). This resistance is called the on-resistance $R_{DS(on)}$. The effective resistance of the device is controlled by the v_{GS} applied to the transistor.

$$i_D = k_n\left((v_{GS} - V_{th})v_{DS} - \frac{1}{2}v_{DS}^2\right) \tag{1.2}$$

1.4 CMOS inverter

The circuit in figure 1.5 is a standard CMOS inverter. Ideally, it will take a logic high input at v_{IN} and output a logic low output at v_{OUT} or take a logic low input at v_{IN} and output a logic high output at v_{OUT}. An ideal logic high signal is equal to V_{DD} and an ideal logic low signal is equal to 0 V. In the circuit, if $v_{IN} = V_{DD}$, then the NMOS will turn on and the PMOS will have $v_{GS} = 0$ V. If the PMOS is off and the NMOS is on, then the output signal v_{OUT} will get pulled to

0 V. Conversely, when $v_{IN} = 0\,V$, the NMOS is off and the PMOS is on, so the output is pulled to $v_{OUT} = V_{DD}$ through the PMOS transistor.

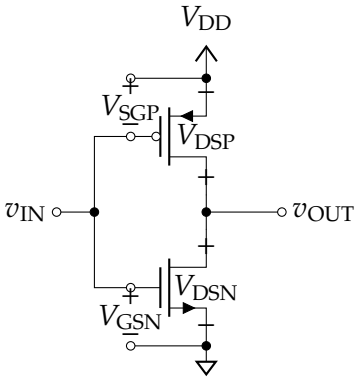

Figure 1.5: CMOS inverter circuit.

In the real world, logic inputs to an inverter are not perfectly equal to the supply voltages. We must develop some key parameters of a logic gate to explore what a real inverter will treat as a logic high or low and the input and output. We will use the voltage transfer characteristic to explore how an inverter behaves when the input is not perfect.

1.5 Voltage transfer characteristic

A two transistor CMOS inverter is shown in figure 1.5. When applied as a logic element, the transistors in this configuration spend most of the time in either the "on" or "off" state. That is, when the p-channel MOSFET (PMOS) unit is on, the n-channel MOSFET (NMOS) unit is off, and vice versa. Thus, most of the time, the transistors are not dissipating much power and therefore not much heat. This is one of the several core advantages digital signaling has over analog.

Most of the heat created by logic circuits is generated during the transition of signals from low to high and vice versa. Typically, the produced heat follows at least a square law, that is

$$Q \propto f^2$$

As a result the industry is trending to multi-processor systems in favor of faster clock speeds. In general, doubling the clock speed produces at least 4 times the heat while doubling the number of processors results in roughly the same processing power with only 2 times the heat.

Referring again to figure 1.5, we take a closer look at the inverter's operation under each valid input state

- If v_{IN} is a logic low[1], then:
  1. The NMOS transistor is off because $V_{GSN} < V_{GS(th)N}$.
  2. The PMOS transistor is on because $V_{SGP} > \left|V_{GS(th)P}\right|$.
  3. v_{OUT} is logical high because the output is brought to V_{DD} by the PMOS transistor.
- If v_{IN} is a logic high[2], then:
  1. The NMOS transistor is on because $V_{GSN} > V_{GS(th)N}$.

[1] Sometimes referred to as logic 0.

[2] Sometimes referred to as logic 1.

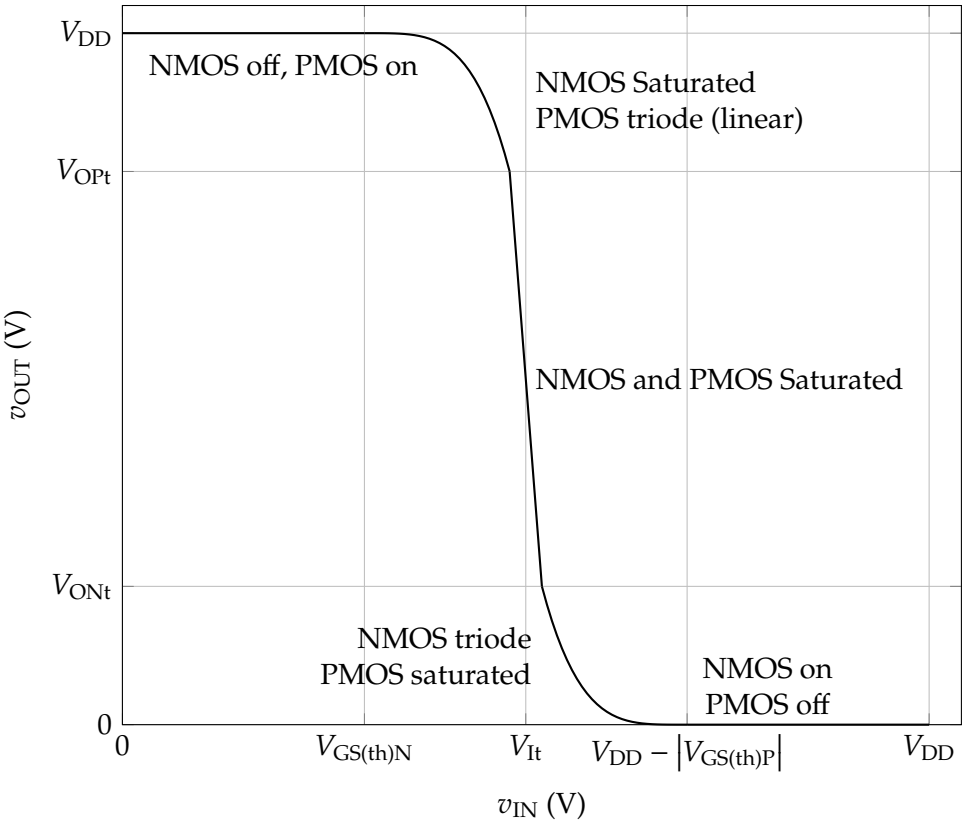

Figure 1.6: CMOS inverter voltage transfer characteristic with transition points and transistor operation modes labeled.

2. The PMOS transistor is off because $V_{SGP} < |V_{GS(th)P}|$.
3. v_{OUT} is logical low because the output is brought to ground by the NMOS transistor.

The typical inverter voltage transfer characteristic function is shown in figure 1.6. Here, it is annotated with the operation modes of the NMOS and PMOS transistors during the transition between the "off" and "on" states. The critical points in the transition are:

$(V_{GS(th)N}, V_{DD})$	When $0 \leq v_{IN} < V_{GS(th)N}$, the NMOS is in cutoff and, therefore, off. The PMOS is on because $V_{SGP} \approx V_{DD} > \left\|V_{GS(th)P}\right\|$ and in the linear region because V_{DSP} is small.
	When $V_{GS(th)N} \leq v_{IN} < V_{It}$, the NMOS begins to conduct and because V_{DSN} is large, it passes into the saturation region. The PMOS remains in the linear region because V_{DSP} is still small.
(V_{It}, V_{OPt})	When v_{IN} approaches V_{It}, v_{OUT} approaches V_{OPt}. At this point, the PMOS also passes into the saturation region. Both transistors are in saturation on the segment between (V_{It}, V_{OPt}) and (V_{It}, V_{ONt}).
(V_{It}, V_{ONt})	When $v_{OUT} = V_{ONt}$, the NMOS transistor enters the linear region and the PMOS transistor remains in saturation until $v_{IN} = V_{DD} - \left\|V_{GS(th)P}\right\|$.
$(V_{DD} - \left\|V_{GS(th)P}\right\|, 0\,V)$	When $V_{DD} - \left\|V_{GS(th)P}\right\| \leq v_{IN} \leq V_{DD}$, the PMOS transistor turns off. The NMOS is on because $V_{GSN} \approx V_{DD} > V_{GS(th)N}$ and in the linear region because V_{DSN} is small.

Inverters consume most of their power when transitioning. The current flows in through the PMOS transistor and charges the parasitic capacitance at the output then the energy is removed through the NMOS device. When both the NMOS and PMOS are conducting, they have a parasitic resistance that leads to current dissipation in the transistor. If the input transistion is slow, then both transistors will allow current to flow directly from V_{DD} to ground, which can lead to a significant amount of power consumption.

1.6 Noise margins

The transfer characteristic shown in figure 1.7 is identical to the transfer characteristic shown in figure 1.6. However, the points of interest are pertinent to the discussion of noise margins.

The foundation of the concept of noise margins is the concept of small signal gain. Small signal gain is equal to the slope of the relationship between v_{OUT} and v_{IN}. The small signal gain varies greatly throughout the transfer characteristic.

- When v_{IN} is small, the small signal gain is approximately 0.
- When v_{IN} is near V_{IL}, the small signal gain approaches -1.
- When v_{IN} is between V_{IL} and V_{IH}[3], the small signal gain is a large negative number.

[3] That is, near V_{It}.

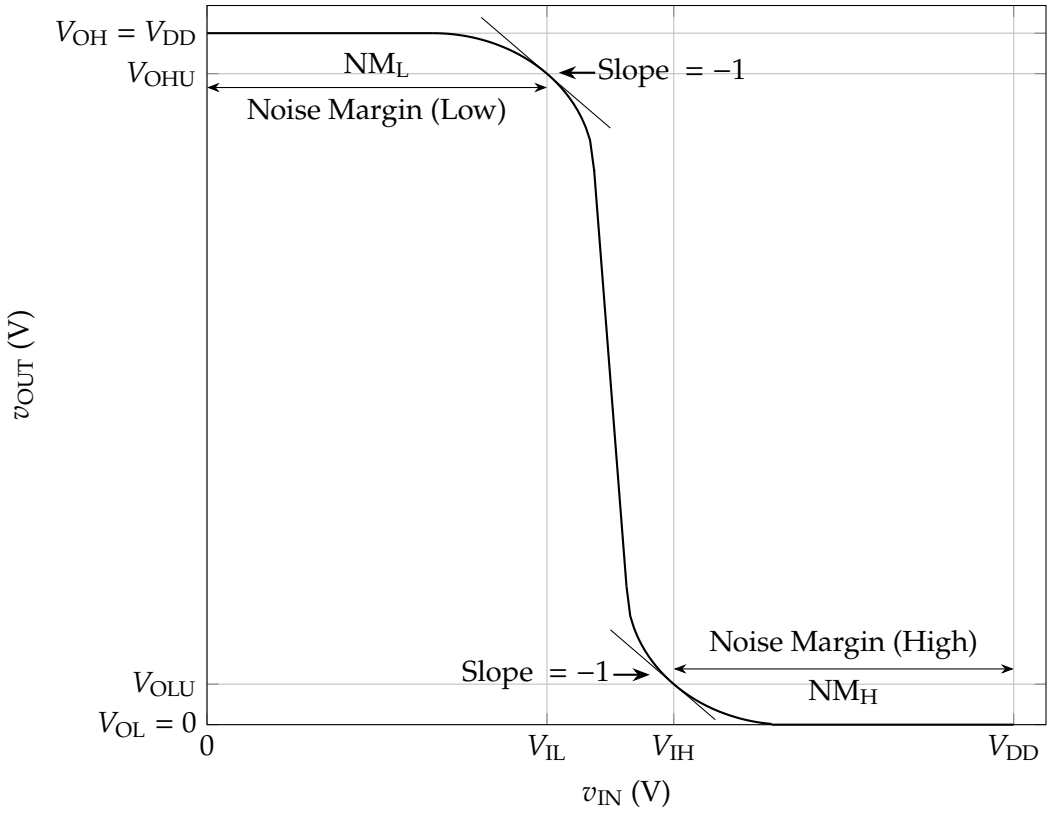

Figure 1.7: CMOS inverter voltage transfer characteristic with transistor input and output signals and noise margin parameters labeled.

- When v_{IN} is near V_{IH}, the small signal gain approaches -1.
- When v_{IN} is near V_{DD}, the small signal gain is approximately 0.

In figure 1.7, if $v_{IN} = \frac{V_{IL}}{2}$, the output voltage is $v_{OUT} = V_{DD}$.

Furthermore, if a small noise signal is added to v_{IN}, so that: $v_{IN} = \frac{V_{IL}}{2} \pm \frac{V_{IL}}{8}$ and the output voltage remains approximately equal to V_{DD}.

This result is very desirable. It shows that, even though v_{IN} is not a perfect logic low, the output remains a clear logic high.

This convenient situation stems from the fact that, in this region, the small signal gain is 0.

Clearly, a similar situation exists as v_{IN} approaches V_{DD}. In this case, v_{IN} can vary considerably but v_{OUT} remains approximately equal to 0. v_{IN} is not a perfect logic high, but v_{OUT} remains a clear logic low.

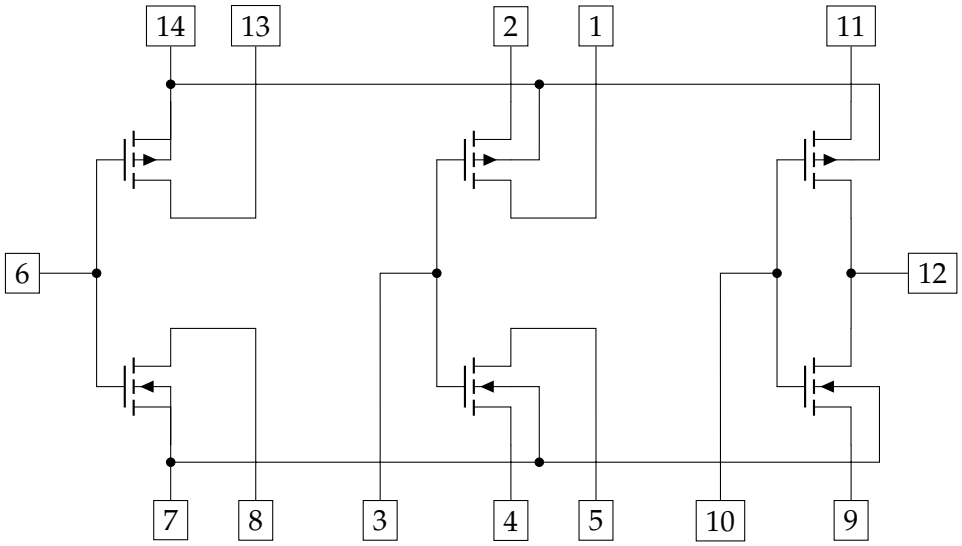

Figure 1.8: dual complementary pair plus inverter.

The regions that tolerate considerable variation of logic inputs and still produce clear logic outputs are the noise margins. For our purposes, we will define the noise margin as the area where magnitude of the small signal gain is less than 1, that is, where the inverter is attenuating any noise at the input. Every signal has some noise. Noise in electronic signals arises from many sources.(4)

(4) Some common sources of noise are the thermal noise that is inherent in resistors and semiconductors, signal leakage through materials, and signals from nearby circuits introduced by capacitive and inductive coupling.

The points $(V_{\text{IL}}, V_{\text{OH}})$ and $(V_{\text{IH}}, V_{\text{OL}})$ are the points where the slope of the transfer characteristic is -1. Below V_{IL}, the magnitude of the small signal gain is less than 1. Above $V_{\text{GS(th)}}$, the magnitude of the small signal is less than 1.

It is standard practice to state that V_{IL} is the largest input voltage that produces a recognized logic high output. and V_{IH} is the smallest input voltage that produces a recognized logic low output.

Because of the noise attenuating abilities of the inverter, a single inverter can help clean up a noisy digital signal.

1.7 The CD4007UB [2] dual complementary pair plus inverter

The CD4007UB [2] multipurpose device consists of three n-channel and three p-channel enhancement mode devices packaged to provide access to each device. These versatile parts can be reconfigured to create a wide array of logic gates and even some analog circuits. Each input is diode protected

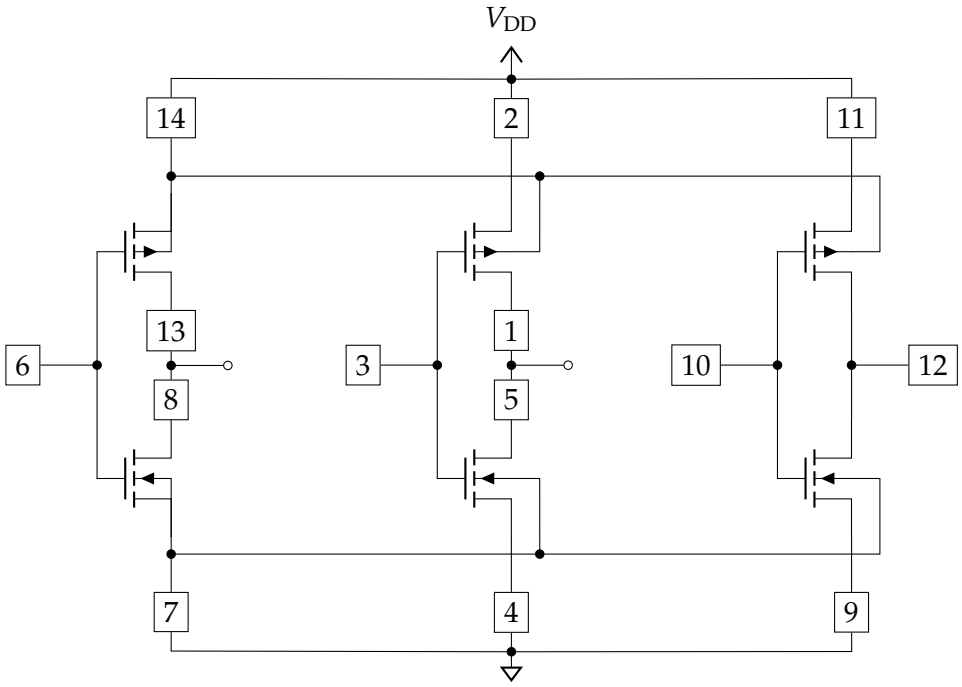

Figure 1.9: CD4007UB arranged as three inverters.

to prevent static damage. Figure 1.8 shows the schematic and pin assignments for the standard 14-pin dual in-line package.

In figure 1.8, it can be seen that the substrate is accessible for the transistors. This can be useful for biasing the substrate in non-standard ways, but typically the NMOS substrate is connected to the lowest voltage in the circuit, typically ground, and the PMOS bulk connection should be connected to the highest voltage in the circuit, typically V_{DD}. In the 3 terminal MOSFETs you have used before, the bulk connection for the PMOS or NMOS is connected to the source terminal, but for this device you need to make sure that the bulk connection is biased correctly.

Figure 1.9 shows the transistors arranged to form three inverters. In each circuit, the unused inputs to the inverters will be connected to ground. This practice is generally followed to ensure that the unused inverters are held in a fixed state. If the practice is not followed, the unused inverters may oscillate or otherwise dissipate power unnecessarily.

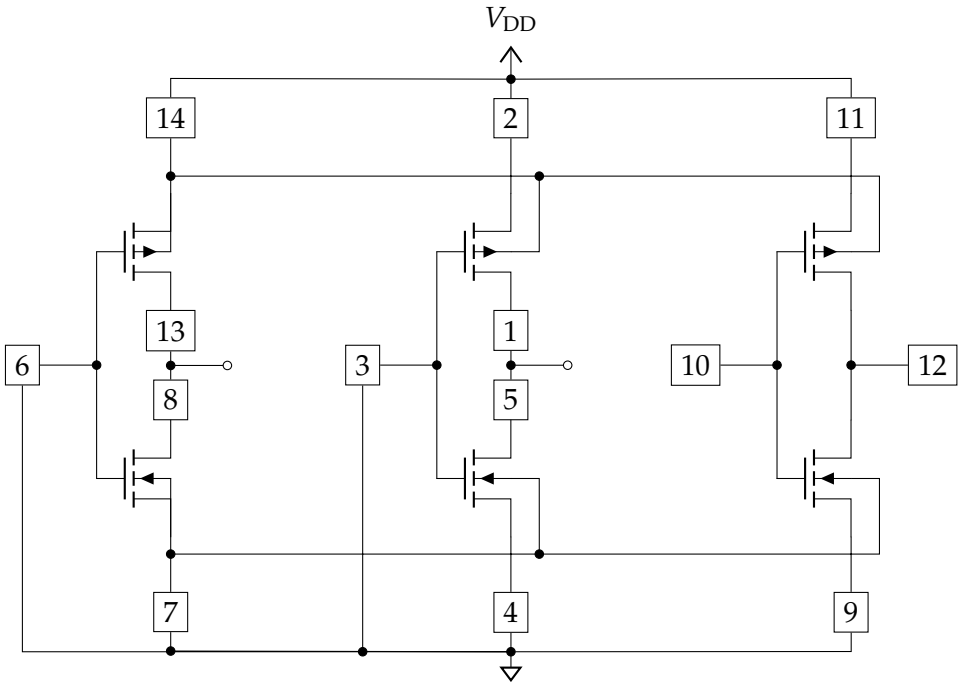

Figure 1.10: Circuit arrangement for measurement of inverter transfer characteristics.

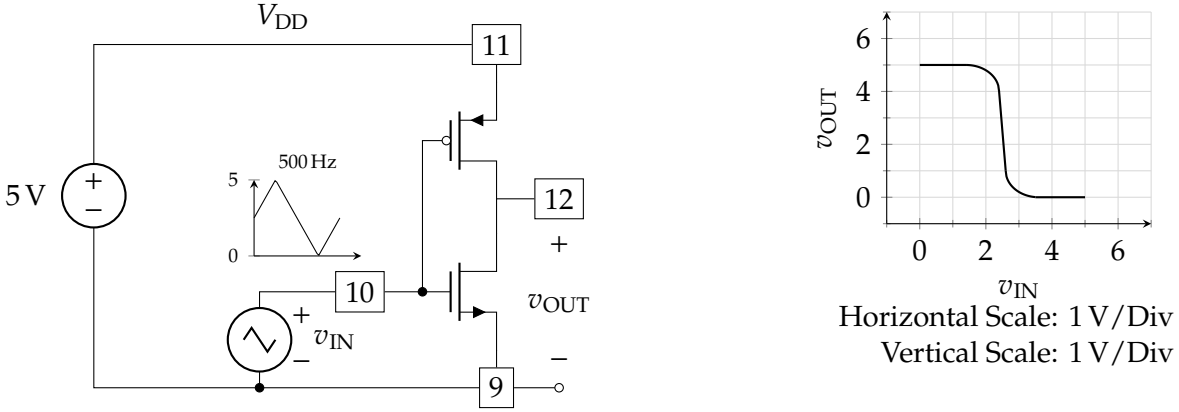

Figure 1.11: A test set to obtain typical transfer characteristics for an inverter.

1.8 A test set to obtain typical transfer characteristics

The set circuit of figure 1.11 consists of two loops:

1. **Drain supply** V_{DD} is held constant 5 V. No current limiting resistor is needed.
2. **Input signal** v_{IN} is swept from 0 V to 5 V. No current limiting resistor is needed.

Caution: Ensure that $-0.3\,\text{V} \leq v_{\text{IN}} \leq V_{\text{DD}} + 0.3\,\text{V}$ for all conditions by adjusting v_{IN} before connecting it to the input.

To obtain the solid characteristic curve shown in figure 1.11, V_{DD} is set to 5 V. Then, the input signal is carefully adjusted and applied. Use the XY mode of the oscilloscope to obtain the display.

1.9 Tasks

Task 1.9.1: Measurement refresher

In order to refresh your knowledge of the measurement equipment, please complete the following:

1. Use the function generator to generate the following signal:

$$2\sin(2\pi 750t)$$

2. *Capture* a screenshot of the waveform using the oscilloscope.
3. *Adjust* the oscilloscope view to plot several cycles of the waveform.
4. *Vary* the trigger level from −4 V to 4 V.
5. *Adjust* the horizontal offset.
6. *Adjust* the vertical offset.
7. *Describe* what each control does.
8. *Connect* the power supply output to the DMM input.
9. *Set* the power supply to 3.3 V.
10. *Measure* the DC and AC RMS values of the power supply output using the DMM.[a]

[a] Use the "voltmeter" tool on the AD2

Task 1.9.2: Measure the voltage transfer characteristic of a CMOS inverter

1. *Build* the CD4007UB circuit shown in figure 1.10. It is important to connect pin 3 and pin 6 to ground to prevent oscillations in the other two inverters as well as connect pin 7 and 14 correctly in order to bias the substrate.
2. *Add* the function generator and connect the oscilloscope to measure v_{IN} and v_{OUT} as shown in the circuit in figure 1.11.
3. *Draw* and *label* the circuit diagram for the circuit you built.
4. *Set* V_{DD} to 5 V.

5. *Apply* a 500 Hz 0 V to 5 V triangle wave to v_{IN}.
6. *Capture* a screenshot showing v_{IN} and v_{OUT} using the oscilloscope.
7. Change the display to XY mode and *Capture* the transfer characteristic and label the transition points:
   a) *Determine* by estimation and *label* the points
   $$\left(V_{GS(th)N}, V_{OH}\right), (V_{It}, V_{ONt}), (V_{It}, V_{OPt}), \left(V_{DD} - \left|V_{GS(th)P}\right|, 0\,V\right)$$
   b) *Label* the status of the NMOS and PMOS next to each of the five sections of the curve.
8. *Capture* another printout and label the noise margin parameters:
   a) *Determine* by estimation and *label* the points
   $$(V_{IL}, V_{OH}) \text{ and } (V_{IH}, V_{OL})$$
   b) *Determine* the magnitude of the noise margins and *label* the transfer characteristic with the noise margins.
   c) *Compare* the noise margins with the margins specified by the CD4007UB datasheet [2]. Note that the datasheet provided values are worst-case values, so you should not treat them as ideal values.

Task 1.9.3: A Digital Ring Oscillator

Up to this point we have looked at the DC characteristics of an inverter. We will now explore how fast the inverter is by creating a ring oscillator. Ring oscillators are distributed across the surface integrated circuit (IC) wafers to test the wafer's quality by determining the speed of the inverters.

1. *Create* a digital ring oscillator by cascading three logic inverters in series, with the output each stage driving the input of its successor. Feedback the output of the third inverter to the input of the first one. If the circuit does not start oscillating on its own, connect the input of one of the inverters to V_{DD} through a 100 kΩ resistor temporarily. The ideal oscillation frequency is $f_{osc} \approx {}^{1}/_{3(t_{PLH}+t_{PHL})}$.
2. *Obtain* an scope printout showing the oscillator working using an x10 probe[a] and *measure* the oscillation frequency, f_{osc}.
3. *Measure* the propagation delay of the inverters using a ×10 probe to measure the time from the $V_{DD}/2$ of the input to the $V_{DD}/2$ of the output of a single inverter using cursors on the oscilloscope display.
4. *Compare* the measured propagation delay with the CD4007UB datasheet [2].

[a] The normal inputs of the AD2 cannot be adjusted to x10, but that is acceptable for this experiment.

1.10 References

[1] *NVIDIA ampere ga102 GPU architecture*, V2.0, NVIDIA Corporation, 2020. [Online]. Available: https://www.nvidia.com/content/PDF/nvidia-ampere-ga-102-gpu-architecture-whitepaper-v2.pdf.

[2] *CMOS dual complementary pair plus inverter*, CD4007UB, Texas Instruments, Sep. 2003. [Online]. Available: http://www.ti.com/lit/ds/symlink/cd4007ub.pdf.