

# Sequential Circuit

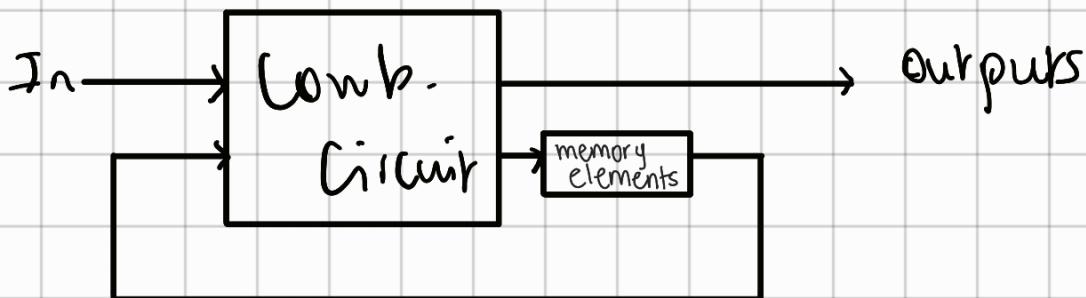
**Memory Elements:** Devices capable of storing information

**State of the Circuit at a Given Moment:**  
The Binary info stored at the el(s) at that moment

**(Combinational Circuit):** Outputs = Function(inputs)

**Sequential Circuit:**

Outputs = Function( inputs, circuit state)  
Next State = Function( present state, inputs)



Etat = state  
Sorties = output  
Suivant = next  
entrée = input

} common french terms.

When does the state of Seq. Circ. Change

- During the change of state of its inputs  
=> Asynchronous Sequential Circuit
- At discrete moments: Clock Signal.  
=> Synchronous / Clocked Sequential Circuit

Storage elements (memory) used in clocked sequential circuits are called Flip-Flops.

- A flip-flop is a binary storage device capable of storing a bit of information.
- In a stable state, the output of a flip-flop is 0 or 1.
- A sequential circuit can use multiple flip-flops to store as many bits as necessary.
- A change in the state of flip-flops is initiated only by a transition of the clock signal.

Example: the clock signal changes from 0 to 1.

the response time of the combinational circuit must be less than the period of the clock signal

An element of memory in a digital circuit can maintain a binary state indefinitely.

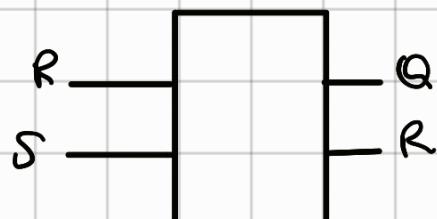
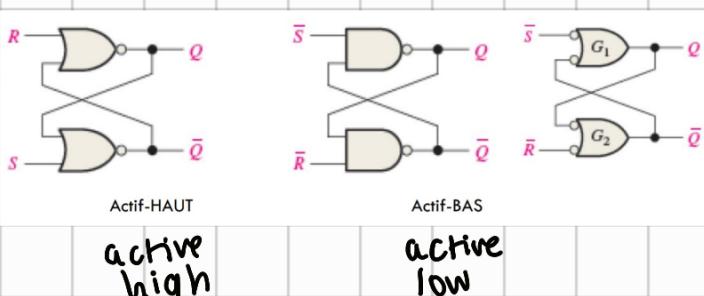
- Power supplied to the circuit
- Change of state according to an input signal

Differences between types of memory elements:

- Number of inputs
- How inputs affect the binary state

Latches: operate based on signal levels

FlipFlops: controlled by a clock transition

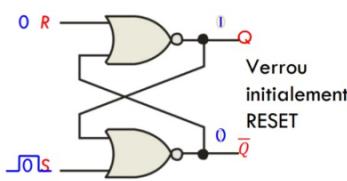


$$\begin{aligned} S = \text{Set} &= 1 \\ R = \text{Reset} &= 0 \end{aligned}$$

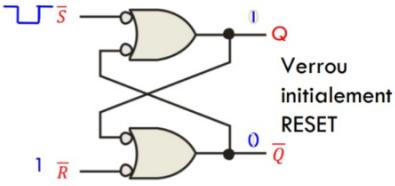
→ An active high SR latch is in stable (locked) condition when both inputs are low

$$Q(t+1) = \overline{R + \bar{Q}}$$

$$\overline{Q(t+1)} = \overline{(S + Q)}$$



latch initially  
reset



here in stable condition  
When both inputs are high

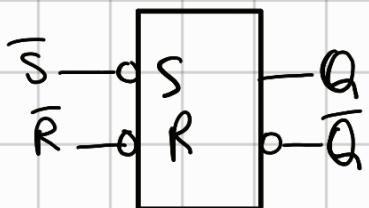
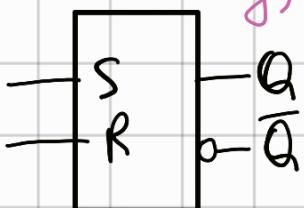
in  $\rightarrow$  we can't have both high  
in  $\circledast \text{D}$  we can't have both low

$Q$  {  $Q \xrightarrow{\text{present}}$   
 $Q^+, Q^{++} \xrightarrow{\text{next}}$

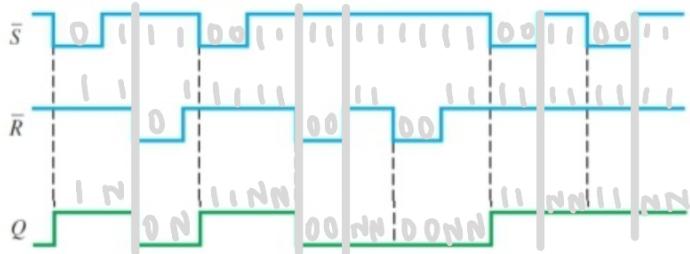
$Q$   
 $Q(t+1)$

S	R	$Q$	$\bar{Q}$
0	0	q	$\bar{q}$
0	1	0	1
1	0	1	0
1	1	0	0

No change (memory)  
Reset  
Set  
Invalid

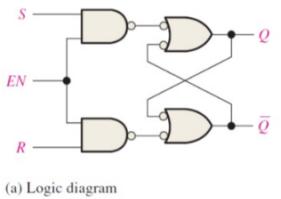


- Quelle sera la sortie du Verrou  $\bar{S} - \bar{R}$  actif-BAS pour les entrées suivantes?

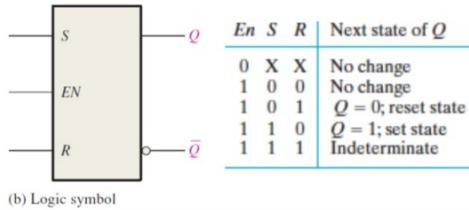


ISSUE: Issue with SR latches: parasitic signal on the inputs causing the latch to change

Solution: Latch with an enable (latched Latch)  
↳ EN must be high for the latch to respond to changes in S and R.



(a) Logic diagram

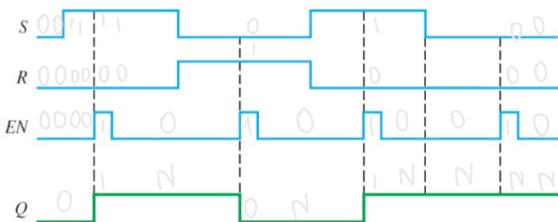


(b) Logic symbol

<i>En</i>	<i>S</i>	<i>R</i>	Next state of <i>Q</i>
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$ ; reset state
1	1	0	$Q = 1$ ; set state
1	1	1	Indeterminate



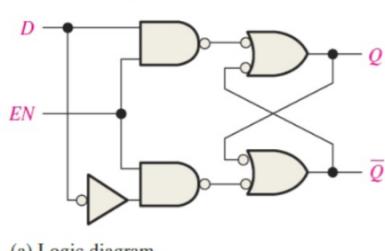
- Quelle est la forme d'onde de sortie *Q* si les entrées suivantes sont appliquées sur un verrou avec ENABLE étant initialement en état RESET



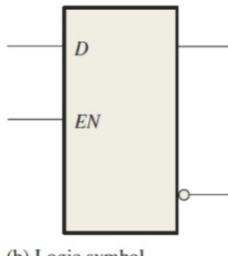
## Issue: Invalid Inputs | For bidden State

Solution: D Latch

- Single input *D* (for Data) + EN
- Our pur *Q* follows *D* + EN.
  - *D* = high, EN = high  $\Rightarrow$  Latch Set
  - *D* = low, EN = high  $\Rightarrow$  Latch Reset



(a) Logic diagram

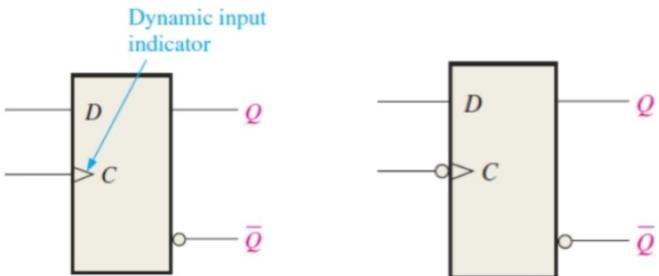


(b) Logic symbol

No change  $\Rightarrow$  EN=0  
 Ser  $\Rightarrow$  D=1  
 Reset  $\Rightarrow$  D=0

## Flip Flops

- A flip flop differs from a latches in the way it changes state.
- Clocked device, where only the clocked edge determines when a new bit is entered.
  - The active edge can be positive (rising) or negative (falling)



## D flip flop

the D input of the D flip flop is synchronous  
 ↳ the input is transmitted to the flip flop's output on the active edge (rising or falling) of the clock

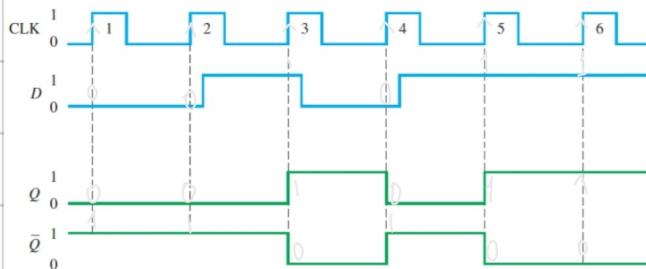
### Truth Table (Rising Edge)

D	CLK	Q	$\bar{Q}$
0	↑	0	1
1	↑	1	0

Reset

Set

- Quelles sont les formes d'onde des sorties  $Q$  et  $\bar{Q}$  de la bascule pour les entrées D et CLK suivantes



## JK Flip Flop

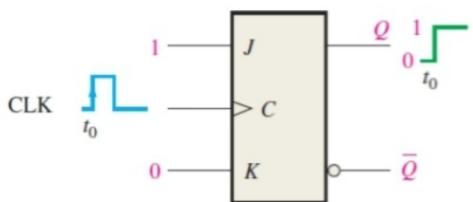
- D flip flop most used in logic circuits
- requires fewer gates for its construction
- other flip flops: JK and T
- Three operations: set - reset - toggle.
- D flip flop allows two operations: set and reset.
- JK flip flop allows all three operations

\* The J and K inputs of the JK flip flop are synchronous.  
→ inputs are transmitted to the flip flop's output on the active edge (rising or falling) of the clock.

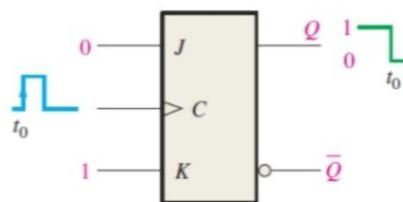
## Truth Table:

J	K	clk	Q	$\bar{Q}$
0	0	↑	$Q_0$	$\bar{Q}_0$
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	$\bar{Q}_0$	$Q_0$

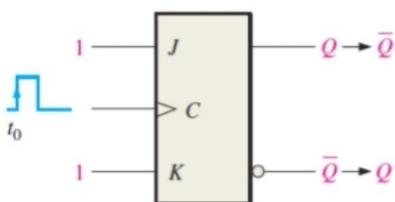
No change (memory)  
Reset  
Set  
Toggle.



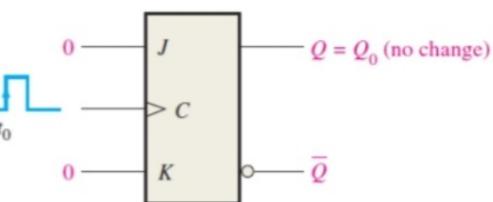
(a)  $J = 1, K = 0$  flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b)  $J = 0, K = 1$  flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

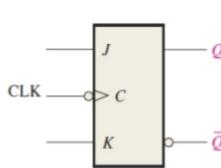
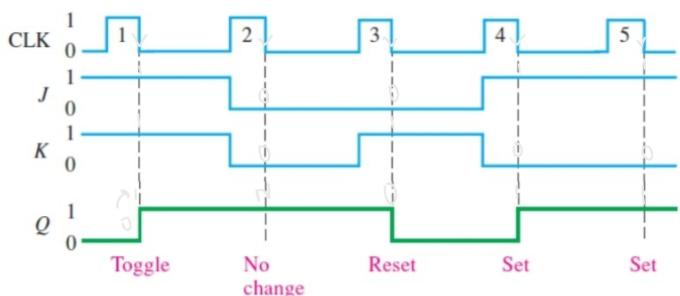


(c)  $J = 1, K = 1$  flip-flop changes state (toggle).



(d)  $J = 0, K = 0$  flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

- Quelle est la forme d'onde Q à la sortie de la bascule J-K pour les formes d'onde d'entrée suivantes? (Note: front actif descendant)

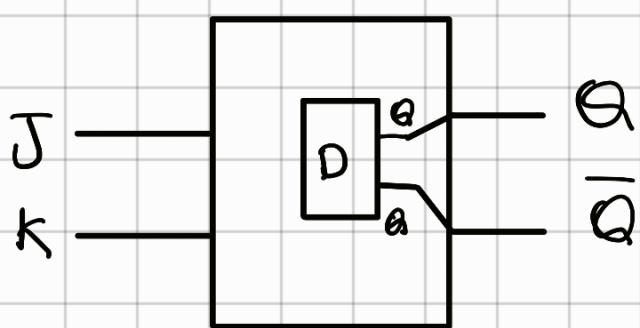


(falling edge active)

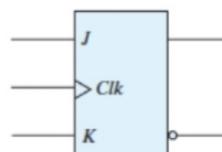
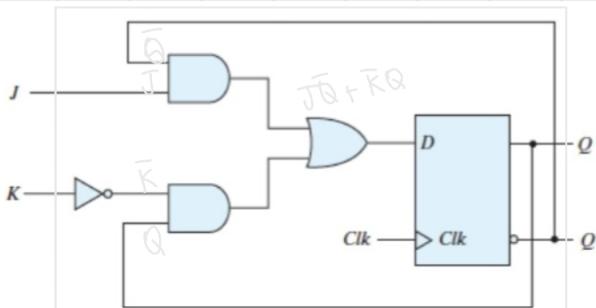
Design and Implement a JK flip flop using a D flip flop and logic gates

J	K	Q	$Q^*$	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	0	0
1	0	1	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

JK	Q	0	1
00	0	0	1
01	0	1	1
11	1	1	1
10	1	1	1



$$D = Q^* = \bar{J}Q + \bar{K}Q$$



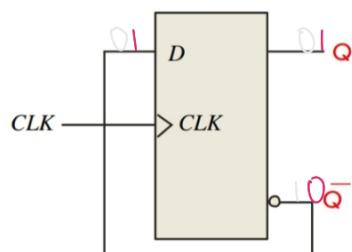
(a) Circuit diagram

(b) Graphic symbol

$$D = J\bar{Q} + \bar{K}Q$$

### D flip flop in toggle mode

- D can operate in toggle mode by conn the output Q to D
- the flip flop only changes on the active edge  $\Rightarrow$  the output changes only with each clock pulse

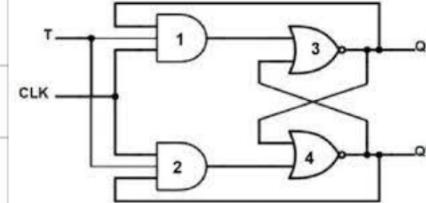
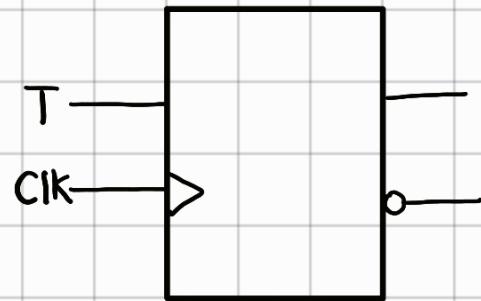


## Flip Flop T

$T = 0 \Rightarrow$  unchanged state  
 $T = 1 \Rightarrow$  toggle.

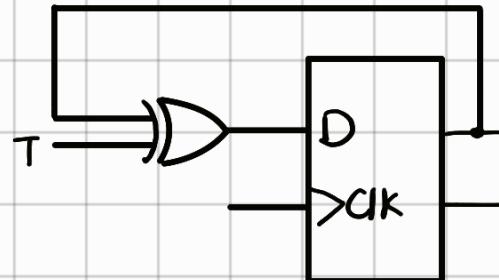
Q	T	Q <sub>ck</sub>	Q <sup>+</sup>
0	0	↑	0
0	1	↑	1
1	0	↑	1
1	1	↑	0

$$Q^+ = Q \oplus T$$



Design and implement a T flip flop using  
a) D flip flop  
b) JK flip flop.

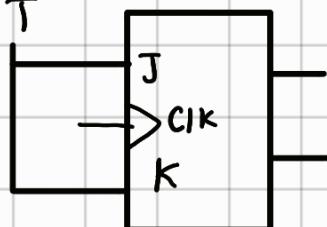
$$a) D = Q^+ = Q \oplus T$$



T	Q	Q <sup>+</sup>	J	K	J K
0	0	0	0	0	0 X
0	1	1	0	0	X 0
1	0	1	1	0	1 X
1	1	0	0	1	X 1

T	Q	Q <sup>+</sup>	J	K
0	0	0	0	0
0	1	1	0	0
1	0	1	1	0
1	1	0	0	1

$$J = T \quad K = T$$



Characteristic Table relationship b/w current state and next state of the flip flop based on inputs

JK:	J	K	Q*
0 0	0	0	Q
0 1	0	1	0
1 0	1	0	1
1 1	1	1	Q̄

D:	D	Q*
0	0	0
1	1	1

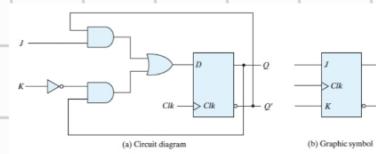
T:	T	Q*
0	0	Q
1	1	Q̄

## Characteristic Equations:

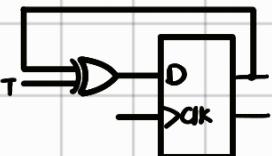
flip flop D:  $Q(t+1) = D$

flip flop JK:  $Q(t+1) = J\bar{Q} + \bar{K}Q$

flip flop T:  $Q(t+1) = T \oplus Q = T\bar{Q} + \bar{T}Q$



$$D = J\bar{Q} + \bar{K}Q$$



Next State =  $f(\text{inputs, present state})$

## Synchronous Inputs

Synchronous inputs (D or J-K) are transferred to the active edge of the clock.

Most flip-flops have asynchronous inputs

- Affect the output independently of the clock.

- Normally called PRESET (PRE) and CLEAR (CLR)

- Usually Active-LOW

Connected to override the input effect synchronous D and the clock.

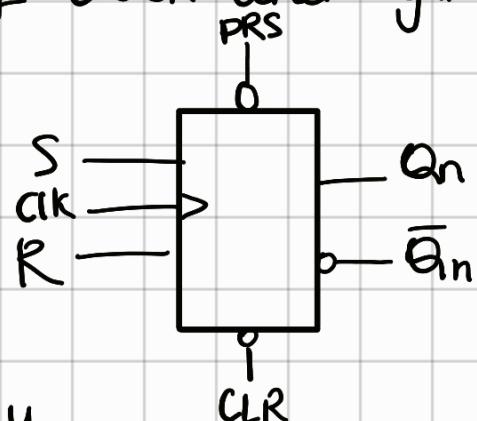
- PRESET and CLEAR are not practically low in same time

*preset = 0  $\Rightarrow Q_n = 1$*

*clear = 0  $\Rightarrow Q_n = 0$  because  $Q_n = 1$*

regardless of the values of clock and syn. inputs

PR	CLR	$Q_n$
0	0	INDEFINITE
0	1	1
1	0	0
1	1	will perform normally

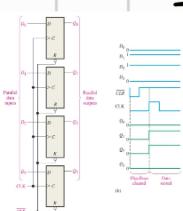


## Flip Flop Usage

→ Parallel Storage of Data

⇒ A group of flip flops are connected to data lines parallel and clocked at the same time.

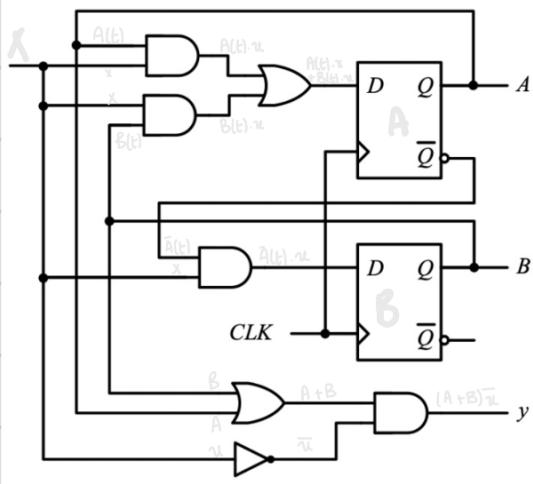
⇒ The Data is stored until the clock pulse next



# Analysis of Clocked Sequential Circuits

The analysis of a sequential circuit consists of:

- obtaining a state equation or transition equation
- obtaining a table state for the time sequence of inputs, outputs, and internal state.
- Draw a state diagram
- Draw a timing diagram



input(s):  $u$

flipflops: 2 D flipflops :  $D_A, D_B$

output(s):  $y$

$$Q(t+1) = D$$

$$A(t+1) = A u + B u$$

$$B(t+1) = \bar{A} u$$

$$y(t) = (A+B)\bar{u}$$

} state equations

## State Table

Present State	Input	Next State	Output
A B	$u$	A B	$y$
0 0	0	0 0	0
0 0	1	0 1	0
0 1	0	0 0	1
0 1	1	1 1	0
1 0	0	0 0	1
1 0	1	1 0	0
1 1	0	0 0	1
1 1	1	1 0	0

OR

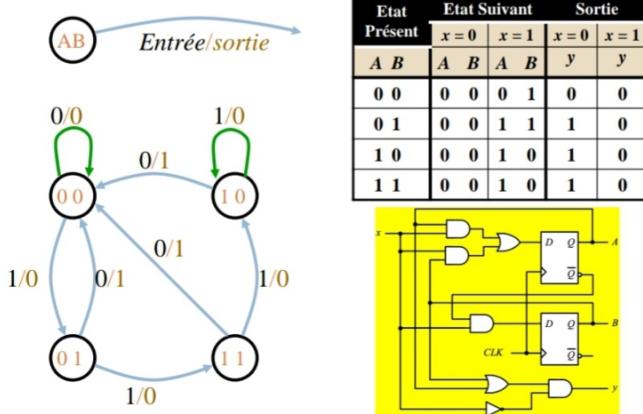
Present State	Next State		Output	
A B	$x=0$	$x=1$	$x=0$	$x=1$
0 0	0 0	0 1	0	0
0 1	0 0	1 1	1	0
1 0	0 0	1 0	1	0
1 1	0 0	1 0	1	0

t

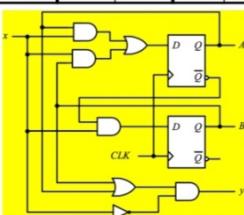
t+1

t

# State Diagram



Note:  $n$  flipflops  
 $\rightarrow 2^n$  states.



## Example (D flipflop)

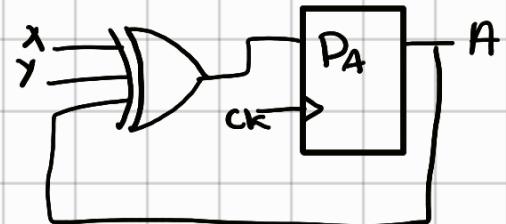
- Analyser le circuit décrit par l'équation d'entrée

$$D_A = A \oplus x \oplus y$$

- Pas d'équation de sortie  $\Rightarrow$  la sortie est celle de la bascule  $\Rightarrow A$

No output equation  $\Rightarrow$  the output is that of the flip flop  $\Rightarrow A$ .

inputs:  $x, y$   
 flipflops: 1 D flipflop ( $A$ )  
 outputs:  $A$ .

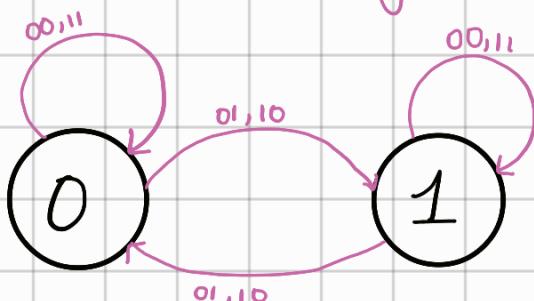


State Equation:  $A(t+1) = A^+ = A^* = D_A = A \oplus x \oplus y$

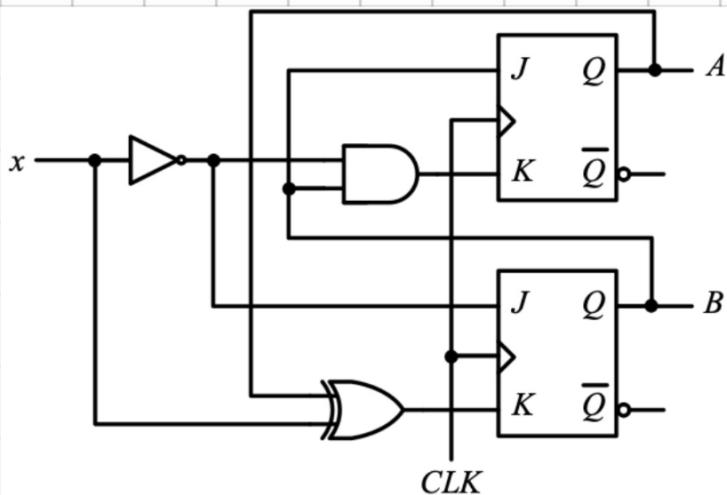
### State Table:

A	x	y	$A^+$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

### State Diagram:



# JK Flip Flop Analysis Diagram



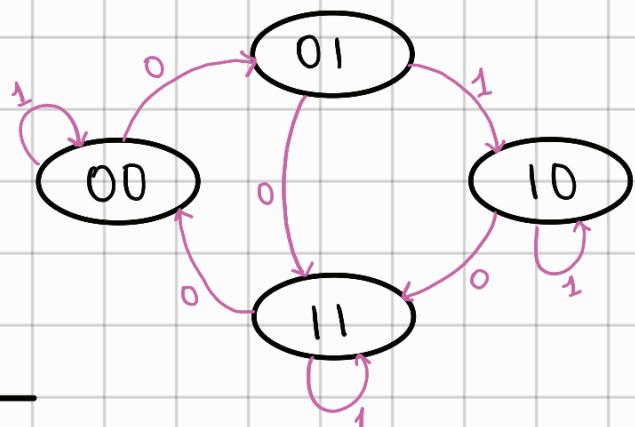
Input(s):  $u$   
 FlipFlop(s): 2 JK Bf. A, B  
 Output(s): no output

State Table:

A	B	$u$	$A^*$	$B^*$	$J_A$	$K_A$	$J_B$	$K_B$
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

I/O Equations

$$\begin{aligned}
 J_A &= B \\
 K_A &= B\bar{u} \\
 J_B &= \bar{u} \\
 K_B &= A \oplus u
 \end{aligned}$$



$A^*$ :	$x$	0	1
$AB$		0	1
00	0	0	0
01	1	1	1
11	0	1	1
10	1	1	0

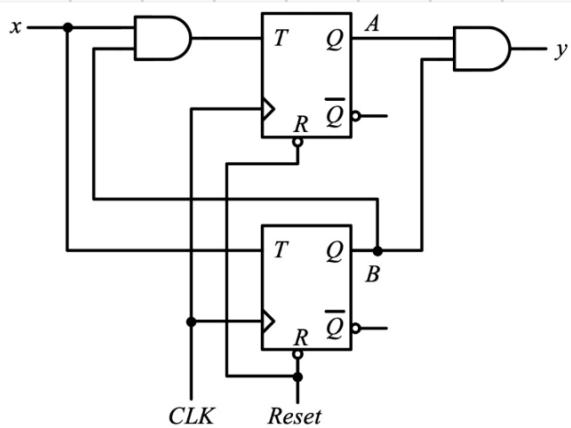
$B^*$ :	$u$	0	1
$AB$		0	1
00	0	1	0
01	1	1	0
11	0	0	1
10	1	0	0

State Equations

$$A^* = \bar{A}B + Bu + A\bar{B}$$

$$B^* = \bar{A}\bar{u} + \bar{B}\bar{u} + ABu$$

# T Flip Flop Analysis Diagram



Input(s) :  $u$

Flipflop(s): 2 T flip flops A,B

Output(s) :  $y$

Input Equation:

$$T_A = Bu$$

$$T_B = u$$

$$y = AB$$

A	B	$u$	$A^*$	$B^*$	$T_A$	$T_B$	y
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	0	1	0	0	0
0	1	1	1	0	1	1	0
1	0	0	1	0	0	0	0
1	0	1	1	1	0	1	0
1	1	0	1	1	0	0	1
1	1	1	0	0	1	1	1

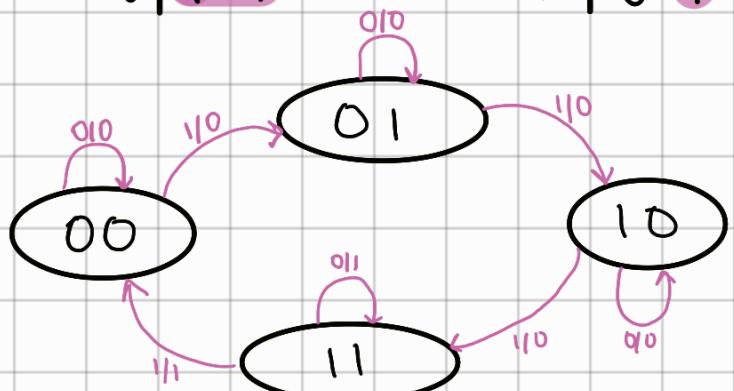
$A^*$ :	$AB \setminus x$	0	1
00	00	0	0
01	01	0	1
10	11	1	0
11	10	1	1

$B^*$ :	$A_B \setminus u$	0	1
00	00	0	1
01	01	1	0
11	11	1	0
10	10	0	1

State Equations:

$$A^* = \bar{A}Bx + A\bar{u} + \bar{A}\bar{B}$$

$$B^* = B\bar{x} + \bar{B}x = B \oplus x$$



Mealy and Moore

Mealy Model: output is a function of both the present state and the input

Moore Model: output is a function of only the present state

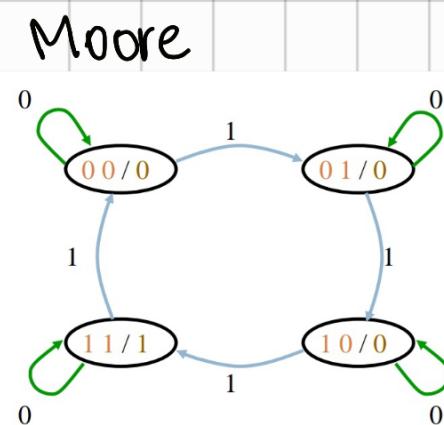
In a Moore Model the outputs of the seq. circuit are synchronized with the clock, because they depend only on flip-flop outputs that are synchronized with the clock

The output of the Mealy Machine is the value that is present immediately before the active edge of the clock

Basically when the output is independent of the input (ex:  $y = \overline{Q_B} + Q_A$ ) it's Moore.

Mealy		Moore			
Etat Present	E	Etat Suivant	S		
A	B	x	A	B	y
0 0	0	0 0	0	0	0
0 0	1	0 1	0	0	0
0 1	0	0 0	1	0	1
0 1	1	1 1	0	1	0
1 0	0	0 0	1	0	1
1 0	1	1 0	0	1	0
1 1	0	0 0	1	1	1
1 1	1	1 0	0	1	0

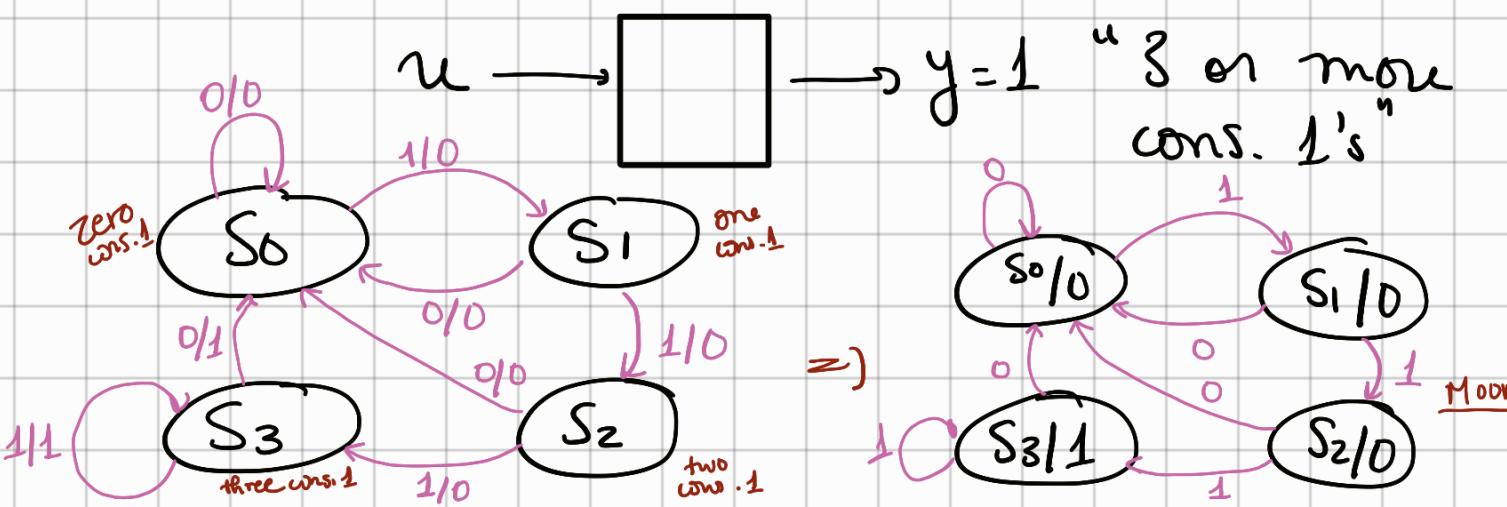
Mealy		Moore			
Etat Present	E	Etat Suivant	S		
A	B	x	A	B	y
0 0	0	0 0	0	0	0
0 0	1	0 1	0	0	0
0 1	0	0 1	0	1	0
0 1	1	1 0	0	0	0
1 0	0	1 0	0	0	0
1 0	1	1 1	0	1	0
1 1	0	1 1	1	1	1
1 1	1	0 0	1	0	0



## Design of Timed Sequential Circuit

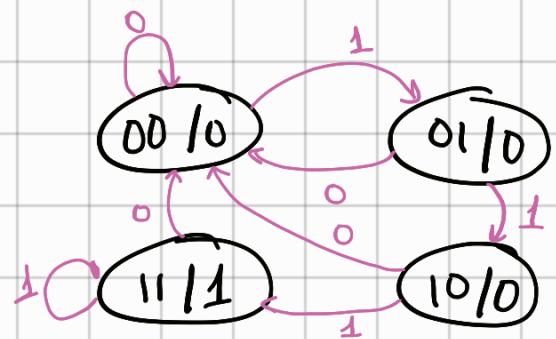
Example:

Detect 3 or more consecutive 1's



4 States  $\Rightarrow$  2 flipflops

State	A	B
S <sub>0</sub>	0	0
S <sub>1</sub>	0	1
S <sub>2</sub>	1	0
S <sub>3</sub>	1	1



Present State	Input	Next State	Output		
A	B	u	A <sup>+</sup>	B <sup>+</sup>	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

Flip Flop D: State equation = Input Equation

$$A^+ = D_A \quad B^+ = D_B \quad y = ?$$

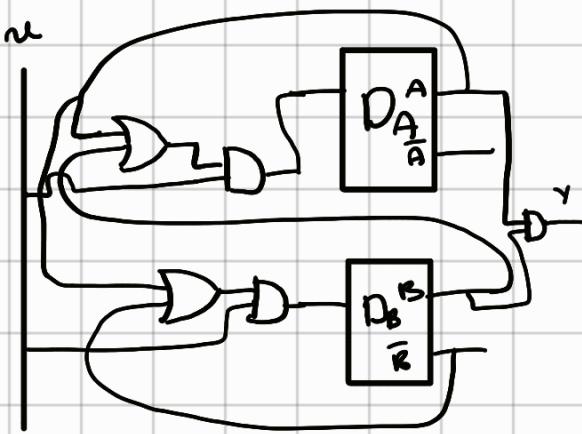
A <sup>u</sup>	B <sup>u</sup>	0	1
00	0	0	0
01	0	1	
11	0	1	
10	0	1	

A <sup>u</sup>	B <sup>u</sup>	0	1
00	0	1	u
01	0	0	
11	0	1	
10	0	1	

$$y = AB$$

$$\begin{aligned} A^+ &= Bu + Au \\ &= u(A + B) \end{aligned}$$

$$\begin{aligned} B^+ &= Au + \bar{B}u \\ &= u(A + \bar{B}) \end{aligned}$$





## WAY 2:

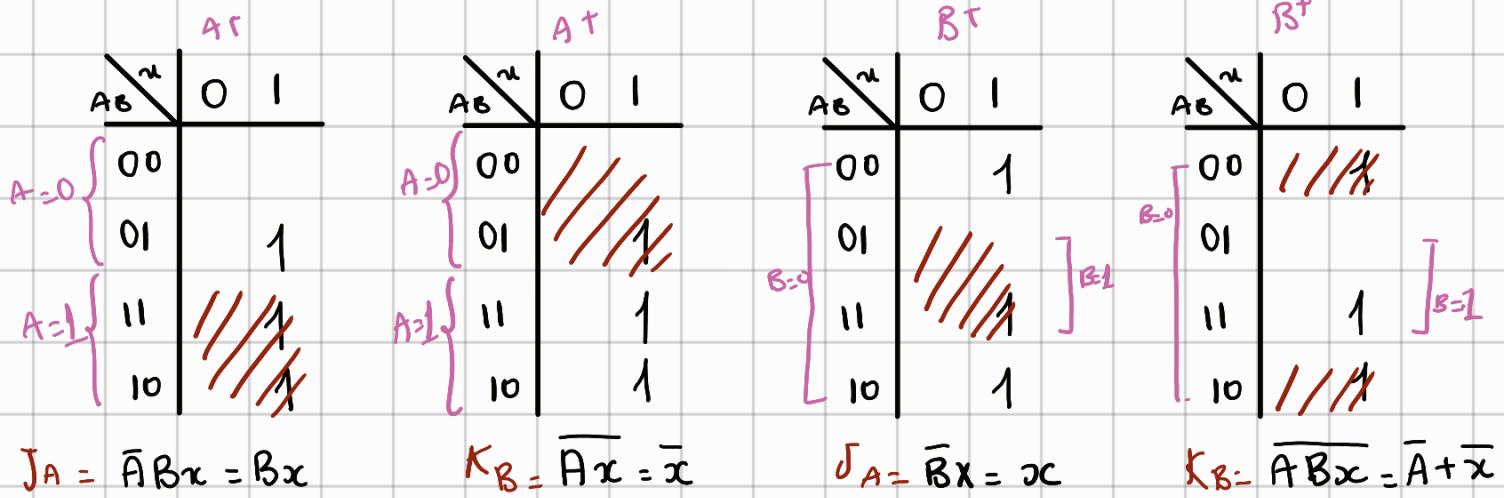
$$Q^+ = J\bar{Q} + \bar{K}Q$$

$$\begin{aligned} Q = 0 &\Rightarrow Q^+ = J \\ Q = 1 &\Rightarrow Q^+ = \bar{K} \end{aligned}$$

Present State		Input	Next State		Output
A	B	x	A <sup>+</sup>	B <sup>+</sup>	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	1	1
1	1	1	1	1	1

$$\begin{aligned} A^+ &= \bar{J}A + \bar{K}_{AA}A \\ A = 0 &\quad \bar{J}A = A^+ \\ A = 1 &\quad K_A = \bar{A}^+ \end{aligned}$$

$$\begin{aligned} B^+ &= JB + \bar{K}_B B \\ B = 0 &\quad JB = B^+ \\ B = 1 &\quad K_B = \bar{B}^+ \end{aligned}$$



## T Flip Flop:

Etat Présent	Entrée	Etat Suivant	Entrée Bascule
A B	x	A B	T <sub>A</sub> T <sub>B</sub>
0 0	0	0 0	0 0
0 0	1	0 1	0 1
0 1	0	0 0	0 1
0 1	1	1 0	1 1
1 0	0	0 0	1 0
1 0	1	1 1	0 1
1 1	0	0 0	1 1
1 1	1	1 1	0 0

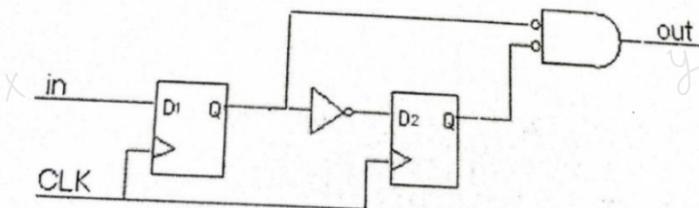
TA: AB	0	1
00		
01		
11		
10		

TB: AB	0	1
00		
01		
11		
10		

$$T_A = A\bar{x} + \bar{A}Bx$$

$$\begin{aligned} T_B &= B\bar{x} + \bar{B}Ax + \bar{A}x \\ &= B \oplus x \times \bar{A}x \\ \text{or } & B \oplus x + \bar{A}B \end{aligned}$$

# Exercise



- Give the input and output equations of this circuit.
- Give the state table of this circuit.
- Draw the circuit state diagram.
- Deduce if this circuit is a Mealy or Moore system. Justify your answer.
- Re-implement the circuit using JK flip-flops

a) input(s):  $\text{in}$

flip flops: 2 D flip flops  $D_1, D_2$ .

output(s):  $y$ .

$$D_A = \text{in}$$

$$D_B = \bar{A}$$

$$y = \overline{A}_1 \cdot \overline{B}$$

}

$$D_1 = \text{in}$$

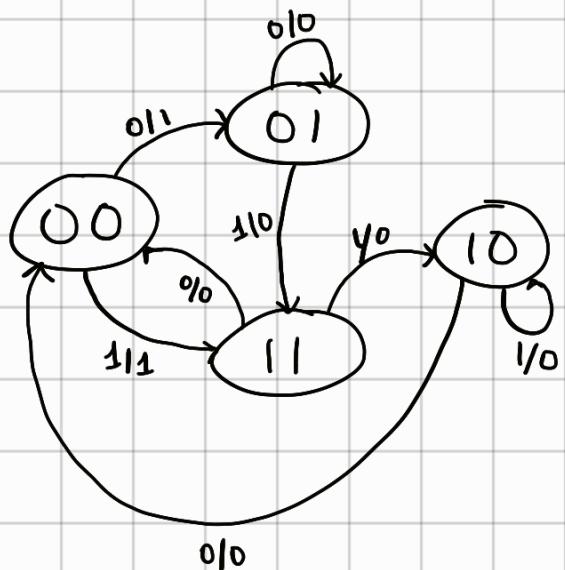
$$D_2 = \overline{Q}_1$$

$$y = \overline{Q}_1 \overline{Q}_2$$

b)

present state	inp	next state	out	
A	B	$A^+$	$B^+$	$y$
0	0	0	1	1
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	0

c)



d) Moore since the output isn't influenced by the input, as in the output for each state doesn't change with the change of input.

$$e) A^+ = J\bar{A} + \bar{K}A$$

$$A=0 \quad A^+ = J$$

$$A=1 \quad A^+ = \bar{K}$$

$$B^+ = J\bar{B} + \bar{K}B$$

$$B=0 \quad B^+ = J$$

$$B=1 \quad B^+ = \bar{K}$$

$A^+$	0	1
$\bar{A}\bar{B}$	0	1
00	0	1
01	0	1
11	0	1
10	0	1

$B^+$	0	1
$\bar{A}\bar{B}$	0	1
00	1	1
01	1	1
11	0	0
10	0	0

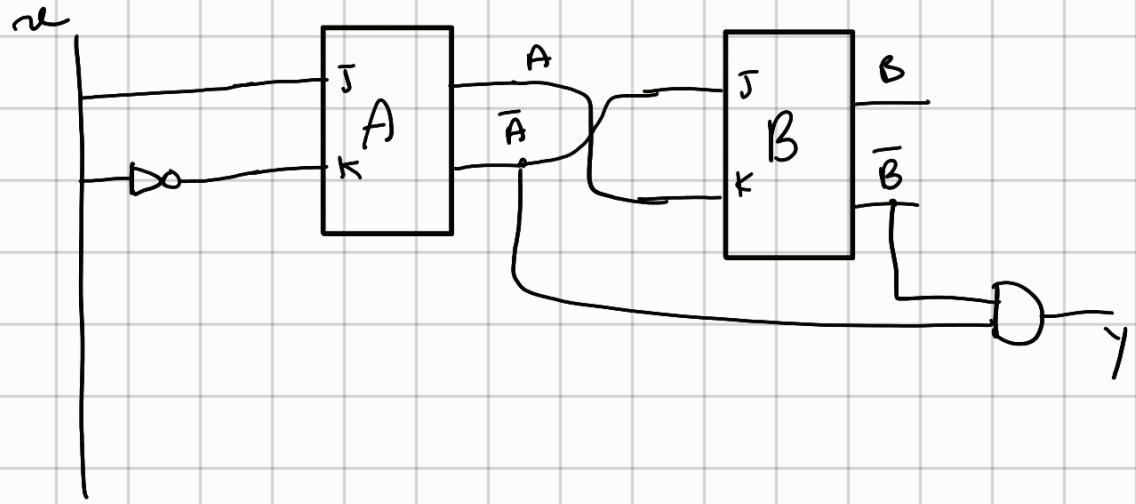
$$J_A = \bar{A}x = x$$

$$K_A = \bar{A}\bar{x} = \bar{A} + \bar{x} = \bar{x}$$

$$J_B = \bar{A}\bar{B} = \bar{A}$$

$$K_B = \bar{A}B = A + \bar{B} = A$$

$$Y = \bar{A}\bar{B}$$



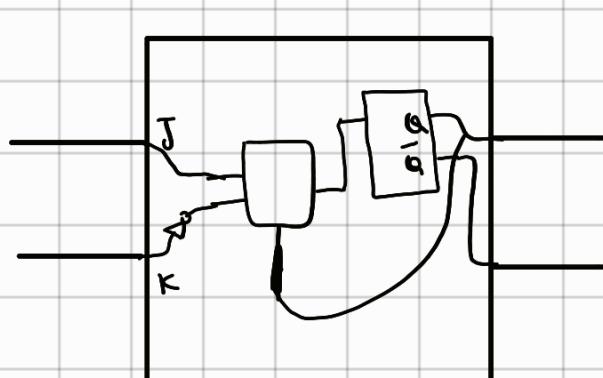
Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter.

Show that the characteristic equation for the complement output of a JK flip-flop is

$$Q'(t+1) = J'Q' + KQ$$

A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively.

(a) Tabulate the characteristic table.      (b) Derive the characteristic equation.

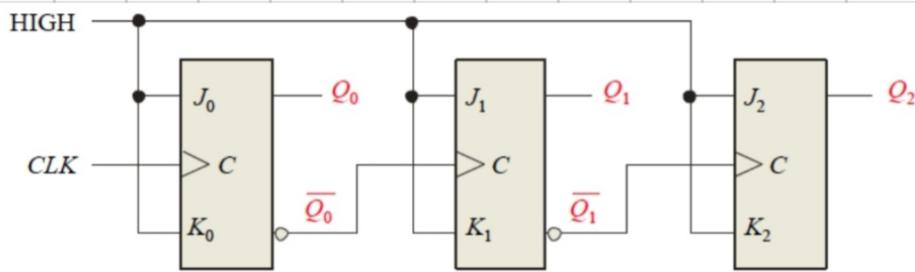


$$\text{JK: } Q^+ = J\bar{Q} + \bar{K}Q$$

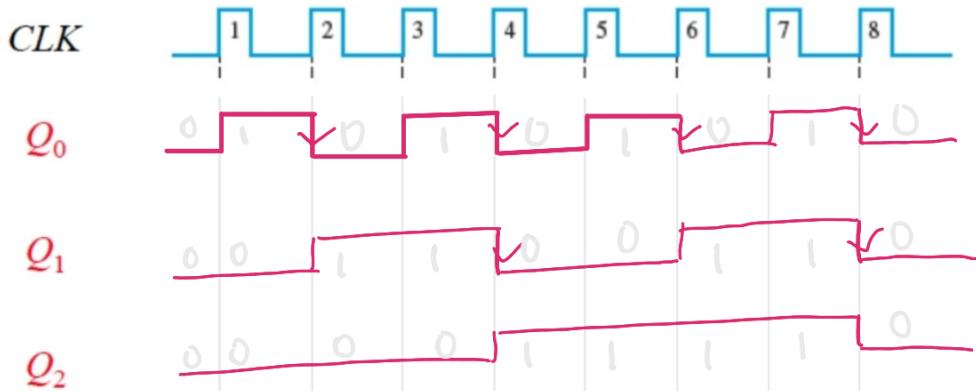
$$\text{D: } Q^+ = D$$

# Counters

## Asynchronous

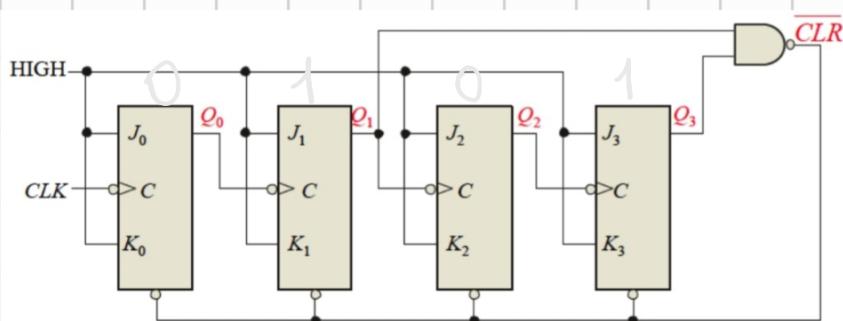


divides freq.  
by 2.  
counts from 0-7

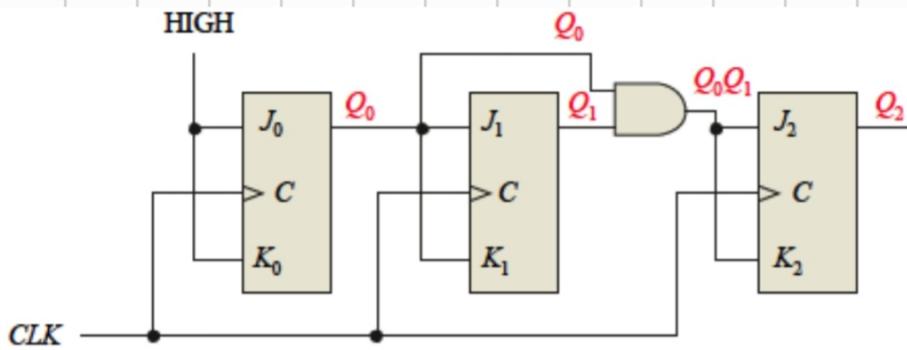


## Asynchronous Decade Counters

Count from 0-9, when it reaches 1010, the counter resets



## Synchronous



$$Q_2 Q_1 Q_0$$

$$\begin{array}{l} 0 \\ 0 \\ 0 \end{array}$$

$$\begin{array}{l} 0 \\ 0 \\ 1 \end{array}$$

$$\begin{array}{l} 0 \\ 1 \\ 0 \end{array}$$

$$\begin{array}{l} 0 \\ 1 \\ 1 \end{array}$$

$$\hline \begin{array}{l} 1 \\ 0 \\ 0 \end{array}$$

$$\begin{array}{l} 1 \\ 0 \\ 1 \end{array}$$

$$\begin{array}{l} 1 \\ 1 \\ 0 \end{array}$$

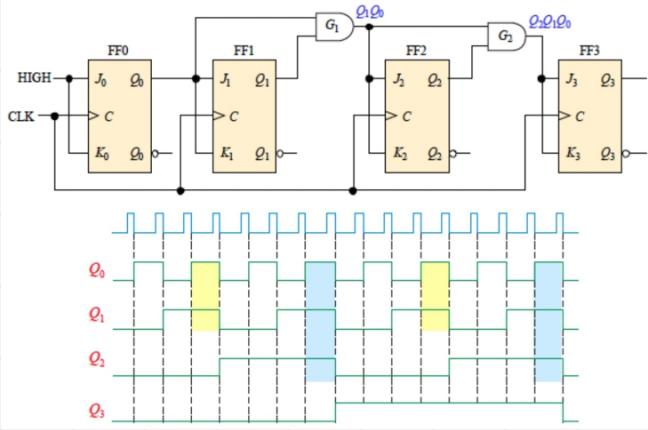
$$\begin{array}{l} 1 \\ 1 \\ 1 \end{array}$$

$Q_2 = 1$   
when  
 $Q_1 Q_0 = 1$

Analyse: circuit  $\rightarrow$  Input Equation  $\rightarrow$  State Eq.  $\rightarrow$  State Table  $\rightarrow$  State Diagram  $\rightarrow$  function

Design: Problem  $\rightarrow$  State Diagram  $\rightarrow$  State Table  $\rightarrow$  State & imp. eq.  $\rightarrow$  Scheme circ.

### 4 bits counter



### Synchronous BCD Counter

-  $Q_0$  toggles on each clock pulse  $\Rightarrow J_0 = K_0 = 1$

-  $Q_1$  toggles on next clock pulse each time  $Q_0 = 1 \wedge Q_1 = 0$   
 $\Rightarrow J_1 = K_1 = Q_0 \cdot \bar{Q}_3$

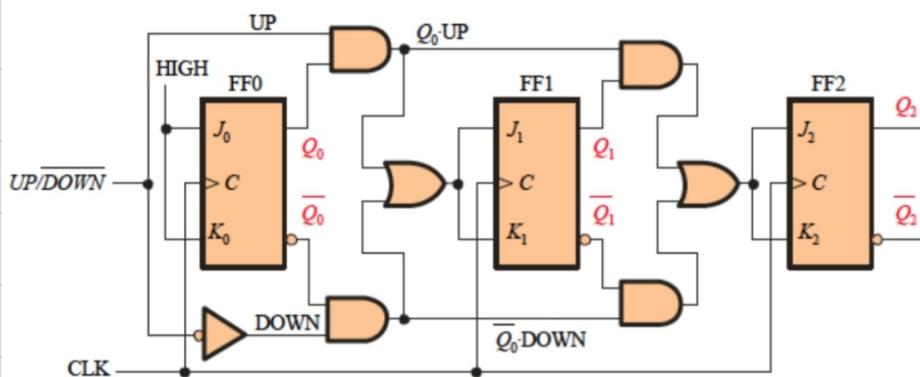
-  $Q_2$  toggles on next clock pulse each time both  $Q_0 \wedge Q_1 = 1$   
 $\Rightarrow J_2 = K_2 = Q_0 \cdot Q_1$

$Q_3$  toggles for 2 conditions:

$$1) Q_0 = 1, Q_1 = 1, Q_2 = 1.$$

$$2) Q_0 = 1, Q_3 = 1$$

$$\Rightarrow J_3 = K_3 = Q_0 \cdot Q_1 \cdot Q_2 + Q_0 \cdot Q_3$$



} counts up or down

## Exercise

Develop a 3-bit synchronous up/down counter for a sequence of UP/DOWN counter for a sequence of a 3-bit gray code in using JK flipflops. The counter must count UP when the UP/DOWN input is 1 and down if input is 0.

→ Binary

0 0 0

0 0 1

0 1 0

0 1 1

1 0 0

1 0 1

1 1 0

1 1 1

Gray

0 0 0

0 0 1

0 1 1

0 1 0

1 1 0

1 1 1

1 0 1

1 0 0

$Q_2 \ Q_1 \ Q_0$

0 0 0

0 0 1

0 1 1

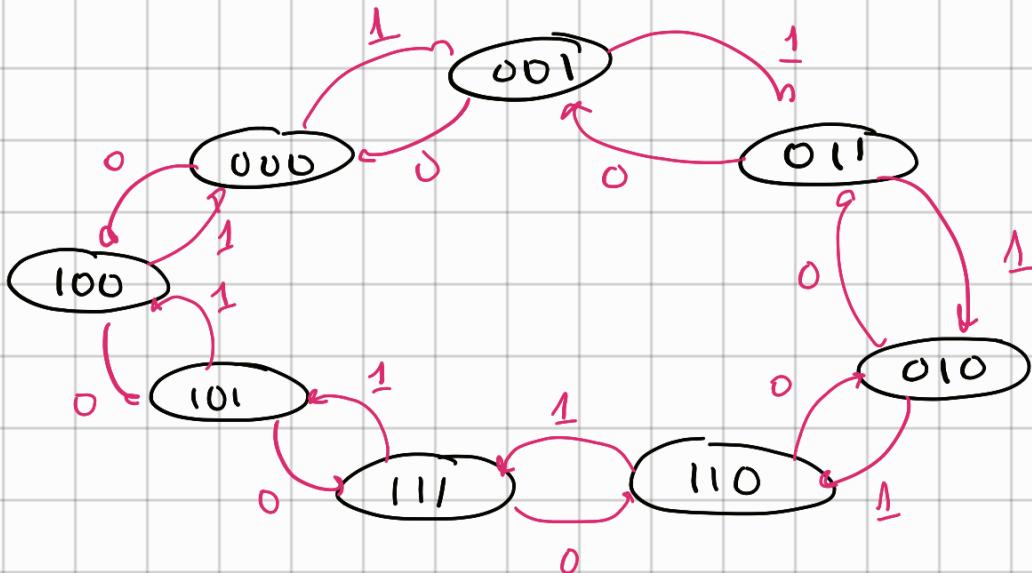
0 1 0

1 1 0

1 1 1

1 0 1

1 0 0



A	B	C	X	$A^{-1}$	$B^*$	$C^*$
0	0	0	0	1	0 0	
0	0	0	1	0	0 1	
0	0	1	0	0	0 0	
0	1	1	1	0	1 1	
0	1	0	0	0	1 0	
0	1	0	1	1	0 1	
0	1	0	1	1	1 1	
0	1	1	1	1	1 0	
0	1	1	0	0	0 1	
0	1	1	1	0	0 0	
1	0	0	0	1	0 1	
1	0	0	1	0	0 0	
1	0	1	0	1	1 1	
1	0	1	1	1	1 1	
1	0	1	1	1	0 0	
1	1	0	0	0	1 0	
1	1	0	1	1	1 1	
1	1	1	0	1	0 0	
1	1	1	1	1	1 1	
					$\bar{B}\bar{C}x + B\bar{C}x$	
						$Bx + \bar{B}\bar{x}$

$$J_A = \bar{B}\bar{C}\bar{x} + B\bar{C}x$$

$$J_B = \bar{A}Cx + AC\bar{x}$$

$$J_C = B\bar{x} + \bar{B}\bar{x} = B \oplus x$$

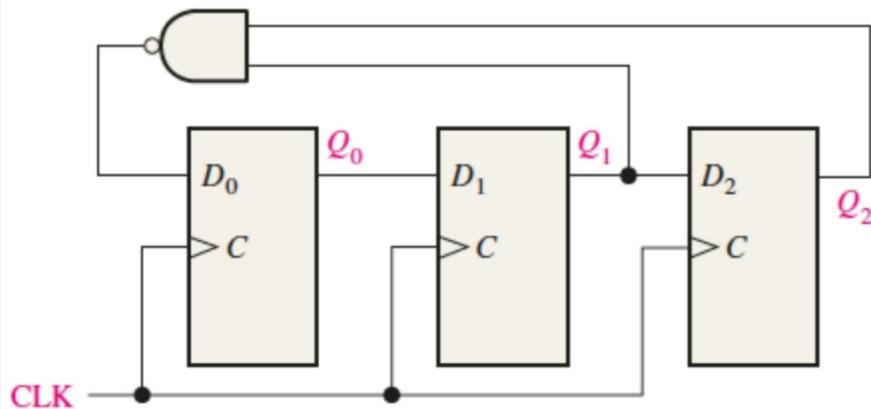
$$K_A = B\bar{C}\bar{x} + \bar{B}\bar{C}x$$

$$K_B = ACx + \bar{A}C\bar{x}$$

$$K_C = Bx + \bar{B}\bar{x} = B \odot x$$

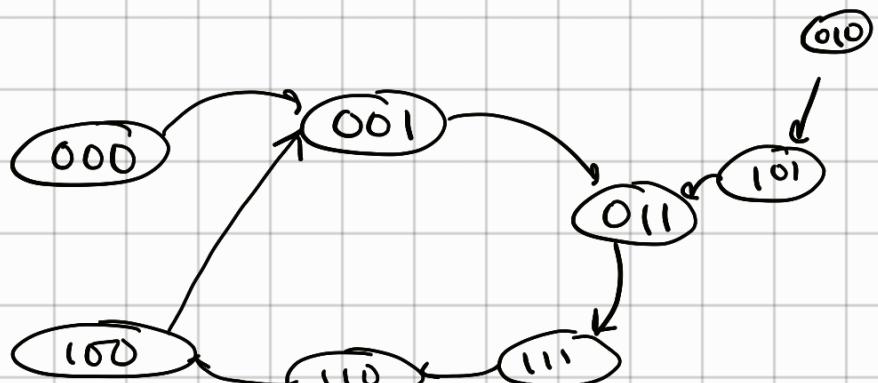
## Exercise

Develop the sequence of the following counter.



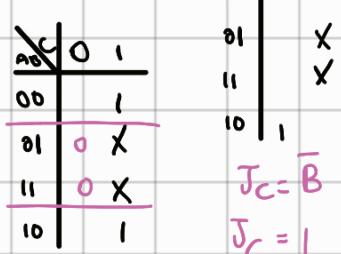
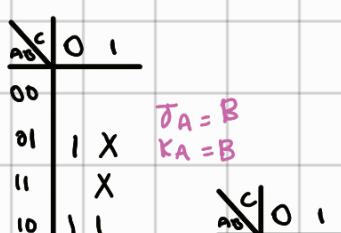
$$D_0 = \overline{Q_1 Q_2}, \quad Q_2^* = D_2 \\ D_1 = Q_0, \quad Q_1^* = D_1 \\ D_2 = Q_1, \quad Q_0^* = D_0$$

$Q_2$	$Q_1$	$Q_0$	$Q_2^*$	$Q_1^*$	$Q_0^*$
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	1	1	1
1	1	1	1	1	0
1	1	0	1	0	0
1	0	0	0	0	1
0	1	0	1	0	1
1	0	1	0	1	1

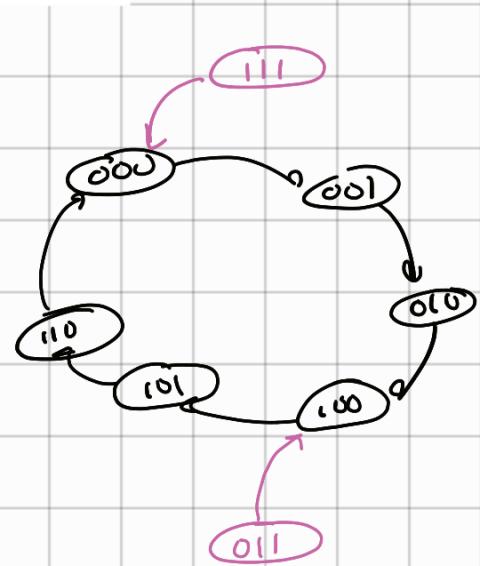


Use JK flip-flops to design a 3-bit self-correcting counter with the repeated binary sequence: 0, 1, 2, 4, 5, 6. Show what happened if the counter is started in any of unused states.

$A$	$B$	$C$	$A^*$	$B^*$	$C^*$
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	X1	X0	X0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	X0	X0	X0



$$J_B = C \\ K_B = 1$$

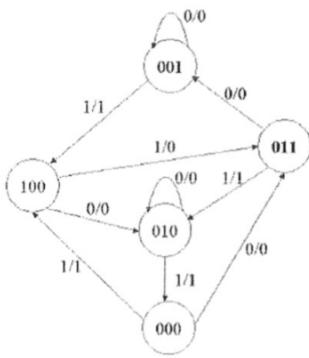


A sequential circuit has three flip-flops A, B, C; one input x; and one output, y. The state diagram is shown in next figure.

The circuit is to be designed by treating the unused states as *don't-care* conditions.

Analyze the circuit obtained from the design to determine the effect of the unused states.

- 1) Use D flip-flops in the design.
- 2) Use J-K flip-flops in the design.



A	B	C	x	$A^*$	$B^*$	$C^*$	y
---	---	---	---	-------	-------	-------	---

000	000	000	0	0	1	1	0
000	000	001	1	1	0	0	1
000	001	010	0	0	0	1	0
000	011	111	1	1	0	0	1
010	000	000	0	0	1	0	0
010	001	001	0	0	0	0	1
011	000	000	0	0	0	1	0
011	000	001	0	0	1	0	0
011	001	010	0	0	0	1	1
011	011	111	1	X	X	X	X
100	000	000	0	1	0	0	0
100	000	001	0	1	0	0	1
100	001	010	0	1	0	1	0
100	010	111	1	X	X	X	X
100	111	X	X	X	X	1	X
101	000	000	0	X	X	X	X
101	000	001	0	X	X	X	X
101	001	010	0	1	0	1	0
101	010	111	1	X	X	X	X
101	111	X	X	X	X	1	X
110	000	000	0	X	X	X	X
110	000	001	0	X	X	X	X
110	001	010	0	1	0	1	0
110	010	111	1	X	X	X	X
110	111	X	X	X	X	1	X
111	000	000	0	0	1	1	0
111	000	001	0	0	1	1	0
111	001	010	0	0	1	1	0
111	010	111	1	X	X	X	X
111	111	X	X	X	X	1	X

$$J_A = \bar{B}x$$

$$J_B = \bar{C}\bar{x} + A$$

$$J_C = \bar{A}\bar{B}\bar{x} + Ax$$

$$K_A = 1$$

$$K_B = \bar{C}x + C\bar{x} = C \oplus x$$

$$K_C = Cx$$

$$y = \bar{A}x$$

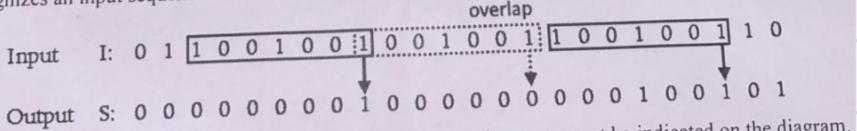
Draw a table with missing States and add them to diagram

AB	00	01	11	10
	00	1	1	
	01	1	1	
	11	X	X	X
	10	1	X	X

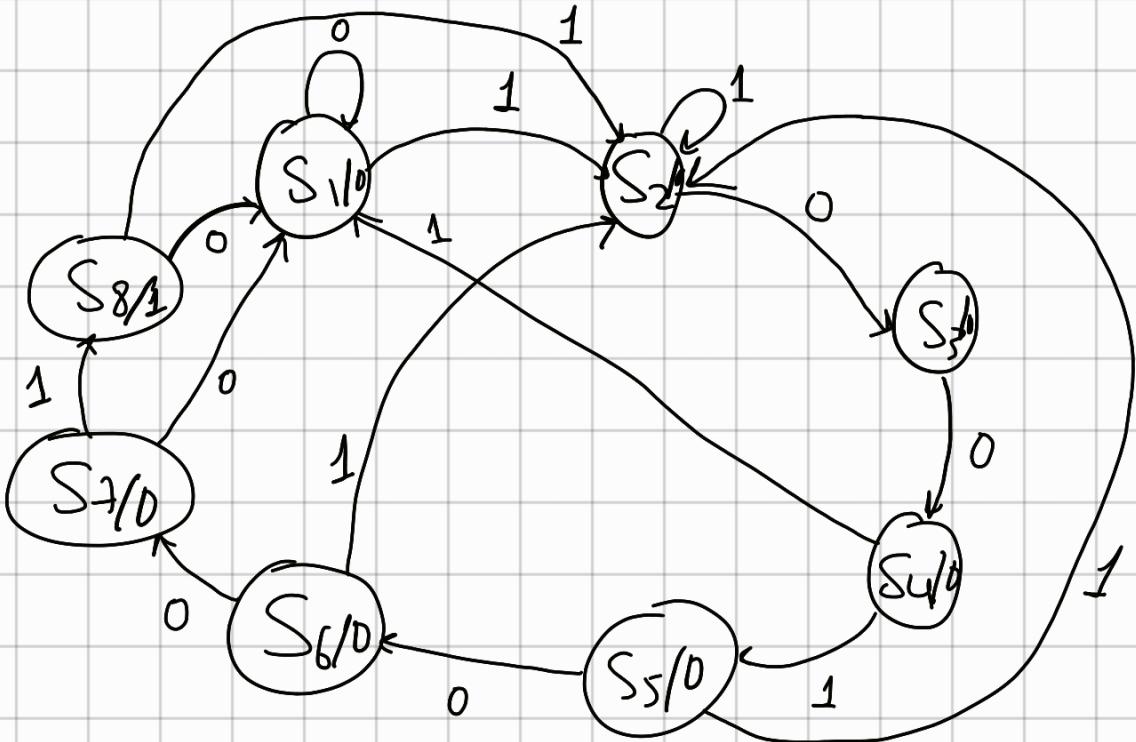
(15 pts)

**Exercise IV**

Draw the state diagram of a Moore-type sequential circuit with one input (I) and one output (S) that recognizes an input sequence of the form: 1 0 0 1 0 0 1 without overlapping.



The states of the diagram are labeled  $S_1, S_2, \dots$ . The inputs and outputs must be indicated on the diagram.



Design a logic circuit that controls the elevator door in a three-story building. The circuit has four inputs. M is a logic signal that indicates when the elevator is moving (M=1) or stopped (M=0). F<sub>1</sub>, F<sub>2</sub>, and F<sub>3</sub> are floor indicator signals that are normally LOW, and they go HIGH only when the elevator is positioned at the level of that particular floor. For example, when the elevator is lined up level with the second floor, F<sub>2</sub>=1 and F<sub>1</sub>=F<sub>3</sub>=0. The circuit output is

the OPEN signal, which is normally LOW and will go HIGH when the elevator door is to be opened. Find the simplified design and draw the diagram of the elevator circuit.

Note: Because the elevator cannot be lined up with more than one floor at a time, the cases when more than one floor inputs can be treated as don't care condition. When the elevator reaches at on floor and stops, the door opens.

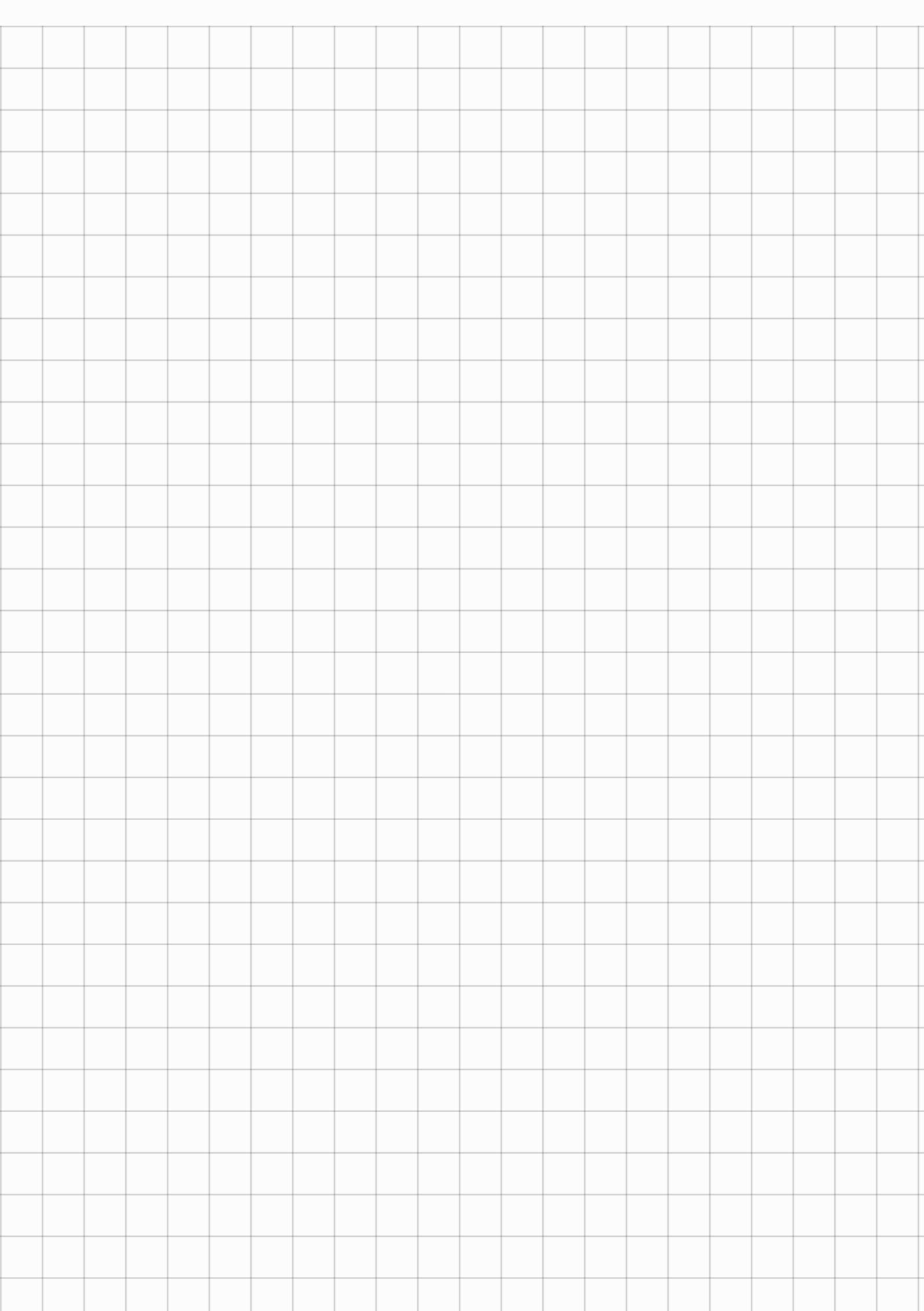
M	F <sub>1</sub>	F <sub>2</sub>	F <sub>3</sub>	Output
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	x
0	1	0	0	1
0	1	0	1	x
0	1	1	0	x
0	1	1	1	x
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	x
1	1	0	0	0
1	1	0	1	x
1	1	1	0	x
1	1	1	1	x

M	F <sub>1</sub>	F <sub>2</sub>	F <sub>3</sub>	Output
				00
				01
				11
				10

Legend: 1 = Open, X = Don't Care

$$\begin{aligned}
 & \overline{M} F_1 + \overline{M} F_3 + \overline{M} F_2 \\
 &= \overline{M} (F_1 + F_2 + F_3)
 \end{aligned}$$

1 XXX 0



# Julia Abdallah

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## Summary

I am a Computer Science student dedicated to my studies. Currently looking for a job that would allow me to further enhance my skills in Web Development, Software Engineering, Data Science, or any related fields.

## EDUCATION

### Computer Engineering | Lebanese University Faculty of Engineering

2020 – 2023

### Bachelor's in Computer Science | Lebanese University Faculty of Sciences

2023 – Present

## EXPERIENCE

### Private Math, Physics, and Chemistry Teacher

Feb 2019 – Oct 2019

### Coding Instructor | BrightChamps

Jan 2022 – Jan 2024

### Team Lead | BrightChamps

July 2022 – Jan 2024

### HR Manager | BrightChamps

June 2023 – August 2023

## SKILLS

- **Programming:** C, C++, Java, C#, HTML, CSS, JavaScript, Python
- **Software:** Office, AutoCAD, MATLAB
- **Languages:** English (fluent), French (fluent), Arabic (native)
- **Teamwork:** Project management, conflict resolution, leadership
- **Communication:** Public speaking, presentation, adaptability

# Fawzi Abdallah

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## Profile

An educator with extensive experience in teaching electricity at technical schools and holding an administrative position as the Head of Practical Lessons. With a strong background in both practical and theoretical aspects of electrical engineering, I have a proven track record of effectively managing and enhancing practical training programs. My commitment to educational excellence, combined with my administrative skills, uniquely qualifies me for the role of Head of Practical and Theoretical Lessons. I am dedicated to fostering a comprehensive learning environment that integrates hands-on experience with in-depth theoretical knowledge.

## Experience

### *Teacher*

#### **Mashghara Technical Institute**

1987-1992

Taught all electricity-related courses for BT, ensuring comprehensive coverage of both theoretical and practical aspects of the curriculum.

### ***Member of Official Practical Exams Committee***

1992-2018

responsible for developing and reviewing exam content, supervise the conduct of exams to maintain fairness, provide instructions, and evaluate students' performance according to set criteria. Additionally, compile and submit results and reports, regulations while addressing any issues that arise during the exams.

### ***Electrical Workshop Supervisor***

#### **Mashghara Technical Institute**

1997-2002

Responsible for overseeing the daily operations of the electrical workshop, this role includes managing and maintaining all workshop equipment, ensuring a safe and productive learning environment, and providing hands-on training to students.

### ***Head of Practical Lessons***

#### **Hammana Technical Institute**

2002-2009

Oversee and manage the practical aspects of educational programs, ensuring students receive comprehensive hands-on training aligned with theoretical coursework.

***Head of Practical Lessons***  
**Rafic Hariri Technical Institute**

2009-2024

Oversee and manage the practical aspects of educational programs, ensuring students receive comprehensive hands-on training aligned with theoretical coursework.

***Teacher: TS&LT***  
**Rafic Hariri Technical Institute**

2009-2024

## **Education**

***Leningrad Polytechnic University***  
1980-1987  
Master in electromechanical engineering

## **Skills & Abilities**

- Leadership and Management
- Technical Proficiency
- Problem-Solving
- Communication

# Julia Abdallah

Computer Science Student at LU

Bekaa, Lebanon

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## Summary

I am a Computer Science student dedicated to my studies. Currently looking for a job that would allow me to further enhance my skills in Web Development, Software Engineering, Data Science, or any related fields.

## EDUCATION

### Computer Engineering | Lebanese University Faculty of Engineering

2020 – 2023

### Bachelor's in Computer Science | Lebanese University Faculty of Sciences

2023 – Present

## EXPERIENCE

### Private Math, Physics, and Chemistry Teacher

Feb 2019 – Oct 2019

### Coding Instructor | BrightChamps

Jan 2022 – Jan 2024

### Team Lead | BrightChamps

July 2022 – Jan 2024

### HR Manager | BrightChamps

June 2023 – August 2023

## SKILLS

- **Programming:** C, C++, Java, C#, HTML, CSS, JavaScript, Python
- **Software:** Office, AutoCAD, MATLAB
- **Languages:** English (fluent), French (fluent), Arabic (native)
- **Teamwork:** Project management, conflict resolution, leadership
- **Communication:** Public speaking, presentation, adaptability