Arm® Cortex®-M33 32-bit MCU+FPU, 375 DMIPS 250 MHz, 128 Kbytes flash memory, 32 Kbytes RAM, I3C

Datasheet - production data

Features

Includes [redacted] state-of-the-art patented technology

Core

- Arm® Cortex®-M33 CPU with FPU, frequency up to 250 MHz, MPU, 375 DMIPS (Dhrystone 2.1), and DSP instructions

ART Accelerator

- 8-Kbyte instruction cache allowing 0-wait-state execution from flash memory (frequency up to 250 MHz)

Benchmarks

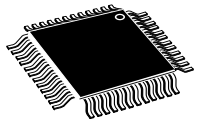
- 1.5 DMIPS/MHz (Drystone 2.1)
- 1023 CoreMark® (4.092 CoreMark/MHz)

Memories

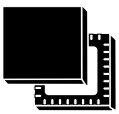
- 128 Kbytes of embedded flash memory with ECC, two banks of read-while-write
- 2-Kbyte OTP (one-time programmable)
- 32-Kbyte SRAM with ECC
- 2 Kbytes of backup SRAM (available in the lowest power modes)

Clock, reset, and supply management

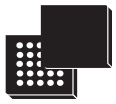
- 1.71 V to 3.6 V application supply and I/O
- POR, PDR, PVD, and BOR
- Embedded regulator (LDO)
- Internal oscillators: 64 MHz HSI, 48 MHz HSI48, 4 MHz CSI, 32 kHz LSI
- Two PLLs for system clock, USB, audio, and ADC
- External oscillators: 4 to 50 MHz HSE, 32.768 kHz LSE
- Low-power modes: Sleep, Stop, Standby, and VBAT



LQFP64 (10 x 10 mm)
LQFP48 (7 x 7 mm)



UFQFPN48
(7 x 7 mm)
UFQFPN32
(5 x 5 mm)



WLCSP25
(2.33 x 2.24 mm)

Low-power modes

- Sleep, stop and standby modes
- V_{BAT} supply for RTC, 32x 32-bit backup registers

General-purpose inputs/outputs

- Up to 49 fast I/Os with interrupt capability (most 5 V tolerant)
- Up to 9 I/Os with independent supply down to 1.08 V

Analog

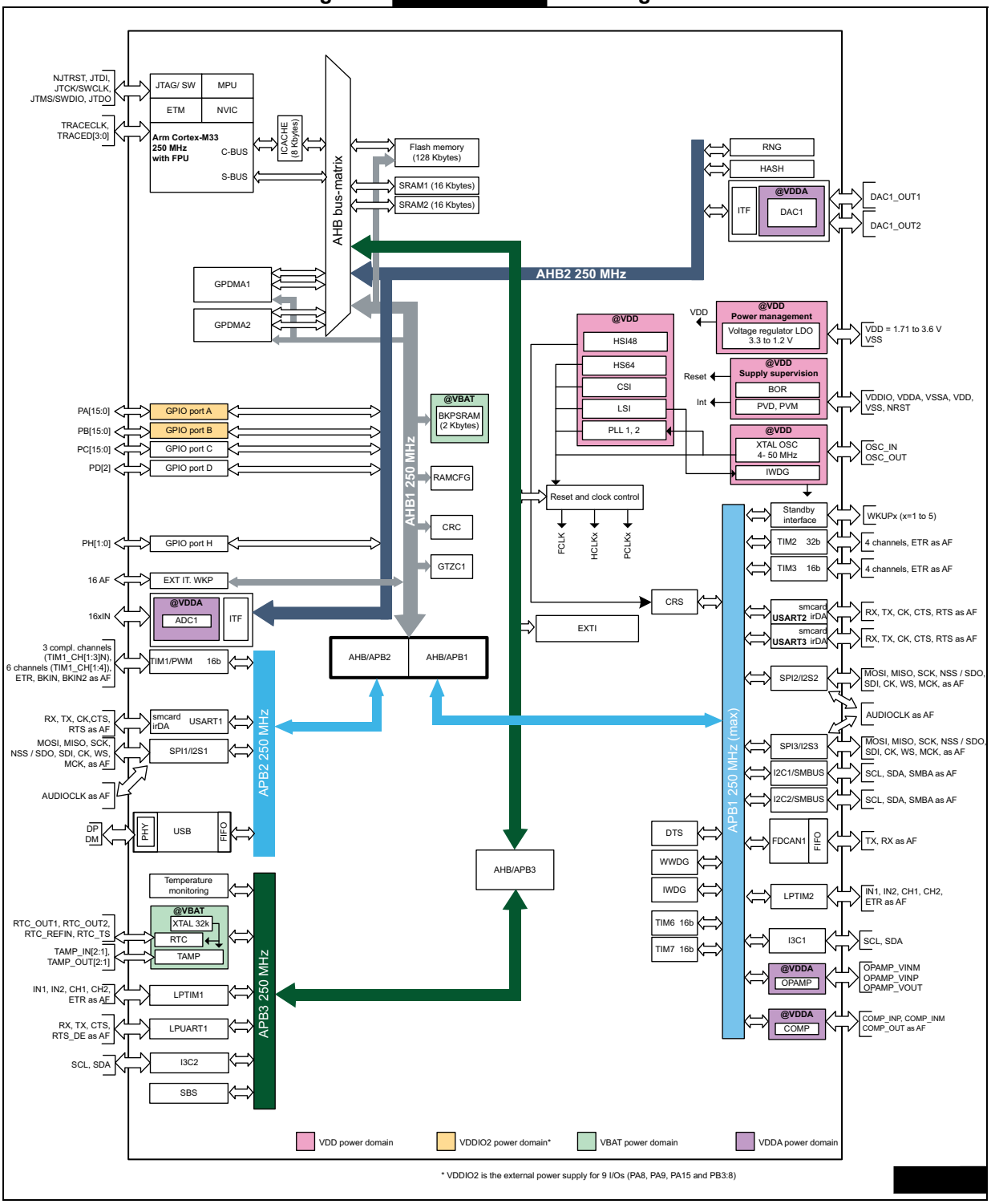
- One 12-bit ADC, up to 2.5 MSPS
- One 12-bit dual-channel DAC
- One ultra-low-power comparator
- One operational amplifier (7 MHz bandwidth)

One digital temperature sensor

Up to 11 timers

- Six 16-bit (including two low-power 16-bit timer available in Stop mode) and one 32-bit timer
- Two watchdogs
- One SysTick timer
- RTC with hardware calendar, alarms, and calibration

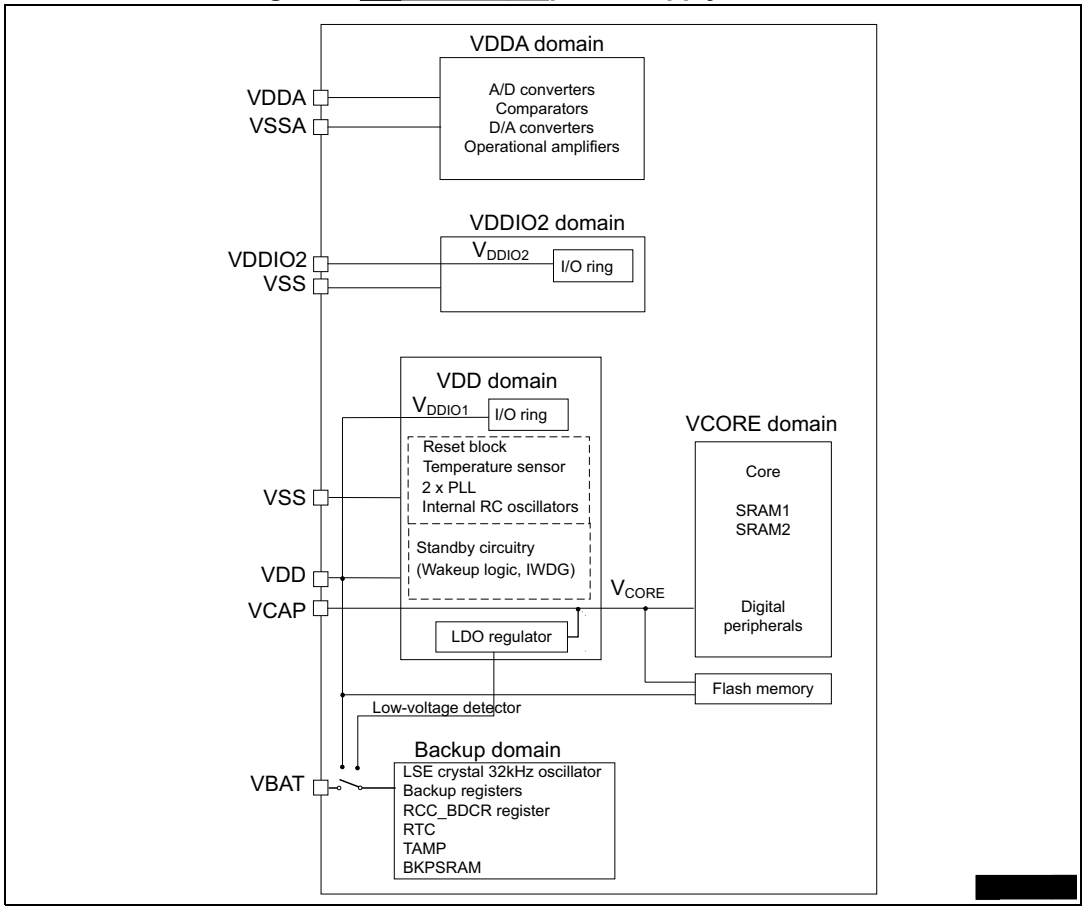
Figure 1. [redacted] block diagram



The [redacted] devices embed an LDO regulator to provide the V_{CORE} supply for digital peripherals, SRAM1, SRAM2, and embedded flash memory. The LDO generates this voltage on the VCAP pin connected to an external capacitor of 2x 2.2 µF typical.

The LDO regulator can provide four different voltages (voltage scaling) and can operate in Stop modes.

Figure 2. [redacted] power supply overview

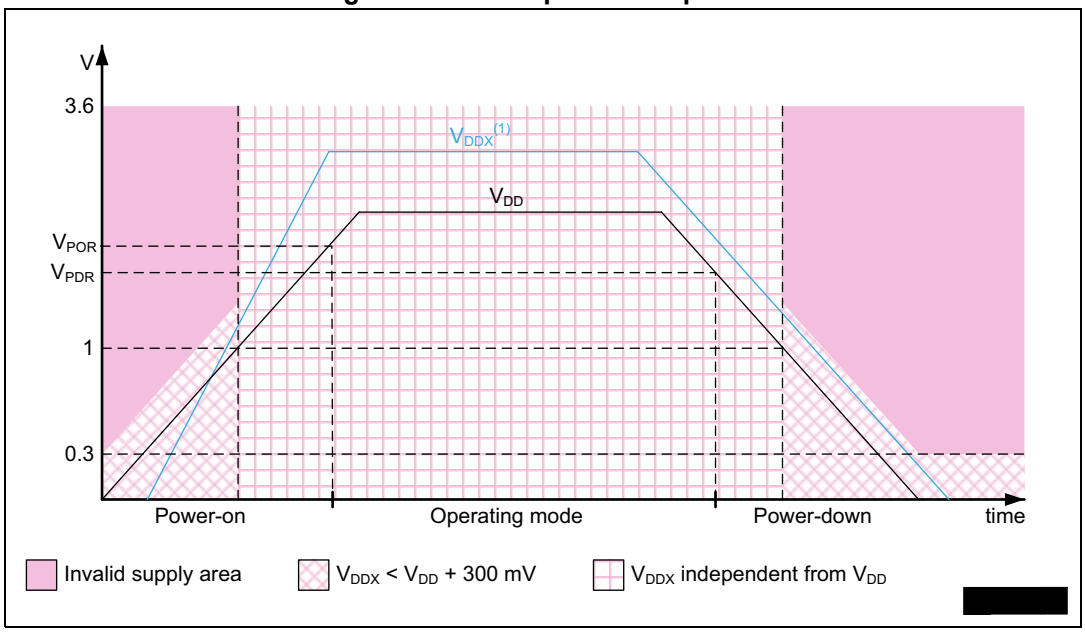


During power-up and power-down phases, the following power sequence requirements must be respected (refer to *Figure 3: Power-up/down sequence*):

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDIO2}) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows external-decoupling capacitors to be discharged with different time constants during the power-down-transient phase.

Figure 3. Power-up/down sequence



1. V_{DDX} refers to any power supply among V_{DDA} and V_{DDIO2}.

3.8.2 Power supply supervisor

The devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a brownout reset (BOR) circuitry:

- Power-on reset (POR)
  The POR supervisor monitors the VDD power supply and compares it to a fixed threshold. The devices remain in reset mode when VDD is below this threshold.
- Power-down reset (PDR)
  The PDR supervisor monitors the VDD power supply. A reset is generated when VDD drops below a fixed threshold.
- Brownout reset (BOR)
  The BOR supervisor monitors VDD power supply. It can be enabled/disabled through BORH_EN option bit. Once enabled, three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when VDD drops below this threshold.
- Programmable voltage detector (PVD)
  The PVD monitors the VDD power supply by comparing it with a threshold selected from a set of predefined values.
  It can also monitor the voltage level of the PVD_IN pin by comparing it with an internal VREFINT voltage reference level.
  An interrupt can be generated when VDD drops below the VPVD threshold and/or when VDD is higher than the VPVD threshold. The interrupt service routine can then

  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus) specification rev 1.3 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming
- Wakeup from Stop capability
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 5. I2C implementation

I2C features(1)	I2C1	I2C2
Standard-mode (up to 100 Kbit/s)	X	X
Fast-mode (up to 400 Kbit/s)	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X
Programmable analog and digital noise filters	X	X
SMBus/PMBus hardware support	X	X
Independent clock	X	X
Wakeup capability	X	X

1. X: supported

3.26 Improved inter-integrated circuit (I3C)

The I3C interface handles communication between this device and others, like sensors and host processor(s), that are all connected on an I3C bus.

The I3C peripheral implements all the required features of the MIPI I3C specification v1.1. It can control all I3C bus-specific sequencing, protocol, arbitration and timing, and can be acting as controller (formerly known as master) or as target (formerly known as slave).

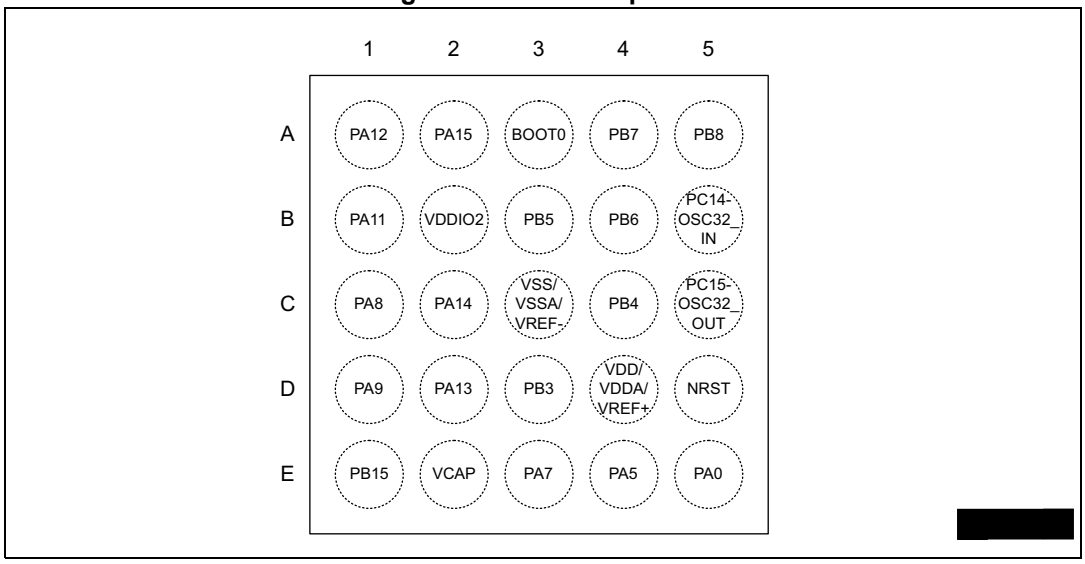
The I3C peripheral, acting as controller, improves the features of the I2C interface still preserving some backward compatibility: it allows an I2C target to operate on an I3C bus in legacy I2C fast-mode (Fm) or legacy I2C fast-mode plus (Fm+), provided that this latter does not perform clock stretching.

The I3C peripheral can be used with DMA in order to off-load the CPU.

4 Pinout, pin description and alternate function

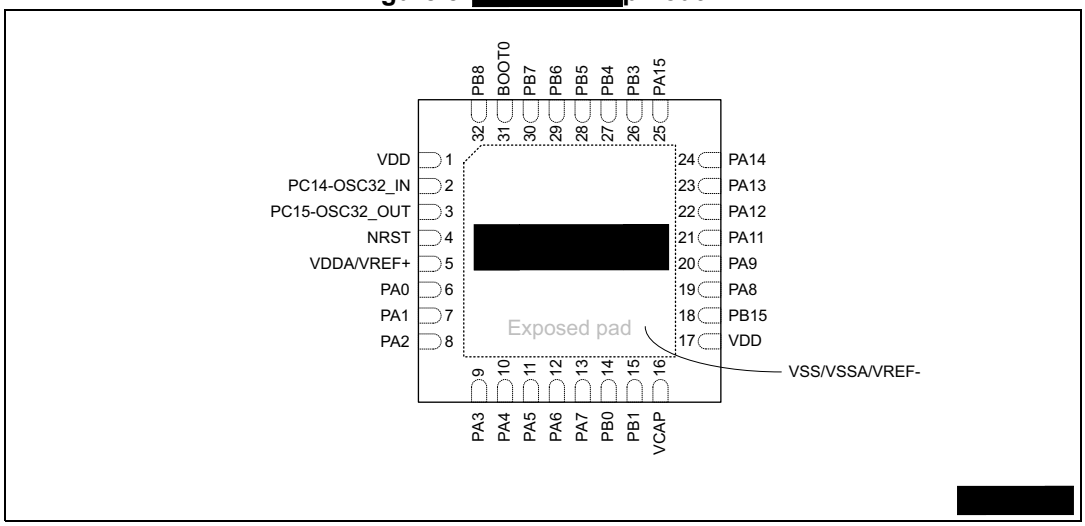
4.1 Pinout/ballout schematics

Figure 4. WLCSP25 pinout



The above figure shows the package top view.

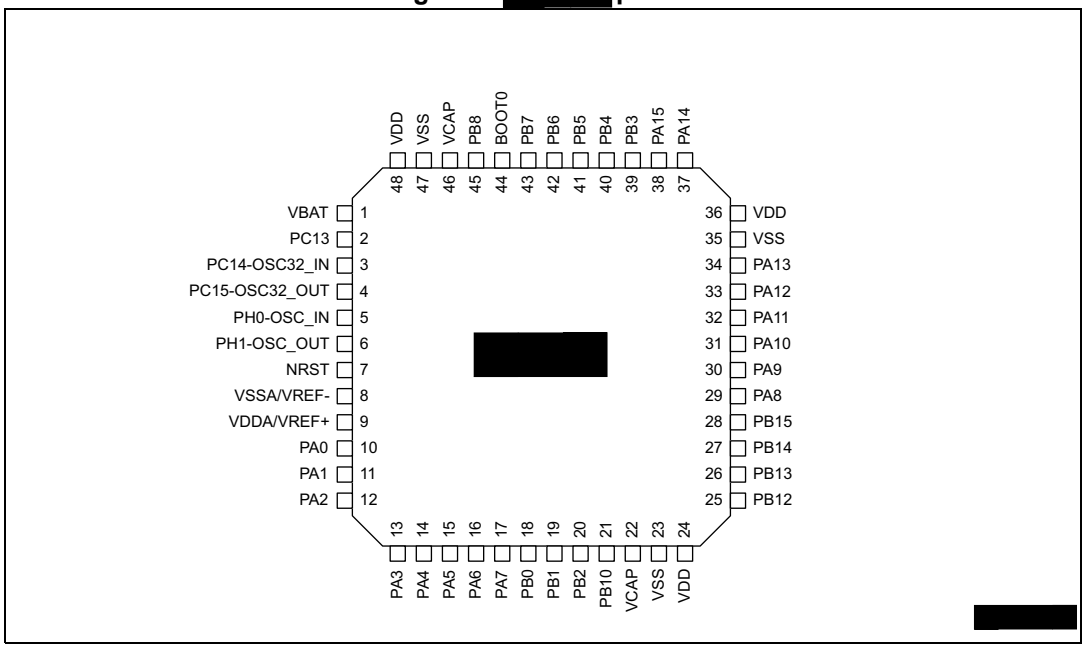
Figure 5. pinout[a]



The above figure shows the package top view.

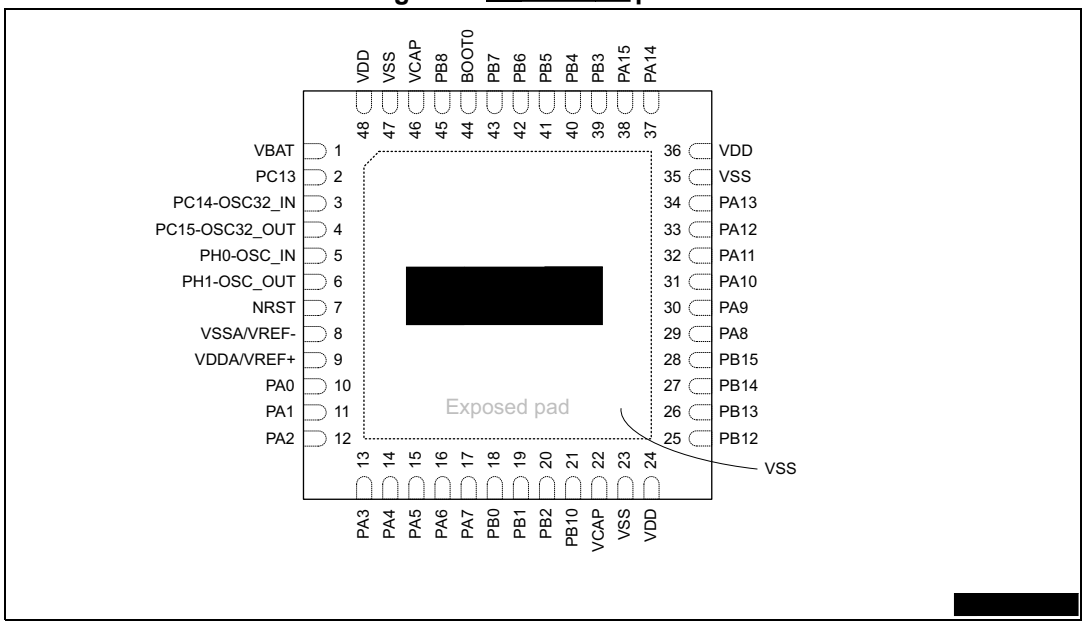
a. There is an exposed die pad on the underside of the package. This backside pad must be connected and soldered to PCB ground.

Figure 6. pinout



The above figure shows the package top view.

Figure 7. pinout



The above figure shows the package top view.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests in production on 100% of the devices with an ambient temperature at T_J = 25 °C and $T_J = T_{Jmax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes, and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, $V_{DD} = V_{DDA}$ = 3.3 V (for the 1.71 ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

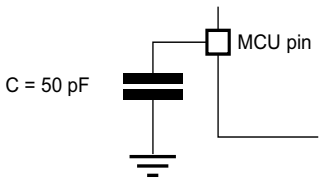
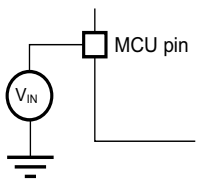
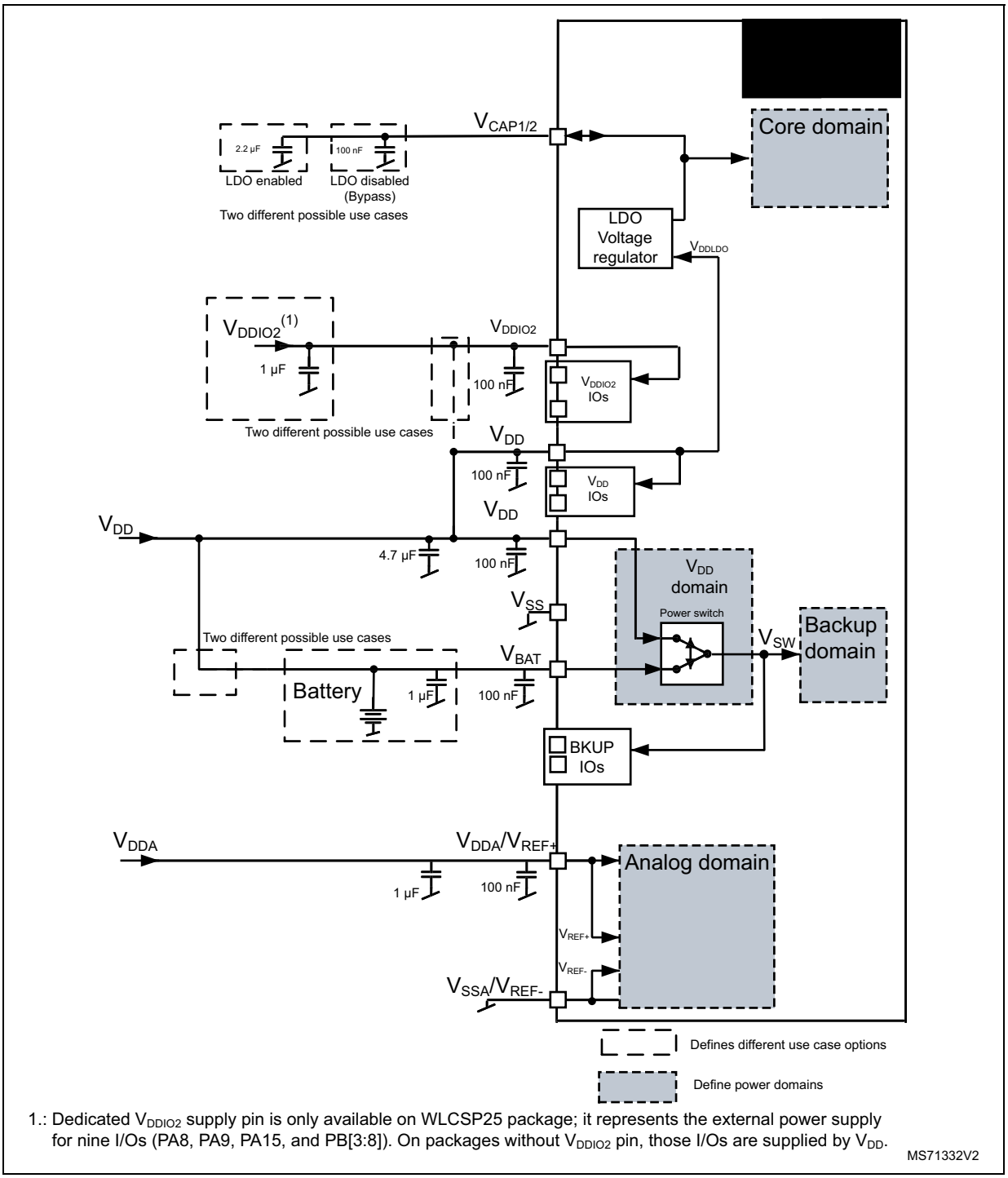


Figure 10. Pin input voltage



5.1.6 Power supply scheme

Figure 11. Power supply scheme



1.: Dedicated V_{DDIO2} supply pin is only available on WLCSP25 package; it represents the external power supply for nine I/Os (PA8, PA9, PA15, and PB[3:8]). On packages without V_{DDIO2} pin, those I/Os are supplied by V_{DD}.

MS71332V2

Caution: If there are two VCAP pins (such as LQFP64 package), each pin must be connected to a 2.2 µF (typical) capacitor (for a total around 4.4 µF). If only one VCAP pin is available then it must be connected to a 4.7 µF capacitor.

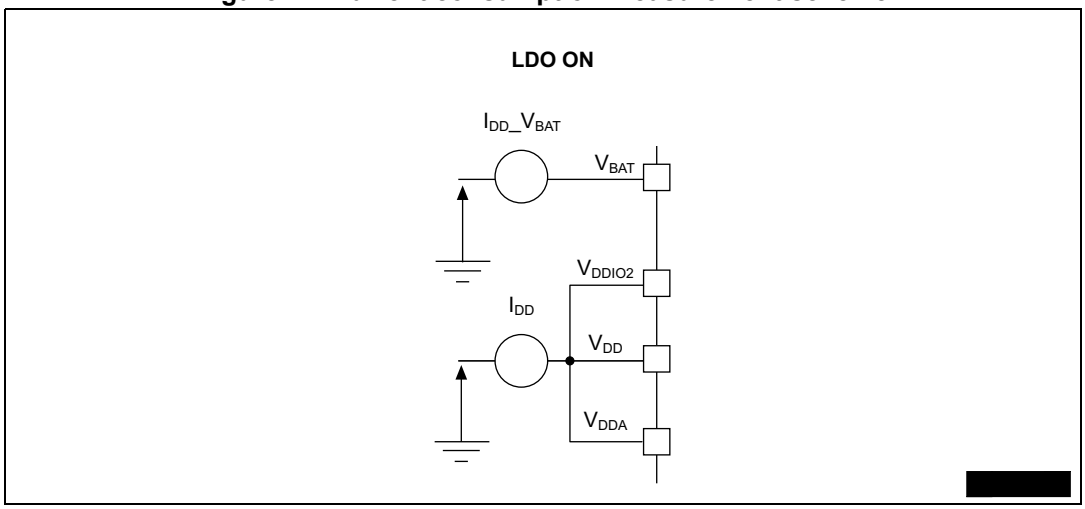
Note: Refer to "Getting started with [redacted] Series hardware development" ([redacted] for more details.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA}, and so on) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

5.1.7 Current consumption measurement

The I_{DD} parameters given in various tables in the next sections represent the total MCU consumption including the current supplying V_{DD}, V_{DDIO2}, V_{DDA}, and V_{BAT}.

Figure 12. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13: Voltage characteristics*, *Table 14: Current characteristics*, and *Table 15: Thermal characteristics* can cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 13. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	External main supply voltage (including V_{DD}(2)(3)(4), V_{DDA}, and V_{DDIO2}, and V_{BAT})	-0.3	4.0	V
V_{DDIOx}(3)- V_{SS}	I/O supply when HSLV= 0	-0.3	4.0	V
	I/O supply when HSLV = 1	-0.3	2.75	

5. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 15. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	130(1)	°C

1. The junction temperature is limited to 105 °C in the VOS0 voltage range.

5.3 Operating condition

5.3.1 General operating conditions

Table 16. General operating conditions

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	HSLV(1) = 0	1.71(2)	-	3.6	V
		HSLV(1) = 1	1.71(2)	-	2.7	V
V_{DDIO2}(3)	PA8, PA9, PA15 and PB[3:8] I/Os supply voltage	At least one I/O in PA8, PA9, PA15 and PB[3:8] is used, HSLV(1) = 0	1.08	-	3.6	V
		At least one I/O in PA8, PA9, PA15 and PB[3:8] is used, HSLV(1) = 1	1.08	-	2.7	
		PA8, PA9, PA15, and PB[3:8] are not used, HSLV(1) = 0	0	-	3.6	
V_{DDA}	Analog supply voltage	COMP is used	1.62	-	3.6	V
		DAC is used	1.8	-		
		OPAMP is used	2.0	-		
		ADC is used	1.62	-		
		ADC, DAC, OPAMP, and COMP are not used	0	-		
V_{BAT}	Backup operating voltage	-	1.2	-	3.6	V

Table 17. Maximum allowed clock frequencies

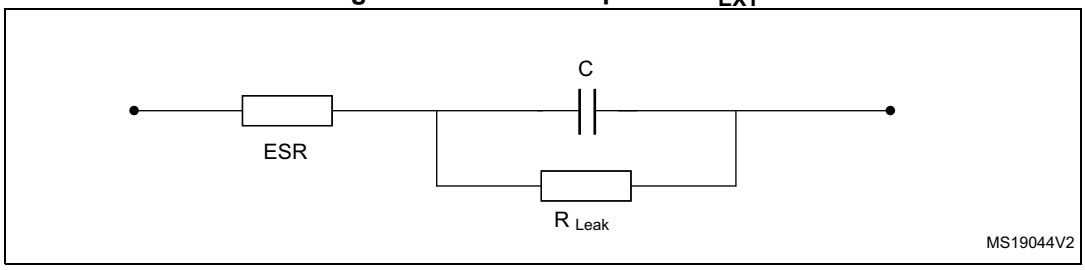
Symbol(1)(2)	Parameter	VOS0	VOS1	VOS2	VOS3	Unit
f_{CPU}	CPU	250	200	150	100	MHz
f_{HCLK}	AHB	250	200	150	100	
f_{PCLK}	APB	250	200	150	100	
$f_{fdcan\_ker\_ck}$	FDCAN	250	200	150	100	
$f_{I2C\_ker\_ck}$	I2C[1:2]	250	200	150	100	
$f_{I3C\_ker\_ck}$	I3C[1:2]	250	200	150	100	
$f_{lptim\_ker\_ck}$	LPTIM[1:2]	250	200	150	100	
$f_{rcc\_tim\_ker\_ck}$	TIM[1:3],TIM[6:7]	250	200	150	100	
f_{rng_clk}	RNG	50	50	50	50	
$f_{spi\_ker\_ck}$	SPI[1:3]	250	200	150	100	
$f_{lpuart\_ker\_ck}$	LPUART1	250	200	150	100	
$f_{usart\_ker\_ck}$	USART1/2/3	250	200	150	100	
$f_{usb\_ker\_ck}$	USB	50	50	50	50	
$f_{adc\_ker\_ck}$	ADC	125	100	75	50	
f_{dac_pclk}	DAC	250	200	150	100	
$f_{rtc\_ker\_ck}$	RTC	1	1	1	1	

1. Specified by design - Not tested in production.
2. The maximum kernel clock frequencies can be limited by the maximum peripheral clock frequency (refer each peripheral electrical characteristics).

5.3.2 VCAP external capacitor

Stabilization for the embedded LDO regulator is achieved by connecting an external capacitor C_{EXT} to the VCAPx (one or two pins depending on the packages). C_{EXT} is specified in *Table 18: VCAP operating condition*. Two external capacitors must be connected to VCAP pins (refer to STM32H5 Series hardware development ([redacted]).

Figure 13. External capacitor C_{EXT}



1. Legend: ESR is equivalent series resistence.

Table 18. VCAP operating condition

Symbol	Parameter	Conditions
CEXT	External capacitor for LDO enabled	2.2 µF(1)
ESR	ESR of external capacitor	< 100 mΩ

1. This value corresponds to CEXT typical value. A variation of ±20% is tolerated

When the internal LDO voltage regulator is switched OFF, the two 2.2 µF VCAP capacitors are not required. However all VCAPx package pins must be connected together and it is recommended to add a ceramic filtering capacitor of 100 nF as close as possible to each VCAPx pin.

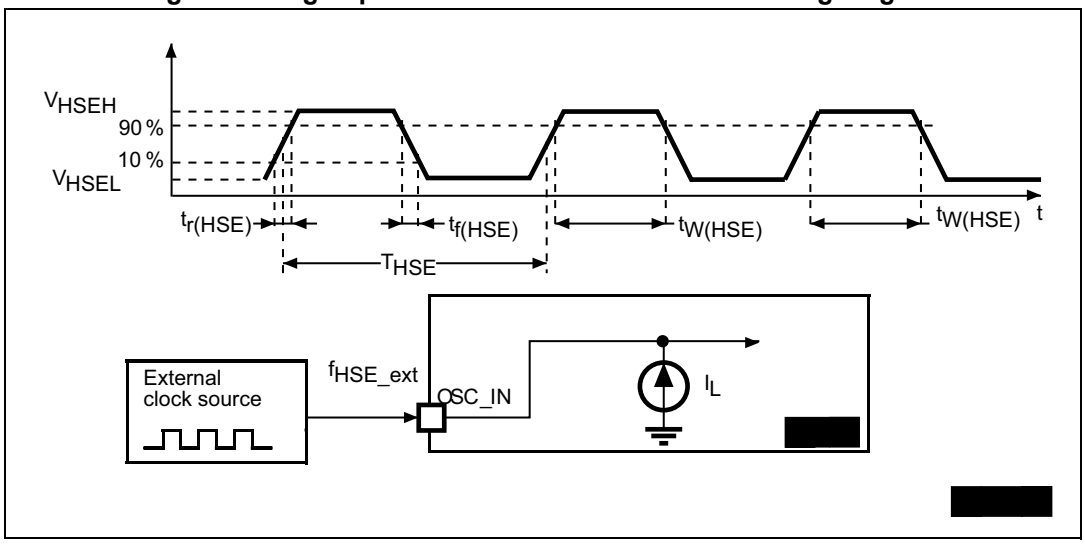
5.3.4 Embedded reset and power control block characteristics

The parameters given in *Table 20: Embedded reset and power control block characteristics* are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in *Table 16: General operating conditions*.

Table 20. Embedded reset and power control block characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after POR is detected	V_{DD} rising	-	377	550	µs
$V_{POR/PDR}$	Power-on/power-down reset threshold (BORH_EN =0)	Rising edge	1.62	1.67	1.71	V
		Falling edge	1.58	1.62	1.68	
V_{BOR1}	Brownout reset threshold 1 (BORH_EN =1)	Rising edge	2.04	2.10	2.15	
		Falling edge	1.95	2.00	2.06	
V_{BOR2}	Brownout reset threshold 2 (BORH_EN =1)	Rising edge	2.34	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{BOR3}	Brownout reset threshold 3 (BORH_EN =1)	Rising edge	2.63	2.70	2.78	
		Falling edge	2.54	2.61	2.68	
V_{PVD0}	Programmable voltage detector (PVD) threshold 0	Rising edge	1.90	1.96	2.01	
		Falling edge	1.81	1.86	1.91	
V_{PVD1}	Programmable voltage detector (PVD) threshold 1	Rising edge	2.05	2.10	2.16	
		Falling edge	1.96	2.01	2.06	
V_{PVD2}	Programmable voltage detector (PVD) threshold 2	Rising edge	2.19	2.26	2.32	
		Falling edge	2.10	2.15	2.21	
V_{PVD3}	Programmable voltage detector (PVD) threshold 3	Rising edge	2.35	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{PVD4}	Programmable voltage detector (PVD) threshold 4	Rising edge	2.49	2.56	2.62	
		Falling edge	2.39	2.45	2.51	
V_{PVD5}	Programmable voltage detector (PVD) threshold 5	Rising edge	2.64	2.71	2.78	
		Falling edge	2.55	2.61	2.68	
V_{PVD6}	Programmable voltage detector (PVD) threshold 6	Rising edge	2.78	2.86	2.94	
		Falling edge	2.69	2.76	2.83	
$V_{POR/PDR}$	Hysteresis for power-on/power-down reset	Hysteresis in run mode	-	43	-	mV
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BOR (unless BORH_EN = 0) and PVD	Hysteresis in run mode	-	100	-	
$I_{DD\_BOR\_PVD}$(2)	BOR and PVD consumption from V_{DD}	-	-	-	0.630	µA
$I_{DD\_POR\_PDR}$	POR and PDR consumption from V_{DD}	-	0.8	-	1.2	

Figure 14. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the *Table 36: Low-speed external user clock characteristics* in addition to *Table 53: I/O static characteristics*. The external clock can be low-swing (analog) or digital. In case of a low-swing analog input clock, the clock squarer must be activated (refer to [redacted]).

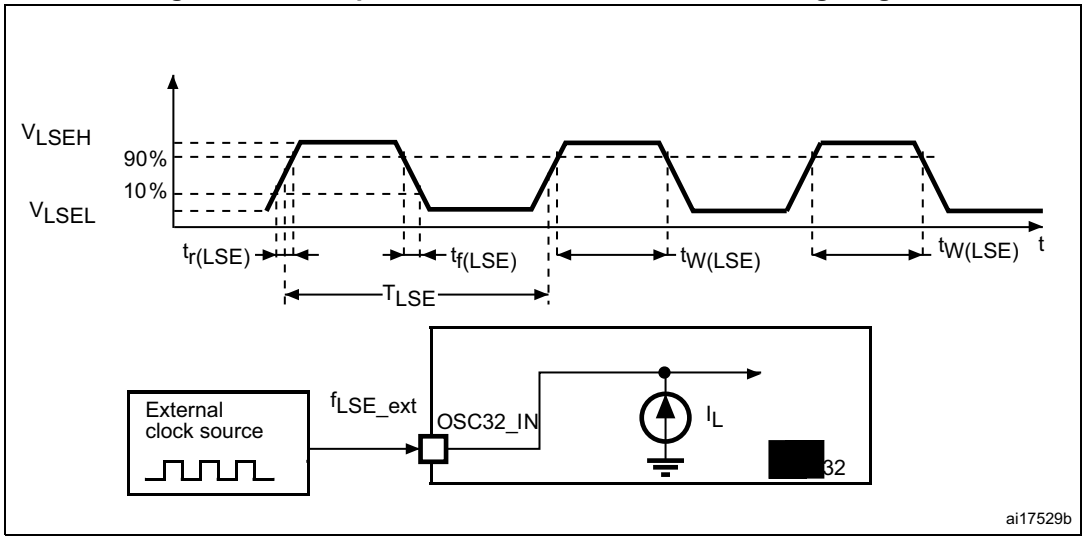
Table 36. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	External digital/analog clock	-	32.768	1000	kHz
V_{LSEH}	Digital OSC32_IN input high-level voltage	External digital clock	0.7 V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_IN input low-level voltage		V_{SS}	-	0.3 V_{DD}	
$t_{w(LSEH)}/t_{w(LSEL)}$	OSC32_IN high or low time	External digital clock	250	-	-	ns
V_{lsw_H}	Analog low-swing OSC_IN high-level voltage	External analog low swing clock	0.6	-	1.225	V
V_{lsw_L}	Analog low-swing OSC_IN low-level voltage		0.35	-	0.8	
V_{lswLSE} (V_{LSEH} -V_{LSEL})	Analog low-swing OSC_IN peak-to-peak amplitude		0.2	-	0.875	
$DuCy_{LSE}$	Analog low-swing OSC_IN duty cycle		45	50	55	%
$t_{r(LSE)}/t_{f(LSE)}$	Analog low-swing OSC_IN rise and fall times	External analog low swing clock, 10% to 90%	-	100	200	ns

1. Specified by design - Not tested in production.

Note: For information on selecting the crystal, refer to the application note [redacted] design guide for [redacted] available from the [redacted]

Figure 15. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 50 MHz crystal/ceramic resonator oscillator.

All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 37*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 37. HSE oscillator characteristics(1)

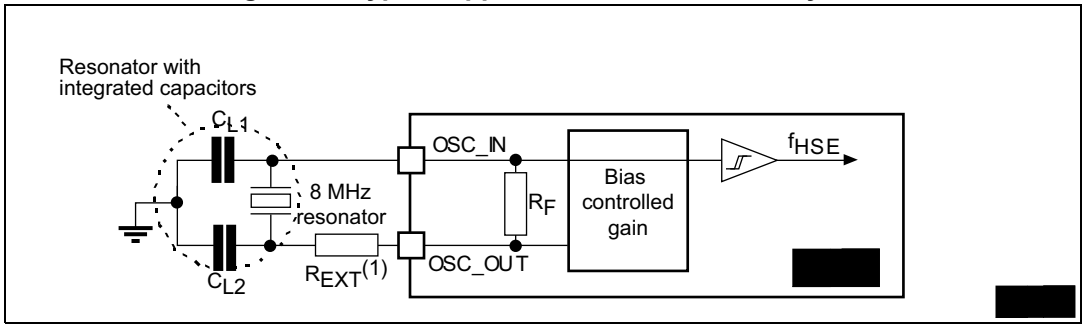
Symbol	Parameter	Operating conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	4	-	50	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	10	mA
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF at 4 MHz	-	0	-	
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF@8 MHz	-	0	-	
		V_{DD} = 3 V, Rm = 20 Ω, CL = 10 pF@16 MHz	-	1	-	
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF@32 MHz	-	1	-	
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF@48 MHz	-	1	-	
$Gm_{critmax}$	Maximum critical crystal gm	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Specified by design - Not tested in production.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note design guide for

Figure 16. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 38*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

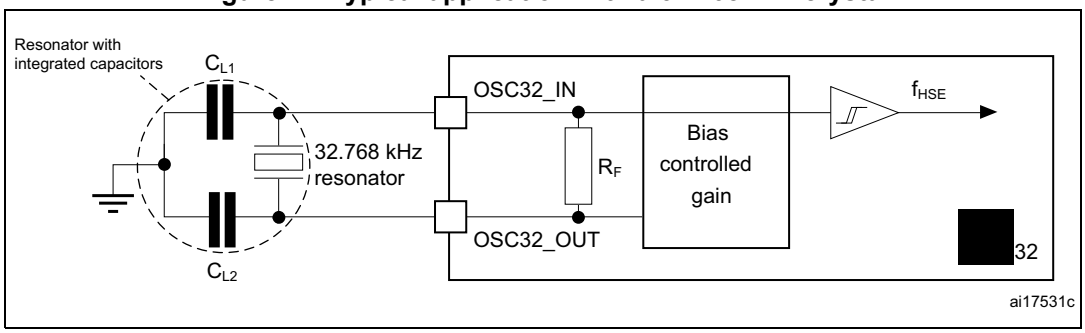
Table 38. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
I_{DD}	LSE current consumption	LSEDRV[1:0] = 01 Medium low drive capability	-	333.000	-	nA
		LSEDRV[1:0] = 10 Medium high drive capability	-	462.000	-	
		LSEDRV[1:0] = 11 High drive capability	-	747.000	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	µA/V
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Specified by design - Not tested in production, unless oterwise specified.
2. Refer to the note and caution paragraphs below the table, and to the application note [redacted] for [redacted].
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note [redacted] design guide for [redacted]

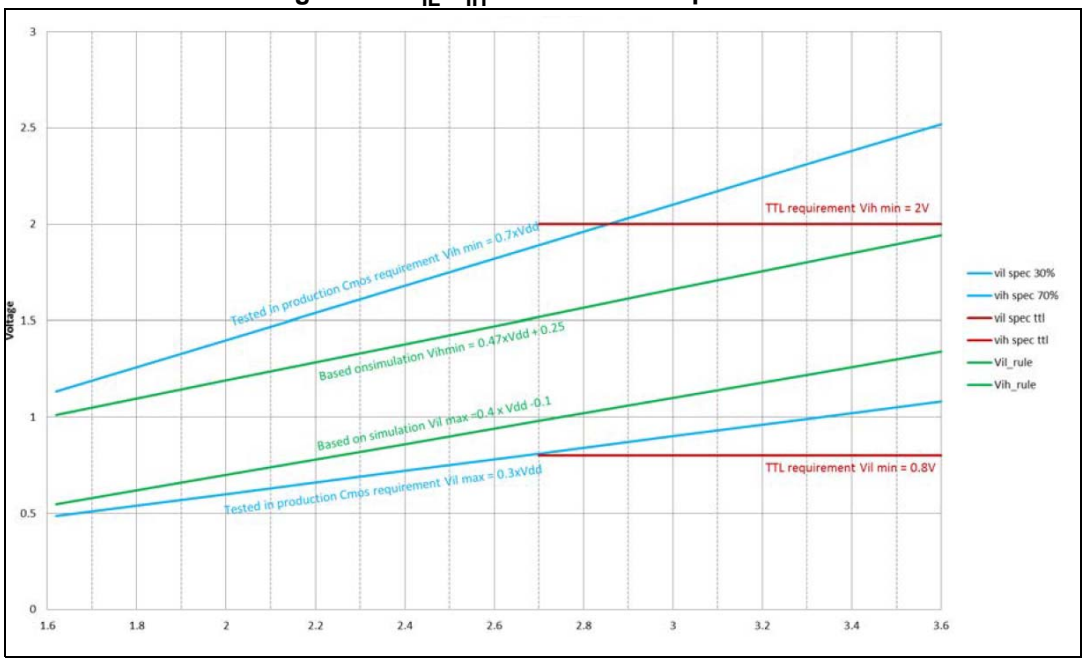
Figure 17. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 18*.

Figure 18. V_{IL}/V_{IH} for all I/Os except BOOT0



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Table 5.2: Absolute maximum ratings*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 14: Current characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 14: Current characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 54: Output voltage characteristics for all I/Os except PC13, PC14 and PC15* and *Table 55: Output voltage characteristics for PC13* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16: General operating conditions*. All I/Os are CMOS and TTL compliant.

Table 54. Output voltage characteristics for all I/Os except PC13, PC14 and PC15

Symbol	Parameter	Conditions(1)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO} = 8 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO} = -8 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD}−0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO} = 8 mA 2.7 V≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO} = -8 mA 2.7 V≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 20 mA 2.7 V≤ V_{DD} ≤ 3.6 V	-	1.3	
V_{OH}(3)	Output high level voltage	I_{IO} = -20 mA 2.7 V≤ V_{DD} ≤ 3.6 V	V_{DD} - 1.3	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 4 mA 1.71 V≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage	I_{IO} = -4 mA 1.71 V≤V_{DD} <3.6 V	V_{DD} - 0.4	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 2 mA 1.08 V≤ V_{DDIO2} ≤ 1.32 V	-	0.3 x V_{DDIO2}	
V_{OH} (3)	Output high level voltage	I_{IO} = -2 mA 1.08 V≤V_{DDIO2} < 1.32 V	0.7 x V_{DDIO2}	-	
V_{OLFM+}(3)	Output low level voltage for an FTf I/O pin in (FT I/O with “f” option)	I_{IO} = 20 mA 2.3 V≤ V_{DD} ≤3.6 V	-	0.4	
		I_{IO} = 10 mA 1.71 V≤ V_{DD} ≤ 3.6 V	-	0.4	
		I_{IO} = 4.5 mA 1.08 V≤ V_{DD} ≤ 3.6 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 13: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

Table 55. Output voltage characteristics for PC13(1)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO} = 3 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO} = -3 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD} - 0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO} = 3 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO} = -3 mA 2.7 V≤ V_{DD} ≤3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 1.5 mA 1.71 V≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	I_{IO} = −1.5 mA 1.71 V≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 13: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

Table 56. Output voltage characteristics for PC14 and PC15(1)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO} = 0.5 mA 2.7 V≤ V_{DD} ≤3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO} = -0.5 mA 2.7 V≤ V_{DD} ≤3.6 V	V_{DD} - 0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) I_{IO} = 0.5 mA 2.7 V ≤ V_{DD} ≤3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	TTL port(2) I_{IO} = -0.5 mA 2.7 V ≤ V_{DD} ≤3.6 V	2.4	-	
V_{OL}(3)	Output low level voltage	I_{IO} = 0.25 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(3)	Output high level voltage	I_{IO} = -0.25 mA 1.71 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 13: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design - Not tested in production.

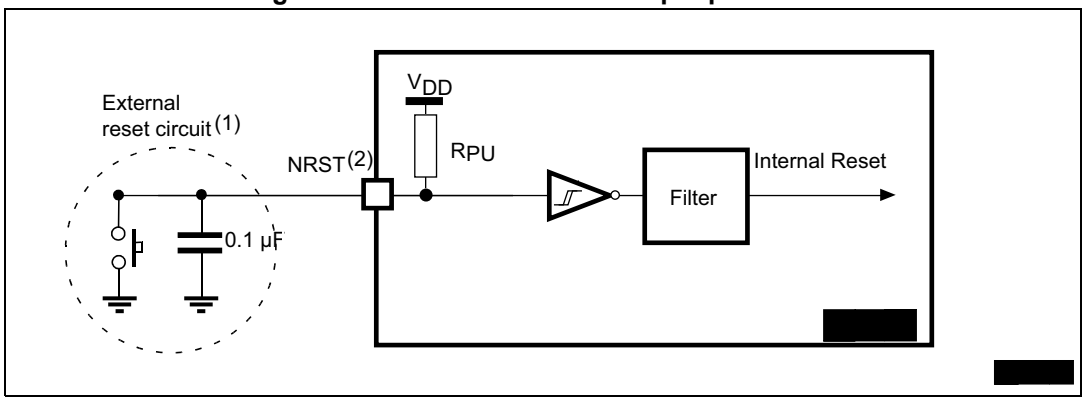
Output buffer timing characteristics (HSLV option disabled)

The HSLV feature (can be enabled over option bytes IO_VDDIO2_HSLV and IO_VDD_HSLV) can be used to optimize the I/O speed when the product voltage is below 2.7 V.

Table 57. Output timing characteristics (HSLV OFF)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)(3)	Maximum frequency	C = 50 pF, 2.7 V≤ V_{DD} ≤ 3.6 V	-	8	MHz
			C = 50 pF, 1.71 V≤V_{DD} ≤ 2 V	-	5	
			C = 40 pF, 2.7 V≤V_{DD} ≤ 3.6 V	-	10	
			C = 40 pF, 1.71 V≤V_{DD}≤ 2 V	-	5	
			C = 30 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	12	
			C = 30 pF, 1.71 V≤V_{DD}≤ 2 V	-	5	
			C = 20 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	14	
			C = 20 pF, 1.71 V≤V_{DD}≤ 2 V	-	5	
			C = 10 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	16	
			C = 10 pF, 1.71 V≤V_{DD}≤ 2 V	-	5	
	t_r/t_f(4)(5)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	18.0	ns
			C = 50 pF, 1.71 V≤V_{DD} ≤ 2 V	-	36.0	
			C = 40 pF, 2.7 V≤V_{DD} ≤ 3.6 V	-	17.0	
			C = 40 pF, 1.71 V≤V_{DD}≤ 2 V	-	34.0	
			C = 30 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	15.5	
			C = 30 pF, 1.71 V≤V_{DD}≤ 2 V	-	32.0	
			C = 20 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	14.2	
			C = 20 pF, 1.71 V≤V_{DD}≤ 2 V	-	30.0	
			C = 10 pF, 2.7 V≤V_{DD}≤ 3.6 V	-	12.2	
			C = 10 pF, 1.71 V≤V_{DD}≤ 2 V	-	27	

Figure 19. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 53*. Otherwise the reset is not taken into account by the device.

5.3.16 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 62. EXTI input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

1. Specified by design - Not tested in production.

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 63* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 16: General operating conditions*.

Table 63. 12-bit ADC characteristics(1)(2)

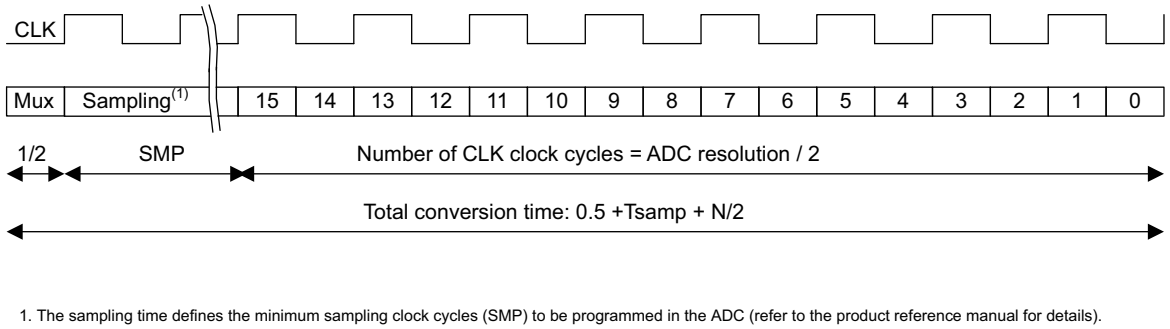
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.62	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	V_{SSA}			
f_{ADC}	ADC clock frequency	1.62 V ≤ V_{DDA} ≤ 3.6 V	1.5	-	37.5	MHz

Table 64. Minimum sampling time versus R_{AIN}(1)(2) (continued)

Resolution	R_{AIN} (Ω)	Minimum sampling time (s)	
		Fast channel	Slow channel(3)
6 bits	47	2.14E-08	3.16E-08
	68	2.23E-08	3.21E-08
	100	2.40E-08	3.31E-08
	150	2.68E-08	3.52E-08
	220	3.13E-08	3.87E-08
	330	3.89E-08	4.51E-08
	470	4.88E-08	5.39E-08
	680	6.38E-08	6.79E-08
	1000	8.70E-08	8.97E-08
	1500	1.23E-07	1.24E-07
	2200	1.73E-07	1.73E-07
	3300	2.53E-07	2.49E-07
	4700	3.53E-07	3.45E-07
	6800	5.04E-07	4.90E-07
	10000	7.34E-07	7.11E-07
	15000	1.09E-06	1.05E-06

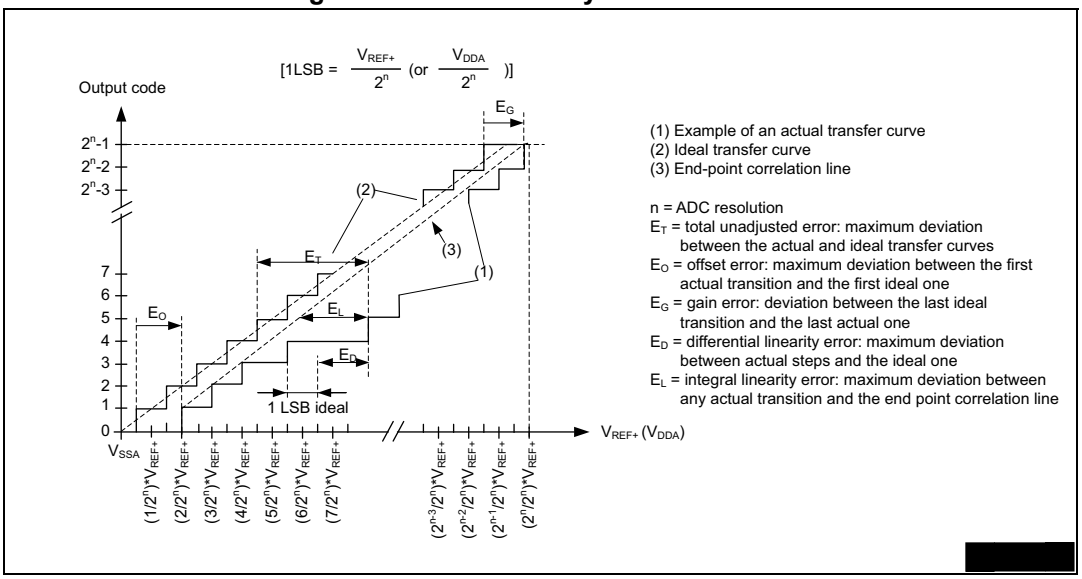
1. Specified by design - Not tested in production.
2. Data valid up to 130 °C, with a 22 pF PCB capacitor, and V_{DDA} = 1.6 V.
3. Slow channels correspond to all ADC inputs except for the fast channels.

Figure 20. ADC conversion timing diagram



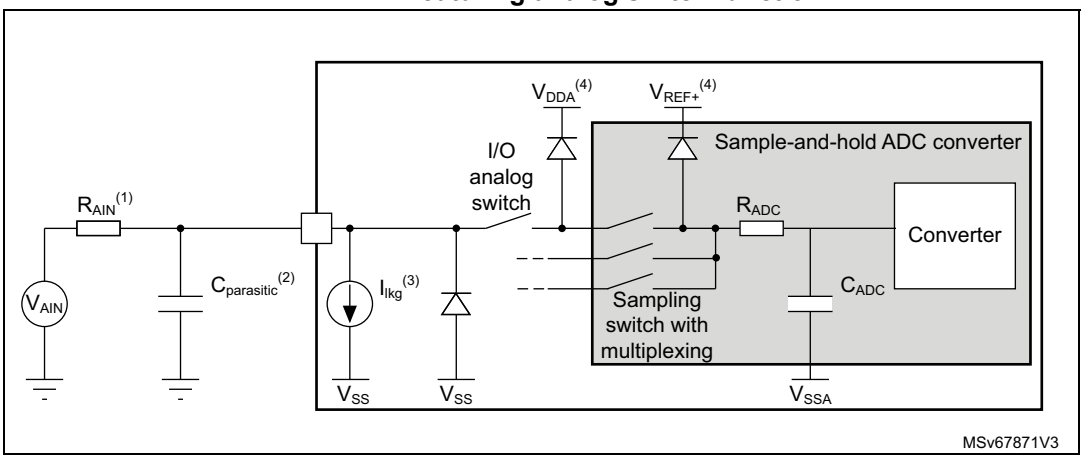
1. The sampling time defines the minimum sampling clock cycles (SMP) to be programmed in the ADC (refer to the product reference manual for details).

Figure 21. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
5. EO = Offset Error: deviation between the first actual transition and the first ideal one.
6. EG = Gain Error: deviation between the last ideal transition and the last actual one.
7. ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
8. EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 22. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function



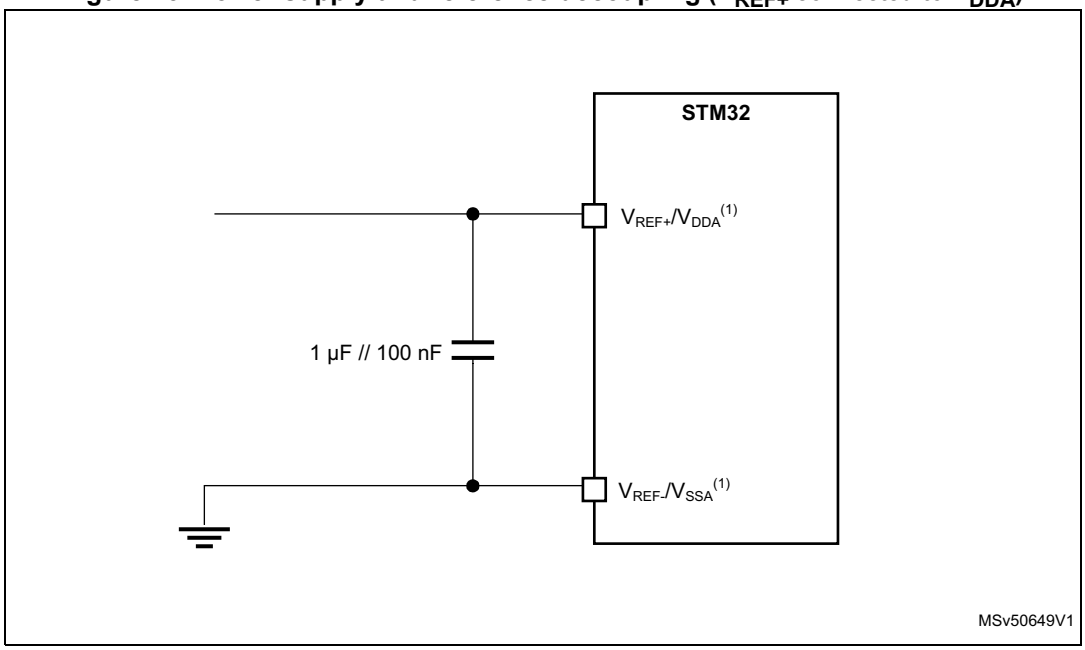
1. Refer to *Table 63: 12-bit ADC characteristics* for the values of R_{AIN}, and C_{ADC}.

4. Refer to *Figure 11: Power supply scheme*.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 23*. The 100 nF capacitors should be ceramic (good quality). They should be placed as close to the chip as possible.

Figure 23. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. [redacted]ternally connected to V_{DDA} while V_{REF-} is internally connected to V_{SSA} (refer to *Table 2: [redacted]eatures and peripheral counts*).

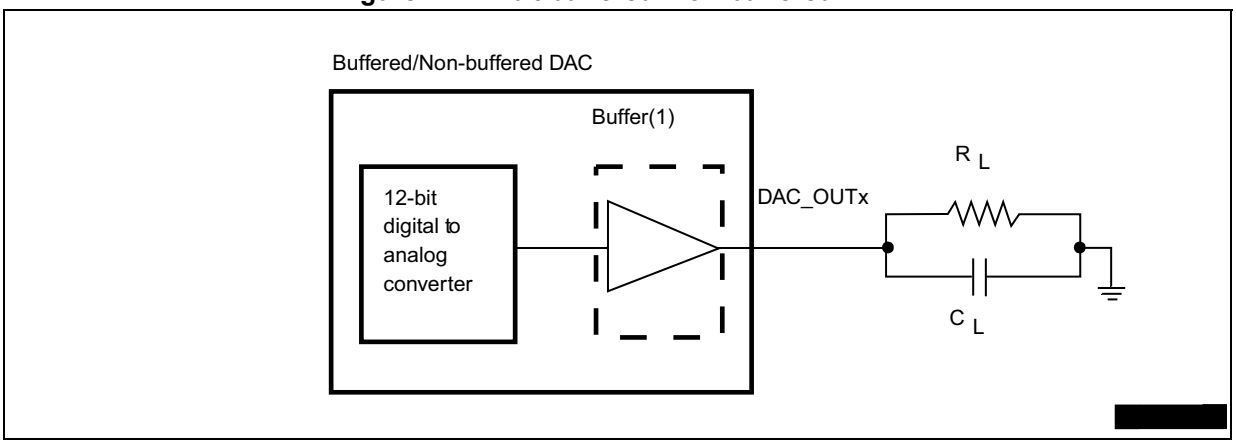
5.3.18 DAC characteristics

Table 66. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.8	3.3	3.6	V
V_{REF+}	Positive reference voltage	-		1.80	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-		-	V_{SSA}	-	V
R_L	Resistive Load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	kΩ
R_O	Output Impedance	DAC output buffer OFF		10.3	13	16	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON	V_{DD} = 2.7 V	-	-	1.6	kΩ
			V_{DD} = 2.0 V	-	-	2.6	kΩ
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF	V_{DD} = 2.7 V	-	-	17.8	kΩ
			V_{DD} = 2.0 V	-	-	18.7	kΩ

1. Evaluated by characterization - Not tested in production.
2. Difference between two consecutive codes minus 1 LSB.
3. Difference between the value measured at Code i and the value measured at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and 0xFFF when the buffer is OFF, and from code giving 0.2 V and (V_{REF+} - 0.2 V) when the buffer is ON.
6. Signal is −0.5dBFS with $F_{sampling}$=1 MHz.

Figure 24. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.19 Analog temperature sensor characteristics

Table 68. Analog temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature (from V_{SENSOR} voltage)	-	-	3	°C
	V_{SENSE} linearity with temperature (from ADC counter)	-	-	3	
Avg_Slope(2)	Average slope (from V_{SENSOR} voltage)	-	2	-	mV/°C
	Average slope (from ADC counter)	-	2	-	
V_{30}(3)	Voltage at 30°C ± 5 °C	-	0.62	-	V
t_{start_run}	Startup time in Run mode (buffer startup)	-	-	25.2	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	9	-	-	
I_{sens}(1)	Sensor consumption	-	0.18	0.31	µA
$I_{sensbuf}$(1)	Sensor buffer consumption	-	3.8	6.5	

1. Specified by design - Not tested in production.
2. Evaluated by characterization - Not tested in production.
3. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.

Table 82. USART characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(TX)}$	Data output hold time	Slave mode 1.71 V < V_{DD} < 3.6 V	7.5	-	-	ns
		Slave mode 1.08 V < V_{DDIO2} < 1.32 V	10.5	-	-	
		Master mode	0	-	-	

1. Evaluated by characterization - Not tested in production.
2. For VDDIO2 OSPEEDRy[1:0] = 11.
3. t_{ker} is the usart_ker_ck_pres clock period.
4. For V_{DDIO2}.

Figure 25. USART timing diagram in Master mode

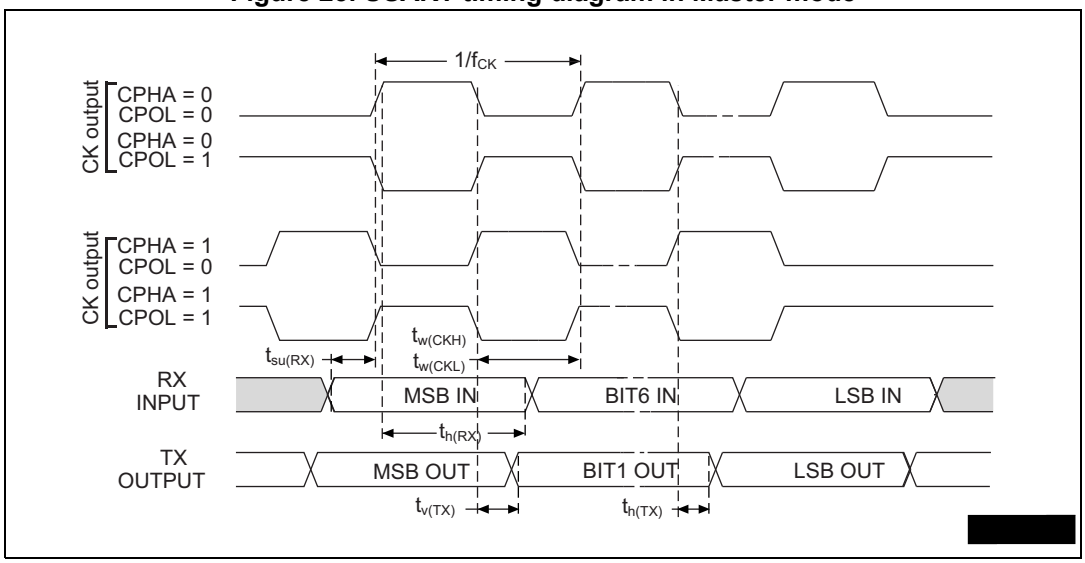
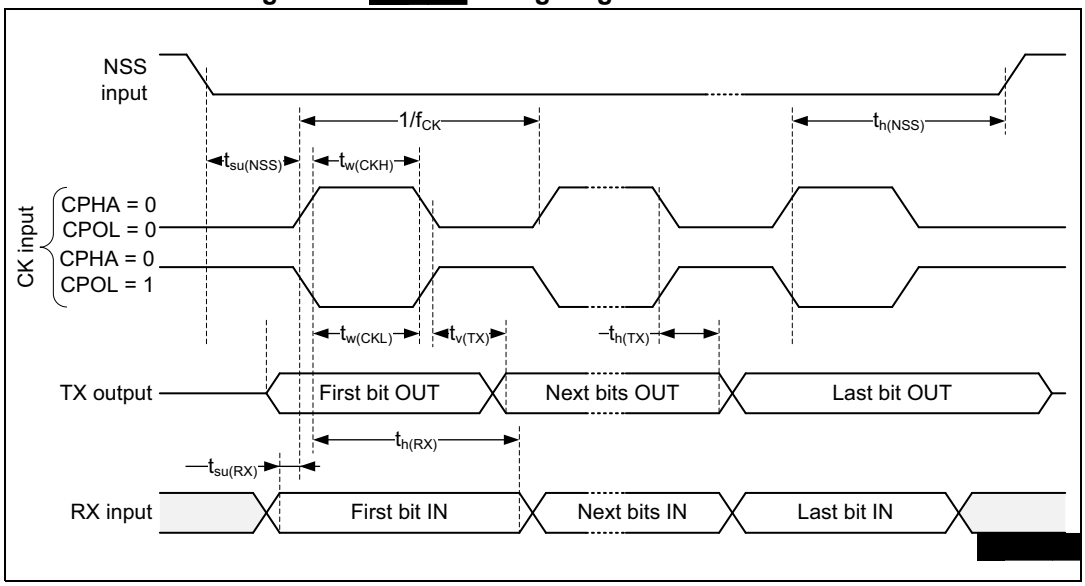


Figure 26. [redacted] timing diagram in Slave mode



SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 83* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 16: General operating conditions* and *Section 5.3.1: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS0

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 83. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(MI)}$	Data input setup time	Master mode	3.5	-	-	ns
$t_{su(SI)}$		Slave mode	2	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	1	-	-	
$t_{h(SI)}$		Slave mode	1.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	6.5	-	15	
$t_{dis(SO)}$	Data output disable time	Slave mode	7.5	-	18	
$t_{v(SO)}$	Data output valid time	Slave mode, $2.7\ V \le V_{DD} \le 3.6\ V$	-	8.5	11.5	
		Slave mode, $1.71\ V \le V_{DD} \le 2.7\ V$	-	10	12	
		Slave mode, $1.08\ V \le V_{DDIO2} \le 1.32\ V$	-	18	21.5	
$t_{v(MO)}$		Master mode	-	1.5	2	
$t_{h(SO)}$	Data output hold time	Slave mode, $1.71\ V \le V_{DD} \le 3.6\ V$	6.5	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Evaluated by characterization - Not tested in production.

Figure 27. SPI timing diagram - slave mode and CPHA = 0

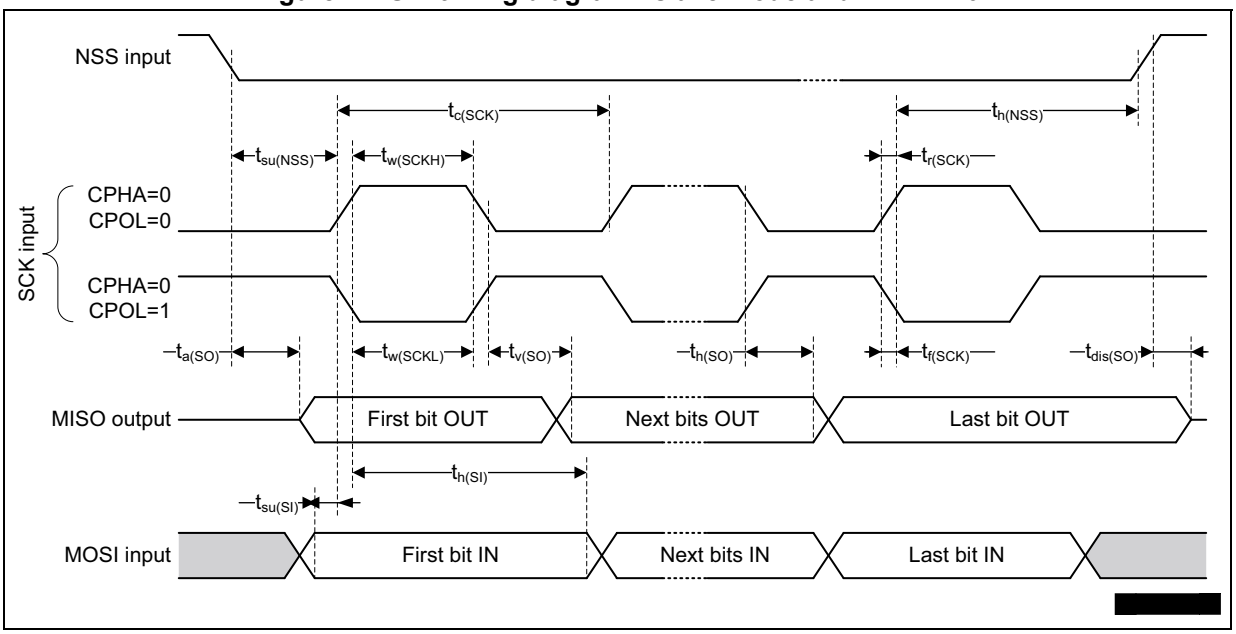
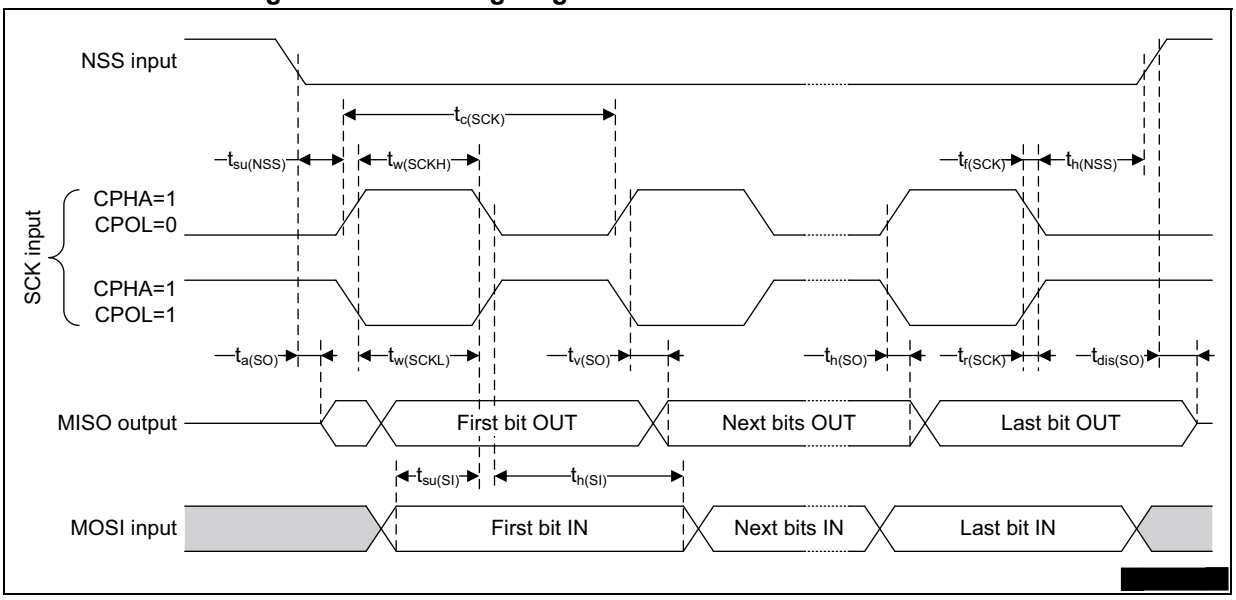
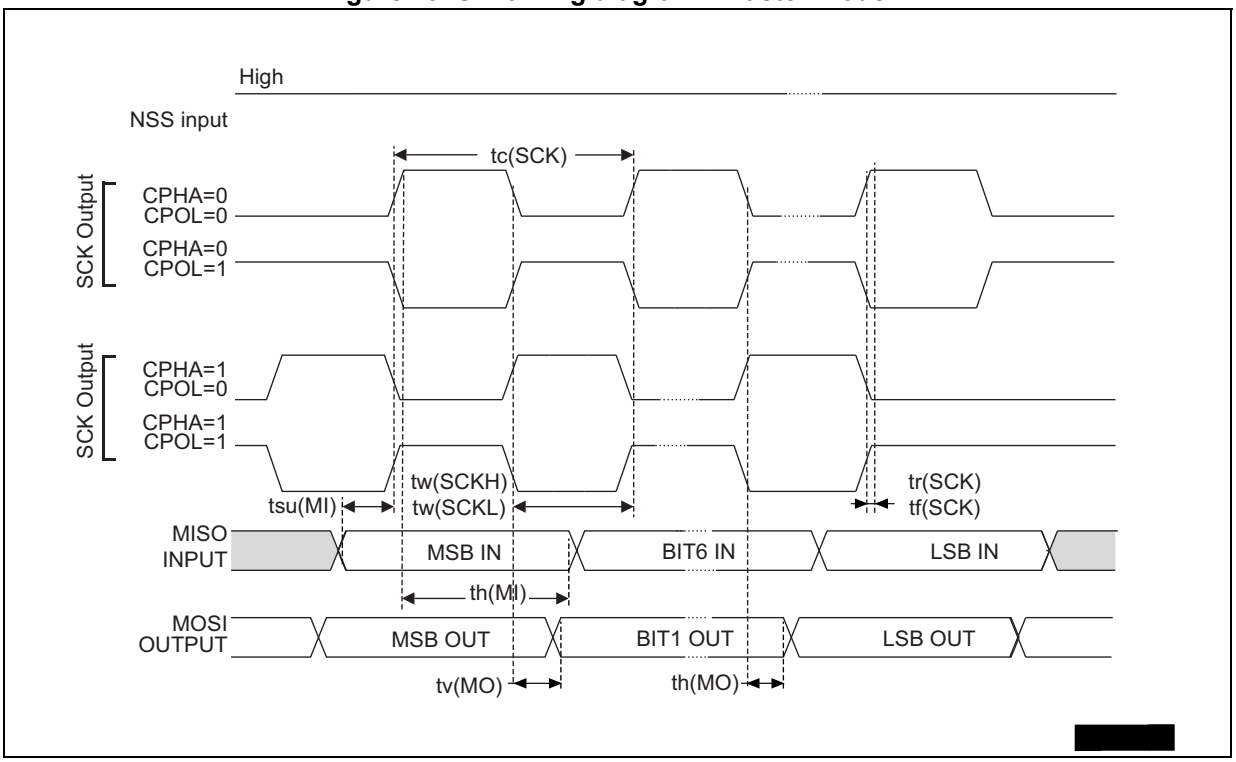


Figure 28. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 29. SPI timing diagram - master mode(1)

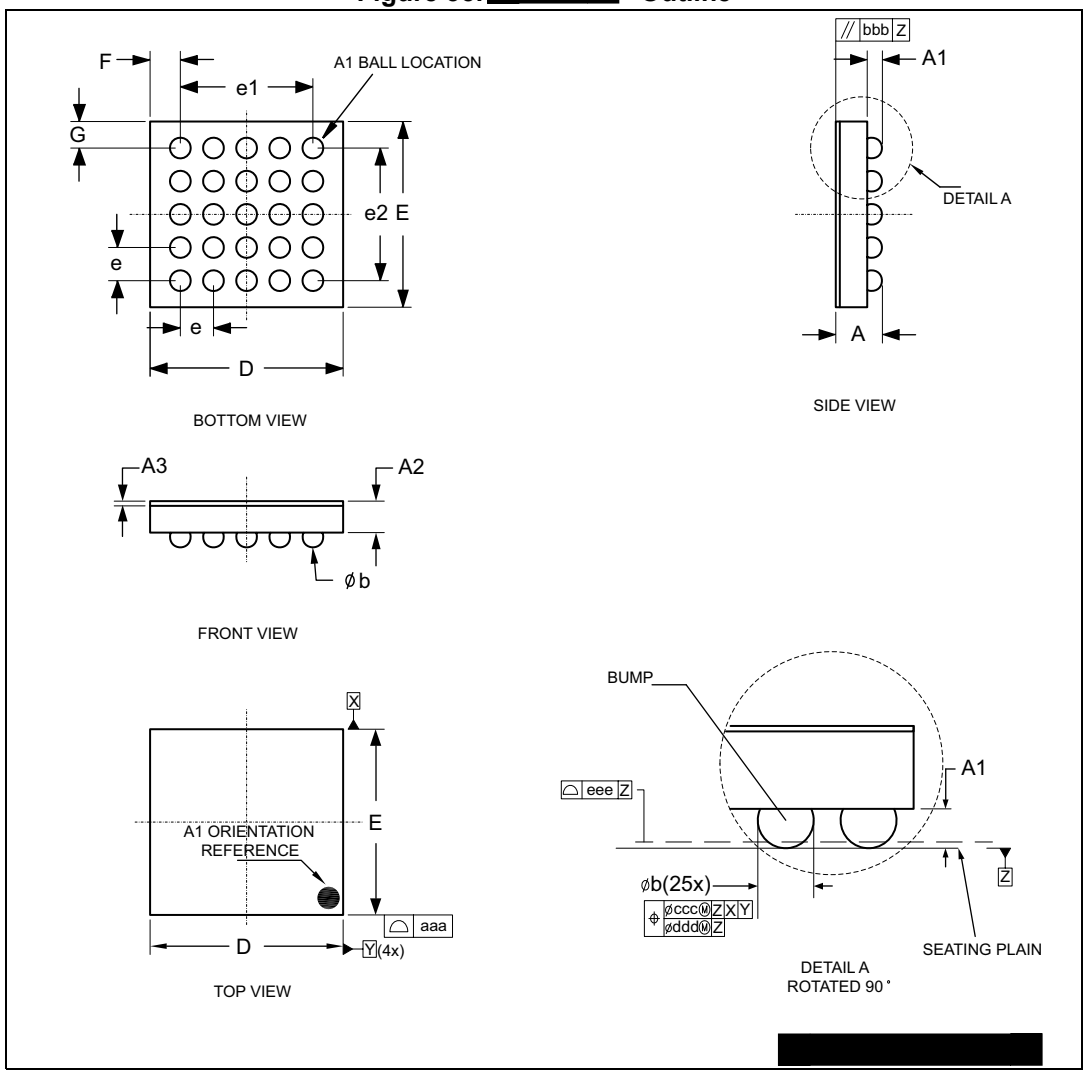


1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

6.1 [redacted] package information

[redacted]s a 25 ball, 2.33 x 2.24 mm, 0.4 mm pitch, wafer level chip scale package.

Figure 35. [redacted] - Outline



1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.The tolerance of position that controls the location of the pattern of balls with respect to datums X and Y. For each ball there is a cylindrical tolerance zone ccc perpendicular to datum Z and located on true position with respect to datums X and Y as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone.

Figure 36. [redacted] - Footprint example

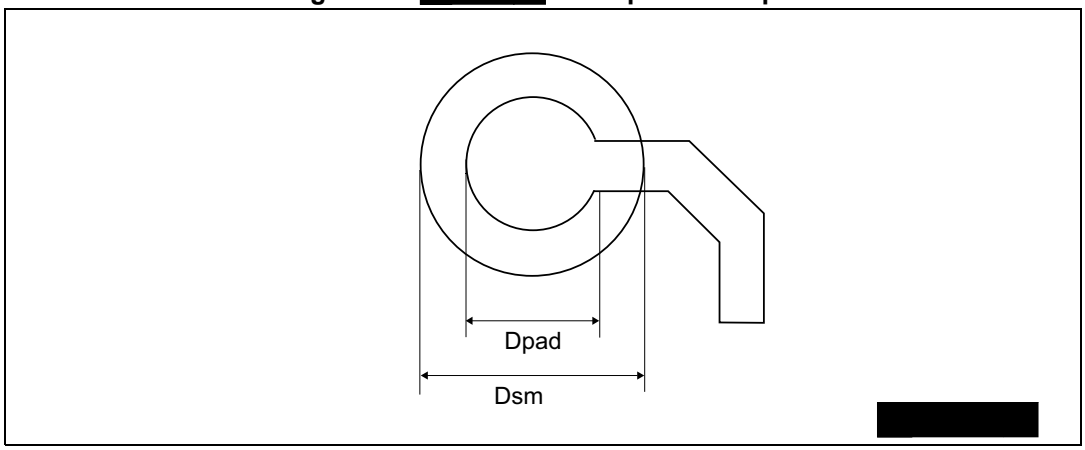


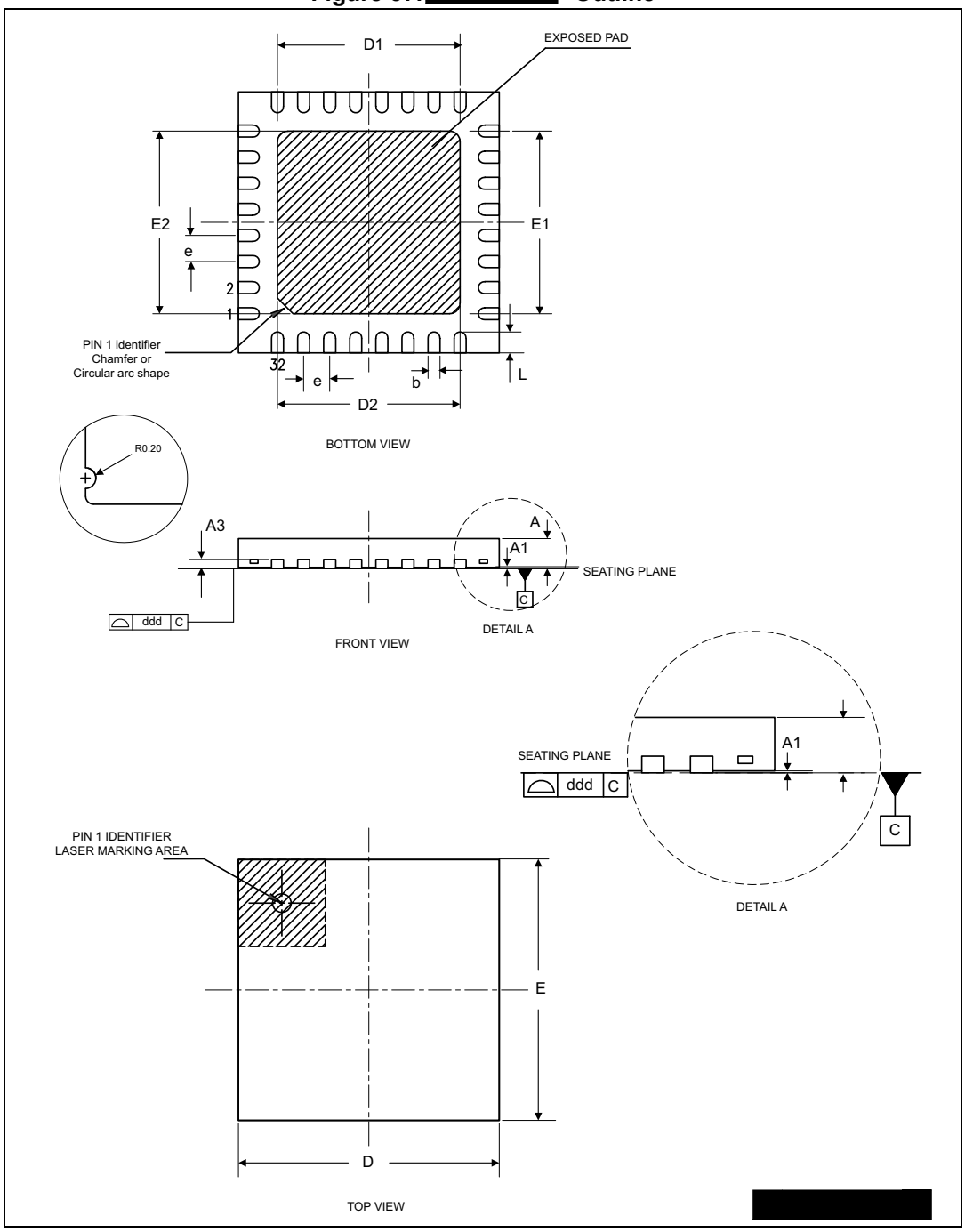
Table 91. [redacted] - Example of PCB design rules

Dimension	Values
Pitch	0.4 mm
Dpad	0,225 mm
Dsm	0.290 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

6.2 [redacted] package information

[redacted] a 32 pins, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package.

Figure 37. [redacted] - Outline



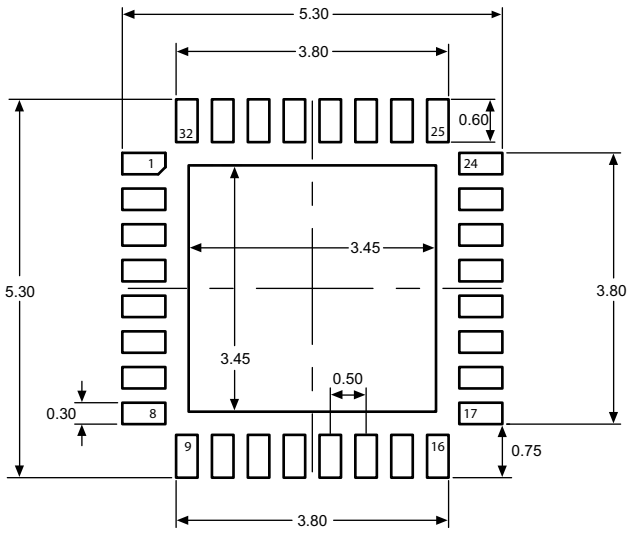
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the [redacted] ackage. It is recommended to connect and solder this backside pad to PCB ground.

Table 92. [redacted] Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	-	0.300	0.0071	-	0.0118
D[2]	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	-	3.700	0.1339	-	0.1457
D2	3.400	-	3.600	0.1339	-	0.1417
E[2]	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	-	3.700	0.1339	-	0.1457
E2	3.400	-	3.700	0.1339	-	0.1457
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimensions D and E do not include mold protrusion, not to exceed 0,15mm.

Figure 38. [redacted] - Footprint example

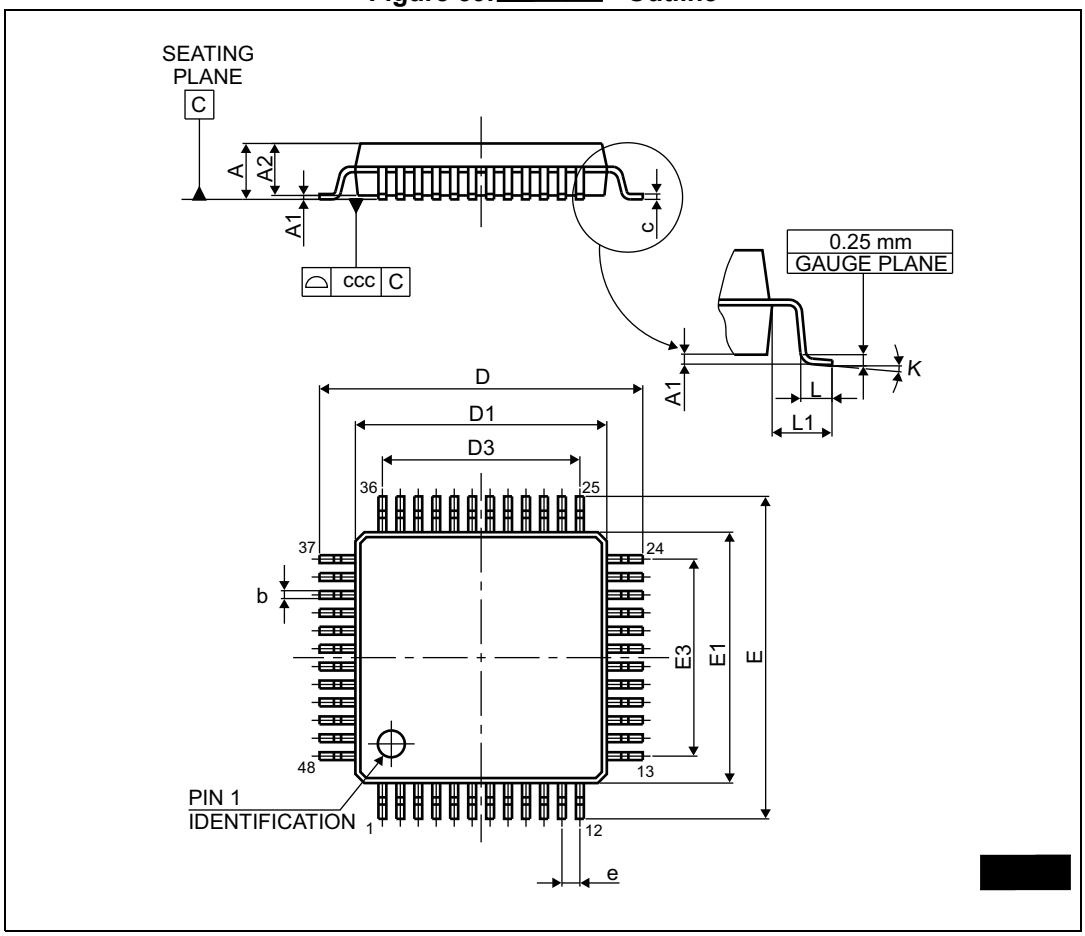


1. Dimensions are expressed in millimeters.

6.3 package information

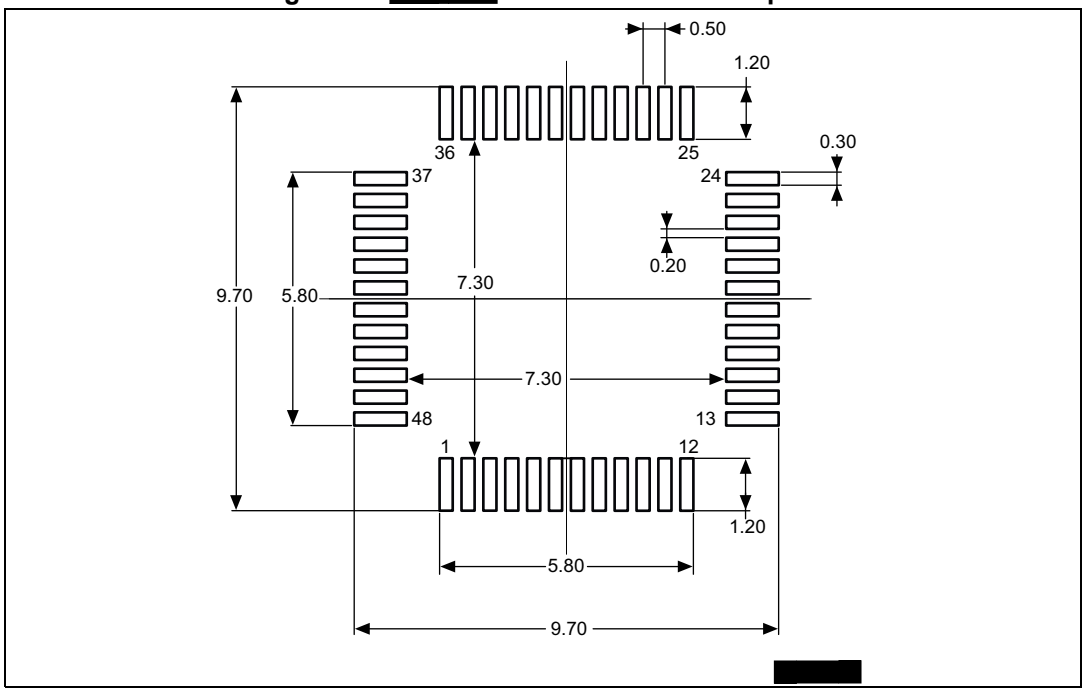
This s a 48-pin, 7 x 7 mm low-profile quad flat package

Figure 39. - Outline



1. Drawing is not to scale.

Figure 40. [redacted] - Recommended footprint

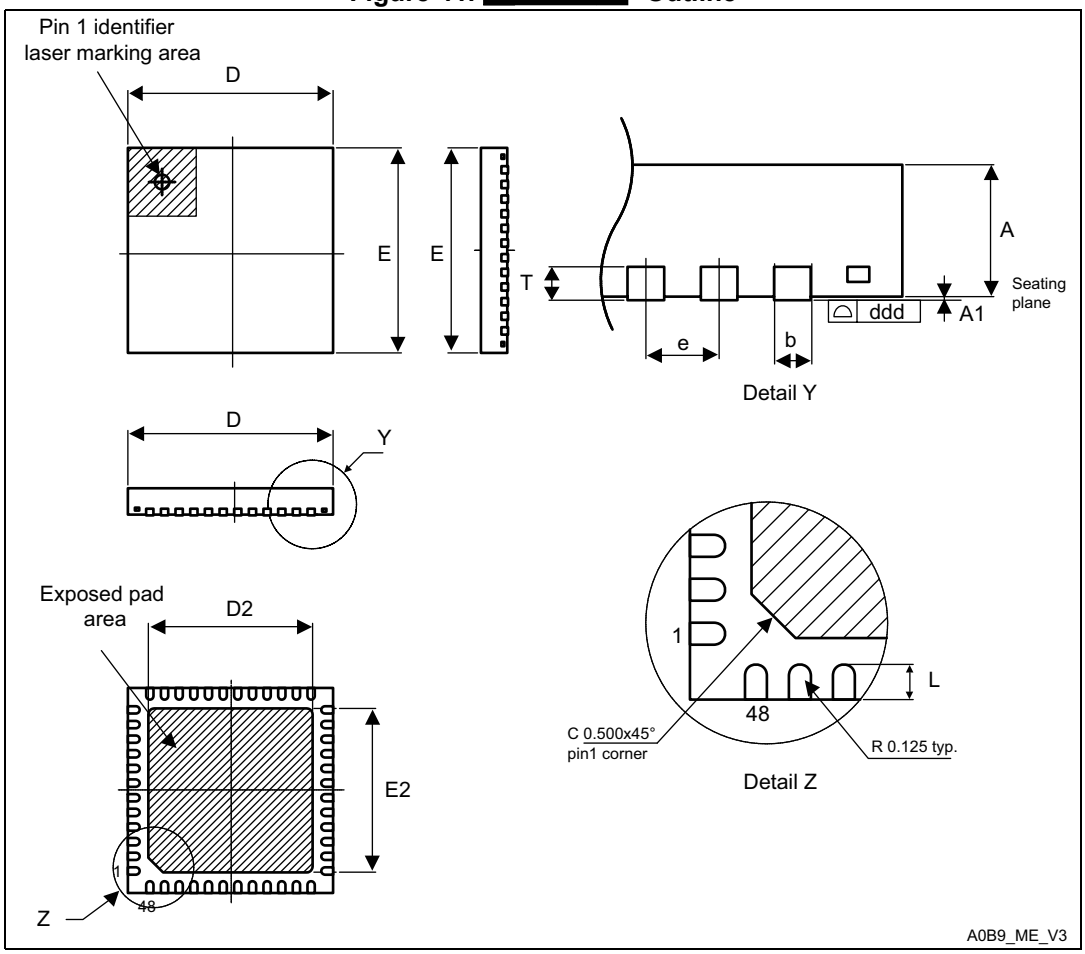


1. Dimensions are expressed in millimeters.

6.4 [redacted] package information

a 48 leads, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package

Figure 41. [redacted]- Outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the [redacted] package. It is recommended to connect and solder this back-side pad to PCB ground.

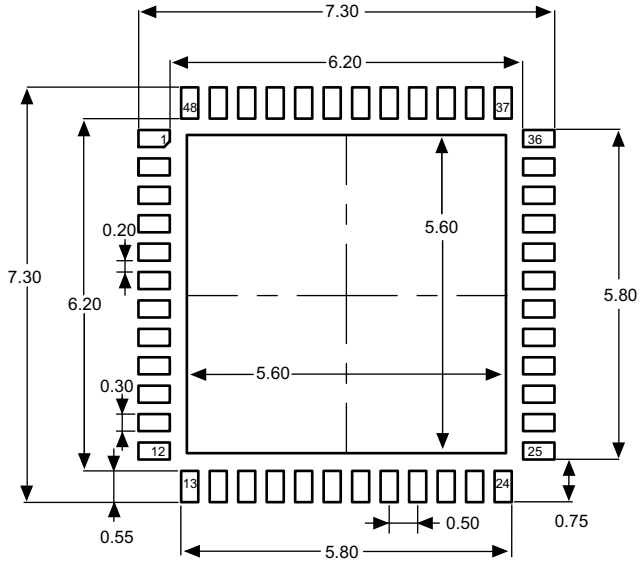
[redacted]

Table 94. [redacted] - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. [redacted] - Recommended footprint



1. Dimensions are expressed in millimeters.

6.5 [redacted]ackage information

[redacted]4-pin, 10 x 10 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 43. [redacted]- Outline(15)