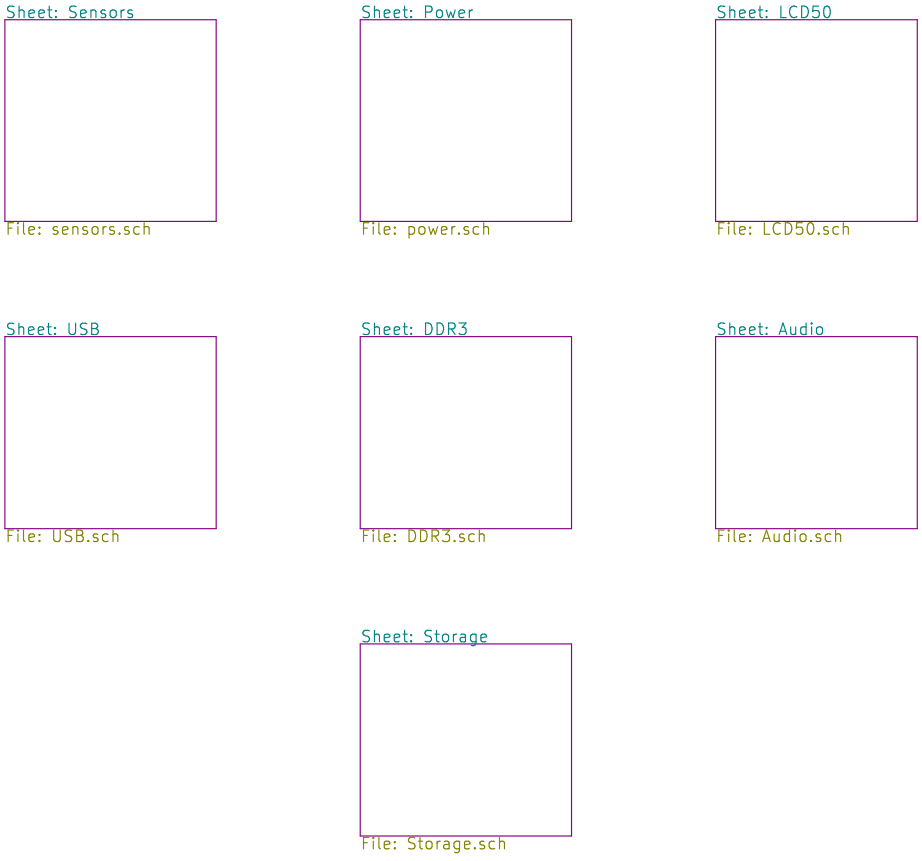
DT01 v3


Sheet: Sensors
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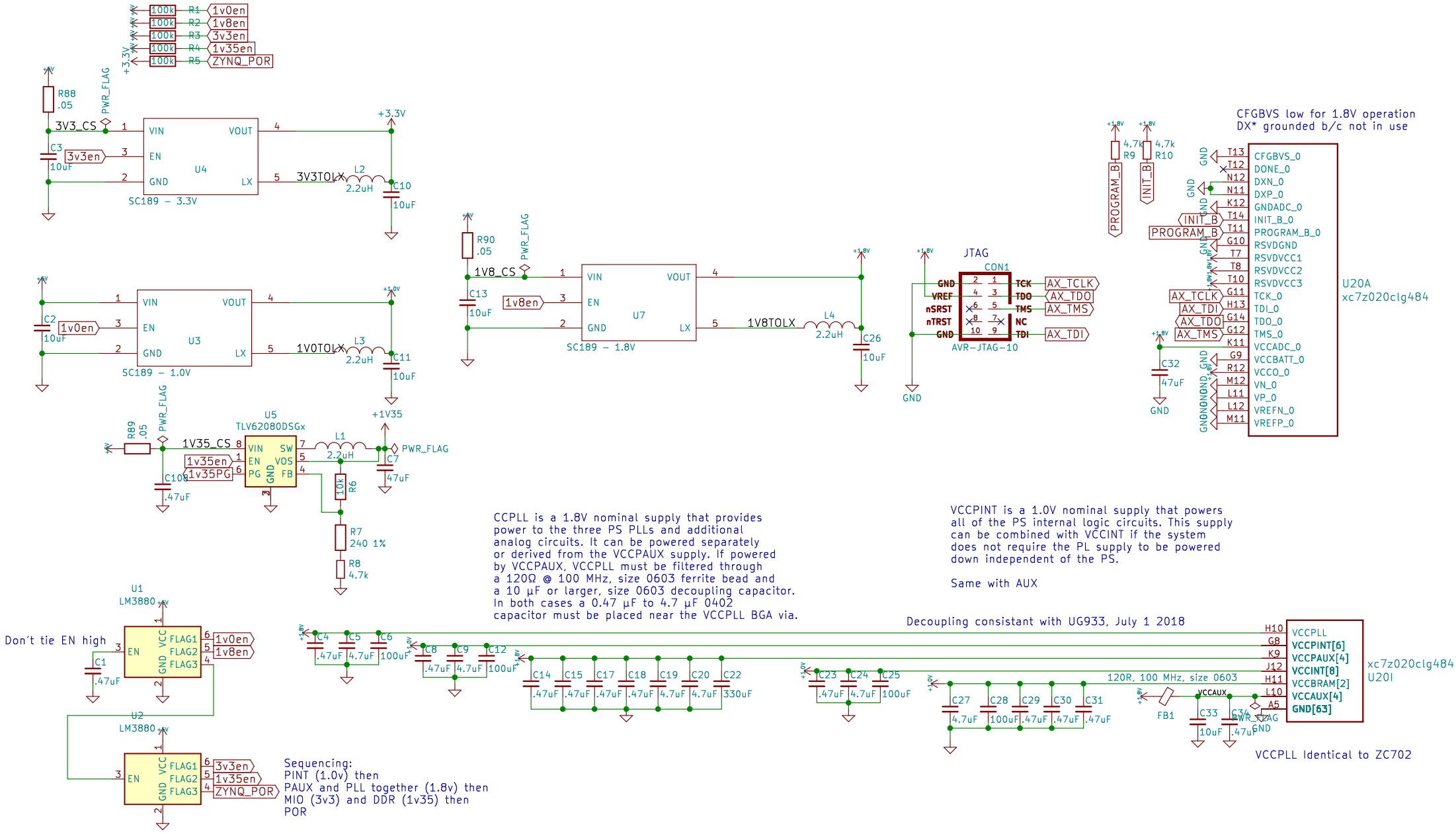
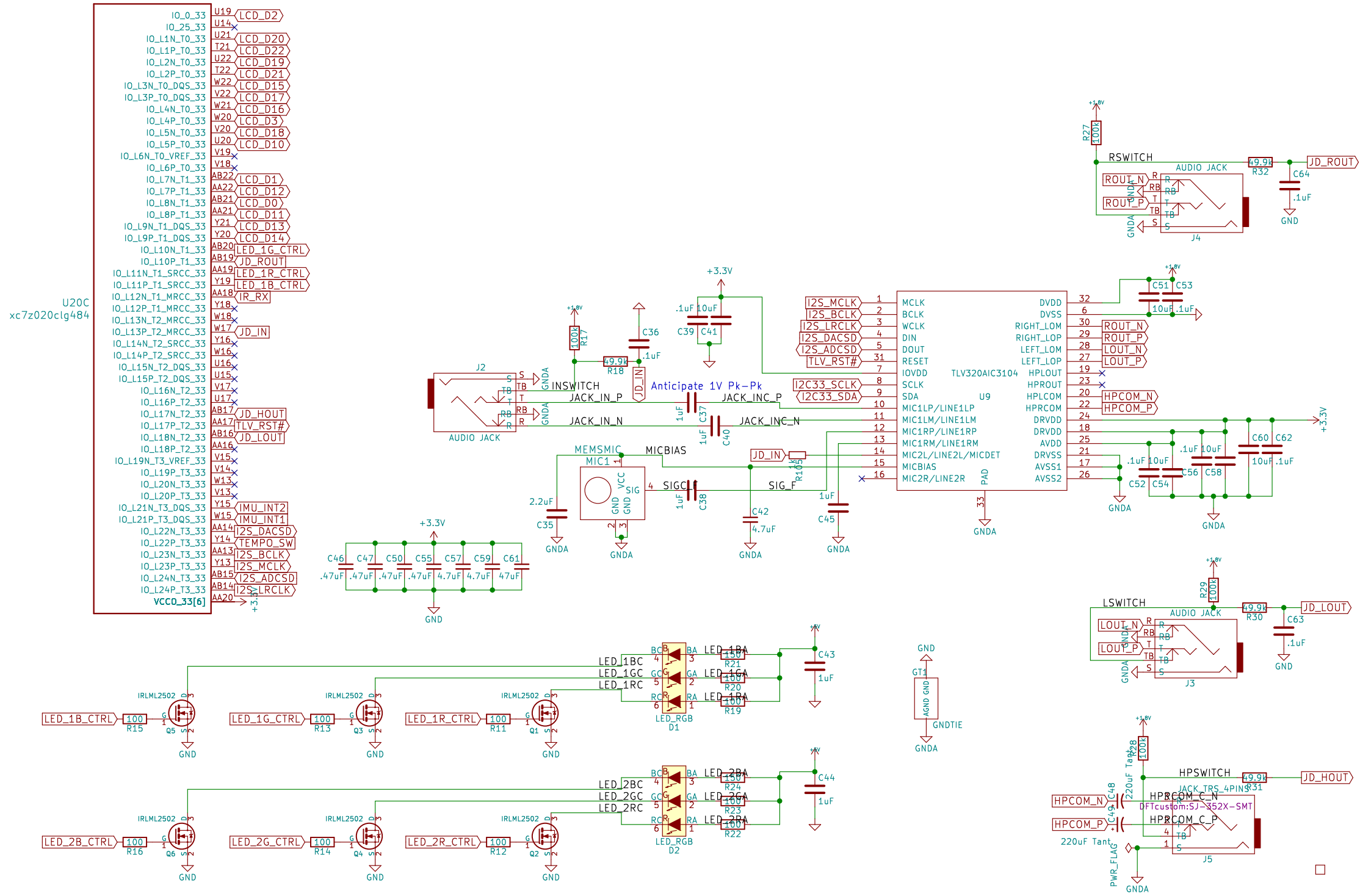
Sheet: Power
File: power.sch
Sheet: LCD50
File: LCD50.sch
Sheet: USB
File: USB.sch
Sheet: DDR3
File: DDR3.sch
Sheet: Audio
File: Audio.sch
Sheet: Storage
File: Storage.sch

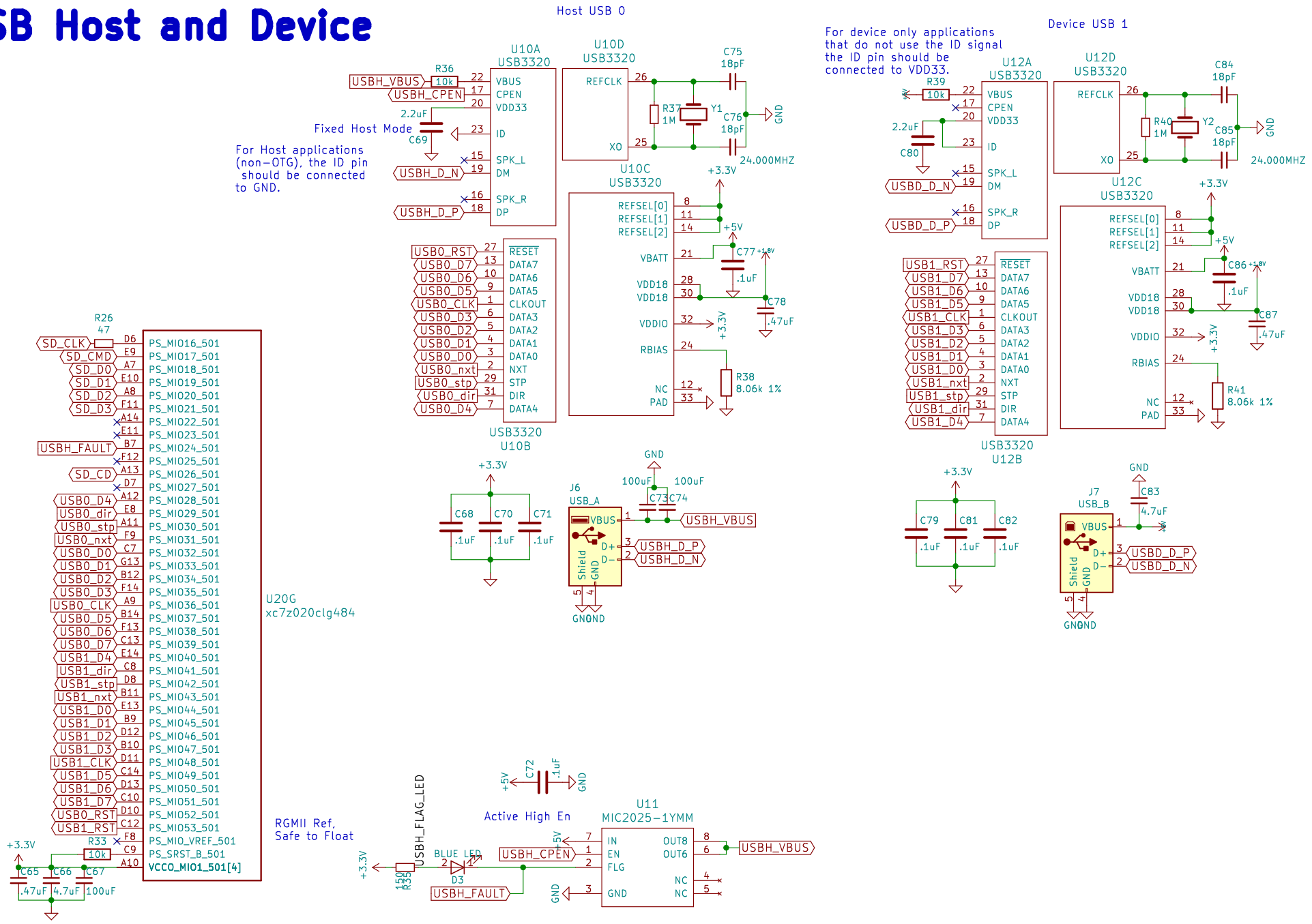
Power


100k R1 1v0en
100k R2 1v8en
100k R3 3v3en
100k R4 1v35en
100k R5 ZYNQ_POR
+3.3V
R88 .05
PWR_FLAG
3V3_CS
U4
VIN
VOUT
EN
GND
LX
SC189 – 3.3V
3v3en
C3 10uF
3V3TOLX
L2 2.2uH
C10 10uF
+3.3V
C2 10uF
1v0en
U3
SC189 – 1.0V
1V0TOLX
L3 2.2uH
C11 10uF
+1.0V
R90 .05
1V8_CS
1v8en
U7
SC189 – 1.8V
1V8TOLX
L4 2.2uH
C26 10uF
+1.8V
JTAG
CON1
GND
VREF
nSRST
nTRST
TCK
TDO
TMS
NC
TDI
AX_TCLK
AX_TDO
AX_TMS
AX_TDI
AVR-JTAG-10
PROGRAM_B
INIT_B
4.7k R9
4.7k R10
CFGBVS low for 1.8V operation
DX* grounded b/c not in use
CFGBVS_0
DONE_0
DXN_0
DXP_0
GNDADC_0
INIT_B_0
PROGRAM_B_0
RSVDGND
RSVDVCC1
RSVDVCC2
RSVDVCC3
TCK_0
TDI_0
TDO_0
TMS_0
VCCADC_0
VCCBATT_0
VCCO_0
VN_0
VP_0
VREFN_0
VREFP_0
U20A
xc7z020clg484
C32 47uF
R89 .05
U5
TLV62080DSGx
1V35_CS
1v35en
1v35PG
VIN
SW
EN
VOS
PG
GND
FB
L1 2.2uH
+1V35
PWR_FLAG
C7 47uF
C108 .47uF
10k R6
R7 240 1%
R8 4.7k
CCPLL is a 1.8V nominal supply that provides power to the three PS PLLs and additional analog circuits. It can be powered separately or derived from the VCCPAUX supply. If powered by VCCPAUX, VCCPLL must be filtered through a 120Ω @ 100 MHz, size 0603 ferrite bead and a 10 µF or larger, size 0603 decoupling capacitor. In both cases a 0.47 µF to 4.7 µF 0402 capacitor must be placed near the VCCPLL BGA via.
VCCPINT is a 1.0V nominal supply that powers all of the PS internal logic circuits. This supply can be combined with VCCINT if the system does not require the PL supply to be powered down independent of the PS.
Same with AUX
Decoupling consistant with UG933, July 1 2018
U1
LM3880
Don't tie EN high
C1 .47uF
FLAG1
FLAG2
FLAG3
VCC
1v0en
1v8en
U2
3v3en
1v35en
ZYNQ_POR
Sequencing:
PINT (1.0v) then
PAUX and PLL together (1.8v) then
MIO (3v3) and DDR (1v35) then
POR
C4 C5 C6 .47uF 4.7uF 100uF
C8 C9 C12 .47uF 4.7uF 100uF
C14 C15 C17 C18 C19 C20 C22 .47uF 4.7uF 330uF
C23 C24 C25 .47uF 4.7uF 100uF
C27 C28 C29 C30 C31 4.7uF 100uF 47uF 47uF .47uF
120R, 100 MHz, size 0603
FB1
VCCAUX
C33 10uF
C34 .47uF
PWR_FLAG
H10 VCCPLL
G8 VCCPINT[6]
K9 VCCPAUX[4]
J12 VCCINT[8]
H11 VCCBRAM[2]
L10 VCCAUX[4]
A5 GND[63]
xc7z020clg484
U20I
VCCPLL Identical to ZC702

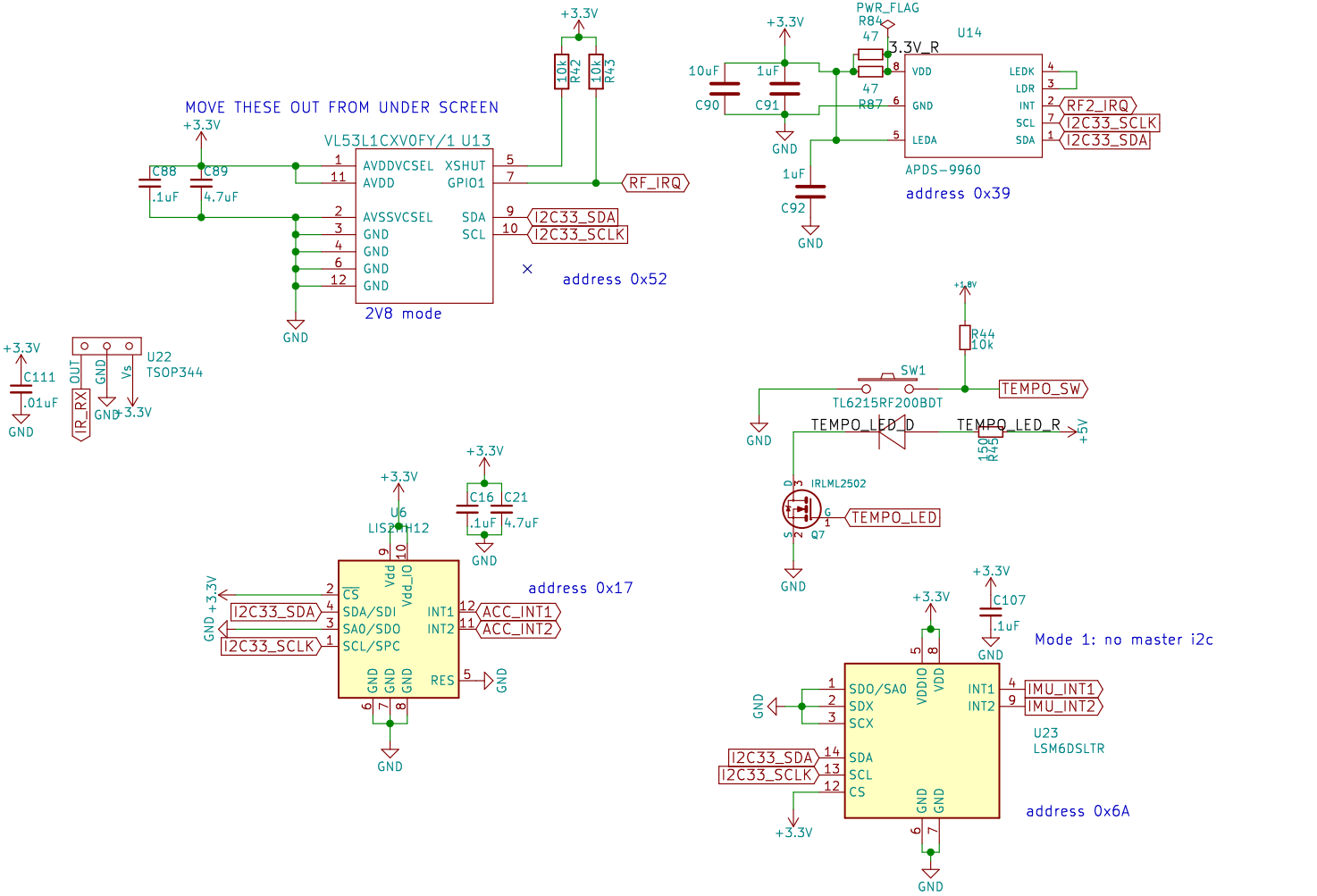
Audio and HDMI



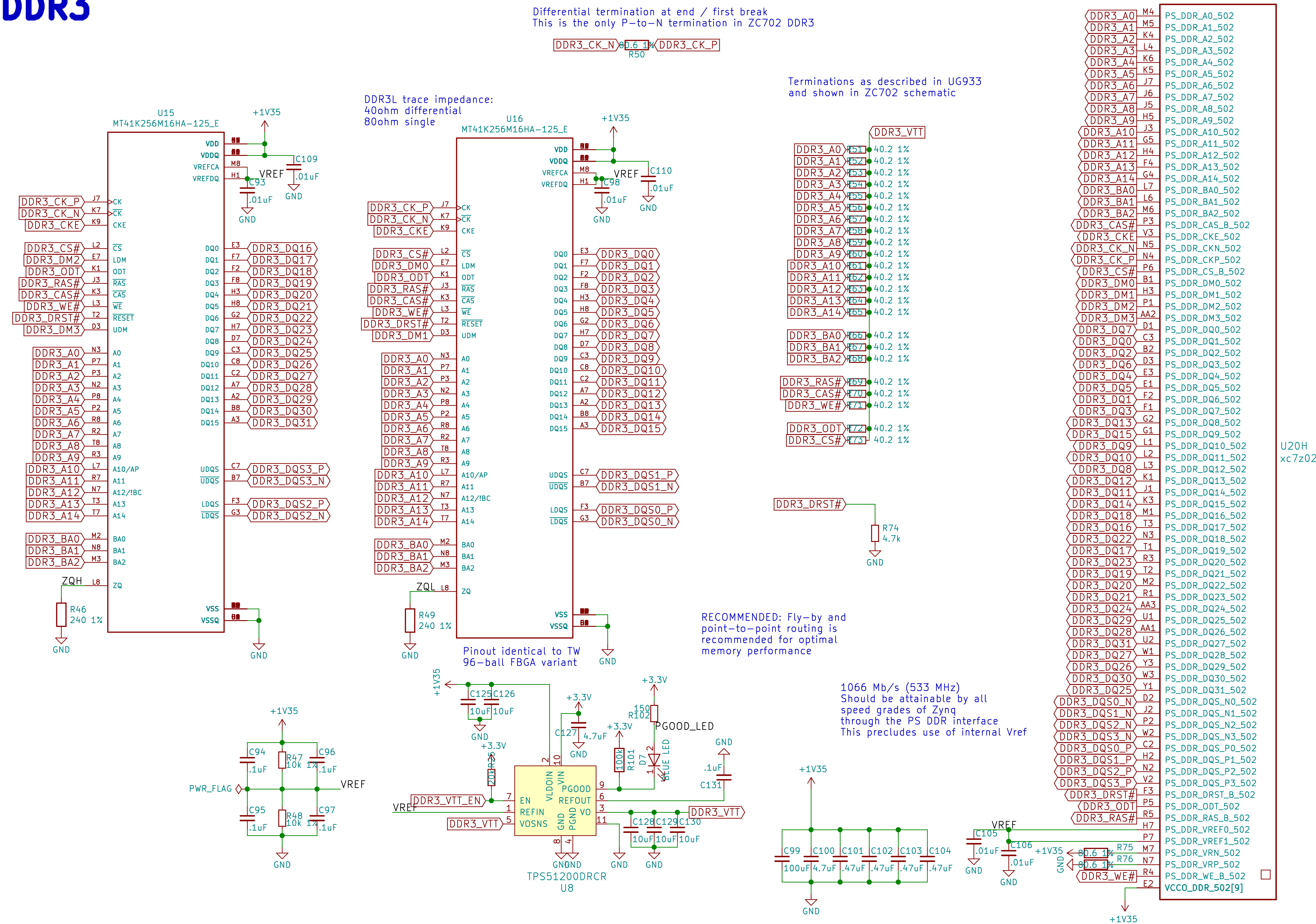
USB Host and Device



Sensors

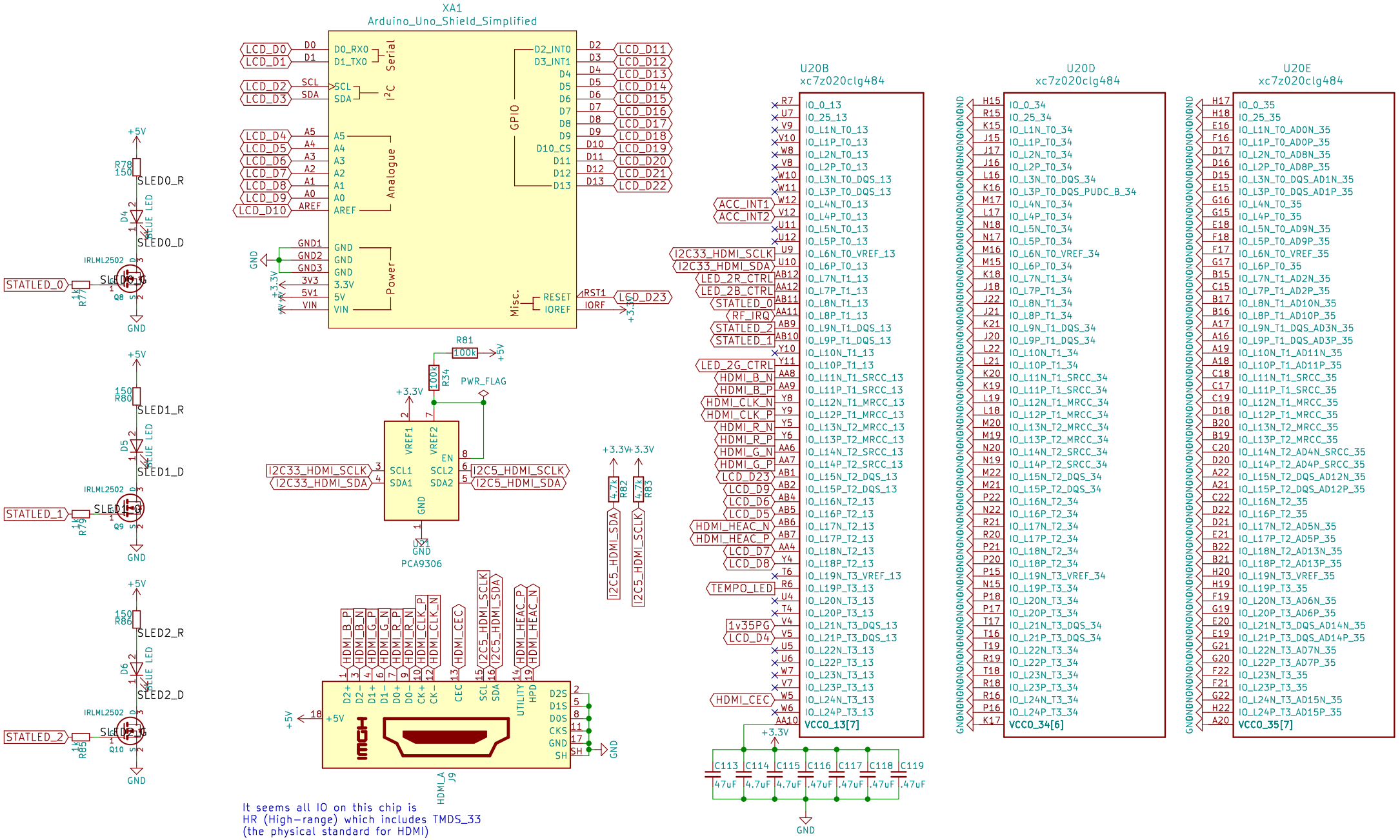

If operating from a single supply, use a 22−Ω resistor in series with the VDD supply line and a 1−µF low ESR capacitor to filter any power supply noise. The previous capacitor placement considerations apply. However note that where LED current is boosted beyond 100mA, it is recommended that the LEDA pin be connected to a separate power supply.
MOVE THESE OUT FROM UNDER SCREEN
VL53L1CXV0FY/1 U13
AVDDVCSEL
AVDD
AVSSVCSEL
GND
XSHUT
GPIO1
SDA
SCL
RF_IRQ
I2C33_SDA
I2C33_SCLK
address 0x52
2V8 mode
C88 .1uF
C89 4.7uF
10k R42
10k R43
PWR_FLAG
R84 47
3.3V_R
U14
VDD
GND
LEDA
LEDK
LDR
INT
SCL
SDA
RF2_IRQ
I2C33_SCLK
I2C33_SDA
APDS−9960
address 0x39
10uF C90
1uF C91
47 R87
1uF C92
U22
TSOP344
OUT
GND
Vs
IR_RX
C111 .01uF
R44 10k
SW1
TL6215RF200BDT
TEMPO_SW
TEMPO_LED_D
TEMPO_LED_R
150 R45
+5V
IRLML2502
TEMPO_LED
Q7
U6
LIS2MDTR12
Vdd
Vdd_IO
CS
SDA/SDI
SAO/SDO
SCL/SPC
INT1
INT2
RES
ACC_INT1
ACC_INT2
address 0x17
C16 .1uF
C21 4.7uF
C107 .1uF
Mode 1: no master i2c
SDO/SAO
SDX
SCX
VDDIO
VDD
INT1
INT2
IMU_INT1
IMU_INT2
U23
LSM6DSLTR
address 0x6A

DDR3



Differential termination at end / first break
This is the only P-to-N termination in ZC702 DDR3
DDR3L trace impedance:
40ohm differential
80ohm single
Terminations as described in UG933
and shown in ZC702 schematic
U15
MT41K256M16HA-125_E
U16
MT41K256M16HA-125_E
Pinout identical to TW
96-ball FBGA variant
RECOMMENDED: Fly-by and
point-to-point routing is
recommended for optimal
memory performance
1066 Mb/s (533 MHz)
Should be attainable by all
speed grades of Zynq
through the PS DDR interface
This precludes use of internal Vref
TPS51200DRCR
U8
U20H
xc7z02
PWR_FLAG
VREF
PGOOD_LED
BLUE LED
DDR3_VTT
+1V35
+3.3V
GND

LCD and Status LEDs



Non-volatile memory