Zynq Evaluation and Development Board

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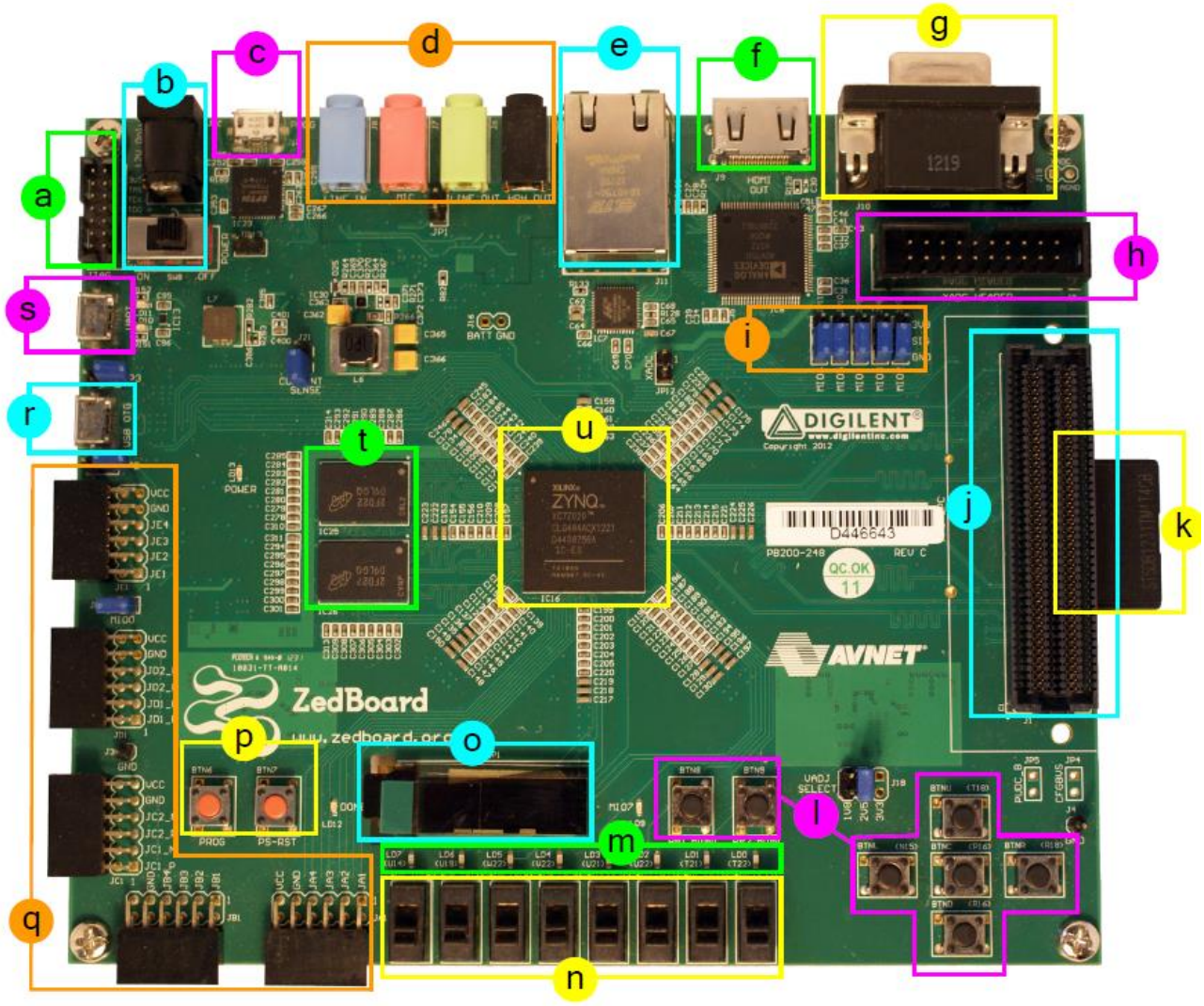
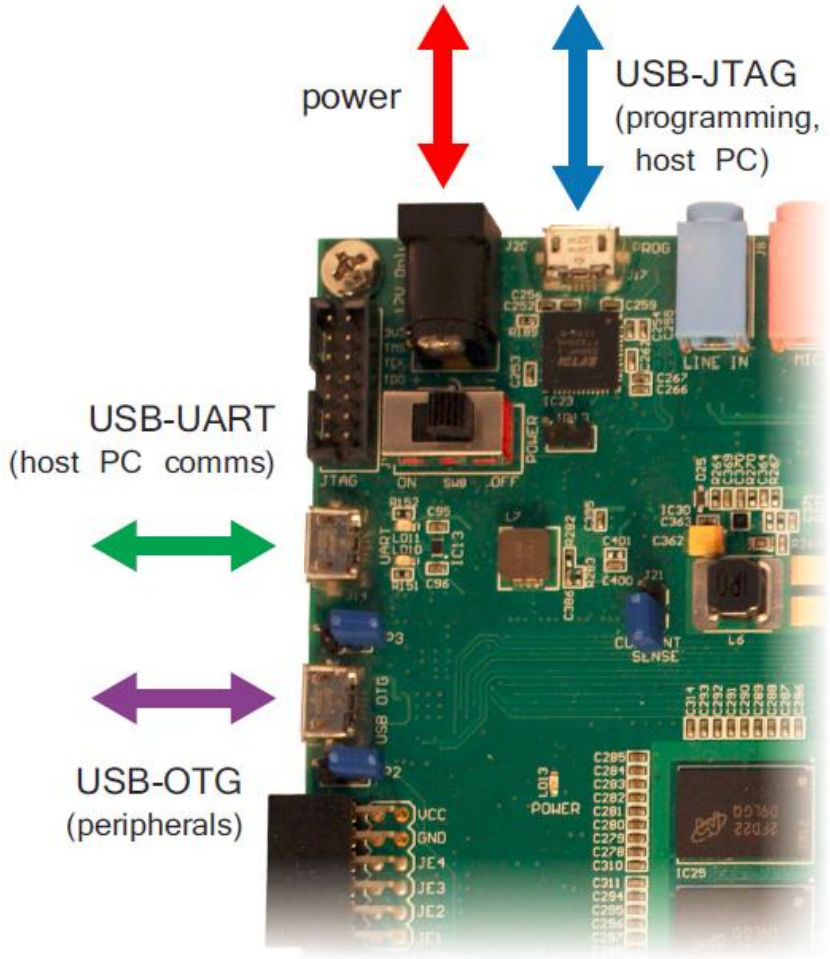
ZedBoard Main Components

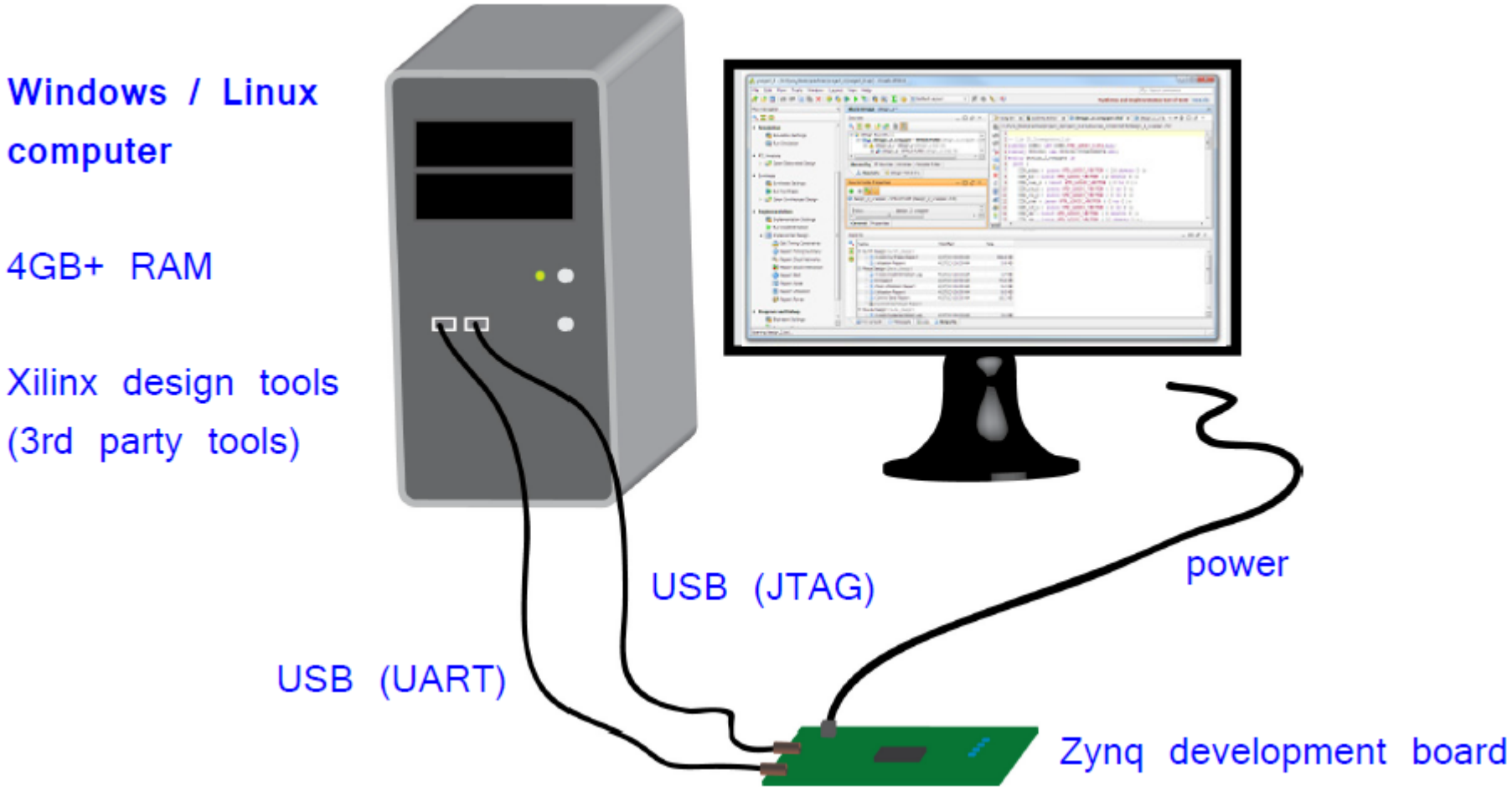


- a Xilinx JTAG connector
- b Power input and switch
- c USB-JTAG (programming)
- d Audio ports
- e Ethernet port
- f HDMI port (output)
- g VGA port
- h XADC header port
- i Configuration jumpers
- j FMC connector
- k SD card (underside)
- l User push buttons
- m LEDs
- n Switches
- o OLED display
- p Prog & reset push buttons
- q 5 x Pmod connector ports
- r USB-OTG peripheral port
- s USB-UART port
- t DDR3 memory
- u Zynq device (+ heatsink)

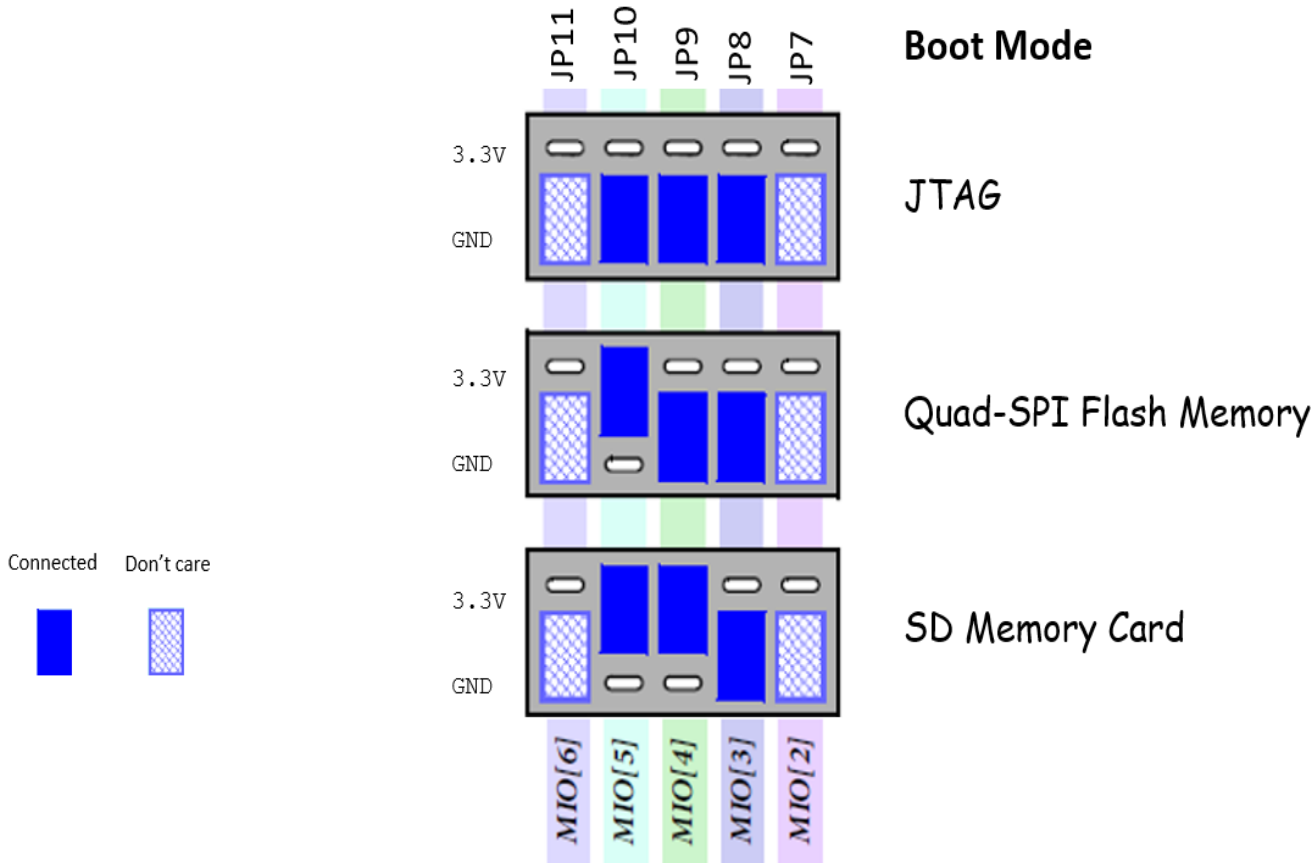
ZedBoard Main Connectors to be Used



Conection Between PC-ZedBoard



Programming the ZedBoard



DRAM Memory

- 512 Mbytes DDR3 connected to the PS part of the Zynq
  - The DDR3 is controled by the DRAM Controller
- It is posible to add more memory to the PL part using the Memory Interface Generator (MIG), for example using a daughter card connected to the FMC connector.
- PS DDR Bandwidth
  - By default the DDR Controller clock is 533MHz
  - Total Bw: 4 * 533 * 2 = 4.2 GB/s

256 Mbit- Serial NOR Flash

PMOD

10/100/1000 Ethernet Phy

USB OTG

SD Card

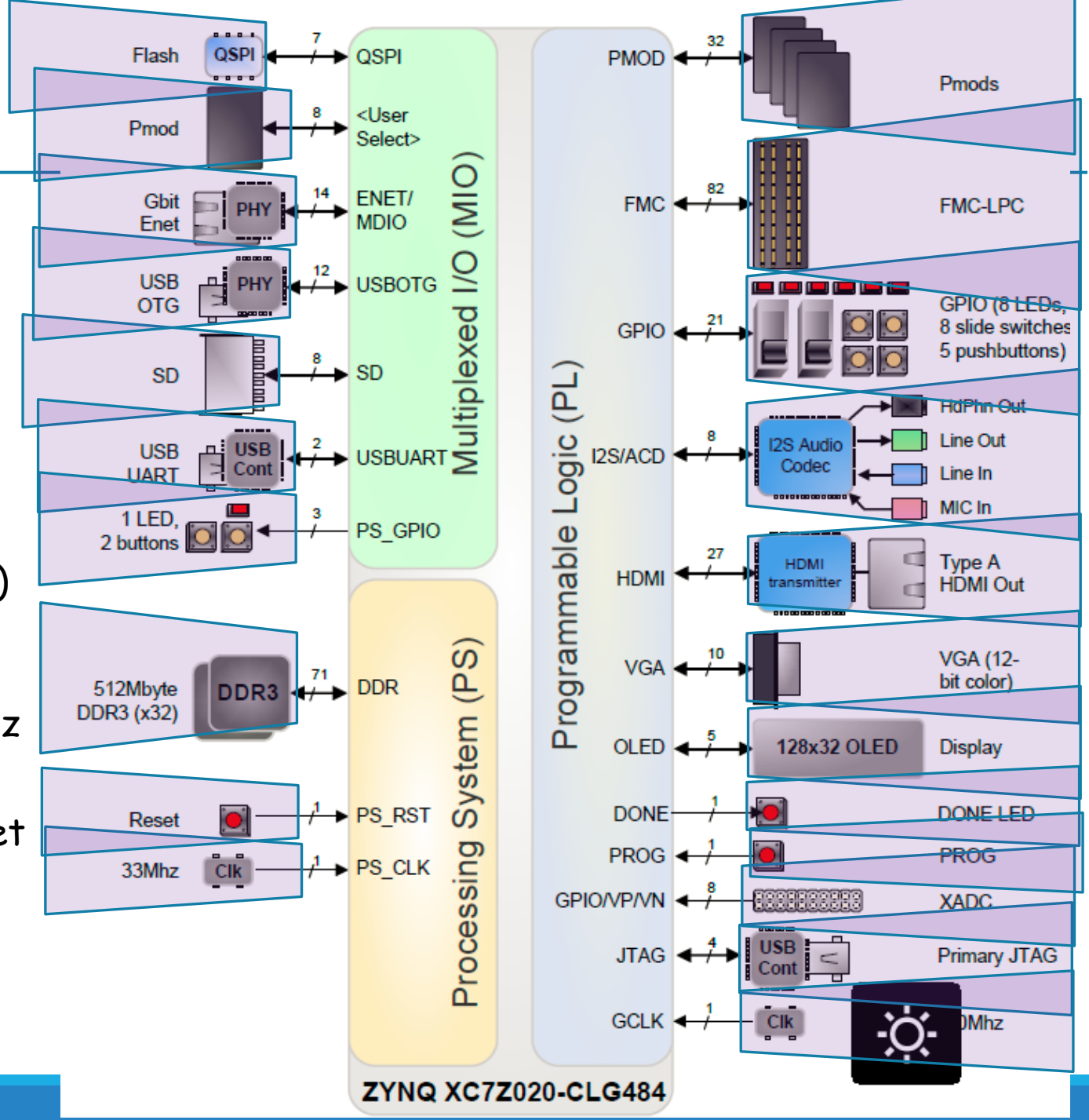
USB-UART

LD9 (PS)
Buttons (PS)

512MB (32 bits)533MHz

Processor Subsystem Reset

Clock



PMOD

LPC FMC Connector

68 Single Ended
34 Differential

LEDs (8)

User I/O

Push Buttons(5)

DIP Switch(8)

AUDIO

HDMI

VGA

OLED

Done Blue LED

Program Push Button

Analog Mixed Signaling (AMS) Connector

USB-JTAG

PL Clock Source
100MHz

ZedBoard Hardware User Guide

ZedBoard

(Zynq™ Evaluation and Development) Hardware User's Guide

Version 2.2
27 January 2014

ZedBoard Clock Sources

2.5 Clock sources

The Zynq-7000 AP SoC's PS subsystem uses a dedicated 33.3333 MHz clock source, IC18, Fox 767-33.333333-12, with series termination. The PS infrastructure can generate up to four PLL-based clocks for the PL system. An on-board 100 MHz oscillator, IC17, Fox 767-100-136, supplies the PL subsystem clock input on bank 13, pin Y9.

ZedBoard Available I/O for the User (1)

2.7 User I/O

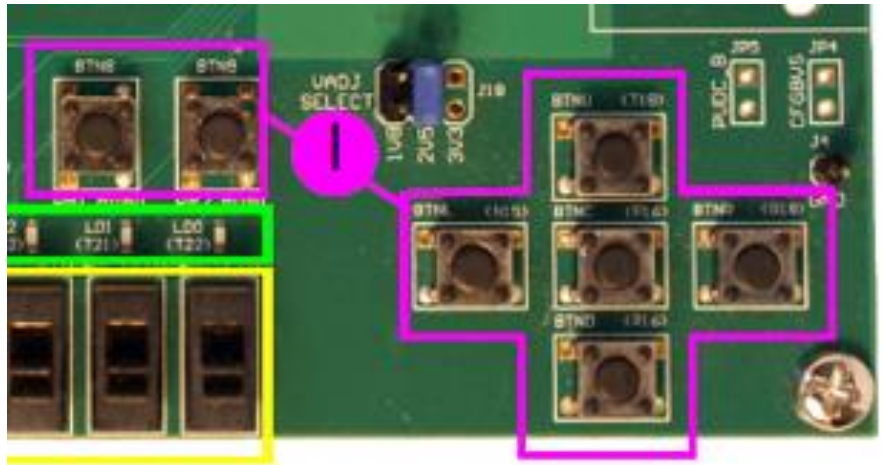
2.7.1 User Push Buttons

The ZedBoard provides 7 user GPIO push buttons to the Zynq-7000 AP SoC; five on the PL-side and two on the PS-side.

Pull-downs provide a known default state, pushing each button connects to Vcco.

Table 12 - Push Button Connections

Signal Name	Subsection	Zynq pin
BTNU	PL	T18
BTNR	PL	R18
BTND	PL	R16
BTNC	PL	P16
BTNL	PL	N15
PB1	PS	D13 (MIO 50)
PB2	PS	C10 (MIO 51)



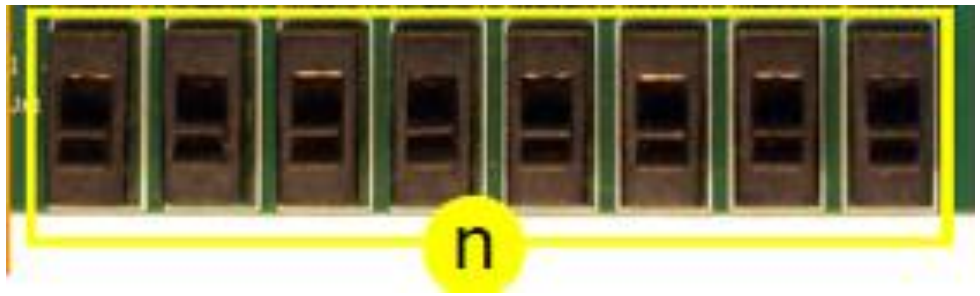
ZedBoard Available I/O for the User (2)

2.7.2 User DIP Switches

The ZedBoard has eight user dip switches, SW0-SW7, providing user input. SPDT switches connect the I/O through a 10kΩ resistor to the VADJ voltage supply or GND.

Table 13 - DIP Switch Connections

Signal Name	Zynq pin
SW0	F22
SW1	G22
SW2	H22
SW3	F21
SW4	H19
SW5	H18
SW6	H17
SW7	M15



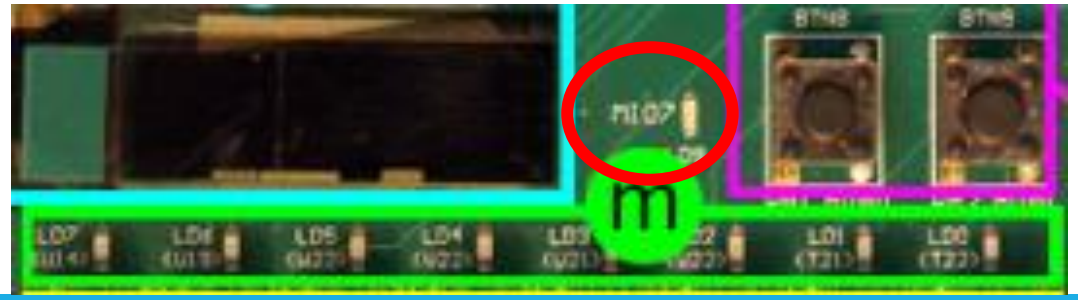
ZedBoard Available I/O for the User (3)

2.7.3 User LEDs

The ZedBoard has eight user LEDs, LD0 – LD7. A logic high from the Zynq-7000 AP SoC I/O causes the LED to turn on. LED's are sourced from 3.3V banks through 390Ω resistors.

Table 14 - LED Connections

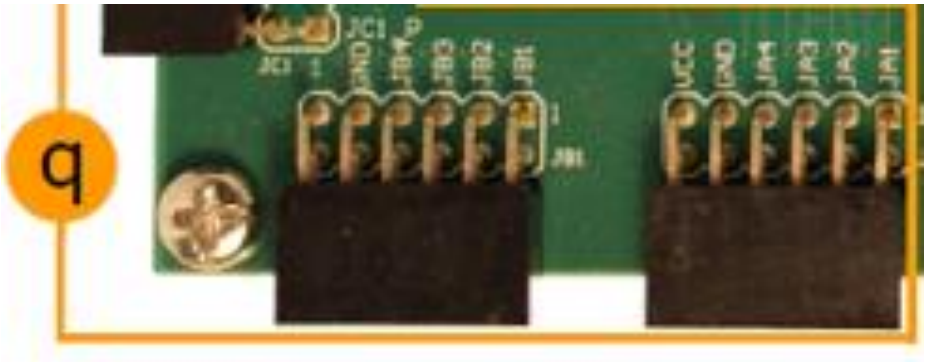
Signal Name	Subsection	Zynq pin
LD0	PL	T22
LD1	PL	T21
LD2	PL	U22
LD3	PL	U21
LD4	PL	V22
LD5	PL	W22
LD6	PL	U19
LD7	PL	U14
LD9	PS	D5 (MIO7)

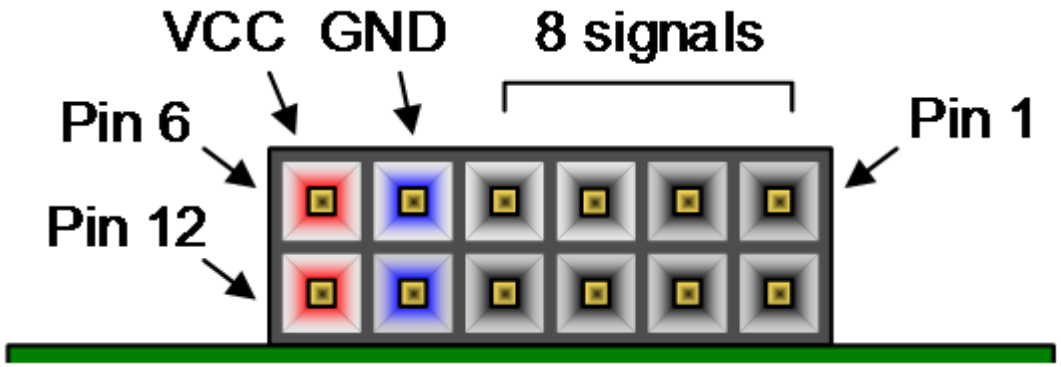


ZedBoard PMOD Connectors

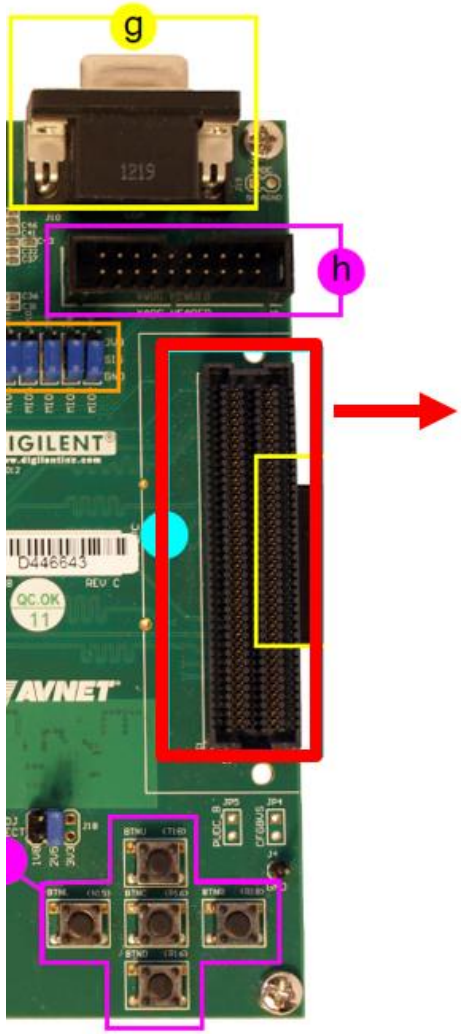
Table 16 - Pmod Connections

Pmod	Signal Name	Zynq pin	Pmod	Signal Name	Zynq pin
JA1	JA1	Y11	JB1	JB1	W12
	JA2	AA11		JB2	W11
	JA3	Y10		JB3	V10
	JA4	AA9		JB4	W8
	JA7	AB11		JB7	V12
	JA8	AB10		JB8	W10
	JA9	AB9		JB9	V9
	JA10	AA8		JB10	V8





ZedBoard Expansion Headers: LPC FMC Card Connector



- **LPC FMC** : Low Pin Count (LPC) FPGA Mezzanine Card Connector
  - 68 single-ended I/O or 34 differential pairs
  - J18 defines the power for the connector: 1.8V by default.
  - The FMC pin out can be copied from the Master UCF

Thanks !!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