

Diseño Digital Avanzado

Instalación de Vitis 2023.1

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Tabla de Contenidos

1. Instalación de Vitis/Vivado

2. Test de Vivado

Instalación de Vitis/Vivado

Instalación de Vitis/Vivado

Xilinx - Vitis Core Development Kit - 2023.1

- Acceder al siguiente link y descargar el instalador web dependiendo del sistema operativo (Windows o Linux).
 - <https://www.xilinx.com/support/download.html>
- Se debe crear un usuario en Xilinx para poder descargar el instalador.
(<https://www.xilinx.com/registration/create-account.html>)
- Despues de descargar el instalador y ejecutarlo dependiendo del SO:
 - Windows: se puede ejecutar directamente el archivo **Xilinx_Unified_2023.1_0507_1903_Win64.exe**
 - Linux: se debe dar permisos de ejecución antes de ejecutar el instalador:
`chmod +x Xilinx_Unified_2023.1_0507_1903_Lin64.bin`
`sudo ./Xilinx_Unified_2023.1_0507_1903_Lin64.bin`
- Ver pasos de instalación en Pag. 5-12

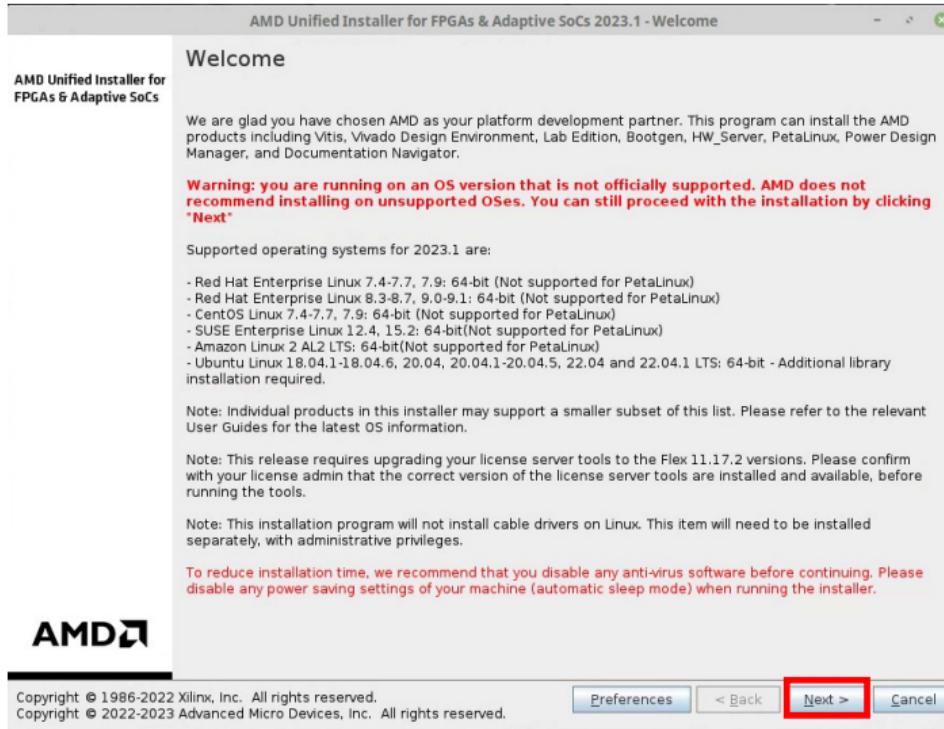
Instalación de Vitis/Vivado

The screenshot shows the AMD Xilinx Downloads page. At the top, there are navigation links for Products, Solutions, Downloads & Support, and a search bar. Below the header, a breadcrumb trail shows the current location: Home / Adaptive Computing Support / Downloads. The main section is titled "Downloads". A dropdown menu is open, showing options like Licensing Help and NIC Software & Drivers. Below this, a sub-menu for "Vivado (HW Developer)" is highlighted. Other options in the sub-menu include Vivado (SW Developer), Vivado Embedded Platforms, Power Design Manager, Alveo Packages, PetaLinux, Device Models, Documentation, and Navigator. On the left, a sidebar lists versions: 2023.1 (highlighted), 2022.2, 2022.1, Vivado Archive, ISE Archive, and CAE Vendor Libraries Archive. The central content area displays the "Vivado ML Edition - 2023.1 Full Product Installation" page. It features an "Important Information" section with a red background and white text, stating: "Vivado™ ML 2023.1 is now available for download: Average QoR Improvement of 8% for Versal™ Adaptive SoCs and 13% for UltraScale+ FPGAs using Intelligent Design Runs; Extending multithreading support for bitstream generation for Versal devices; Enhancements in Report QoR Assessment (RQA); Power Design Manager (PDM) now a part of Unified Installer – Separate from Vivado tool; Added support for Versal HBM devices in Power Design Manager (PDM). We strongly recommend to use the web installers as it reduces download time and saves significant disk space." To the right of this section, there is a table of contents for the installation package:

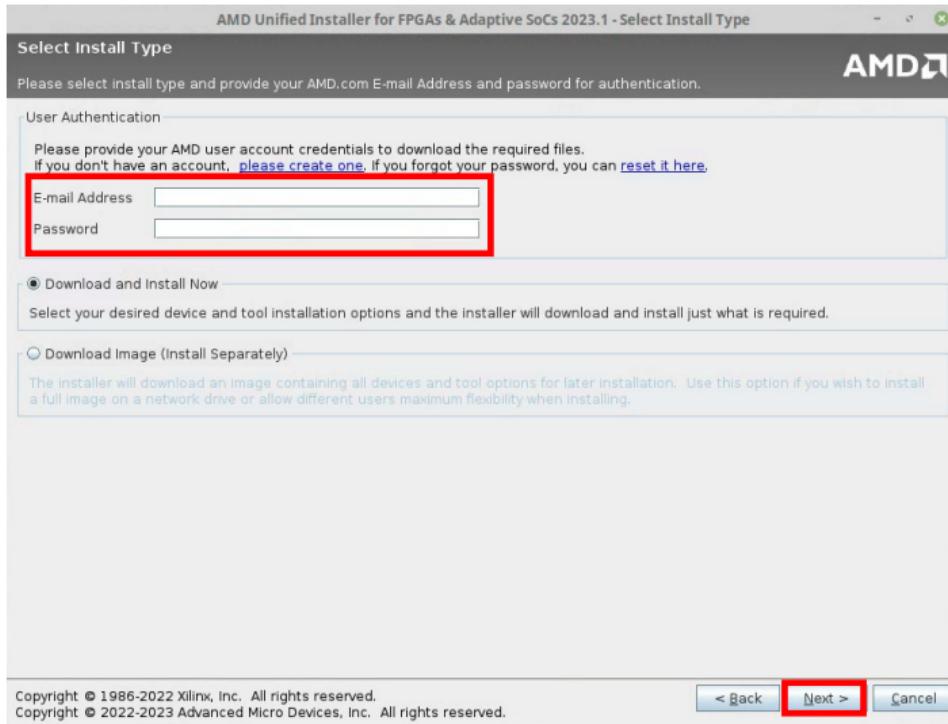
Download Includes	Vivado ML Edition
Download Type	Full Product Installation
Last Updated	May 17, 2023
Answers	2023.x - Vivado Known Issues
Documentation	Release Notes OS Support Update What's New in Vivado
Support Forums	Installation and Licensing

The screenshot shows the AMD Unified Installer download verification page. It features a large red box highlighting the download link for the "AMD Unified Installer for FPGAs & Adaptive SoCs 2023.1: Linux Self Extracting Web Installer (BIN - 265.94 MB)". Below this, the MD5 SUM Value is listed as e47ad71388b27a6e2339ee82c3c8765f. The page also includes a "Download Verification" section with three buttons: Digests, Signature, and Public Key.

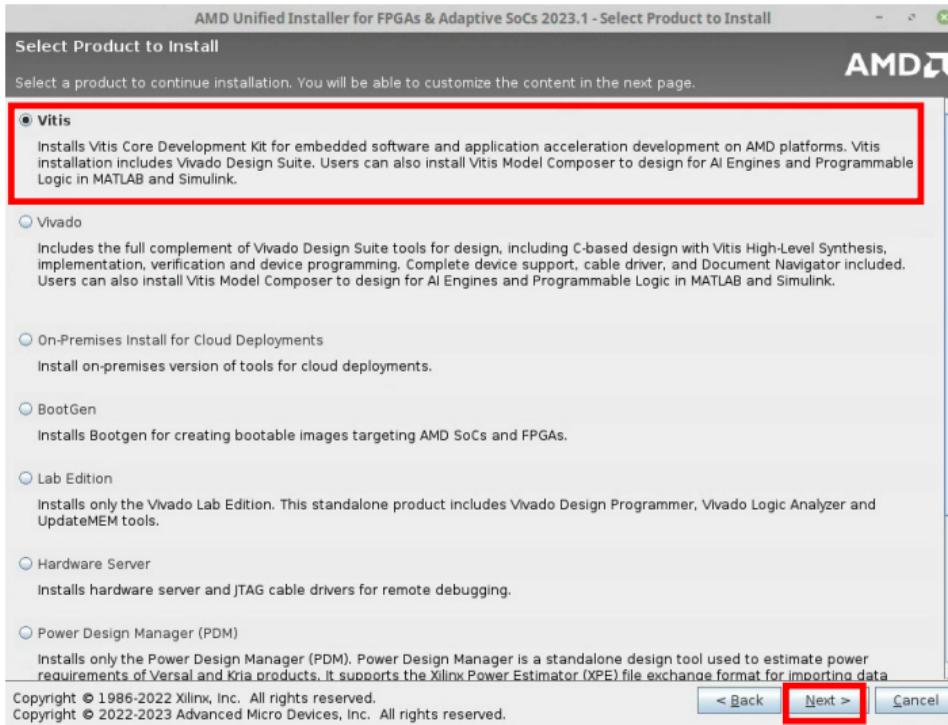
Instalación de Vitis/Vivado



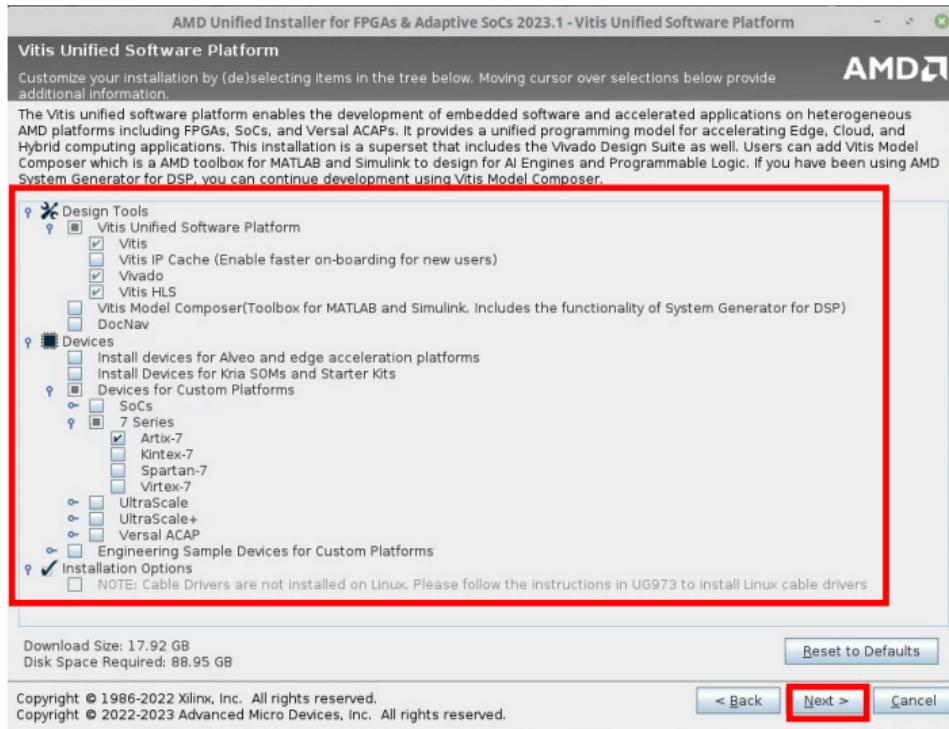
Instalación de Vitis/Vivado



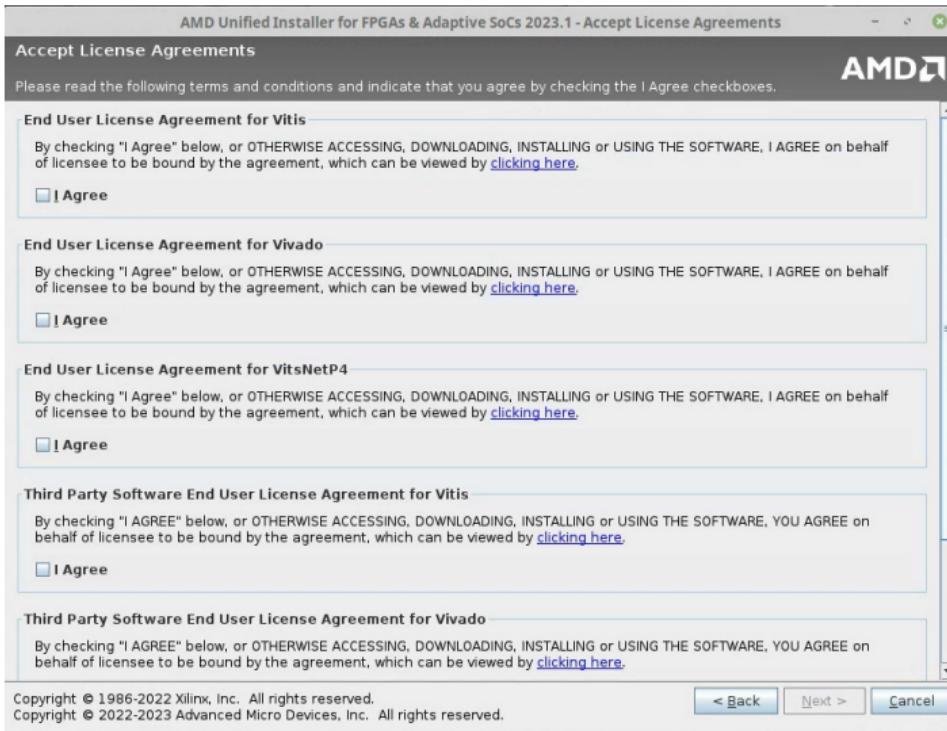
Instalación de Vitis/Vivado



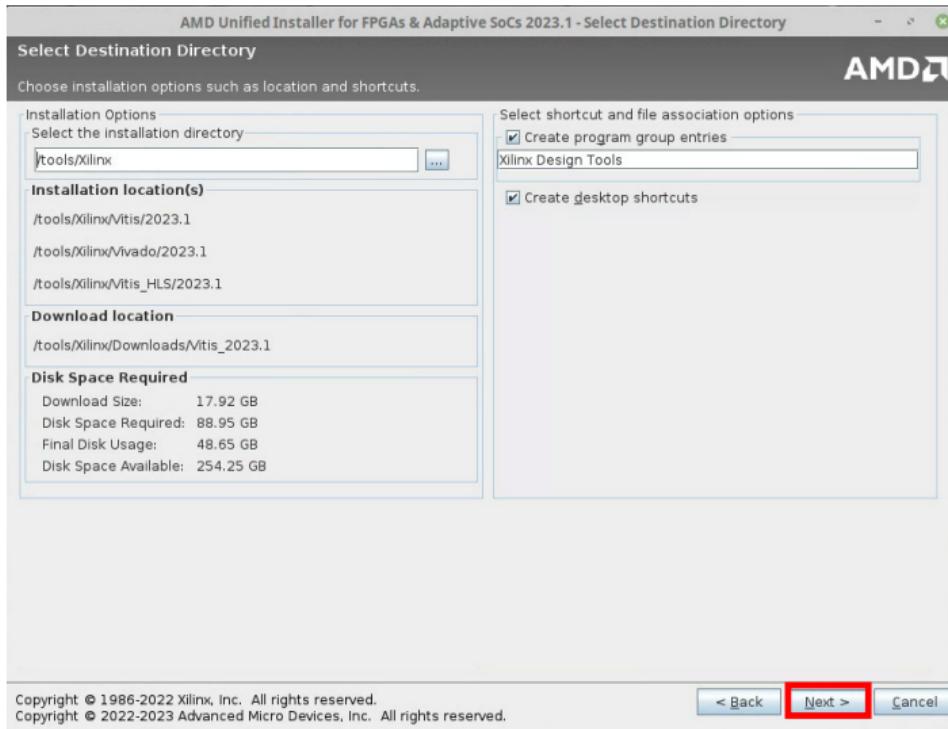
Instalación de Vitis/Vivado



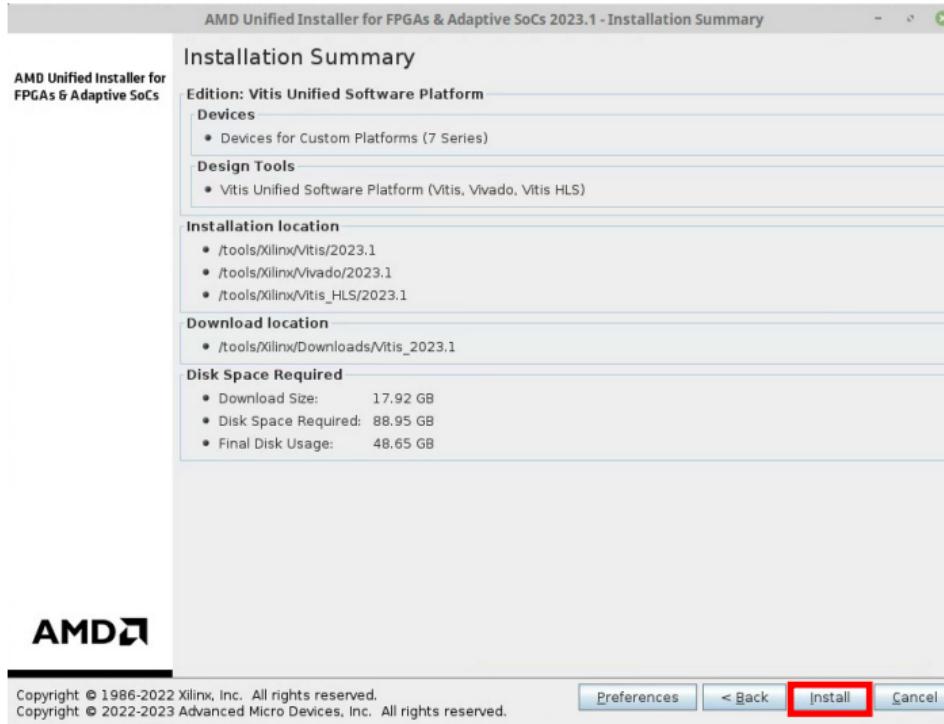
Instalación de Vitis/Vivado



Instalación de Vitis/Vivado



Instalación de Vitis/Vivado



Test de Vivado

Test de Vivado

- Incluir información del Kit de desarrollo en Vivado
 - Ubicar el directorio de instalación **Xilinx/Vivado/2023.1/data/boards/**
 - Descomprimir el archivo **board_files.zip**
 - Copiar el contenido de la carpeta **board_files** a
Xilinx/Vivado/2023.1/data/boards/board_files/
 - Verificar que se encuentre la carpeta del kit a utilizar
Xilinx/Vivado/2023.1/data/boards/board_files/arty-a7-35
- Generar binario de prueba
 - Ejecutar Vivado desde el acceso directo o terminal
 - Crear un proyecto nuevo
 - Seleccionar la placa Arty A7-35
 - Incluir los archivos top_microblaze.v, tb_top_microblaze.v y Arty-A7-35-Master.xdc
 - Simular el diseño y verificar el funcionamiento
 - Generar el binario
 - Los pasos mencionados se detallan en las figuras de las Pag. 16 - 33

Test de Vivado

NOTA

- En caso de tener problemas en la ejecución de la síntesis o simulación en Linux, es conveniente tener como lenguaje principal **en_US.UTF-8**.

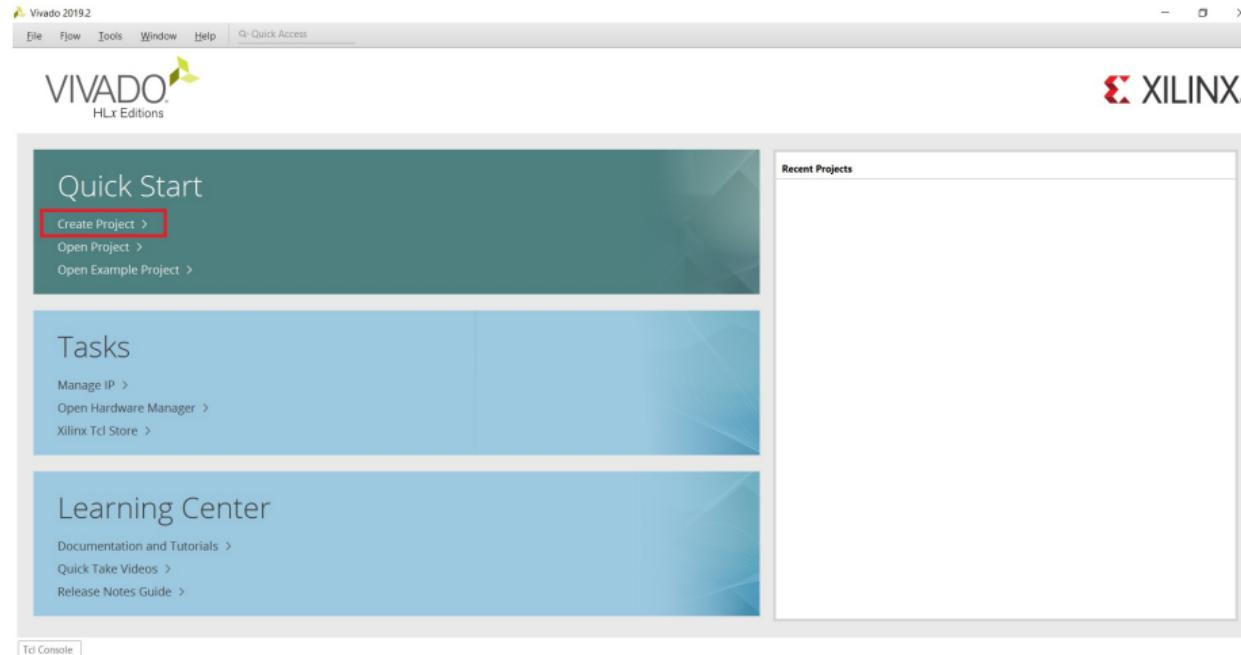
Opción 1 Habilitar **en_US.UTF-8** desde el archivo **locale**.

- `sudo nano /etc/locale.conf`

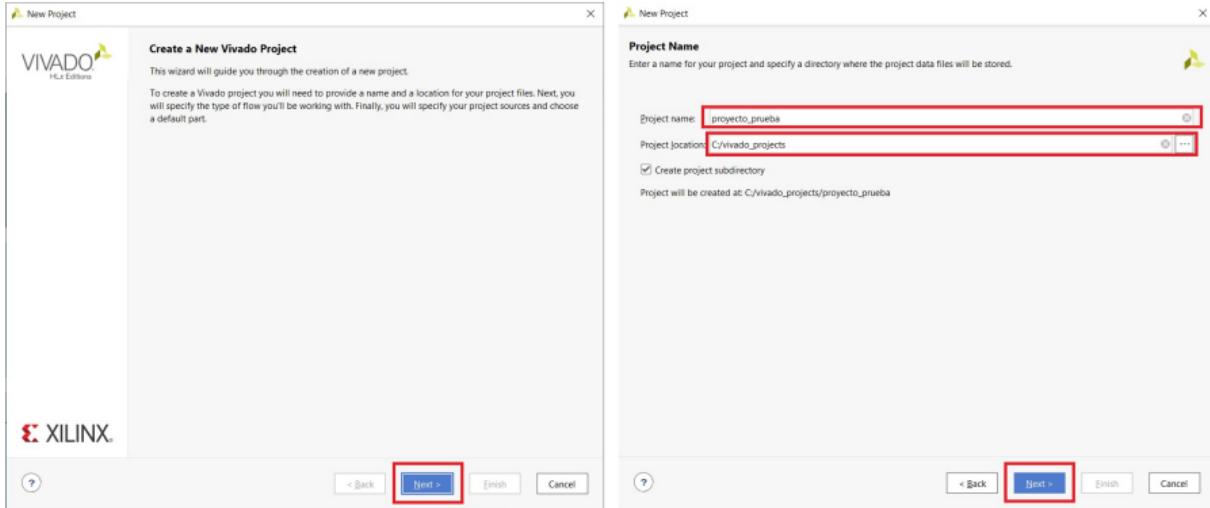
Opción 2 Ejecutar Vivado anteponiendo la definición del lenguaje.

- `LC_ALL=en_US.UTF-8 /tools/Xilinx/Vivado/2023.1/bin/vivado`

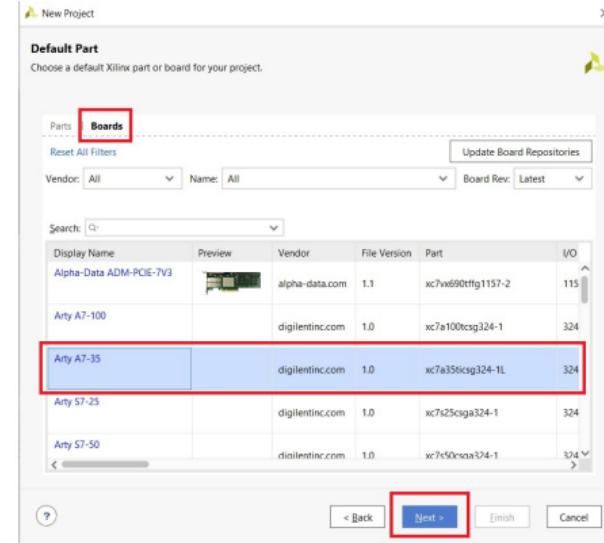
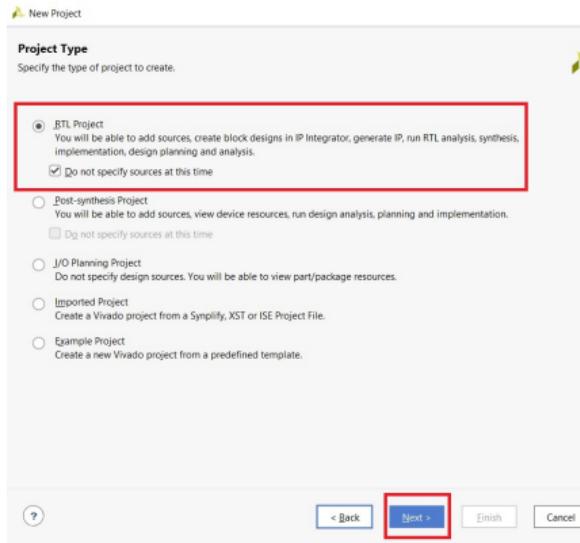
Test de Vivado



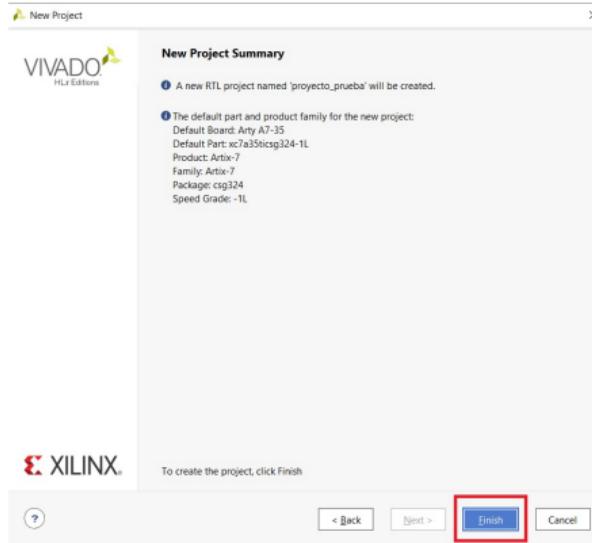
Test de Vivado



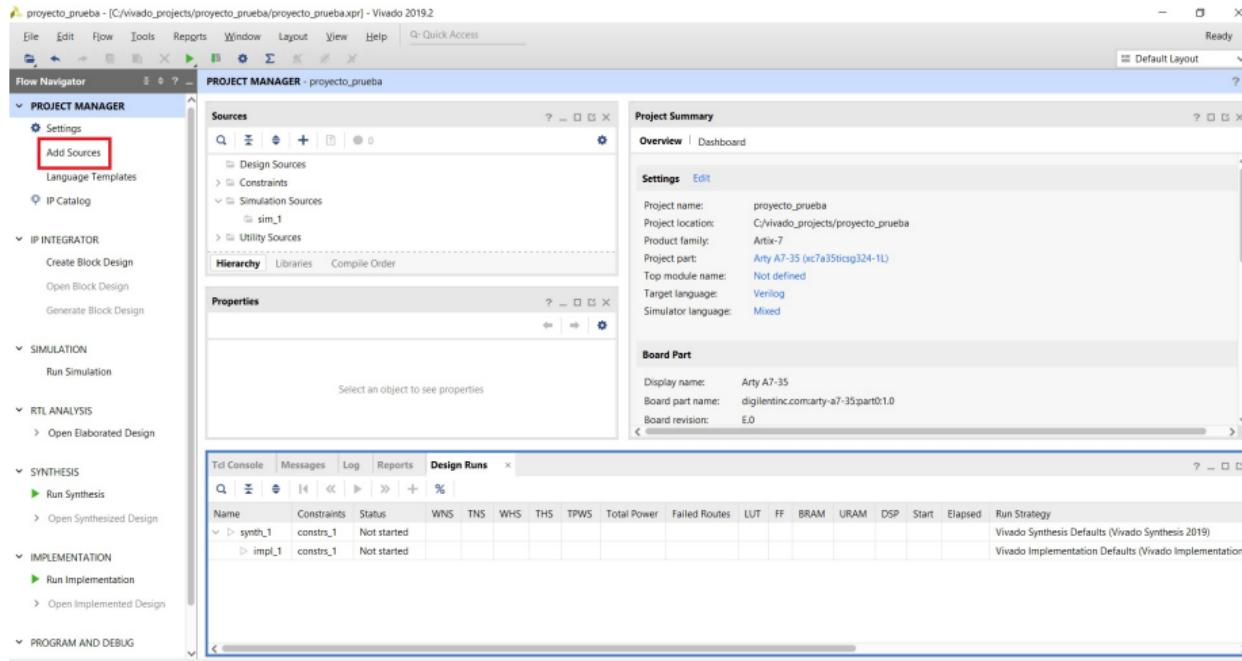
Test de Vivado



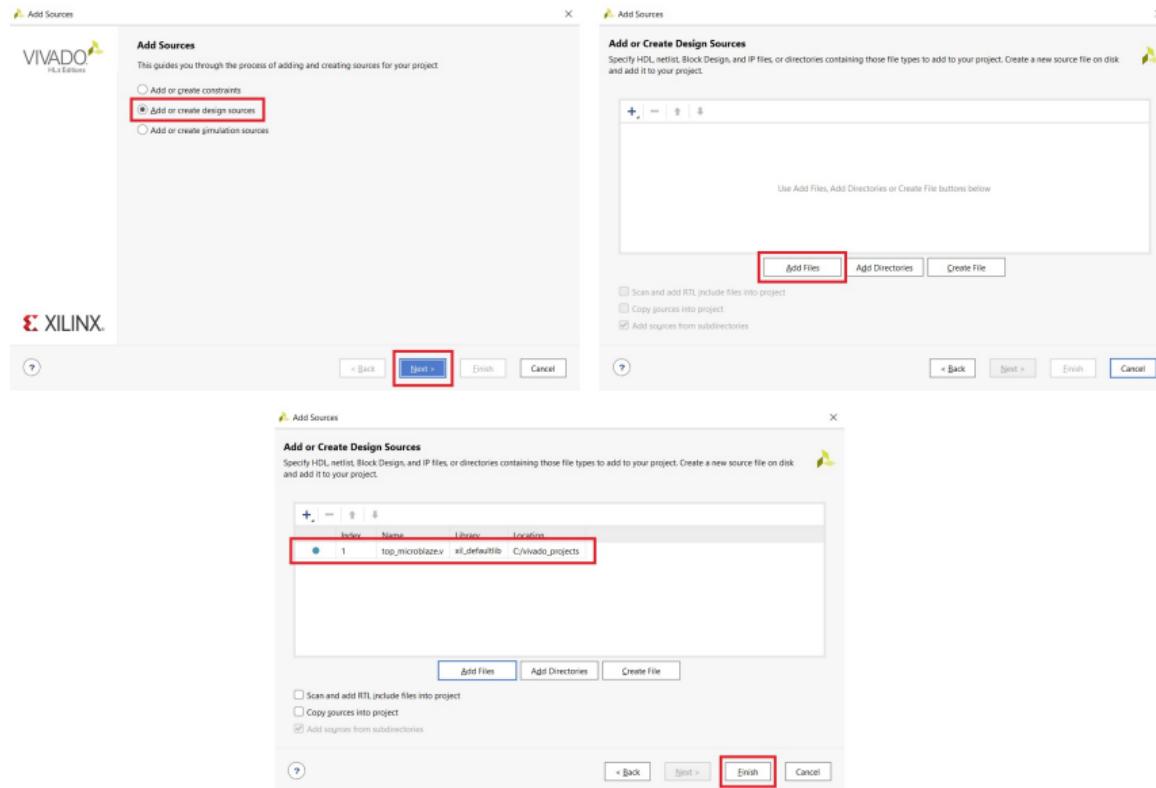
Test de Vivado



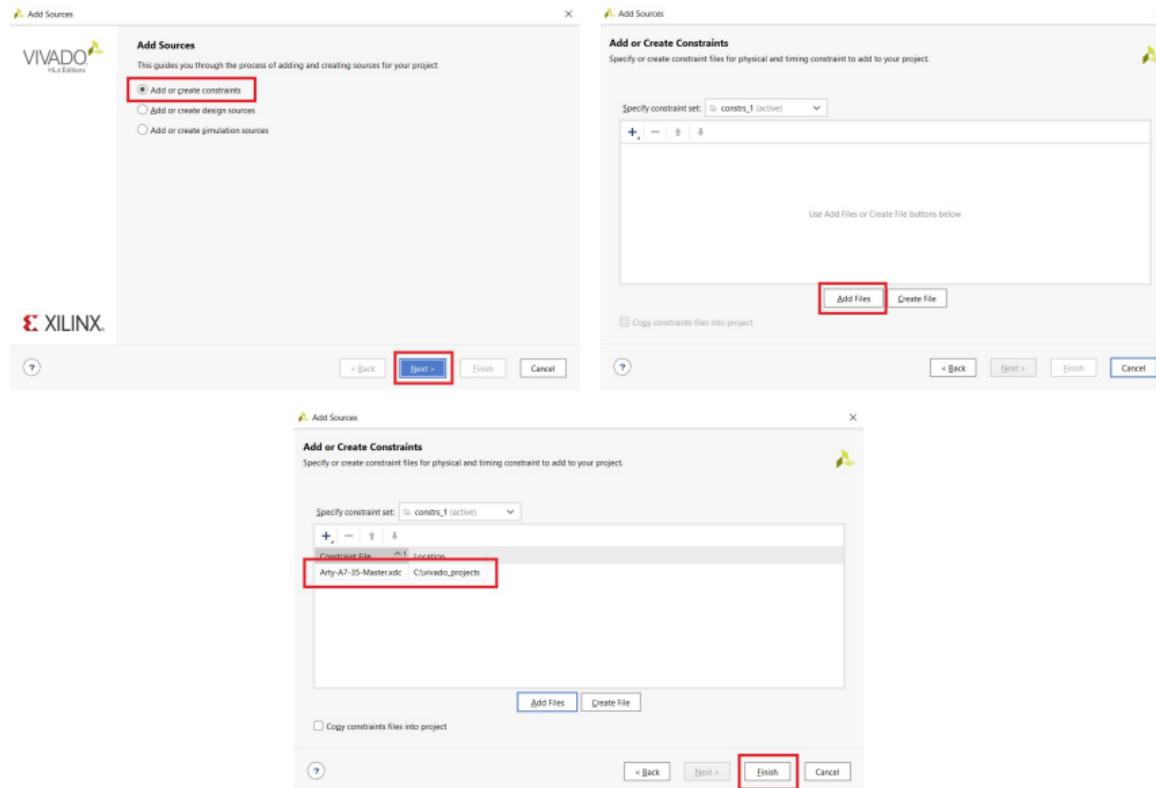
Test de Vivado



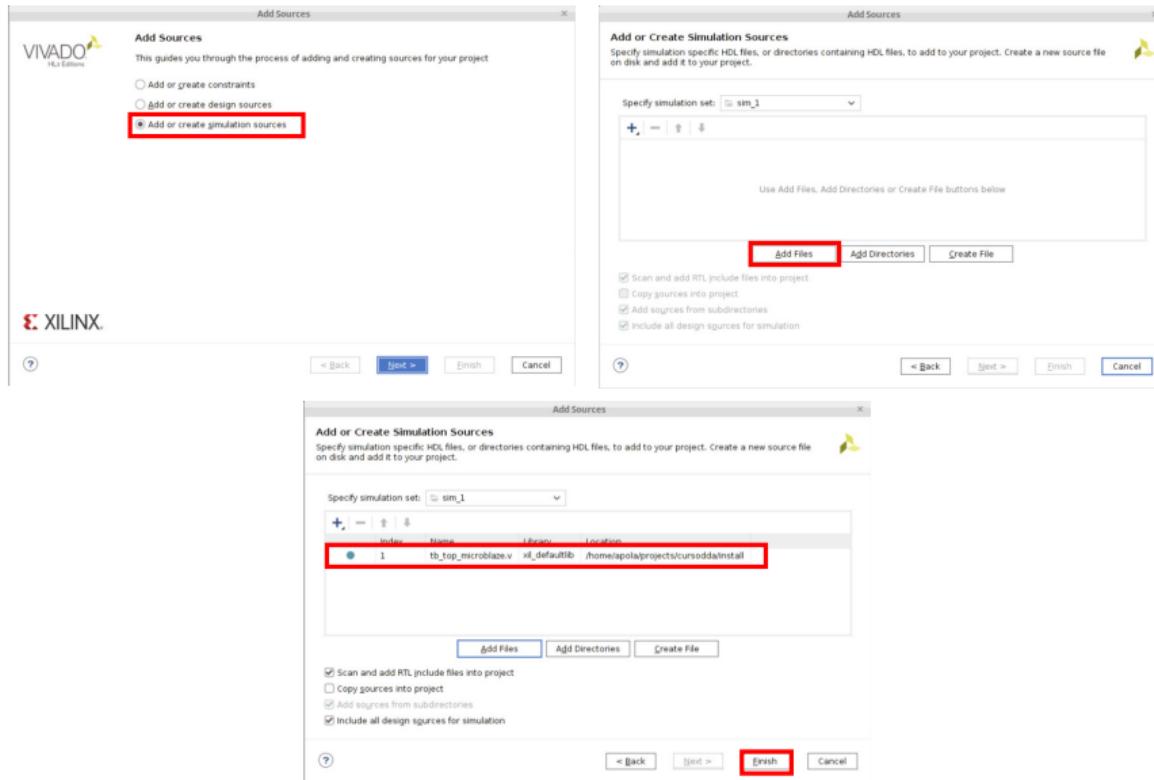
Test de Vivado



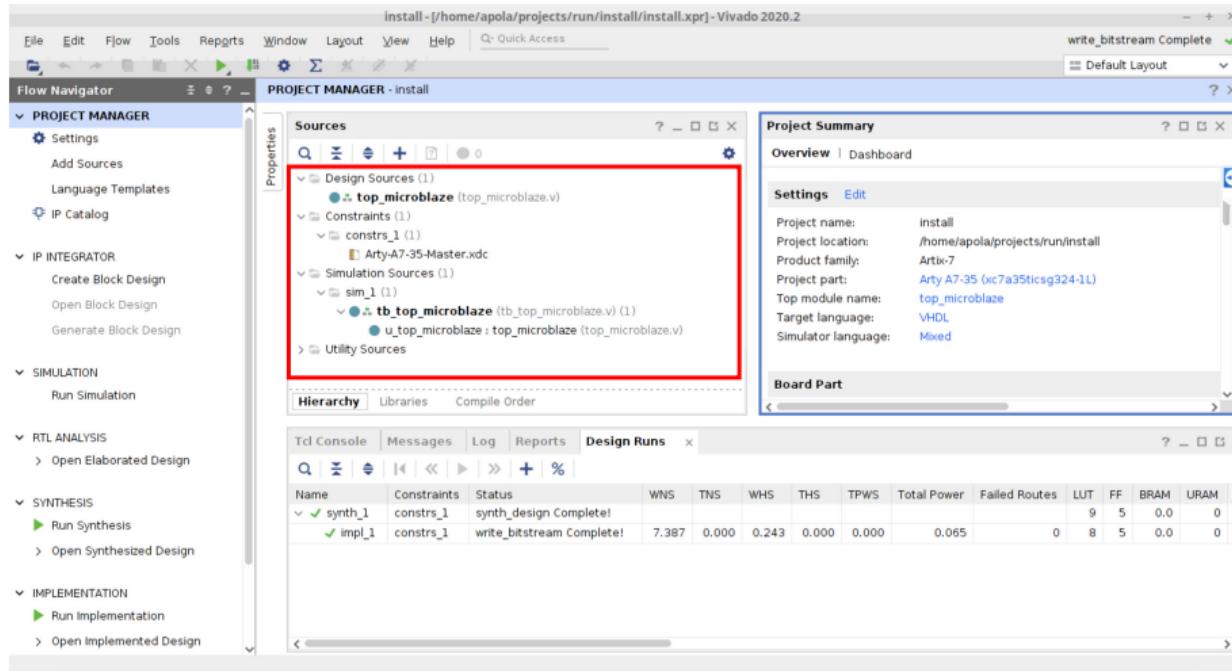
Test de Vivado



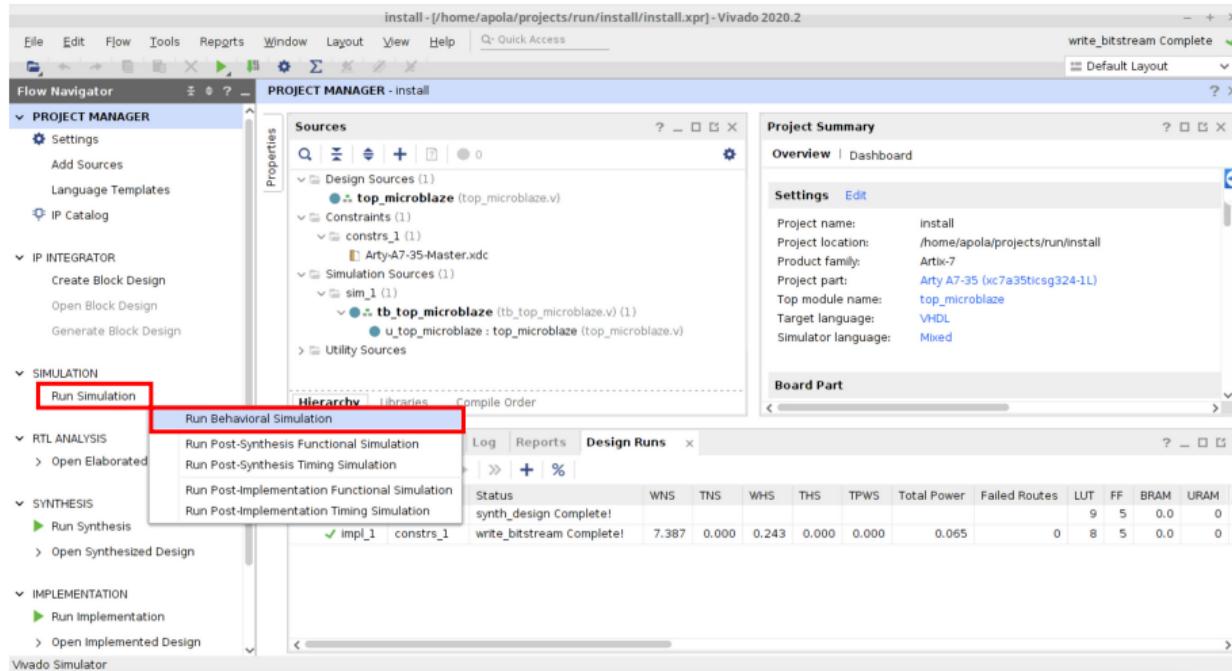
Test de Vivado



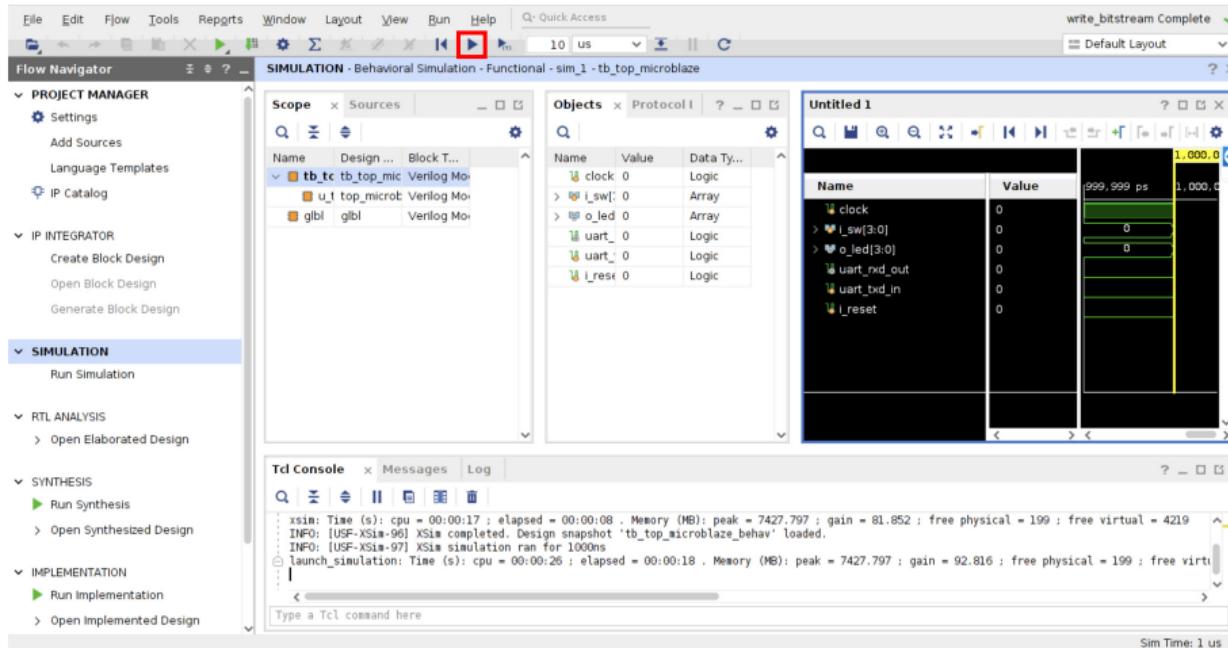
Test de Vivado



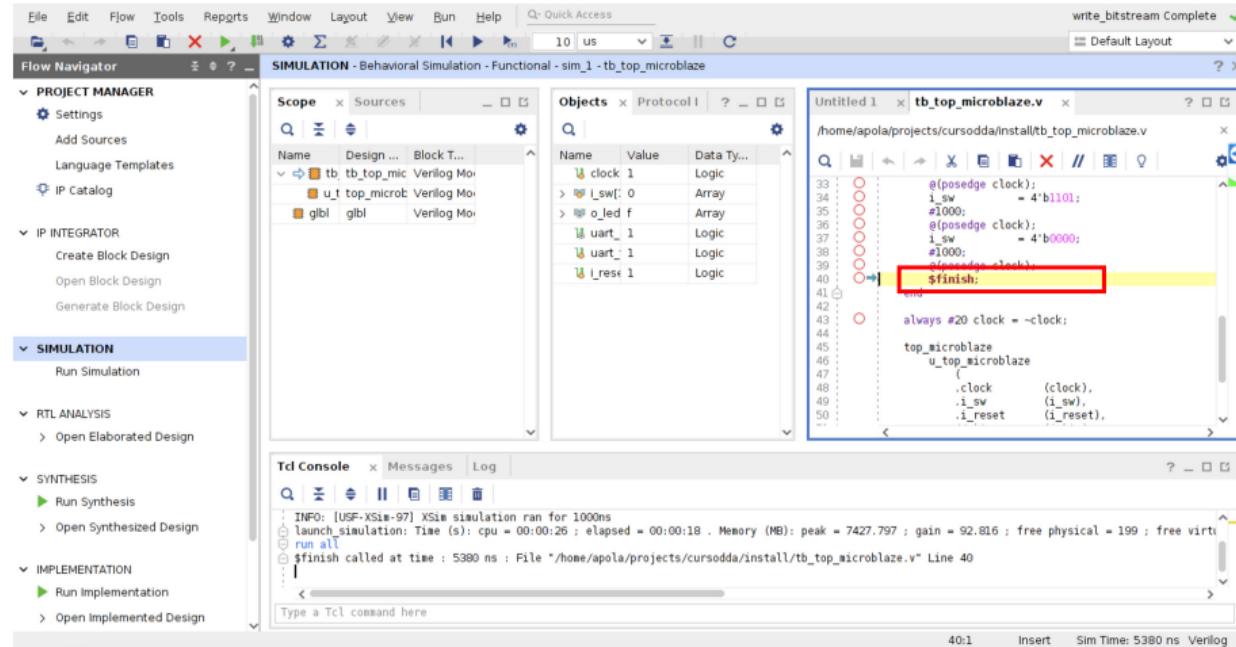
Test de Vivado



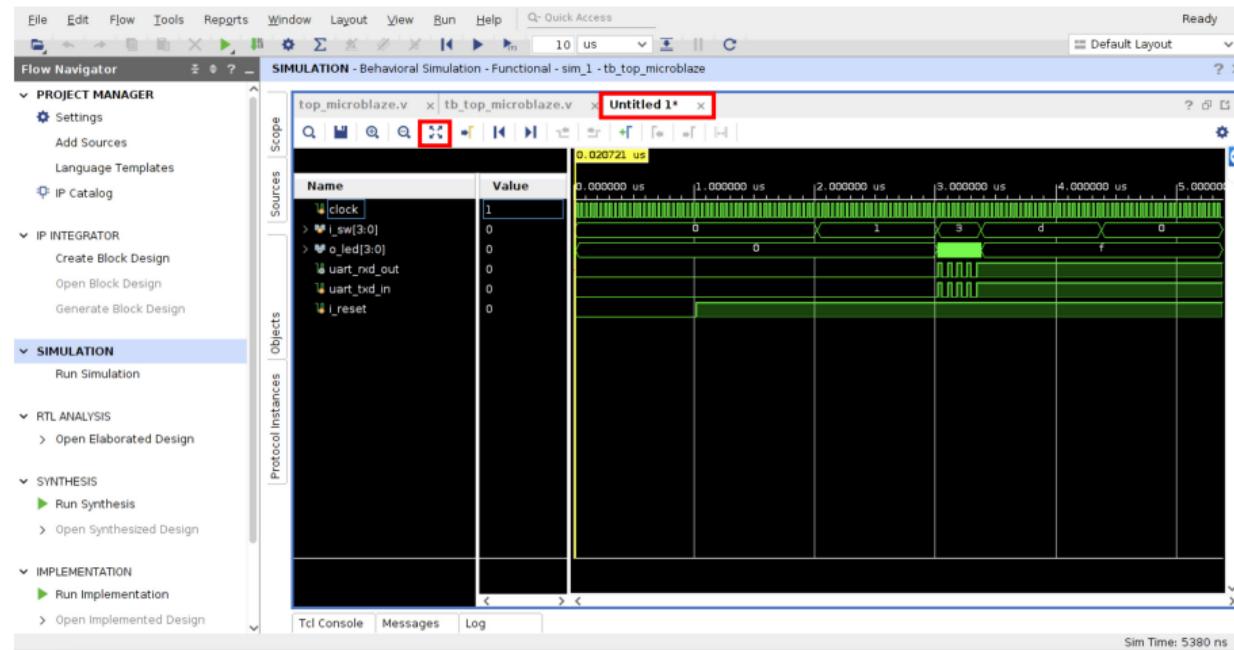
Test de Vivado



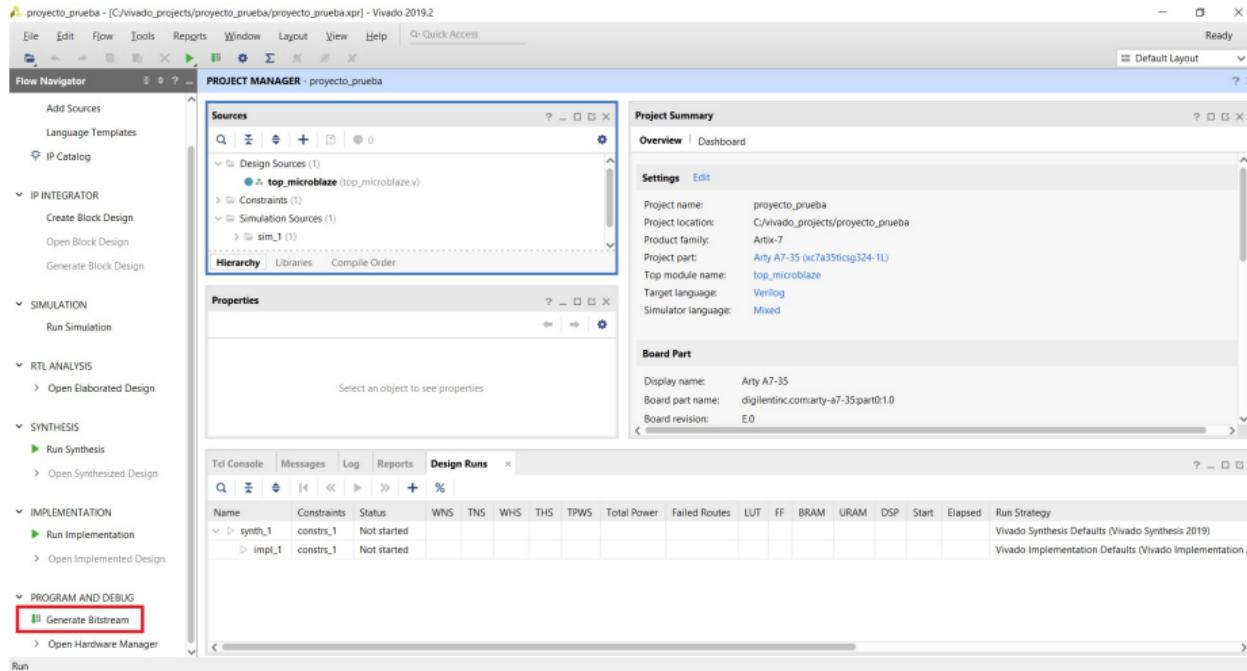
Test de Vivado



Test de Vivado



Test de Vivado



Test de Vivado

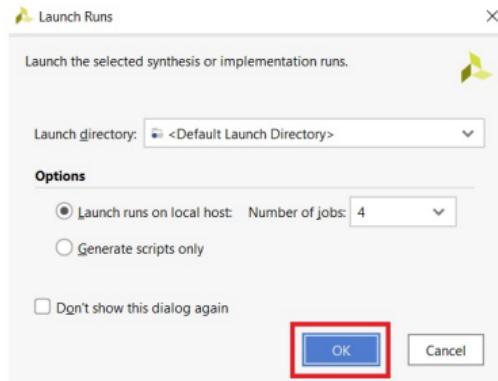
No Implementation Results Available

 There are no implementation results available. OK to launch synthesis and implementation? 'Generate Bitstream' will automatically start when synthesis and implementation completes.

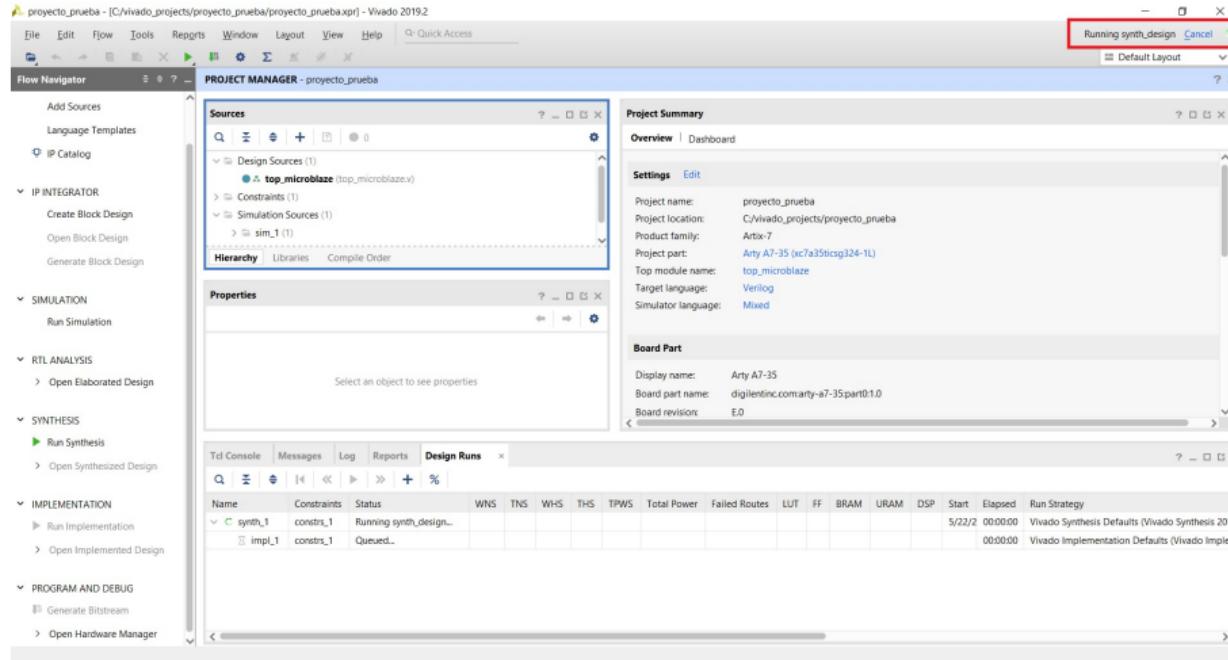
Don't show this dialog again

Yes

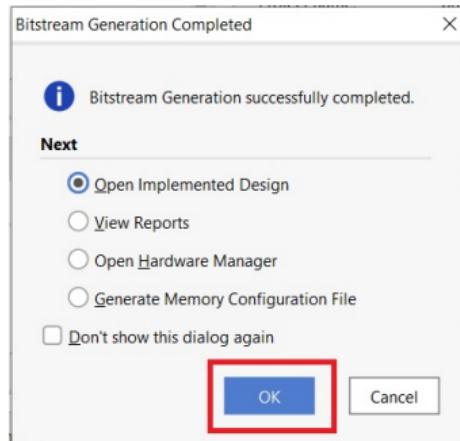
No



Test de Vivado



Test de Vivado



Test de Vivado

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access write_bitstream Complete ✓ Default Layout

Flow Navigator

- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic
 - PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

IMPLEMENTED DESIGN - xc7a35ticsg324-1L

Sources Netlist Project Summary Device top_microblaze.v tb_top_microblaze.v

Source File Properties Arty-A7-35-Master.xdc General Properties

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 7.387 ns	Worst Hold Slack (WHS): 0.243 ns	Worst Pulse Width Slack (WPWS):
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWNS):
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints:
Total Number of Endpoints: 5	Total Number of Endpoints: 5	Total Number of Endpoints:

All user specified timing constraints are met.

Timing Summary - impl_1 (saved)