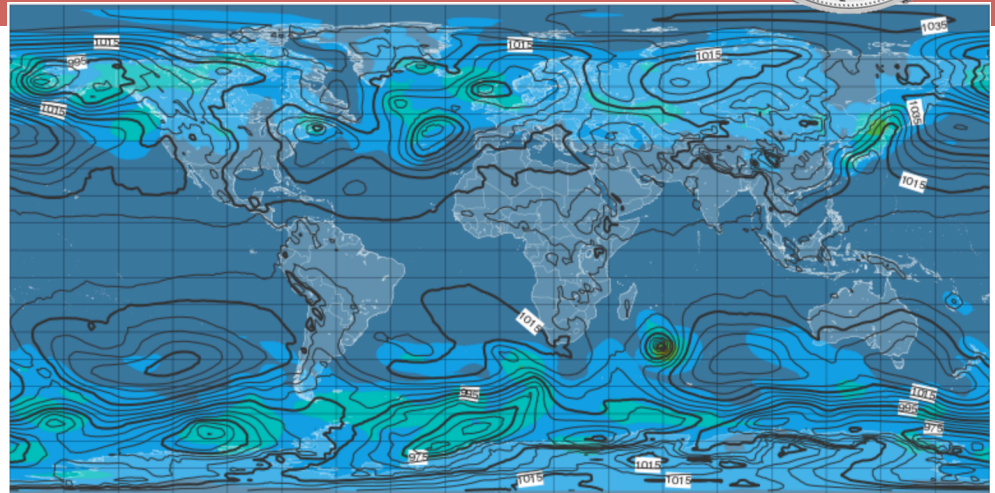
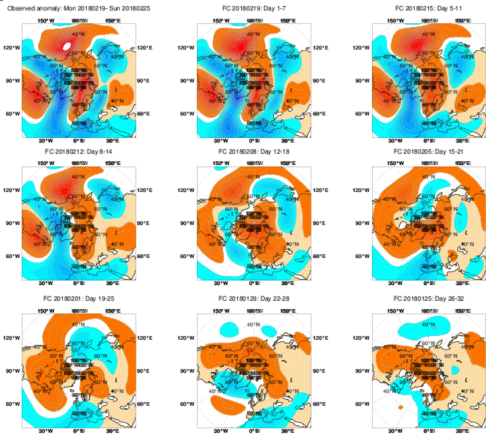


Weather Forecasting Performance Analysis on Isambard

Mihail-Calin Ionescu, supervised by Simon McIntosh Smith
University of Bristol, Department of Computer Science



Isambard

- Tier 2 Supercomputer - The first ARM HPC cluster, it will have over 10,000 ARMv8 cores.
- Two Thunderx2 x 32 cores per node
- Incorporates multiple architectures: x86 (Broadwell), XeonPhi, Nvidia Pascal GPUs

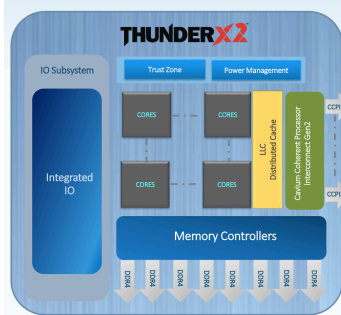
Aims

- Exploring how well the code works out of the box, the higher bandwidth provided by Thunderx2 should lead to better performance compared to Broadwell
- Comparing different compilers (Cray, Intel, GNU, ARM HPC)
- Comparing vectorisation levels (AVX vs NEON vs SVE)
- Potential benefits of HBM-style memories on future CPUs

Progress

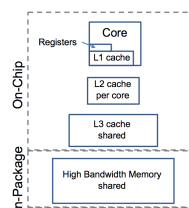
- Obtained runtime analysis, roofline models for a subset of the ESCAPE dwarfs
- Starting building OpenIFS on Isambard

Cavium CN99XX - 1st member of THUNDERX2 Family



- 24/28/32 Custom ARMv8 cores
- Fully Out-Of-Order (OOO) Execution
- 1S and 2S Configuration
- Up to 8 DDR4 Memory Controllers
- Up to 16 DIMMs per Socket
- Server Class RAS features
- Server class virtualization
- Integrated IOs
- Extensive Power Management

2nd gen Arm server SoC
Delivers **2-3X** higher performance



Issues

- ARM nodes availability – offline for 3 week at the moment
- Compilation issues on ARM when using the Cray and ARM HPC compilers

