LAB 3
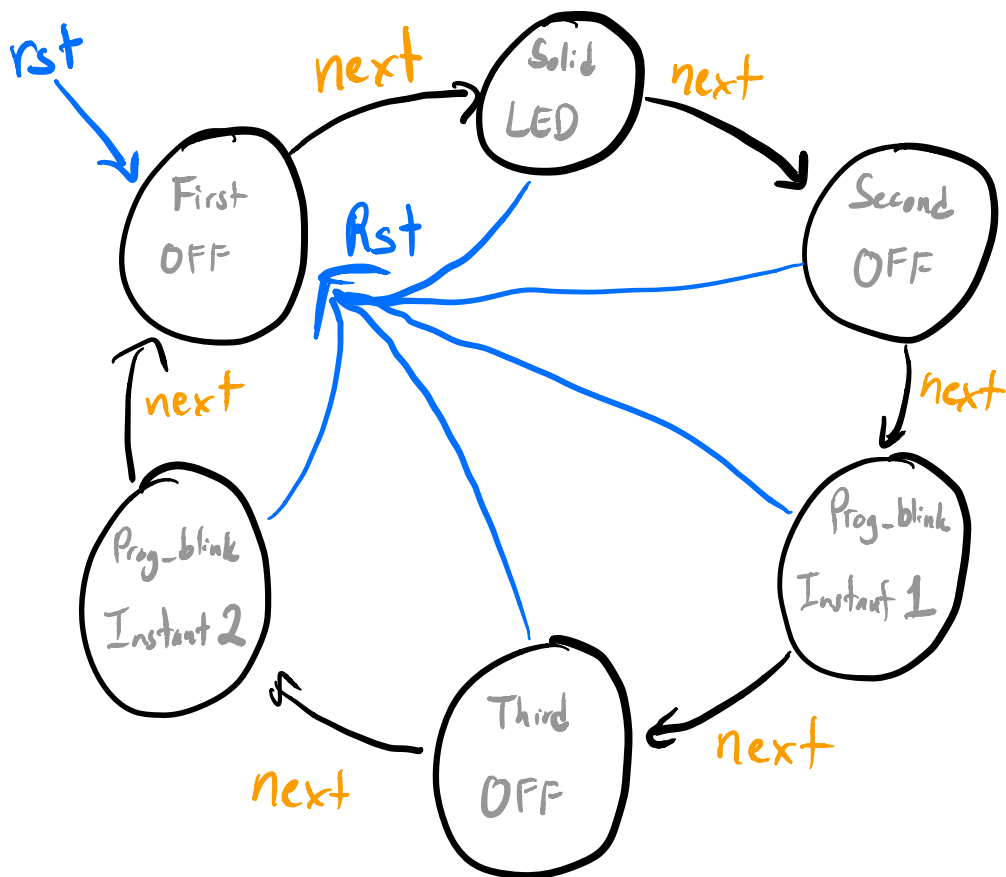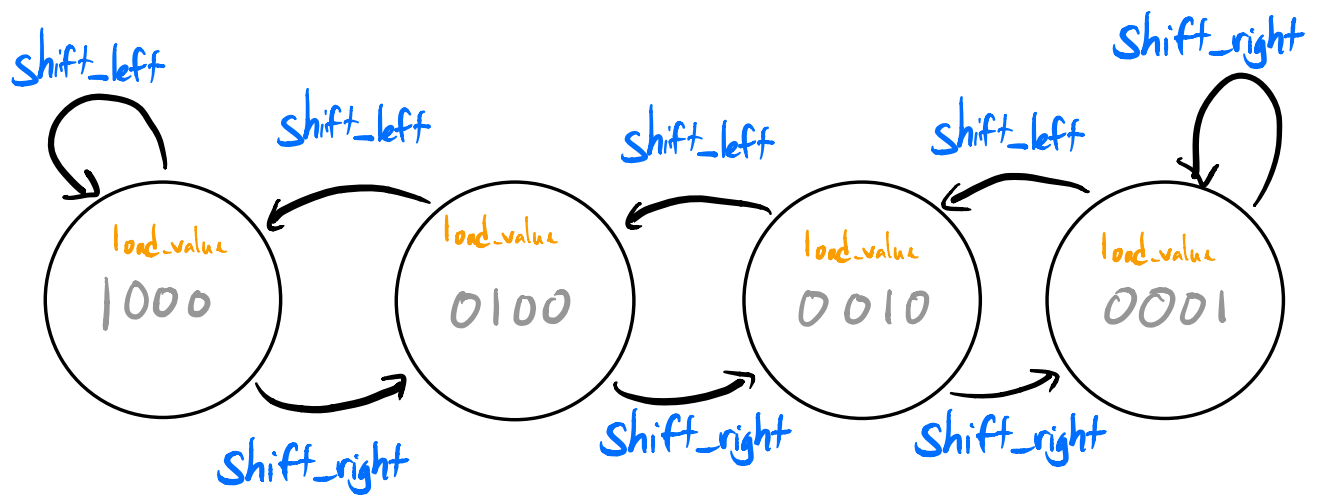
Julia Wang
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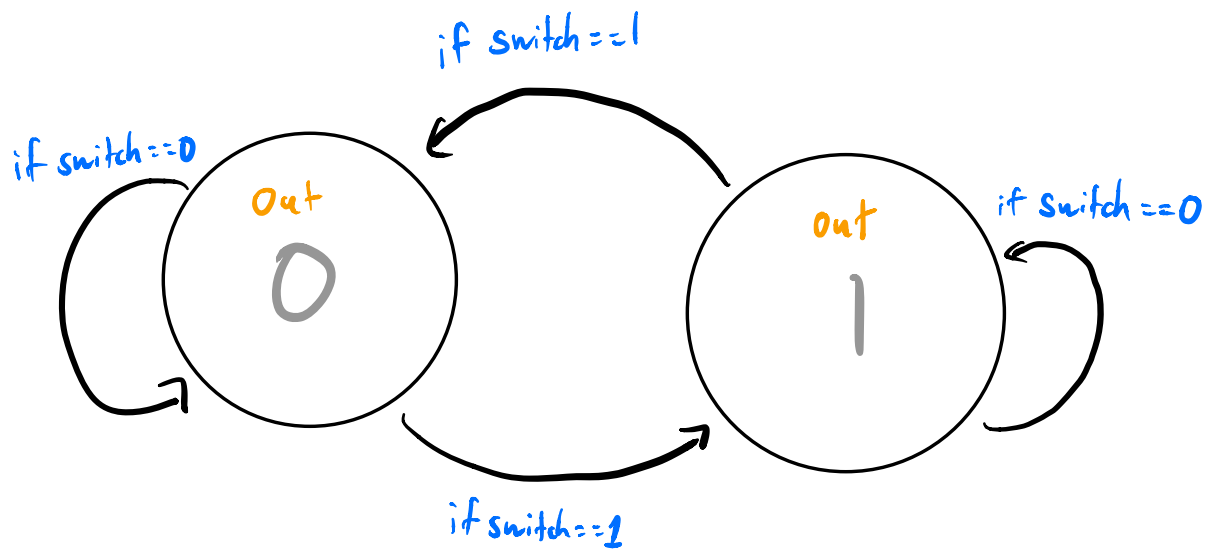
3. Diagrams

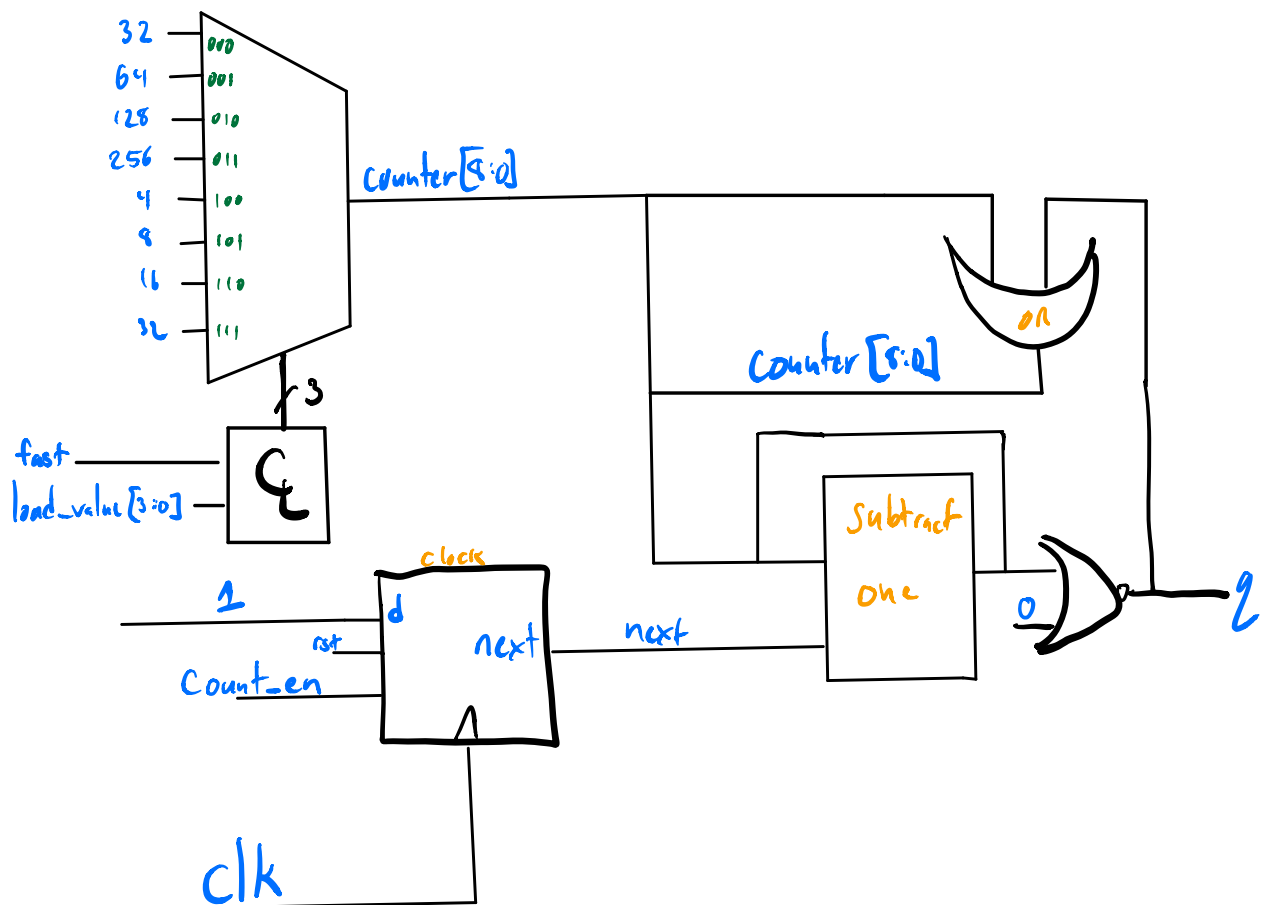## Master FSM
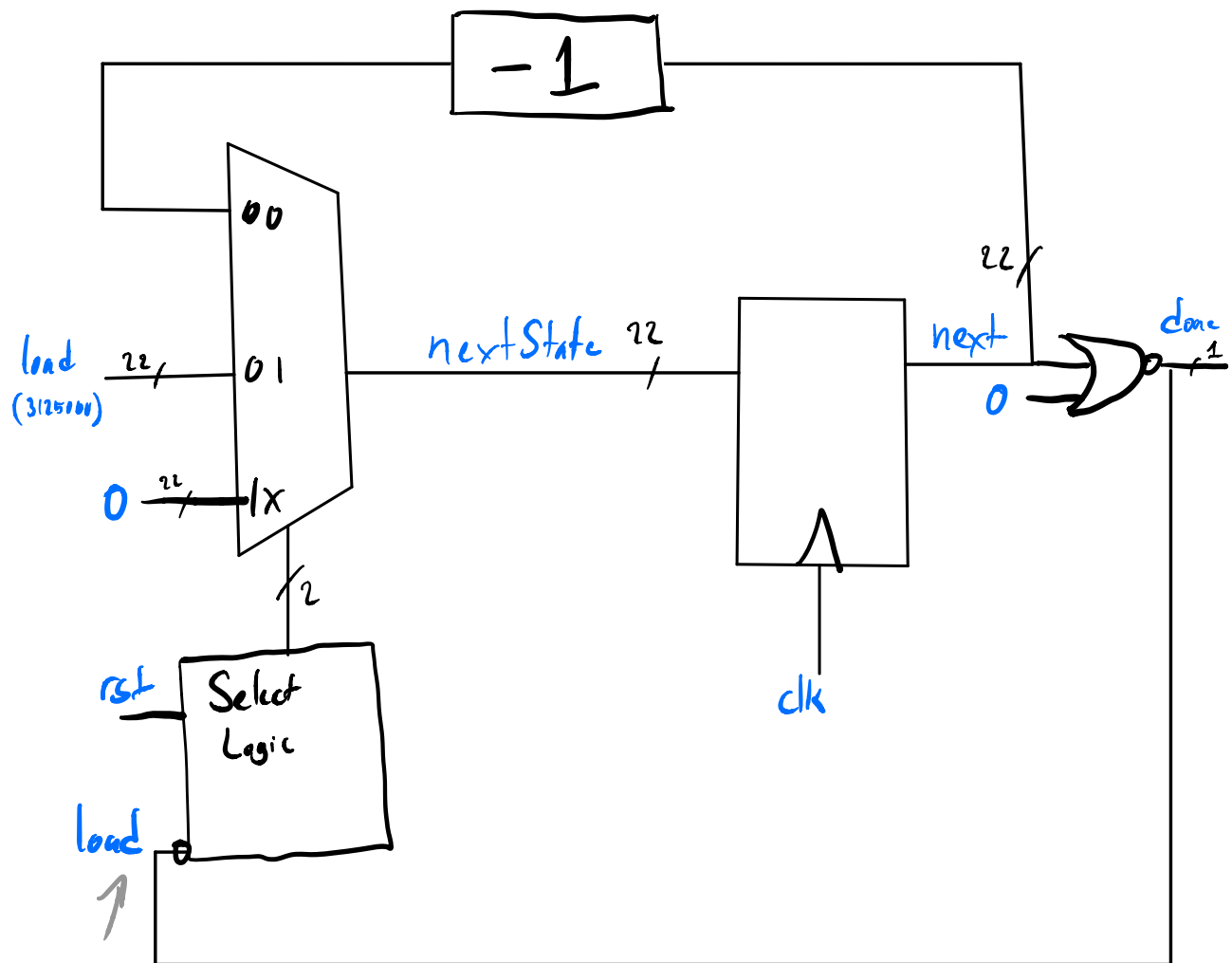
Shifter

Blinker

Timer

32 — 000
64 — 001
128 — 010
256 — 011
4 — 100
8 — 101
16 — 110
32 — 111

counter[5:0]

3

fast
load_value[3:0]

C

counter[5:0]

or

1

clock

d

rst

count_en

next

next

Subtract
one

0

q

clk

Beat 32

Beat 32

The circuit contains:
- A **-1** block at the top connected in a feedback loop
- A multiplexer with inputs labeled `00`, `01`, `1X`
  - `00` connects to the -1 feedback loop
  - `01` connects to `load (3125000)` with width `22`
  - `1X` connects to `0` with width `22`
  - Output labeled `nextState` with width `22`
- A register (flip-flop) clocked by `clk`, output labeled `next` with width `22`
- A NOR/OR gate producing `done` (width `1`), with a `0` input
- A **Select Logic** block with inputs `rst` and `load`, output width `2`

Annotations:
- `load (3125000)` — `22`
- `0` — `22`
- `nextState` — `22`
- `next` — `22`
- `done` — `1`
- `clk`
- `rst`
- `load` — is on when done == 0