Transient Temperature Response of a Power Transistor

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Abstract—The results obtained from a computer-aided thermal analysis of a microwave power transistor are presented. The transistor is somewhat unique in that it has a junction-to-carrier thermal time constant of only about 50 μs. The application for which this transistor was desired required that it handle a pulsed power dissipation wherein each pulse has the shape of a fourth power cosine curve with a 7 μs on-time and 130 watts peak power. The half-power pulsewidth is, therefore, only about 2.5 μs. Although the pulse duration is quite short, the junction undergoes temperature excursions of about 30°C during any single pulse. These temperature excursions cannot possibly be detected by either direct electrical measurements or infrared experimental techniques but, nevertheless, have an important effect on the life and reliability of the transistor.

The computer-aided analysis technique and the results are discussed in general throughout the paper. Points of interest include the temperature distribution both on and within the chip, the effects of temperature dependent material properties, the use of a heat spreader under the chip, and, finally, the meaning and significance of the thermal time constant for the junction, the chip, the carrier, and other parts of the electronic package.

I. INTRODUCTION

A. Reliability

Before any semiconductor device is considered for use in high power applications some method of thermal evaluation will inevitably be applied. One of the main reasons for evaluation is generally to estimate the reliability or mean-time-to-failure (MTF) of the device. Microwave power transistors are of particular interest to many of us working in the communications field. These devices are relatively expensive, must operate under high power pulsed conditions, and yet must be highly reliable. That reliability depends very strongly on the absolute temperature of the device [2]. As a rough rule of thumb for microwave devices such as considered here, the MTF will be cut in half for every 10°C rise in junction temperature.

B. Transistor Geometry

The device we are about to study is the multijunction microwave power transistor shown in Fig. 1. This figure is a photographic plan view of the transistor device, along with other associated capacitors and conductors, mounted on the same 0.25 in square by 0.025 in thick beryllia carrier. The silicon chip is bonded onto a gold conductor which, in turn, is bonded onto the carrier. Overall, the chip is 0.0365 in wide, 0.125 in long, and 0.003 in thick.

This transistor device has 16 junction regions all of which operate in parallel. The device must be capable of handling a relatively high rate of power dissipation that occurs as a time sequence of power pulses. The frequency, power dissipation, and duty cycle of each pulse or series of pulses are usually tailored to provide or gather specific information from the microwave system. From the thermal standpoint, the analysis usually boils down to the determination of two main response characteristics for any given power sequence; first, the average temperature rise must be found, and second, the instantaneous temperature response or excursion about that average must be determined.

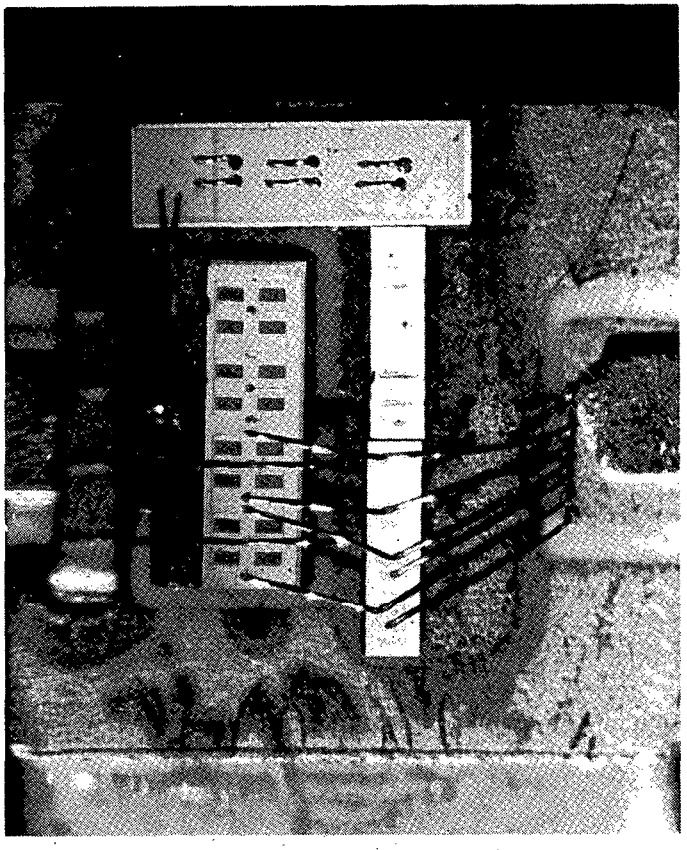

Fig. 1. Multijunction microwave power transistor, associated capacitors, and conductors mounted on 0.25-in square beryllia carrier.

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II. THE PROBLEM

A. Power Pulse Sequence

The transistor device indicated above was proposed for use in a radar system. The power sequence would consist of a series of symmetrical pulses, one-half of which is shown in Fig. 2. Each pulse has 130 watts peak power dissipation and an overall "on-time" or base width of 7 μs. The duty factor (i.e., the on/off time ratio) for this application was expected to vary from about 0.2% to 58%. The problem then was to determine the temperature response of the transistor junction for a specified "worst case" sequence of power pulses.

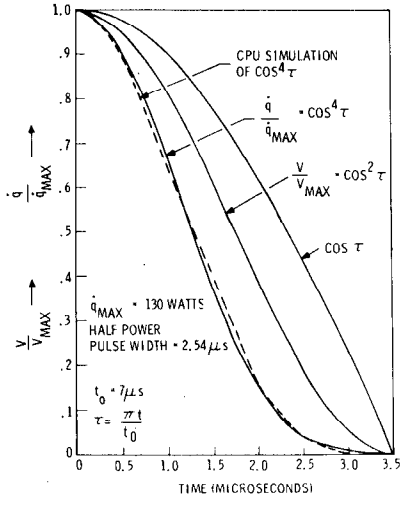

Fig. 2. Computer simulation of power dissipation pulse.

In general, a 7 μs on-time, such as for the pulse duration indicated above, would be of little concern in most transistor studies. The problem exists here because of the high rate of power dissipation. Depending upon the thermal resistance and the effective time constant of the device, the temperature excursion during this pulse could become quite important. As it turns out, the junction effective thermal time constant is relatively short and even though the thermal resistance is very low, the combination of high power dissipation and short time constant causes relatively large excursions in the junction temperature response.

III. METHOD OF SOLUTION

A. Computer-Aided Analysis

To determine the transient temperature response of the transistor device a computer-aided thermal analysis was performed. In essence, this method entails the use of engineering judgment to create a mathematical model that will accurately simulate the thermal characteristics inherent in the physical device. The model is then used to provide numerical input data to a heat transfer computer program. In this case a finite difference program was used to solve the heat transfer equations relating the temperature and material properties of small geometrical volumes, called nodes, that form the geometry of the model. Specific temperature data are found for specially selected inputs from which desired thermal characteristics are then determined by engineering interpretation. The computed solution provides specific data that are in equilibrium with all prescribed boundary conditions, complex geometries, time-dependent heat generation rates, and temperature dependent material properties. Experience with this method of simulation has consistently yielded results that are in good agreement when compared with reliable experimental measurements. Besides being accurate and nondestructive, this method provides a simple tool to study thermal effects caused by parameter changes within the model.

B. Special Advantage

As this study proceeds, several unique advantages of computer-aided simulation will become apparent. To set the framework, one might calculate that the 130 watt pulse has an equivalent "square" pulsewidth of about 2.5 μs time duration. Any experimental measurement device attempting to pick up a temperature excursion of this time duration would not be very effective. For example, the time constant of the Barnes Engineering Model RM-2A infrared radiometric microscope has a time constant of about 8 μs. This is a very fast response time as far as infrared microscopes are concerned but this scope could hardly be expected to pick up a 2.5 μs excursion. During this short time period the scope would probably register about 30% of the actual temperature excursion. This assumes of course that the scope is focused and calibrated on an opaque (to the proper infrared wave length) surface directly over the junction region. This last precaution is necessary since silicon is somewhat transparent to the infrared wave lengths.

IV. THE MATHEMATICAL MODEL

A. Simplified Model

In this study it was desired to estimate the operating temperature response in the "hottest" junction region of the chip, that being one of the innermost junction regions. Utilizing symmetry where possible only an inner junction region need be modeled to provide the desired data. In addition, it is known from past experience that transient temperature effects in the chip attenuate very rapidly as the distance from the junction increases. Therefore, it is only necessary to simulate a small portion of the electronic package in order to derive accurate junction temperature response characteristics. Thus the mathematical model includes only a single junction region of the chip plus a very small portion (to a depth of about 9 mils) of the chip carrier. A plan view and cross-sectional view of the resulting simulation model is shown in Fig. 3. From this model thermal characteristics within the chip, that is, from the junction to the carrier-chip interface, can be predicted very accurately.

B. Superimposed Solutions

Usually a computer-aided analysis is only required at the chip level and the rest of the package can be adequately handled by other techniques. However, if the geometry of the package is quite complex or has asymmetric time-dependent heat generation, it may then be desirable to simulate

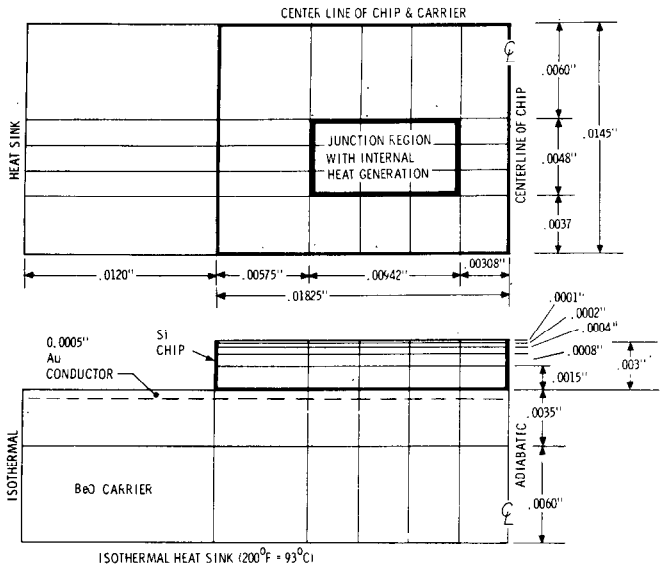

Fig. 3. Computer simulation model of innermost junction region of multijunction microwave power transistor.

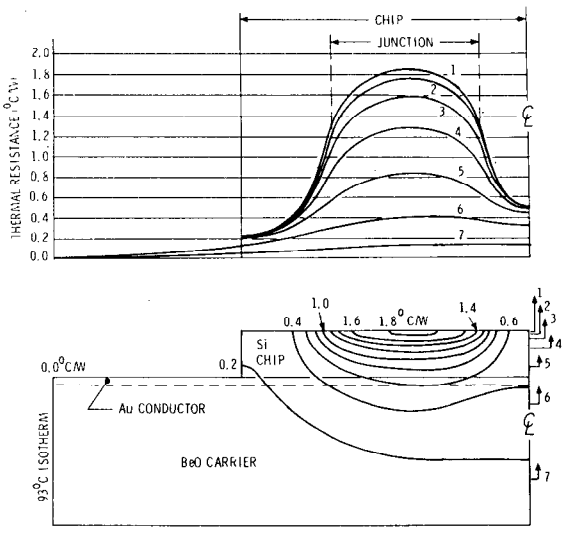

Fig. 4. Thermal resistance and isothermal profiles through innermost junction region of multijunction microwave power transistor.

additional portions of the package. For example, another model, more coarsely structured than the first, can easily be designed to simulate the thermal effects from the carrier-chip interface to some point closer to the ultimate heat sink. The results of the two studies can then be superimposed to provide a very accurate and complete analysis of the whole electronic package. In this way, the analysis can be tailored to provide consistent accuracy throughout the whole package and, overall, will be relatively inexpensive with respect to both computer costs and engineering time required.

V. HEAT TRANSFER CHARACTERISTICS OF THE CHIP

A. Steady State Temperature Rise

For a constant rate of power dissipation the temperature distribution within the chip and carrier will soon stabilize at some steady state value as indicated by the isothermal lines and thermal resistance values shown in Figs. 4 and 5. To aid in interpretation, note that the isothermal (i.e., constant temperature) lines actually represent the intersection of isothermal surfaces with the plane of the paper. Heat will flow only in a direction that is normal to these surfaces. The temperature rise above the heat sink (i.e., bulk BeO carrier) temperature can be determined at any particular location by multiplying that given thermal resistance value by the *total* power dissipation within the chip.

B. Temperature Distribution

Fig. 4 shows isothermal lines and thermal resistance profiles within the chip and carrier while Fig. 5 shows the temperature distribution on the surface of the chip. It is apparent there are high temperature gradients both across the surface and through the depth of the chip. To estimate the junction temperature experimentally one must realize this gradient exists in order to interpret measurements correctly. Note further, that a temperature sensing device located near the edge of the chip, or for that matter near the edge of the

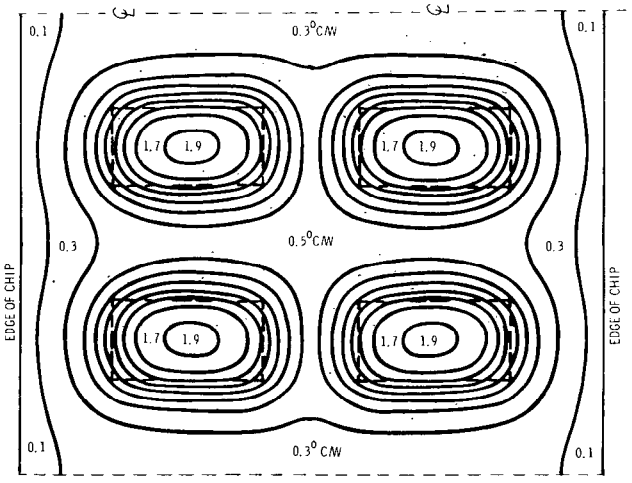

Fig. 5. Thermal resistance and isothermal lines on chip surface of multijunction microwave power transistor.

junction region, will not provide an accurate measure of the peak junction temperature. The temperature rise near the outer edge of this chip, for example, is less than 10% of the actual peak junction temperature rise above that of the bulk carrier temperature.

One fact that has not been shown in Fig. 5 is that there is also a general temperature gradient along the length of the chip just as there is across the width of the chip. Total symmetry has been shown in this figure simply for ease of display. The actual temperature gradient would show that the lower two junction regions are slightly cooler than the centermost junction regions.

C. Temperature Dependent Thermal Conductivity

The thermal resistance values shown in these figures can be used to extrapolate temperature data for various power levels but with a word of caution. Thermal resistance values should be corrected to account for temperature dependent material properties. For example, at 24.8 W average power dissipation,

the conditions under which these figures were plotted, the hot spot junction temperature would be about 1.9°C/W X 24.8 W = 47°C above the 93°C isothermal heat sink temperature. At 2.6 W average dissipation, a computed hot spot thermal resistance was only about 1.7°C/W, or about 11% lower than above. The significance of this is that if the lower value had been used to predict the temperature rise for 24.8 W, we would have underestimated the temperature rise by 11%.

The difference between the thermal resistance values above is due to the nonlinear temperature dependent material properties of the silicon chip and, to a lesser extent, to that of the beryllia carrier. To convince oneself of this, it is only necessary to look at the thermal conductivity k_{Si} of silicon [3]. At 97°C, k_{Si} = 2.55 W/in·°C while at 140°C, k_{Si} = 2.23 W/in·°C, a difference of 14% over a temperature range of only 43°C. Obviously, only the hot spot of the junction will experience this 14% change while the rest of the chip and the carrier will experience a somewhat lower temperature rise and, hence, a lower percent change in the thermal conductivity. Hence the total integrated effect causes the 11% difference indicated above.

D. Thermal Heat Spreader

The temperature distribution near the bottom surface of the chip brings out another question that frequently arises in the application of high power semiconductor devices: What will a thermal heat spreader buy in the way of temperature reduction if used in this application? The answer is fairly straightforward. A large copper heat spreader for which $k(\text{Cu})/k(\text{BeO}) \approx 2$ will reduce the temperature rise within the BeO by a factor of about 50% or roughly from 0.6°C/W to 0.3°C/W. In effect this will reduce the total junction temperature rise by about 17%. The actual reduction will depend on several other factors, however, such as the size of the copper heat spreader and of couse the bond between the copper and the chip and between the copper and the carrier.

In general, semiconductor chips are somewhat thicker than the 0.003 in of this chip so the use of a heat spreader may not always be so effective [1]. In this case, the thermal resistance within the carrier represents a sizable portion of the total carrier-to-junction resistance. The use of a heat spreader in this application could prove to be practical.

VI. TRANSIENT RESPONSE CHARACTERISTICS OF THE JUNCTION

A. Time Constant

Fig. 6 shows the transient temperature response for various portions of the thermal model when the junction is given a step power dissipation function. In this figure the time constant τ is defined as the time it takes for the temperature to reach 63% of its ultimate ΔT value above the heat sink (i.e., bulk BeO carrier) temperature. The effective thermal time constant for each portion of the model is then as indicated and varies from 52 μs for the junction to 720 μs for the major portion of the BeO carrier included in the model.

When specifying the time constant it is important to specify the location of the temperature of interest. As shown in Figs. 4 and 5, the temperature can vary considerably across the chip and presumably through the whole package. The curves plotted in Fig. 6 represent the volumetric averaged temperature for various portions of the model. Further, it is meaningless to talk of any time constant other than the *relative* time constant between the response curves of various portions of the package. In the thermal model considered here, the time constants are all taken relative to that of the simulated heat sink. In the physical device, that heat sink is actually the bulk of the beryllia carrier, and the 93°C isothermal temperature represents the bulk temperature of the carrier.

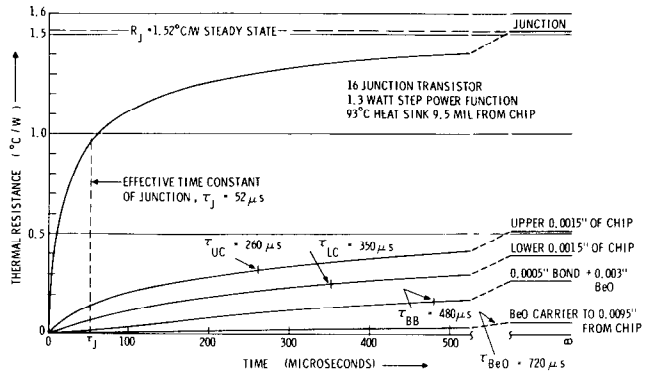

Fig. 6. Transient thermal response to step power function for junction region of multijunction microwave power transistor.

B. Superimposed Response Curves

The effect of the thermal time constant can be seen quite readily from Fig. 6. Within several junction time constants the junction temperature reaches somewhat of an equilibrium state relative to the chip temperature and thereafter increases only as the chip temperature increases. Similarly, within several chip time constants, the chip temperature will attain an equilibrium state relative to the carrier temperature and thereafter increases only as the carrier temperature increases. This same process will continue on down through the electronic package until all parts of the package have reached their equilibrium temperature. The final time constant, for example, that of a heat exchanger, may be on the order of several minutes so the whole package, including the junction, may not reach a final equilibrium temperature for an hour or so after the step power function has been applied.

One important effect, related to that of Section V-C, occurs as each portion of the package increases in temperature. Any increase in temperature is passed directly along to the carrier and the chip, which have a thermal conductivity that decreases with increasing temperature. As a result, the thermal resistance increases and, hence, the junction temperature experiences an even greater increase in temperature than portions of the package located between it and the final heat sink. This nonlinear temperature effect will continue until all components of the system finally reach their equilibrium state.

C. Average Junction Response

Estimating the junction time constant and response characteristics for a step power function is an essential part of the transient analysis. These results tell us what to expect in the

way of transient behavior to some form of complex power schedule. Fig. 7 shows the temperature response of the microwave transistor junction for such a power schedule. As the power changes at the various times, the junction temperature will follow the response curve shown. However, the figure does not show the individual pulse sequence of the power pulse series but rather shows the "average" power dissipation schedule. Nor does it show the fact that the instantaneous junction temperature actually varies considerably about the "time average" junction temperature shown.

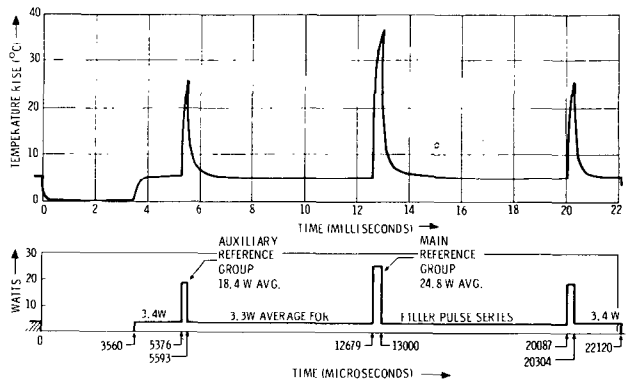

Fig. 7. Transient temperature response of inner junction to time sequence of changing power levels.

Fig. 8 shows the actual last four power pulses in the main reference group of the power schedule indicated above and in Fig. 7. The power pulses in this application always occur in pairs but with various time periods between pairs. This gives rise to the changing average power schedule shown in Fig. 7. There are two main types of pulse series indicated. The main reference group consists of 12 pulse pairs and the auxiliary reference group consists of 6 pulse pairs, but each group has a slightly different duty factor. During the time period just prior to and just after a reference group, pulse pairs occur in another sequence that gives rise to yet another average power schedule, shown and referred to as the filler pulse series. The average rate of power dissipation during each group is therefore different but is easy to determine. Thus, 24.8 watts, for example, is the average power dissipation during the main reference group pulse series.

D. Instantaneous Junction Response

The instantaneous volumetric average junction temperature response to each of several individual power pulses is shown in Fig. 8. The important characteristic to observe is, of course, the temperature variation during each pulse. The time base of each power pulse is only 7 μs long but, during this time, the junction temperature has increased by 30°C and has already started to decrease again. It reaches its peak about 1 μs after the peak of the power pulse. The actual hot spot temperature within the junction will reach its peak about 2 μs after the peak of the power pulse and will be about 5°C higher than the volumetric average junction temperature.

While the junction is undergoing these rapid temperature excursions, the rest of the chip is undergoing proportionally less temperature variation depending upon the distance from

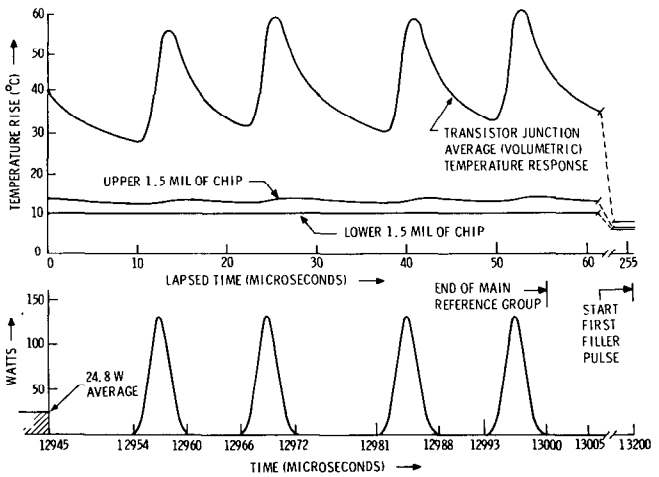

Fig. 8. Transient temperature response of inner junction to individual power pulses near end of main reference group (130 W peak power with 2.5 μs half-power pulsewidth).

the junction. For comparison, the volumetric average temperature for the upper and lower halves of the chip are also shown in Fig. 8.

After the last power pulse in the main reference group, there is a 200 μs time delay before the first filler pulse pair occurs. During this time the junction temperature rise decreases from its peak value of 60°C down to a value of only 8°C. During the first pair of the following filler series, the temperature will increase to a peak of about 38°C and 42°C during the first and second pulses, respectively. If the pulse series is then continued the temperature will thereafter continue to increase in this sawtooth fashion as long as the pulses are sufficiently close together.

VII. CONCLUSIONS

1) Under certain conditions, namely, low thermal resistance, short time constant, and high power dissipation, junction temperature excursions from an average value can be quite large. This can be true even if the pulse duration time is much smaller than the effective junction time constant.

2) The temperature dependent thermal conductivity of silicon and of common ceramic carrier materials, i.e., beryllia and alumina, plays a very important role in determining both the steady state and transient junction temperature. The thermal conductivity decreases with increasing temperature causing an increase in thermal resistance. Thermal resistance data should be corrected for this effect in both theoretical and experimental studies.

3) Temperature varies greatly both across the surface and through the thickness of the chip. The gradient is concentrated, primarily, within a few mils of the junction. A temperature sensing device should therefore be placed as near the center of the junction as possible and, in addition, within the hottest junction region of the chip.

4) The use of a heat spreader between the chip and carrier may be of practical value only if the thermal resistance within the carrier is significant compared to that between the chip-carrier interface and the junction.

5) The effective thermal time constant of the junction

should be measured as a *relative* time constant between the temperature response curves of the junction and the next level of packaging between the chip and the heat sink. In this analysis the next level selected was the bulk portion of the chip carrier.

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Design of Temperature-Controlled Substrates for Hybrid Microcircuits

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Abstract—This paper deals in depth with the criteria that govern the design of temperature-controlled substrates for hybrid microcircuits. Pertinent thermal parameters for the more important microcircuit-fabrication materials are presented in tabular form, along with several useful unit-conversion factors. Substrate heat losses due to conduction, convection, and radiation are then analyzed, and equations are developed for determining optimum substrate temperature, steady-state input power, and warm-up characteristics. Control-circuit design is discussed, and consideration is given to power dissipation by circuitry off as well as on the substrate. The effects of changes in ambient temperature on temperature-controlled-microcircuit performance are analyzed. Two applications of this technology are described.

INTRODUCTION

Electronic-circuit performance can be severely degraded by exposure to a wide range of ambient temperatures. Limiting the effects of ambient-temperature changes by enclosing the circuit in an electronic oven is usually impractical in that it increases size, weight, and power requirements. The use of hybrid microelectronics, on the other hand, not only results in reduced circuit size but also implements the maintenance of a constant circuit temperature. The latter is accomplished by incorporating on the hybrid-microcircuit substrate a heater and a temperature controller.

The sections that follow analyze the criteria for designing temperature-controlled substrates for hybrid microcircuits and describe two applications in which these techniques have been employed.

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BASIC THERMAL DATA

The transfer of heat from one point to another involves the flow of a quantity of heat per unit time. This rate of heat flow is in fact a rate of energy flow, which in turn is equivalent to power. The flow of power in a thermal circuit is directly analogous to the flow of current in an electric circuit and can be represented by the simple ohmic-type equation

$$\Delta T = P\theta_{A-B} \tag{1}$$

where ΔT is the temperature difference between points A and B, P is the power flowing between points A and B, and θ_{A-B} is the thermal resistance between points A and B. The electrical analogs of these and other common thermal parameters, along with the units in which they are normally expressed, are presented in Table I. Some useful thermal-conductivity conversion factors are listed in Table II. Table III is a compilation of pertinent thermal data for the majority of materials used in the fabrication of hybrid microcircuits.

SUBSTRATE HEAT LOSS

A substrate designed to hold a critical component or microcircuit at a constant temperature will contain three functional entities: a heater, a temperature controller, and the component or microcircuit in question. Following a warm-up period, this substrate is held at an elevated temperature in a steady-state condition of thermal equilibrium. In this state, the power applied to the substrate must equal the power coming out of it. The input power is distributed among the three