Julien MASTRANGELO

French engineer in computer science & microelectronics





EDUCATION

2019 – 2022 ISMIN | Mines de St-Etienne (CGCP, Gardanne)

Master of microelectronics and computer science engineering.

Majoring in **embedded systems**, specialisation in **mobility and security**. Analogic electronics, digital electronics, microcontroller systems. Embedded real-time computing, FPGA codesign, VHDL modelling and synthesis. Signal processing, probabilities. Corporate vision & strategy, relationship development.

2021 – 2022 MSc Hybrid Electronics | Aix-Marseille University

Stretchable electronics, sensors, organic optoelectronics, bioelectronics, micro-generators.

2017 – 2019 CPGE MPSI-MP* | Lycée Pothier (Orléans)



WORK EXPERIENCE

APR-SEP 2022 Engineer Intern | Polytechnique Montréal (QC, Canada)

I joined the NSERC Industrial Research Chair for High-Speed and Programmable Packet Processing. I did a case study targeting the Intel® N3000 PAC **FPGA** board and its design flow using the **P4** language.

MAR-AUG 2021 Side-Channel Attacks Intern | Qualcomm (Cork, Ireland)

As an engineering intern at the Qualcomm security lab in Cork, I implemented **side-channel attack** techniques in order to add features to the lab in-house tools. I led practical experimentations with continuous improvements on industrial devices by looking for new solutions in the recent scientific literature.

AUG 2019 Digger | Departmental Archaeology Service of Aveyron

Excavation traineeship. I worked as a volunteer on a protohistoric excavation site from the Iron Age.

2017-2020 Summer jobs | John Deere. Limpa nettoyages (France)

Working for Limpa, I cleaned a high school in compliance with health department regulations. Working for John Deere, I packed spare parts of tractor engines.

FEB 2014 Trainee | CNRS (French national centre of scientific research)

Observation placement. I visited laboratories of the CNRS campus in Orléans.



SKILLS

• French: native

• English: fluent

• German: low-intermediate

- Coding skills: embedded C, C++, VHDL, Codesign, Python, SQL, deep learning, web development, Latex
- Engineering software: Git, Vivado Design, ModelSim, STM32Cube, Proteus 8, Cisco packet tracer



INTERESTS / PROJECTS

- VHDL modelisation and design on FPGA of the AES-128. As a school project, I coded the four basic operations that make up the encryption of AES, the key expander function and the associated FSM. Then, I implemented this AES on an FPGA using Vivado.
- Musician. Trumpet, bass guitar and guitar player. I played an opera (Aïda from Verdi) in Orléans's Zénith. I am part of the French rock band 45Tours as a bass guitar player.
- julienmastrangelo.fr. Online CV developed with HTML5, CSS3, and javascript. More details about my profile, my background and my projects can be found on my website.
- Password wallet. Password wallet is a C-coded program to save passwords based on SHA-256 hash function and XOR-encryption. Source code is available on my GitHub.