Arquitectura de Computadoras

TE2031

2017

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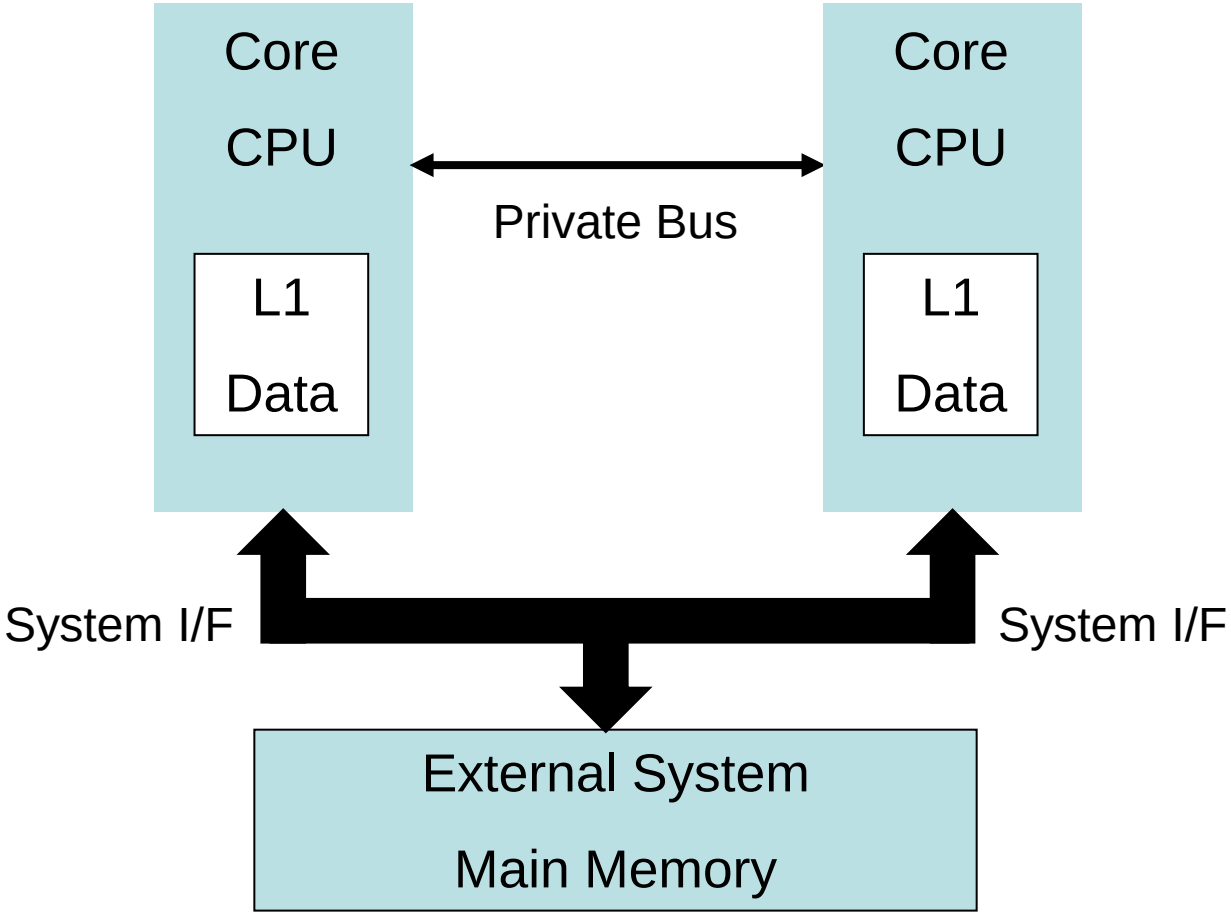
Dual-Core Microprocessor System

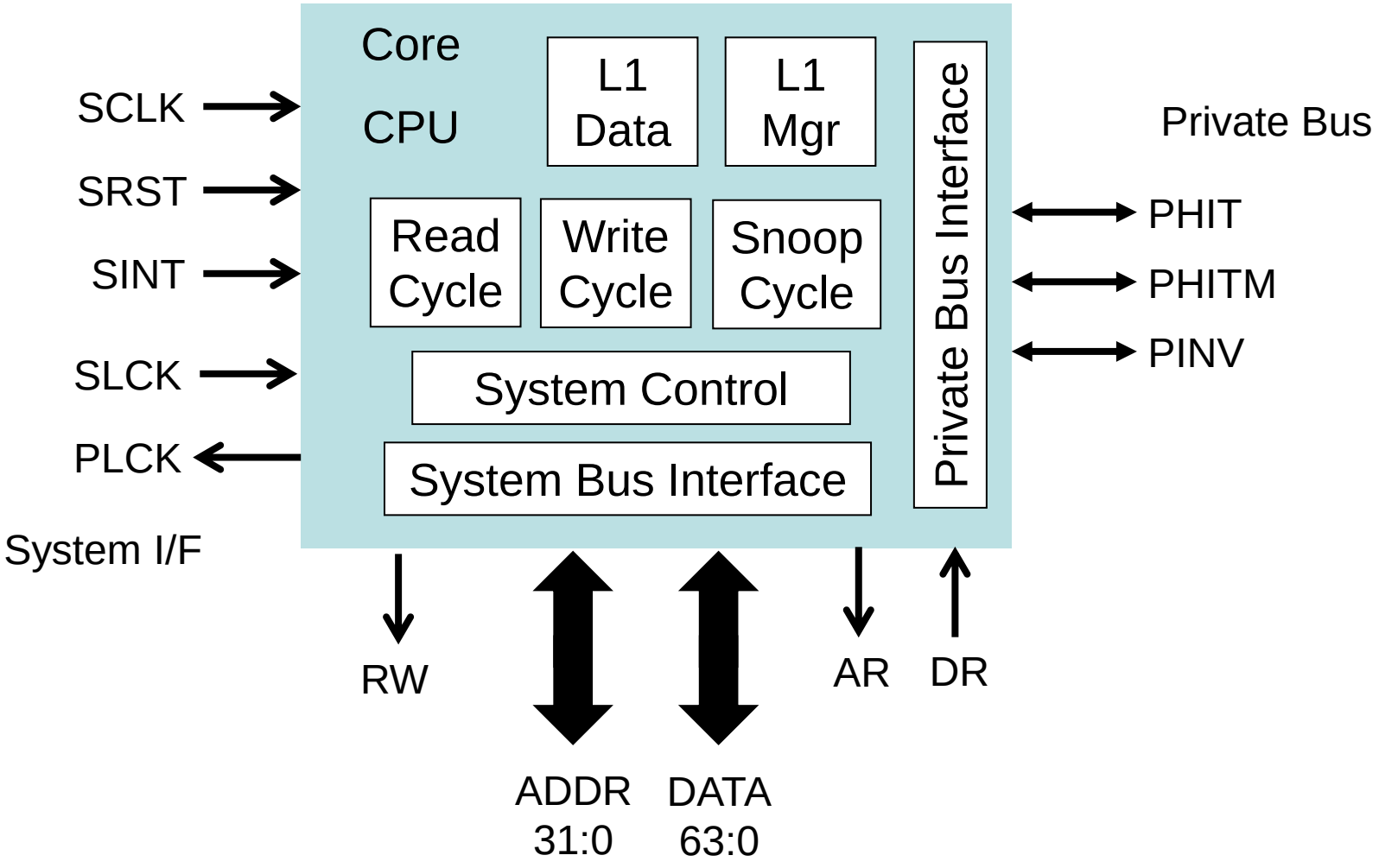
Appendix

Design

System Overview



Core CPU Module



CPU System Initialization

1. Execute reset, wait for interrupt release. SLCK active.
2. L1 cache initializes all lines are invalid, update directory status accordingly
3. Request PLCK, primary CPU has priority, SLCK released then PLCK active.
4. First execute read cycles to populate L1 cache, select target address, push address to ADDR bus, AR active, wait for DR active, data read from main memory on DATA bus ready. Update cache line: status, page, data. Repeat for more than 100 lines. Follow private bus per snoops by other CPU.

CPU System Operation

1. Once initialization done and L1 cache is populated, read and write cycles may execute arbitrarily.
2. L1 data line status may be changed from E to M arbitrarily to produce modified data conditions.
3. SLCK is constantly observed on each clock cycle.
4. SLCK asserted triggers snoop and PLCK is de-asserted. CPU waits a predetermined number of clock cycles to ensure address on ADDR bus is ready for snoop.
5. CPU observes PINV, if asserted and snoop hit then line must be invalidated. Hence other CPU executing a write cycle. Snoop results are indicated through PHIT and PHITM.

CPU L1 Manager

1. Store initial address table and provides address generation algorithm.
2. Provides addresses for L1 cache and for R/W cycles and snoops.
3. Receives snoop results from L1 and provides related information to the system
4. Provides data line transfers to and from L1 cache
5. Actions are triggered by read cycle, write cycle, and snoop cycle modules
6. All actions are synchronized relative to SCLK