Arquitectura de Computadoras

TE2031

2017

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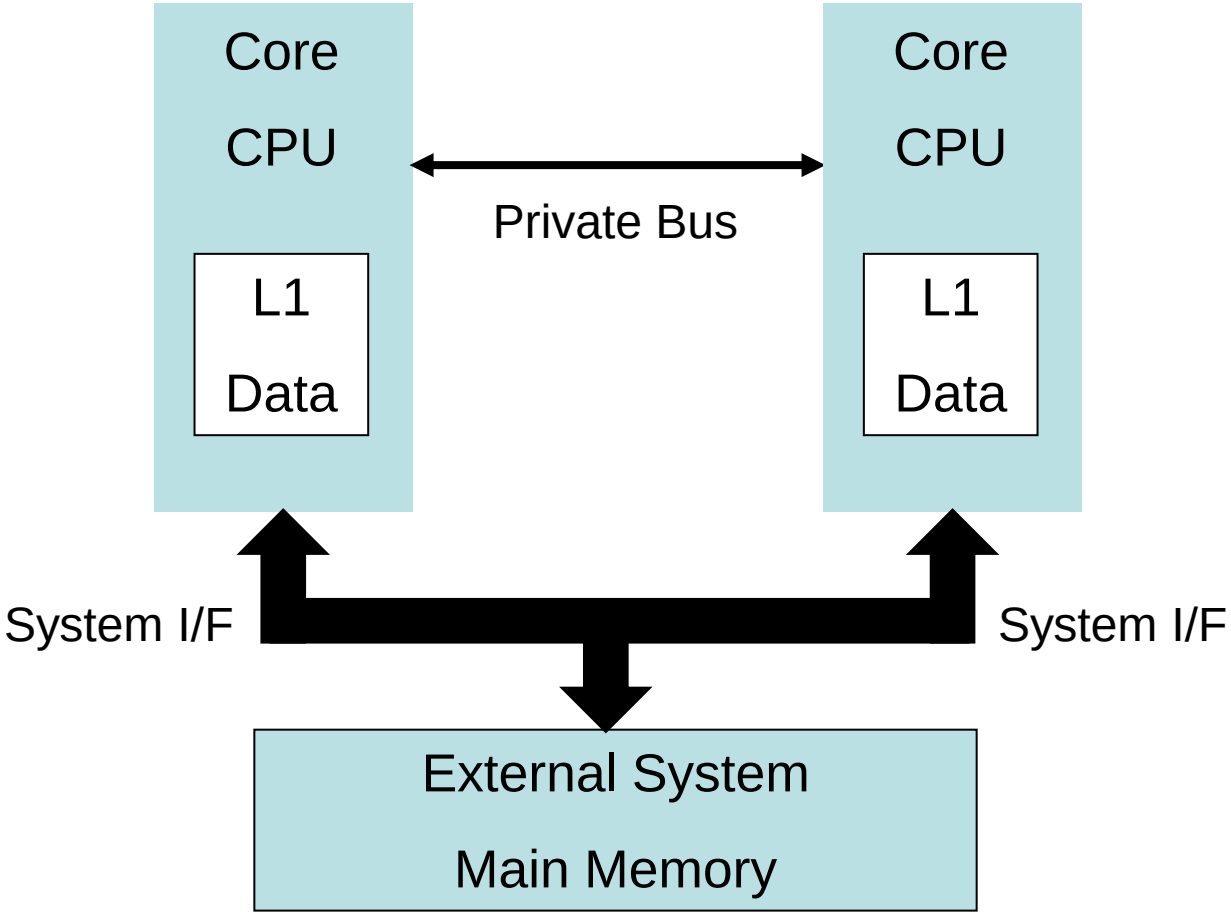
Dual-Core Microprocessor System

System Overview



Phase I

- Core CPU and L1 caches
- Memory management unit: physical address look-up; bus unit address and data buffers, read and write cycles
- L1 cache array: page size 256 lines of one double-word each (4 bytes)

Phase II

- Dual core system interface protocol
- Private phase protocol
- Define data transactions
- Define external system operations
- Implement 2 core-L1 model
- Implement external system model

Phase III

- System Verification
- Define test strategy
- Develop test bench model
- Define coverage criteria (test cases)
- Define 2-core execution approach
- Execute test suites and produce results

Guidelines

- **Design – 1/3**
- **Implementation – 1/3**
- **Verification – 1/3**
- **Documentation is critical**

External Bus Interface

- 24-bit address bus
- 32-bit data bus
- Controls
- System reset
- System clock
- System interrupt
- System interface protocol
- Private interface protocol

External Bus Interface

ADDR	Inout	24 bits	Address bus
DATA	Inout	32 bits	Data bus
RW	output	1 bit	Read or Write cycle
AR	output	1 bit	Address bus ready
DR	Input	1 bits	Data bus ready
SCLK	Input	1 bit	System clock
SRST	Input	1 bit	System reset
SINT	Input	1 bit	System interrupt

System Interface Protocol

PLCK	Output	1 bit	Processor lock
SLCK	Input	1 bit	System lock

A set PLCK/SLCK exists per processor. PLCK asserted means the processor is in control.

SLCK asserted to one processor indicates the other processor is executing a bus read or write cycle. This condition triggers a snoop by the processor not doing the bus cycle.

Private Bus

PHIT	Inout	1 bit	Snoop hit clean
PHITM	Inout	1 bit	Snoop hit modified
PINV	inout	1 bit	Write/Read cycle

PHIT and PHITM indicate a clean hit or modified hit during a snoop operation. These signals are asserted by the processor doing the snoop.

PINV is asserted high by the processor doing a bus write cycle or asserted low by the processor doing a read cycle. When asserted high the processor doing the snoop should invalidate the line corresponding to a snoop hit.

Processor-System Operation

- Both processors and system release control upon completion of system bus operations.
- PLCK may be asserted by one processor only indicating control of the bus. The other processor must sample SLCK asserted and may execute a snoop.
- PHIT and PHITM are driven by the processor performing the snoop.

Memory Addressing

- The lower eight bits of the address bus represent the address code which defines the line index of a 256-line memory table.
- The upper 16 bits of the address bus represent the page reference.
- The RW bit means a read cycle when asserted and a write cycle when deasserted.

Cache

- One memory page is defined as a 256-line table with one double word (32 bits) per line.
- Data caches are one memory page in size.
- Replacement mode is full line.
- The cache uses a write-back policy
- Main memory is two pages in size

System Synchronization

- The system clock synchronizes all external and internal operations.
- System reset assertion is asynchronous but deassertion is synchronous.
- Synchronization triggers through the rising edge of the clock

System Reset

- Upon assertion of the system reset signal the processor initializes all state elements as follows:
- All data cache status bits are set to the invalid state (0).
- All state machines are set to the reset state.
- The system bus is released.
- The processor may start a sequence of memory addressing and read/write operations.

Processor Operation

- The processor should emulate the execution of a program consisting of just data read and write operations.
- The program should be an arbitrary sequence of memory addressing operations using physical addresses and random data.
- Both cache hit and miss conditions should occur.
- Both processors should run their programs simultaneously and support snooping.

External Memory Operation

- External memory should provide multiple pages of data.
- An external memory controller should locate the required page based on the given address to support both read and write operations.
- Snoops between processors take precedence over external memory access.
- DR asserted means data on data bus is present and valid.

System Operation

- Both the processor and the external system must release control of the bus, by deasserting PLCK and SLCK respectively, immediately upon completion of the respective operations.
- The processor or the external system may take control of the bus exclusively, by asserting PLCK or SLCK respectively, after control has been released.
- The processor may execute one read or write cycle without releasing control of the bus.
- When asserted, the system interrupt stops the execution of the current program performing internal wait cycles until the interrupt is deasserted.

Initialization Sequence

1. Upon assertion of the system reset, the system interrupt is also asserted.
2. Upon deassertion of the system reset, the external system takes control of the bus.
3. Then the system releases control of the bus.
4. Finally the system interrupt is deasserted to begin program execution.
5. Upon completion of the initialization sequence one processor should default as the MRM and the other as LRM. Then the MRM will be the last processor in control of the bus and the other will be the LRM.

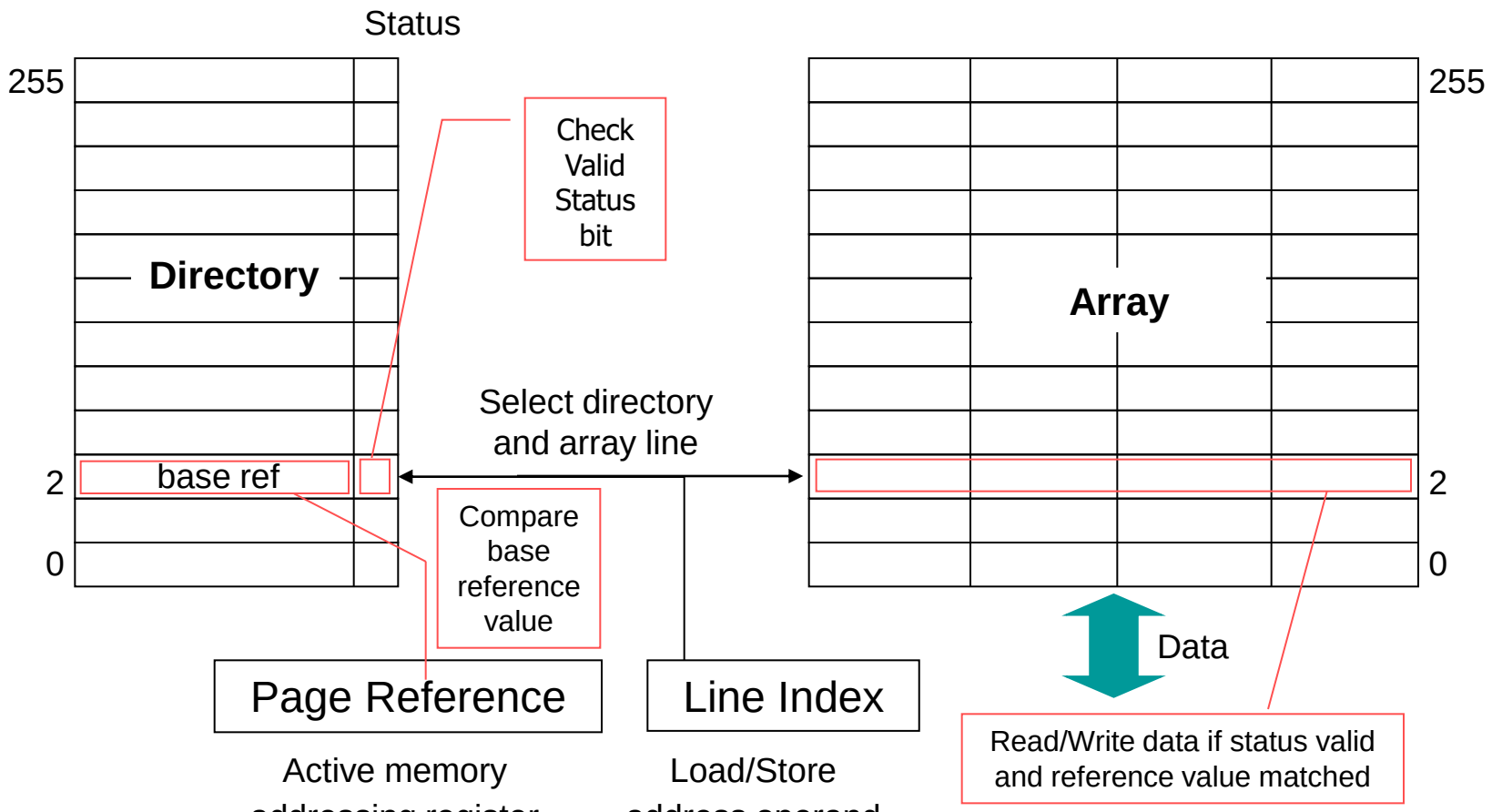
Bus Read Cycle Sequence

1. Assuming two processors PA and PB. If both require a bus cycle due to a cache miss, the current MRM takes precedence.
2. Assuming PA is the MRM doing a bus read cycle, PA should wait for its SLCK to be deasserted and then assert its PLCK to take control and start the read cycle. When PA asserts its AR indicating the address is present on ADDR and SLCK to PB is asserted and PB will do a snoop.
3. In the case of a snoop hit such that PB will provide the data line on DATA, then the external system should wait and sample DATA before providing data from main memory.
4. When DATA is ready coming from PB or from main memory, DR to PA must be asserted indicating completion of the cycle.

Bus Write Cycle Sequence

1. Assuming two processors PA and PB. If both require a bus cycle due to a cache miss, the current MRM takes precedence.
2. Assuming PA is the MRM doing a bus write cycle, PA should wait for its SLCK to be deasserted and then assert its PLCK to take control and start the write cycle. Then PA asserts its AR indicating the address is present on ADDR and the data on DATA; also SLCK to PB is asserted and PB will do a snoop.
3. In the case of a snoop hit such that PB will invalidate the line on its own cache, then the external system should sample DATA to write it on main memory.
4. DR to PA must be asserted indicating completion of the cycle.

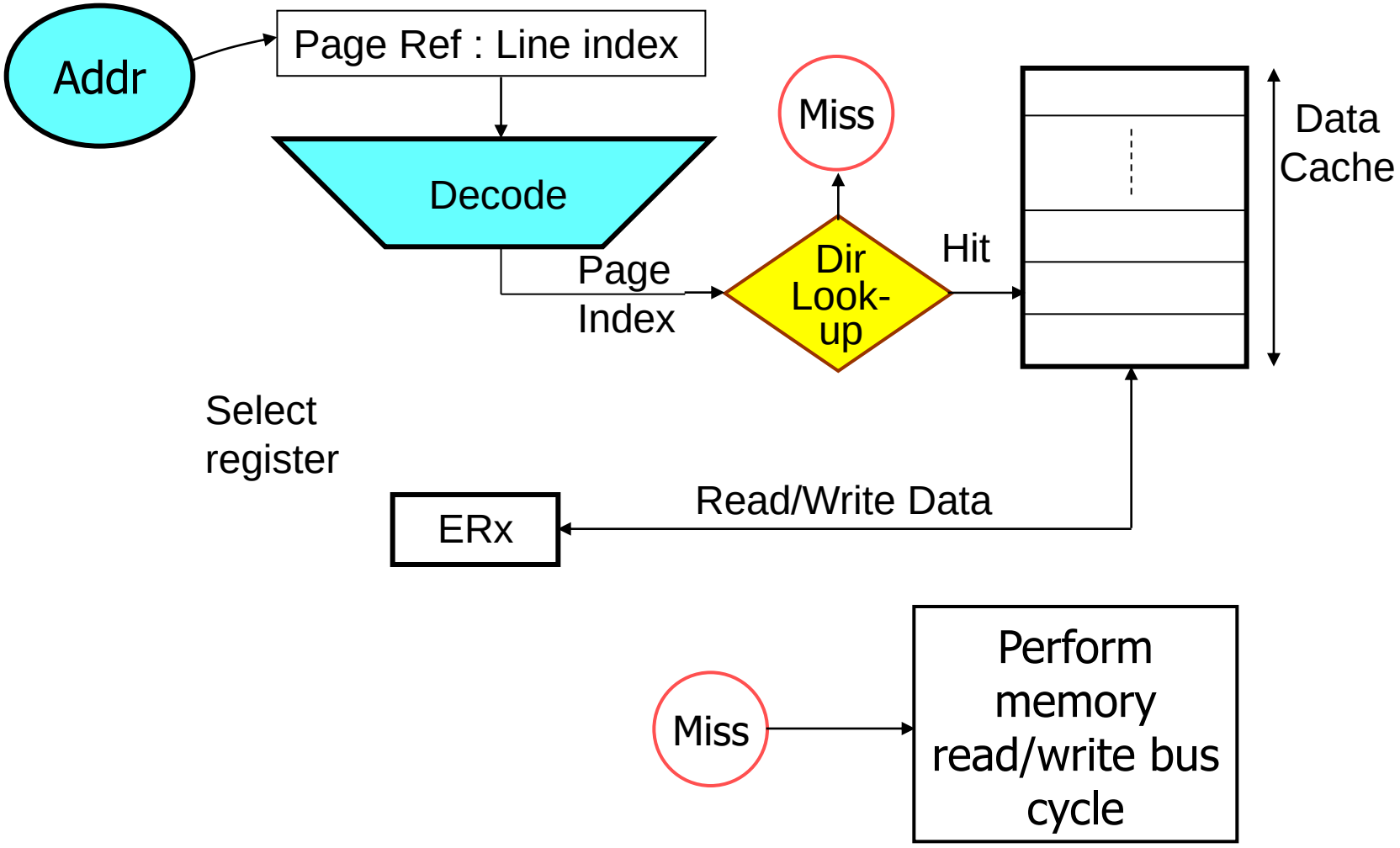
Cache Structure



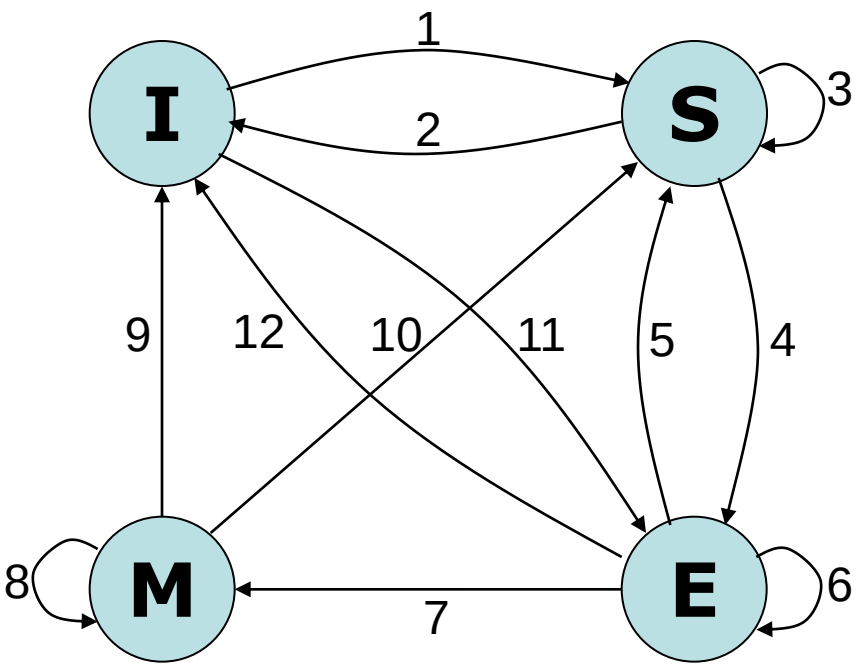
Data Memory Controller

- For a given page reference and the index of a load/store operation, the memory controller determines whether the corresponding data exists in the cache array.
- The index is used to point to the corresponding directory entry; thus if there is a match with the page reference and the status bit is valid, the result is a cache hit; otherwise is a cache miss.
- Upon a cache hit the index points to the entry of the cache array.

Load/Store Operation Execution



MESI



1. Read miss, line fill (WB/WT# = 0)
2. External snoop hit on write (INV=1) or internal snoop hit or FLUSH# or INVD or WBINVD
3. Write hit (WB/WT#=0) or read hit or external snoop hit on read
4. Write hit (WB/WT#=1)
5. External snoop hit on read
6. Read hit
7. Write hit
8. Read hit or write hit
9. Write back: external snoop hit on write (INV=1) or internal snoop hit or FLUSH# or INVD or WBINVD
10. Write back: external snoop hit on read
11. Read miss, line fill (WB/WT#=1)
12. External snoop hit on write (INV=1) or internal snoop hit or FLUSH# or INVD or WBINVD