Performing Signal Integrity Analyses

Summary

Tutorial
TU0113 (v1.2) December 12, 2005

This tutorial looks at performing Signal Integrity (SI) analyses. It covers setting up design parameters like design rules and Signal Integrity models, starting up Signal Integrity from the Schematic and PCB Editors, configuring the tests to be used in the net screening analysis, running further analysis on selected nets, terminating the signal line, setting preferences and working with the resulting waveforms.

With Altium Designer, you can analyze the Signal Integrity performance of a PCB from either the Schematic or the PCB Editors, evaluate net screening results against predefined tests, perform reflection and crosstalk analysis on selected nets, and display and manipulate the waveforms in the Waveform Analysis window.

Signal Integrity overview

Altium Designer includes pre-layout and post-layout Signal Integrity analysis capabilities. Altium Designer's Signal Integrity Analyzer uses sophisticated transmission line calculations and I/O buffer macro-model information as input for simulations. Based on a fast reflection and crosstalk simulator model, the Signal Integrity Analyzer produces accurate simulations using industry-proven algorithms.

Preliminary impedance and reflection simulations can be run from your source schematics prior to final board layout and routing. This allows you to address potential Signal Integrity issues, such as mismatched net impedances, before committing to board layout.

Full impedance, signal reflection and crosstalk analysis can be run on your final board (or a partially routed board) to check the real-world performance of your design. Signal Integrity screening is built into the Altium Designer design rules system, allowing you to check for Signal Integrity violations as part of the normal board DRC (Design Rule Checking) process. When Signal Integrity issues are found, Altium Designer shows you the effects of various termination options, allowing you to find the best solution before modifying your design.

Running a Signal Integrity analysis from a schematic only project

You can perform a Signal Integrity analysis on the design using only a schematic whenever there is no PCB as part of the project. The schematic must be part of a project, as analyses will not run on documents opened as Free Documents. There is no crosstalk analysis available because routed nets are required for this analysis.

When running in schematic only mode, default average track length and impedance can be defined using the SI Setup Options. The Signal Integrity Analyzer also reads the PCB design rules from the schematic for the stimulus and supply nets. These rules can be added as PCB Layout directives or Parameter Set directives on nets in the schematic.

From the Schematic Editor, with the schematic open, select **Tools » Signal Integrity** from the menus. This will first allow you to setup any necessary signal integrity models and then show the signal integrity panel from where you can view initial results and perform further analysis.

Running a Signal Integrity analysis from a PCB project

When running a Signal Integrity analysis from a PCB document, the PCB must be part of a project along with the related schematics. Note that you could also run Signal Integrity from any of the schematic documents in the project and it will have the same effect as running it from the PCB. This will allow both reflection and crosstalk analysis to be performed.

From the PCB Editor, select **Tools » Signal Integrity** which will proceed through the same process as that described above for the schematic only mode.

You can now have some (or none) of the schematic components in the PCB but any that have been placed must be linked with Component Links. This can be checked by selecting **Project » Component Links**. Note also that any unrouted nets will use the Manhattan length between pins to calculate a track length estimate for analysis purposes.

Before running Signal Integrity

In order to run a successful Signal Integrity analysis of the design and obtain accurate results, the following has to be performed before running the analysis.

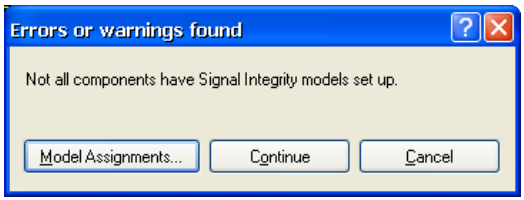
- It is important to note when simulating a net that to obtain meaningful simulation results you will need to have at least one integrated circuit (IC) with an output pin attached to that net. This pin will provide the stimulus for the net, giving the desired simulation results. Resistors, capacitors and inductors, for example, are passive components without a driving source and will therefore not provide simulation results on their own.
- The associated Signal Integrity model type for each component has to be correct. This is achieved via the *Model Assignments* dialog or by manually setting the correct entry for the **Type** field in the *Signal Integrity Model* dialog, when editing the Signal Integrity model associated to the component placed on the schematic source document. If this entry is not defined, the *Model Assignments* dialog will attempt to guess the type of the component based on its characteristics. For more information, see *Adding SI models using the Model Assignments dialog*.
- There must be Supply Nets design rules. Generally, there should be at least two rules, one for power nets and one for ground nets. The scope for these can be either net or net class. Supply nets cannot be analyzed in Signal Integrity. For more information, see *Signal Integrity design rules in Schematic* or *Signal Integrity design rules in PCB*.
- A Signal Stimulus design rule may be set up. You only need a stimulus rule if you want to override the default stimulus, so this is generally not required.
- The layer stack for the PCB must be set up correctly. The Signal Integrity Analyzer requires continuous power planes. Split planes are not supported, so the net that is assigned to the plane is used. If they are not present, they are assumed, so it is far better to add them and set them up appropriately. The thickness of all Layers, Cores and Prepreg must also be set correctly for the board. Use the **Design » Layer Stack Manager** command to set up the layer stack in the PCB Editor. When running Signal Integrity in the schematic only mode, a default two layer board with two

internal planes is used. You could create a blank PCB with a layer stack set up if more control was required.

Adding SI models using the *Model Assignments* dialog

The simplest way to add signal integrity models to your design is to use the *Model Assignments* dialog.

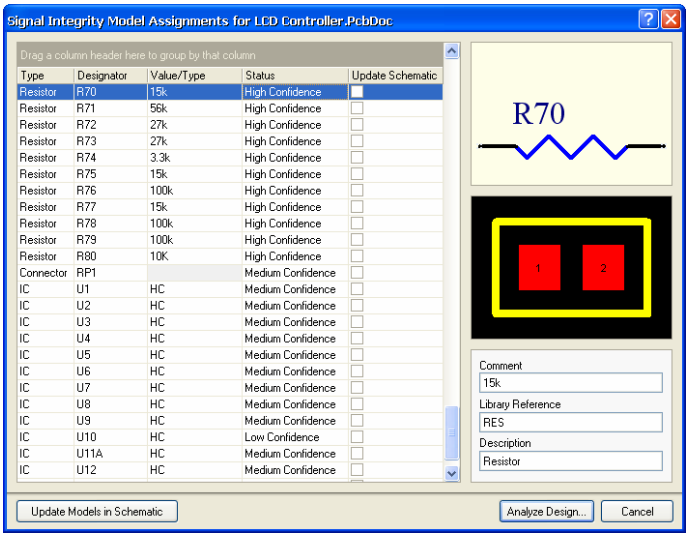
1. Select **Tools » Signal Integrity** from the menus. If you are just starting signal integrity on a project and there are components which do not have signal integrity models attached, you will be prompted by the *Errors or warning found* dialog to set up the model assignments using the *Model Assignments* dialog.



   Alternatively, if you have clicked **Continue** and the Signal Integrity panel is visible, it is possible to enter the *Model Assignments* dialog at any time by clicking the **Model Assignments** button. Note that doing so will cause all results to be cleared and recalculated since any changes to model assignments invalidate any existing results.

   If models have been already set up for all components, the *SI Setup Options* dialog will display. See *Setting up the SI Setup Options* later in this tutorial for more information.

2. If you click on **Model Assignments** in the *Errors or warnings found* dialog, the *Signal Integrity Models Assignments* dialog displays.



   When run, the *Model Assignments* dialog attempts to make educated guesses as to the necessary signal integrity model required for each component that does not contain a signal integrity model. All components, including those with models already defined (and the model information) will be displayed in the *Model Assignments* dialog. Each component will be assigned a status as described below.

Status	Definition
No match	The *Model Assignments* dialog was unable to find any characteristics linking this component to a particular type. It will likely need modification from the user to be set up correctly.
Low confidence	The *Model Assignments* dialog has selected a type for this component, but there was not strong evidence.
Medium confidence	The *Model Assignments* dialog has selected a type for this component and has reasonable confidence for the guess.
High confidence	The *Model Assignments* dialog has selected a type for this component and it fits most of the characteristics usually associated with this type of component.
Model found	An existing model was found for this component.
User modified	A component will change to this status once the user has modified it from the *Model Assignments* dialog's initial guess.
Model added	This status is used when the user has used the *Model Assignments* dialog to modify the schematic document to save the new model.

Modifying component models using the *Model Assignments* dialog

1. Select the component that you want to modify its model.
2. Select the correct type. There are seven types of components for Signal Integrity – resistor, capacitor, inductor, diode, BJT, connector and IC. The type of each component can be selected via a dropdown in that column or by using the right-click menu.
3. Set the value for a resistor, capacitor or inductor. If possible, the *Model Assignments* dialog will attempt to place the correct value for the component in this column based on the comment field and parameters on the component. If this requires modification (or is not present), this should be done at this point. The special case of part arrays (such as resistor arrays) is done via a separate dialog accessed by clicking in the column (see *Manually adding Signal Integrity models to components* for more details).
4. If the component is an IC, the choice of technology type is important as this will determine the characteristics of the pin models used in simulation. This can be selected via the dropdown list in the column or accessed through the right-click menu (**Change Technology**).
5. Finally, it may be necessary to specify more detail than allowed in the *Model Assignments* dialog, such as for IBIS models. This can be achieved by selecting **Advanced** from the right-click menu. See *Manually adding Signal Integrity models to components* for more details on this process.

Saving Models

Once models have been chosen for any or all of the components, the schematic documents can be updated to permanently store this information.

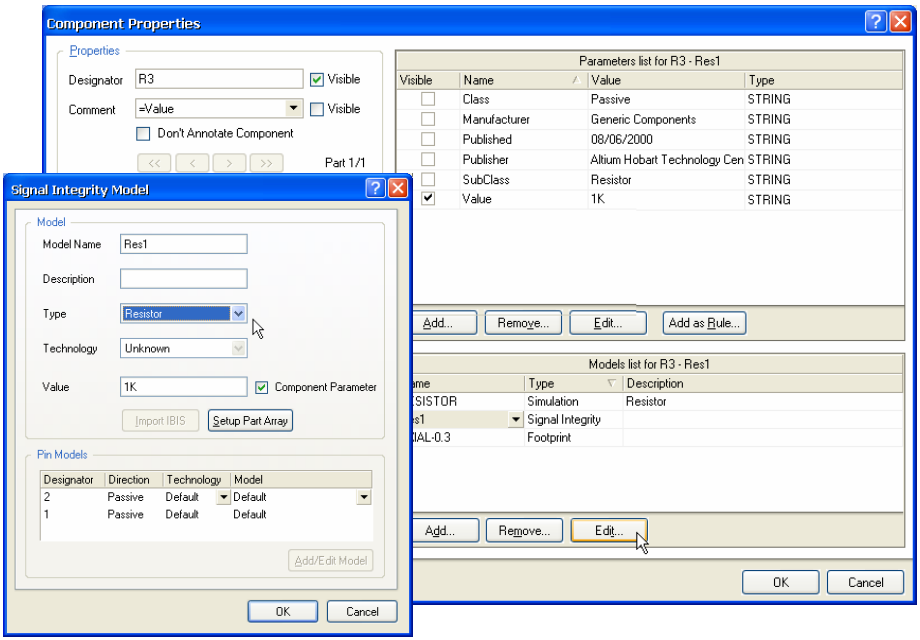
1. Check the **Update Schematic** column in the *Setup Signal Integrity* dialog for all components that are to be updated. Then click the **Update Models in Schematic** button.
2. All new Signal Integrity models (or modified existing ones) for each selected component will be added to the schematic documents. The schematic documents will need to be saved later.

   It is not necessary to save models to proceed with the Signal Integrity analysis process. If models are not saved, the analysis will proceed with all models configured as they are currently shown in the *Model Assignments* dialog. However, the next time the Signal Integrity tool is used, any changes will have been lost.

Manually adding Signal Integrity models to components

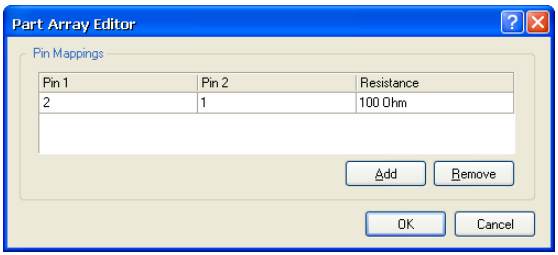
Signal Integrity models are linked into the integrated components. Signal Integrity models can also be included in the new integrated component libraries.

1. To add a Signal Integrity model to a placed component in the Schematic Editor, open the component's *Component Properties* dialog by double-clicking on it.



2. Click **Add** in the Model List and select **Signal Integrity** as the Model Type in the *Add New Model* dialog. Click **OK**. The *Signal Integrity Model* dialog displays.
3. Set up your model and click **OK**.

Setting up passive components



When setting up parts such as resistors and capacitors, it is usually sufficient to enter a type and a value. The value can be entered in the Value field and can be set as a parameter for the whole component.

There is also support for components like resistor arrays. This can be achieved by, after selecting the component type, clicking the **Setup Part Array** button in the *Signal Integrity Model* dialog. The *Part Array Editor* dialog allows the connections between pins and the value/model for those connections to be configured.

Setting up an IC

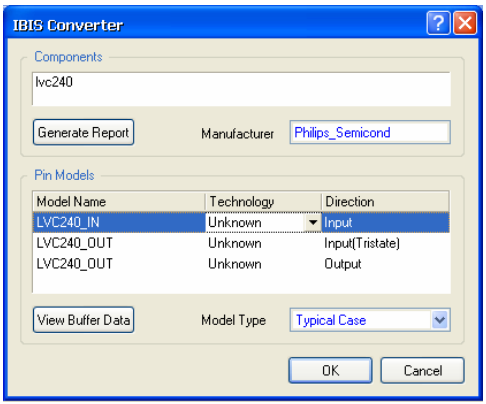
There are several alternatives when setting up an IC type model.

1. After selecting the type (IC), it is sufficient to simply choose a technology type. This will ensure that when simulating this component, the appropriate pin models for that technology will be used.
2. If more control is required, it is possible to assign specific technologies or pin models to individual pins. This can be done by selecting from the drop-down lists for the pins in the pin list at the bottom of the *Signal Integrity Model* dialog. Note that any changes here will override the base technology for the component.

Importing IBIS files

Another important option is the ability to import IBIS files.

1. To use an IBIS (Input/Output Buffer Information) file to specify an IC model's input and output characteristics, click on **Import IBIS** in the *Signal Integrity Model* dialog. Select the IBIS file from the *Open IBIS File* dialog and click **Open**. The *IBIS Converter* dialog displays.



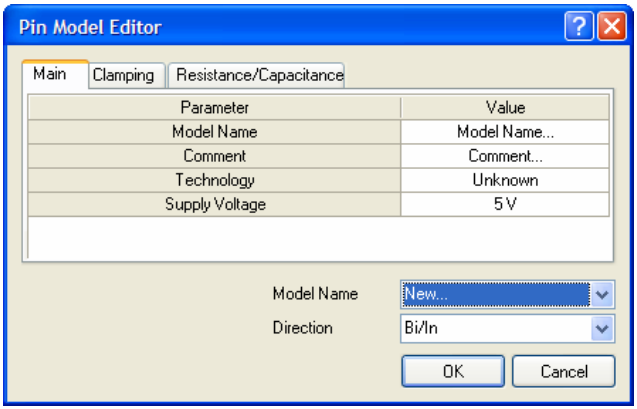
2. Select the required component contained in the IBIS file. Altium Designer will read the IBIS file and import the pin models from the IBIS file into the library of installed pin models. If a duplicate model is found, you will be asked if you wish to override the existing model. Additionally, all pins on the component will have the appropriate pin model assigned as specified in the IBIS file.

3. A report will automatically be generated stating which pins were successfully and unsuccessfully assigned. Further customization is possible by manually selecting the models for the appropriate pins as described above.
4. Click **OK** to complete importing the IBIS information and return to the *Signal Integrity Model* dialog.

Editing Pin Models

It is possible to add or edit an existing pin model by specifying various electrical characteristics of that pin. Note that this is also available for other types such as BJTs, Connectors and Diodes.

1. To modify pin models, click on the **Add/Edit Model** button in the *Signal Integrity Model* dialog, if this button is available for that type. The *Pin Model Editor* dialog displays.



2. Make the necessary changes and click **OK**.
3. If this is a new pin model, that model will now be available for selecting on the pins in this (and other) components.

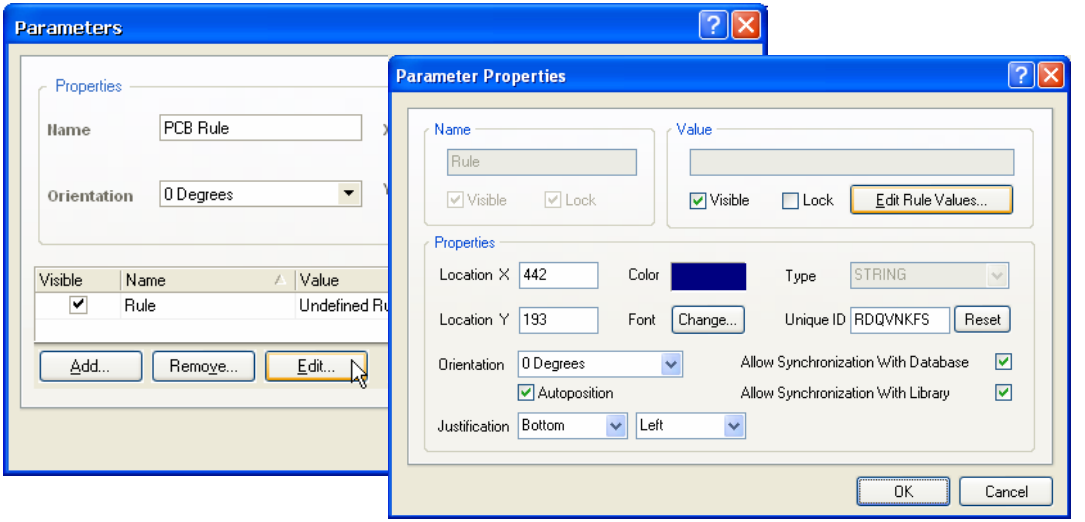
Signal Integrity design rules in Schematic

PCB specific design rules for Signal Integrity can be defined in the schematic if they are added as parameters. For Signal Integrity analysis, we need to add a PCB rule to identify the supply nets and their voltage. We will add a PCB directive to each of the supply nets on the schematic.

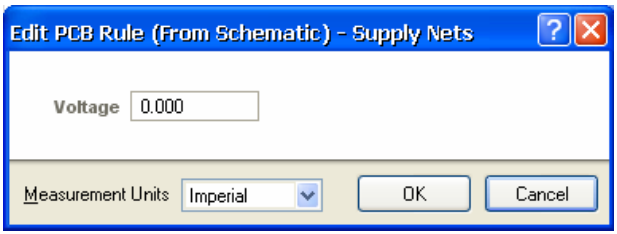
To add the supply nets design rule in the schematic:

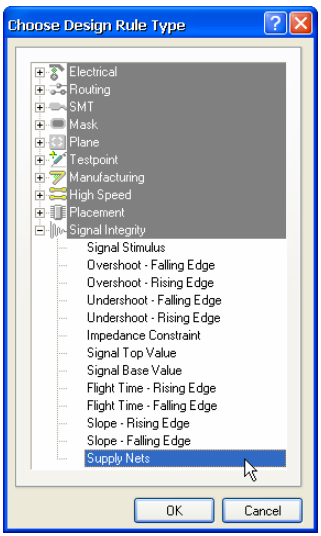
1. Select **Place » Directives » PCB Layout**. The directive will appear floating on the cursor.

2. Press the **TAB** key to display the *Parameters* dialog with an undefined rule already added.
3. Select the undefined rule and click on **Edit**. The *Parameter Properties* dialog displays.



4. Click on **Edit Rule Values** to display the *Choose Design Rule Type* dialog where the rule type can be chosen.
5. Scroll down to the Signal Integrity rules and select **Supply Nets**. Click **OK**. The *Edit PCB Rule (From Schematic)* dialog displays.





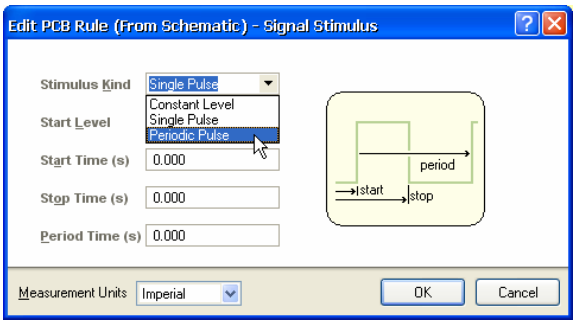
6. Enter the voltage for this supply net and click **OK**. Close all the dialogs by clicking **OK**.
7. Now you can place the PCB Rule directive on the appropriate net. A dot will appear when the directive is properly attached. After transferring the design to PCB layout, the rule is added to the PCB design rules (available for viewing and editing in the PCB Editor using the **Design » Rules** command).
8. Now create another PCB Rule directive for the GND net (voltage = 0) and any other supply nets in the design.
9. Right-click to end directive placement mode.

Note that in the Schematic Editor, the scope of the rule (the set of objects that the rule will target) is defined by where the parameter is added, e.g. on a wire or pin. In the PCB Editor, the scope of a rule is defined within the rule itself.

Signal Stimulus design rule

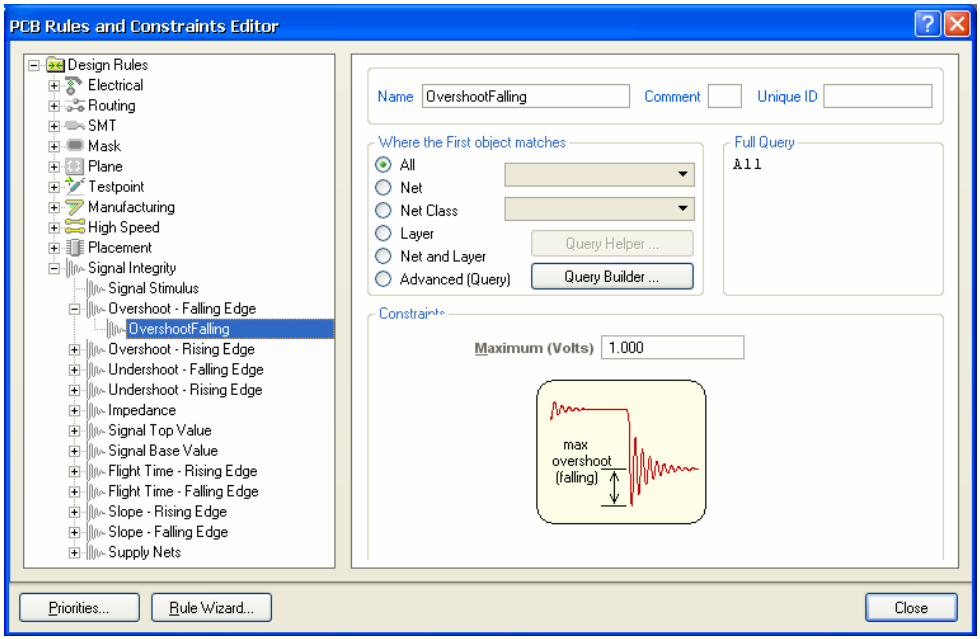
The other design rule that can be set up from within the Schematic Editor is the Signal Stimulus rule. When this rule is run, the stimulus is injected at each output pin on the net being analyzed. This requires a design rule that uses a scope of 'all', so you need to create a sheet parameter for this rule. If you do not set up this rule, the default rule options are used.

1. Select **Design » Document Options** in the Schematic Editor and click on the **Parameters** tab in the *Document Options* dialog to add a sheet parameter. Click on **Add as Rule** to display the *Parameter Properties* dialog.
2. Click on **Edit Rule Values** to display the *Choose Design Rule Type* dialog, scroll down to the Signal Integrity rules and select **Signal Stimulus**. Click **OK**. The *Edit PCB Rule (From Schematic) - Signal Stimulus* dialog displays.
3. Choose the stimulus kind, start level and times. Close the dialogs by clicking **OK**.



Signal Integrity design rules in PCB

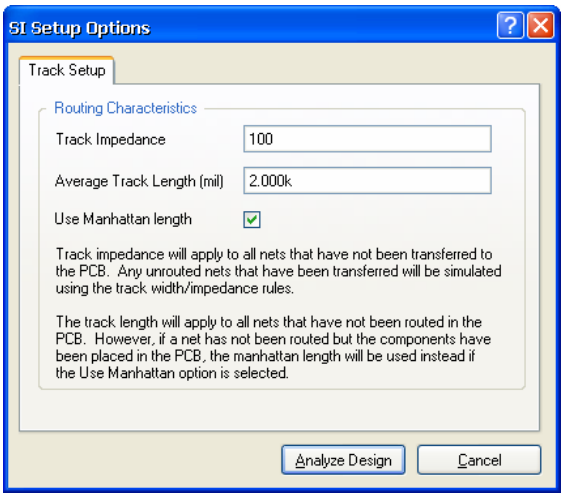
Signal Integrity parameters, such as overshoot, undershoot, impedance and signal slope requirements, can be specified as standard PCB design rules. Select **Design » Rules** in the PCB Editor to set up these rules. You can also set up these rules using parameters in the Schematic Editor and they will appear in the *PCB Rules and Constraint Editor* dialog after transferring the design to PCB layout.



These rules have two purposes. One is when running the standard DRC checks from within PCB; the board can be checked against these rules using the standard screening analysis. The second use for these rules is when using the Signal Integrity panel. These rules can be configured and enabled as tests and the panel will graphically display which nets have failed which tests.

Setting up the SI Setup Options

When you select **Tools » Signal Integrity** and all components have models assigned, the *SI Setup Options* dialog displays the first time you run this command on an open project.



1. Set the track impedance and average track length as required. These routing characteristics are only required if there are any nets not yet transferred to a PCB or unrouted nets in the PCB.

   Note that the Supply Nets and Stimulus tabs only display in schematic only mode.
2. Click on **Analyze Design** to run the initial default screening analysis and display the Signal Integrity panel from where you can further select the nets to analyze for reflection or crosstalk.

   Four default tolerance rules and any Signal Integrity rules set in the schematic or PCB are all enabled and run the first time the design is analyzed. These tolerances can be set later in the Signal Integrity panel by clicking on the **Menu** button and selecting **Set Tolerances**.

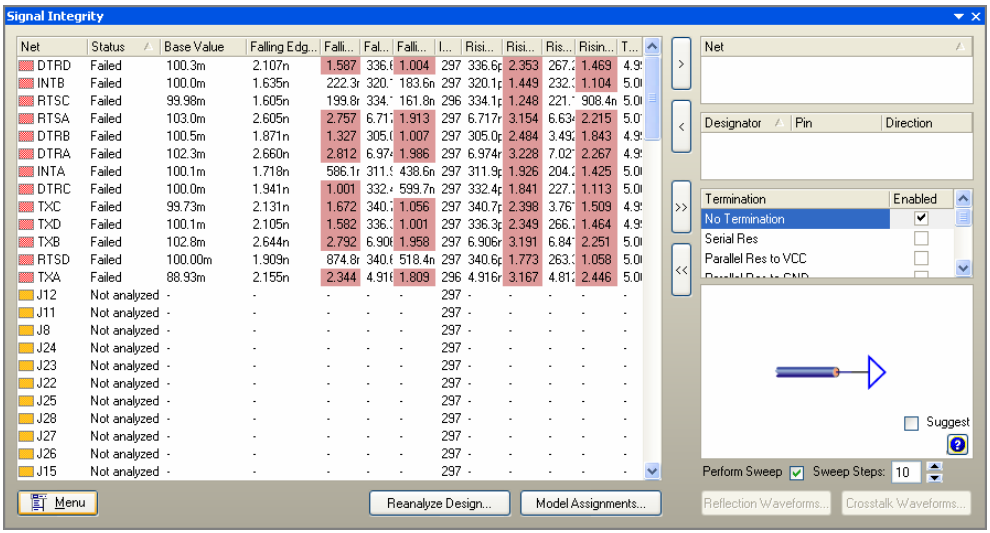
Signal Integrity Setup Options in schematic only mode

1. If there is no PCB available in the project, you can change the SI Setup Options in the Signal Integrity panel at any time by clicking on the **Menu** button and selecting **Setup Options**. The *SI Setup Options* dialog displays.
2. The **Track Setup** tab allows configuration of the default length of tracks when simulating. This is not used when a PCB is present as PCB uses width rules, i.e. if the Manhattan length is not checked, PCB uses this value. Set the Track Impedance in this tab as well.

3. Click on the **Supply Nets** and **Stimulus** tabs to display and enable net and stimulus rule information. These tabs allow another interface for defining these characteristics other than the normal method of providing rules on the PCB or schematic.

Using the Signal Integrity panel

After performing any initial set up, the Signal Integrity panel will be loaded with data from the screening analysis that has just been run. The results of this analysis and a display of which nets have passed the various tests are displayed in the list on the left side of the panel.



Note that there is only one copy of this panel in the system so running **Tools » Signal Integrity** again will clear the existing panel and reload it with a new set of results. This may be used to refresh the results after making changes to either the PCB or Schematic documents in the project or when starting to analyze a new project.

Viewing the screening results

The initial screening analysis provides a fast simulation of many nets to enable you to get more information and identify critical nets for closer examination, such as detailed reflection and/or crosstalk analysis. The left hand side list displays the results of this analysis.

Each net can be in one of three categories: Passed; Failed or Not Analyzed.

- A Passed net had all values inside the bounds defined by the tests.
- A Failed net had at least one value outside the defined tolerance levels. Any values that are failed are colored in light red.
- A Not Analyzed net could not be screened for some reason. To view the reason, right-click (or click on **Menu**), select **Show/Hide Columns** and enable the **Analysis Errors** column.

Failed nets

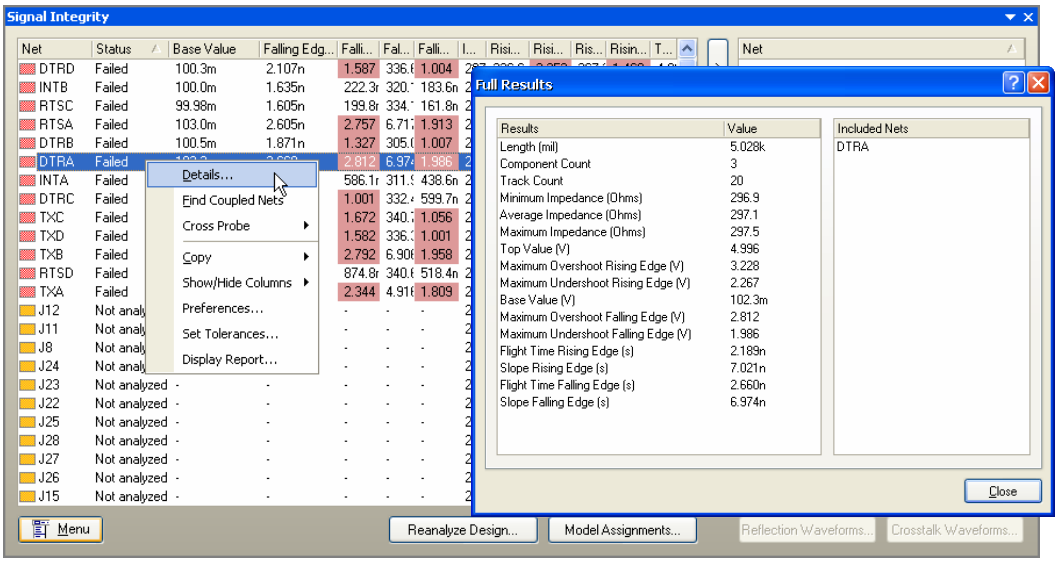
Common reasons for a failure to analyze a net in screening include containing a connector, diode or transistor, and no output pins or multiple output pins. When nets are screened which contain bi-directional pins and there is no dedicated output pin in the net, each bi-directional pin is simulated separately as an output pin. The worst-case result from these simulations is displayed. Note that even though a net could not be analyzed for screening, it may still be able to be checked in reflection and crosstalk simulations.

It is possible for nets to have other errors that will lead to incorrect analysis results in both screening and further simulations. These nets are highlighted in bright red. Also, nets that have been simulated (i.e. nets that are not yet routed on a PCB) are colored in light gray.

Checking Failed or Not Analyzed nets

To view the cause of a Failed or Not Analyzed net:

1. If the nets are highlighted in bright red, select a net and then right-click and select **Show Errors**. This also adds messages to the Messages panel, which can be cross-probed to repair any issues.
2. To view all available information for a selected net, right-click and select **Details**. The *Full Details* dialog shows all the information calculated from the screening analysis and other basic information.



3. Select **Cross Probe** from the right-click menu (or click on **Menu**) to cross probe (jump) to the selected net on either the schematic or the PCB. Use the **F4** shortcut key to toggle display between the Signal Integrity panel and your design.
4. Display which nets are coupled to either a single net or a group of nets by selecting the desired nets and then right-clicking and selecting **Find Coupled Nets**. This will select all nets that are coupled to these selected nets. The criteria for which nets are considered coupled can be configured in the *Preferences* dialog (accessed by clicking the **Menu** button and selecting **Preferences** in the Signal Integrity panel).

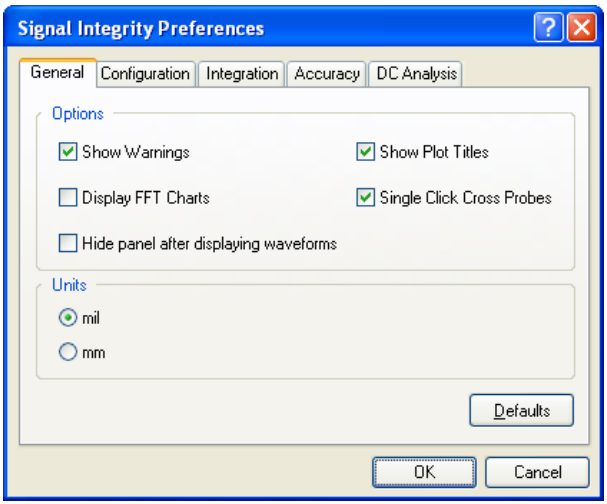
5. Useful information can be copied to the clipboard and pasted into other applications for further processing or reporting. Select the nets required and choose **Copy** from the right-click menu. Additionally, the displayed information can be customized by selecting which columns will be shown using the **Show/Hide Columns** command from the right-click menu.
6. A report highlighting the results generated by the analysis is also available by selecting **Display Report** from the right-click menu in the Signal Integrity panel. This opens the report file `Signal Integrity Tests Report.txt` in the Text Editor and adds it to the project.

Setting Preferences

You can specify various preferences that apply to all the analyses that you have defined. These include general settings, integration method and accuracy thresholds.

Any changes made to the preferences will apply to all projects. All preference settings are stored in the file named `SignalIntegrity.ini`, which is located in the `C:\Documents and Settings\User_name\Application Data\Altium Designer 6` folder.

1. Click on the **Menu** button in the Signal Integrity panel and select **Preferences** to open the *Signal Integrity Preferences* dialog.



2. Click on the related tab to set up preferences and click **OK**.
3. All Signal Integrity preferences can be returned to their defaults by clicking on the **Defaults** button in the *Signal Integrity Preferences* dialog.

General tab

Use this tab to set the error handling options that show hints and/or warnings when errors exist in the design that relate to performing a Signal Integrity analysis. Any hints or warnings encountered will be listed as messages in the Messages panel. If the **Show Warnings** option is enabled and warnings exist, a warning confirmation dialog will appear when trying to access the *Signal Integrity panel*. Additionally, you can opt to hide the Signal Integrity panel after choosing to display waveforms. You can also define the default units for Signal Integrity measurements, whether plot titles and FFT charts will be displayed when the resulting waveforms are shown in Waveform Analysis window.

Configuration tab

The Configuration tab defines various simulation-related thresholds, such as the maximum distance between coupled nets and the minimum length to be considered a coupled section.

Integration tab

This tab defines the numerical integration method used for analysis. The Trapezoidal method is relatively fast and accurate, but tends to oscillate under certain conditions. The Gear methods require longer analysis times, but tend to be more stable. Using a higher Gear order theoretically leads to more accurate results, but increases analysis time. The default is Trapezoidal.

Accuracy tab

The Accuracy tab in the *Signal Integrity Preferences* dialog defines tolerance thresholds and limit settings for various computational algorithms involved in the analysis.

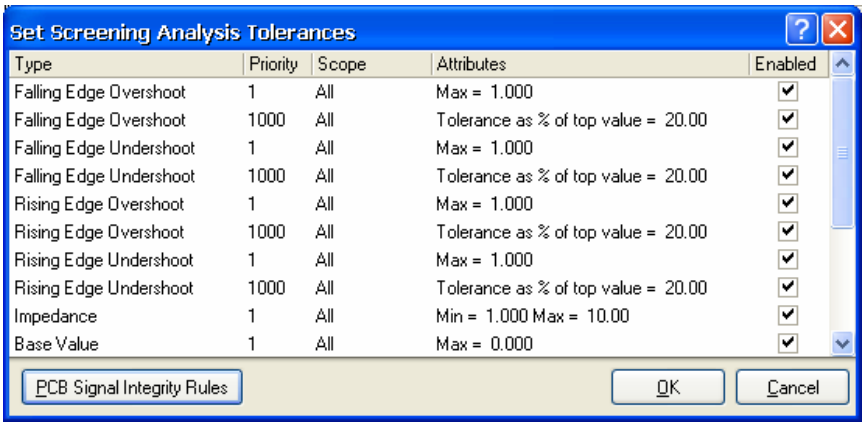
DC Analysis tab

Use this tab to define tolerance thresholds and limit settings for various parameters associated with DC Analysis.

Setting tolerances

Four default tolerance rules and any Signal Integrity rules set in the schematic or PCB are all enabled and run the first time the design is analyzed.

1. To enable or disable these rules, click on the **Menu** button in the Signal Integrity panel and select **Set Tolerances**. The *Set Screening Analysis Tolerances* dialog displays.



2. Click on the **Enabled** checkbox next to a rule type to enable that rule to run when the design is analyzed.
3. Click on **PCB Signal Integrity Rules** (if not in schematic only mode) to open the *PCB Rules and Constraints Editor* dialog where you can add or modify any Signal Integrity rules required. Click **OK** until you return to the Signal Integrity panel.

Preparing Analyses

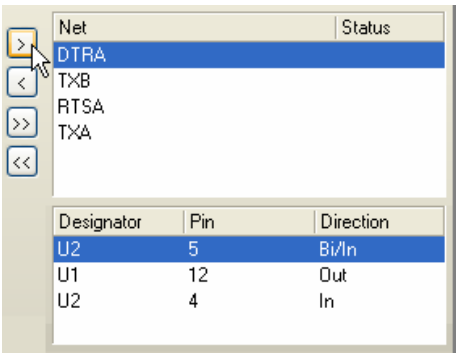
Before running the analyses, we must select the nets to further analyze. We can also Edit Buffers to view or change the component part technology and pin properties, and add terminations to nets, if required.

Selecting nets to analyze

To perform further analysis on nets (reflection and/or crosstalk) the nets must be selected in the right hand list of the Signal Integrity panel.

1. Double-click on a net in the left hand list to select it and move it to the right hand list.

   Alternatively, use the arrow buttons to move nets to and from this selected state. You can multi-select nets in the left hand list by holding down the **Shift** or **Ctrl** keys.



2. Once nets are in this selected state, it is possible to perform further configuration for them before running a simulation.

Setting victim and aggressor nets

In the case of Crosstalk analyses, it is necessary to set a victim or an aggressor net. Note that due to the nature of the analysis, this functionality is only available when two or more nets have been selected (moved to the right hand list).

1. Select a net in the right hand list of nets, right-click and select **Set Aggressor** or **Set Victim** as required. The status of the net is updated.
2. To unset the nets, select **Clear Status** from the right-click menu.

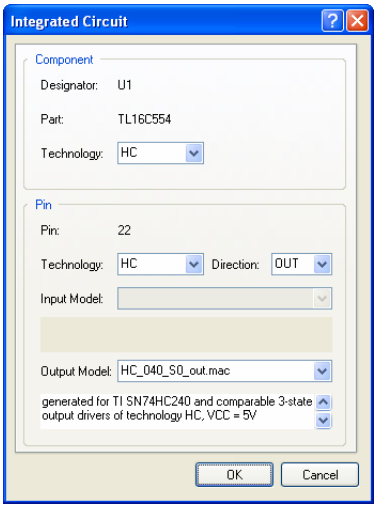
Setting the direction of bidirectional pins

It is possible to set the direction of bidirectional pins in a given net. To set the direction:

1. Select the affected net in the top right hand net list. This will then display a list of pins for that net below.
2. From the list of pins, change the in/out status for each selected bidirectional pin by right-clicking and choosing a status from the right-click menu. These in/out settings will be saved with the project for the next time you use this panel.

3. You can also cross probe to the relevant schematic or PCB document by selecting the **Cross Probe** options from the right-click menu.

Editing Buffers

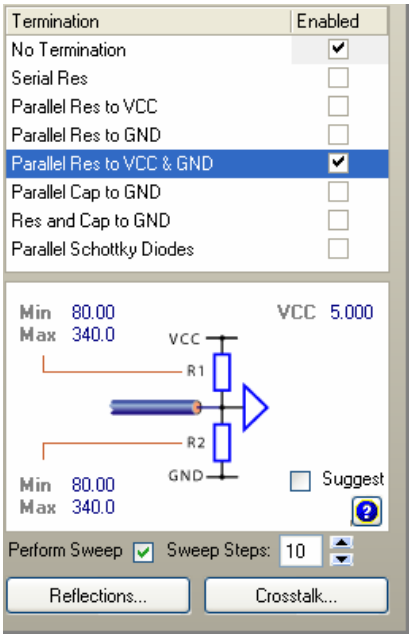


You may wish to view or change the component part technology and pin properties, such as input and output models and pin direction. You can only modify components that are attached to the currently selected net in the right net list. Using the **Edit Buffer** option under the right-click menu in the list of pins, gives access to the component's data dialog.

Note that you are really editing the properties of a pin rather than the whole component, even though you can change the component's technology. Any changes you make using the **Edit Buffer** button will override any technology/pin model setup created when you set up the Signal Integrity model in the schematic.

1. The dialog and options that appear will depend on the type of component the pin belongs to, e.g. resistor, IC, BJT, etc. The *Integrated Circuit* dialog shown is for an IC component type.
2. The Part Technology, Input Model and Output Model fields are context-sensitive. When you choose a Component Part Technology, the default models of the part are taken from this technology.
3. Choosing a Pin Technology and Direction will display a list of relevant input and/or output models to select from. Changes to the technology and direction are used locally in the analysis only and these will not be saved when the panel is reset. Make any necessary changes and click **OK**.

Terminations



The oscillations apparent on a signal waveform are due to multiple reflections on the associated transmission line (trace). These reflections, or 'ringing', occur most often in PCB designs because of driver/receiver impedance mismatch — usually where there is a low impedance driver and a high impedance receiver.

Getting good signal quality at the load would ideally mean zero reflections (no ringing). The level of ringing can be reduced to an acceptable level for the design using a termination.

The Signal Integrity panel incorporates a termination advisor, which enables you to insert 'virtual terminations' into a net at a location you define. In this way, you are free to test various termination strategies, without making physical changes to your board.

Termination simulations available are Series R, Parallel R to VCC, Parallel R to GND, Parallel R to VCC and GND, R and C to GND, Parallel C to GND and Parallel Schottky diodes.

Each termination type can be enabled or disabled in the termination list. When a reflection or crosstalk analysis is run, each enabled termination type will be tried and produce a separate set of waveforms. When the Serial Resistor termination is used, it will be placed on all output pins in the selected net. For other termination types, the termination will be placed on all input pins in the net.

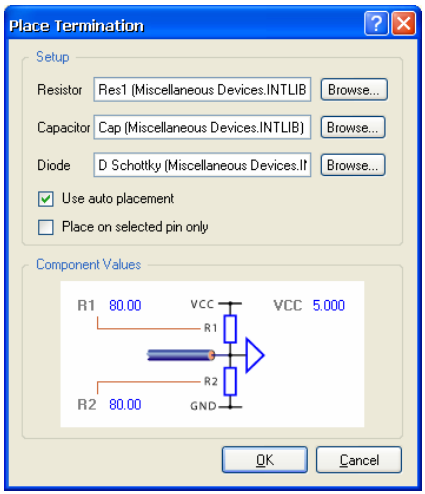
To achieve the best results for the terminations, it will also be necessary to set the value of the parts involved based on the characteristics of the net.

1. When a termination is selected, a diagram showing that termination is displayed below. This diagram will allow the setting of both minimum and maximum values for the resistors and capacitors used in the terminations.
2. Minimum and maximum values are used when the sweep count (shown in the list of terminations) is set to a number greater than one.
3. For more information about a termination type, select it and click the Help (?) button. If you enable the **Suggest** option, suggested values will be calculated (according to the formula noted in the information popup for each termination type) and displayed in light gray. You can accept these values or disable the Suggest option and enter your own values as required.
4. If you want to set up sweeps, ensure **Perform Sweep** is enabled and set the number of **Sweep Steps** required when the analyses are run. Note that a separate set of waveforms will be generated for each sweep for comparison purposes.

Placing a termination on the schematic

Once the waveforms have been created and the optimum termination detected, it may be desirable to place that termination directly on the schematic sheet. This can be achieved by the right-click menu in the termination list. Note that any placement will only apply to the currently selected net.

If you wish to actually place the selected termination circuit on the schematic rather than just use it as a 'virtual termination':

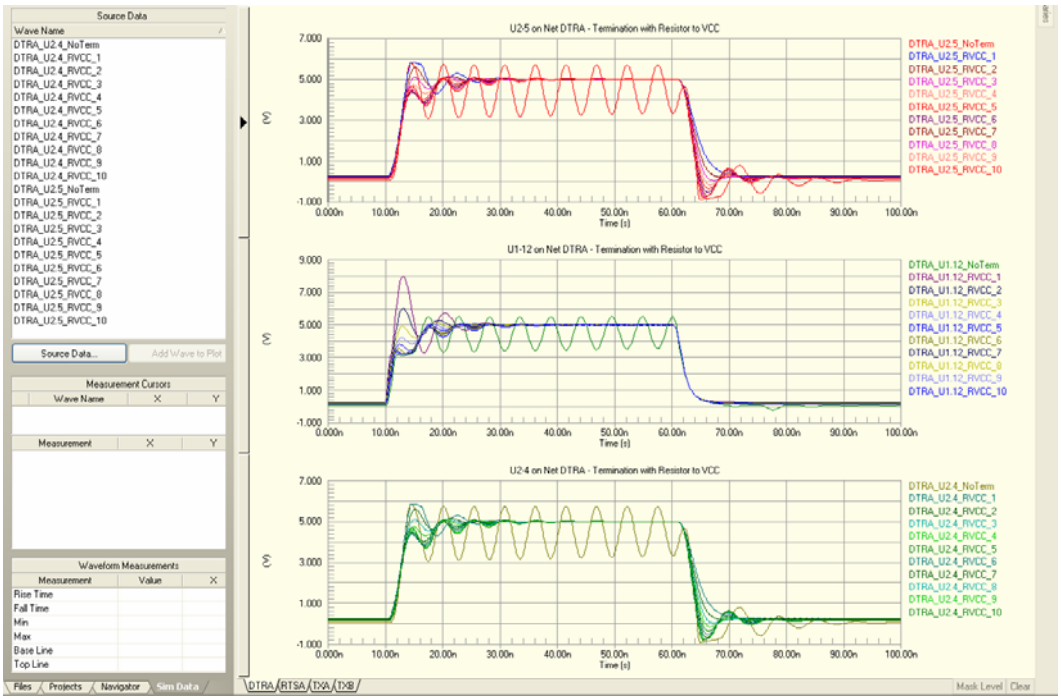


1. Right-click in the Termination section of the Signal Integrity panel and select **Place on Schematic**.
2. The *Place Termination* dialog displays allowing the setting of various properties such as which library components to use for the termination parts, whether to use automatic or manual placement, whether to place on all applicable pins or just the selected pin and the exact values to be used for the parts. Click **OK** to continue.
3. The Signal Integrity Analyzer finds the source schematic document that the pin belongs to. Then, in a free space on the document, it will add the necessary parts with the correct values (resistors, capacitors or whatever is required) and the power objects. Connect this termination circuit to the appropriate pin in the schematic.

   Note that it will still probably be necessary after this to wire the components correctly to the pin. Additionally, if there is a PCB involved as well, these will need to be synchronized and routed in the PCB. Synchronize the PCB to add these parts as well by selecting **Design » Update PCB**.

Running the Analyses

1. Once the nets have been configured as necessary (and any termination options chosen), click the **Reflections** or the **Crosstalks** button in the Signal Integrity panel to generate the waveforms.
2. The analysis commences and a simulation waveform file (`PCBDesignName.sdf`) is generated. This file appears in the **Projects** panel under the `Generated\Simulation documents` folder and opens as a separate tab, displaying the results of the analyses in the Waveform Analysis window of the Simulation Data Editor.
3. For each net you have selected, a chart is generated and displays in the Waveform Analysis window.



Reflection

For a Reflection analysis, one or more nets can be simulated. The number should be kept to a reasonable amount however, as analysis time will increase considerably when analyzing high numbers of nets.

The Signal Integrity Analyzer calculates voltages at nodes of a net using routing and layer information from the PCB and associated driver and receiver I/O buffer models. A 2D-field solver automatically calculates the electrical characterization of the transmission lines. Modeling assumes that DC path losses are small enough to be ignored.

For each net that has been selected, a chart is generated as the result of the simulation with its tab in the Waveform Analysis window marked by the name of the net. The chart will contain waveforms for all termination options.

Crosstalk

For a Crosstalk analysis, at least two nets must be taken over. Two or three nets would normally be considered at any one time when performing a crosstalk analysis, usually a net and its two immediate neighbors.

The level of crosstalk (or the extent of EMI) is directly proportional to the reflections on a signal line. If the signal quality conditions are achieved and reflections are brought down to a near-negligible level through correct signal termination, i.e. the signal is delivered to its destination with minimal signal stray and crosstalk will also be minimized. See *Terminations* for more information.

In a crosstalk analysis, all nets will be displayed in a chart named `Crosstalk Analysis`.

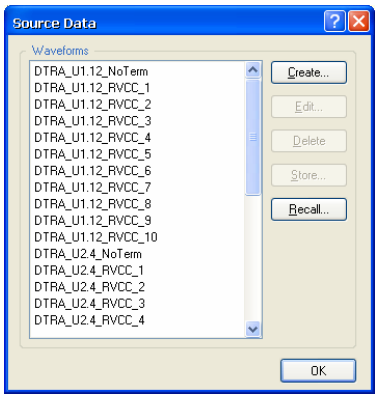
Using the Waveform Analysis window

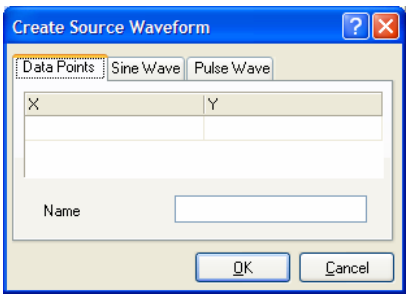
The Simulation Data Editor's Waveform Analysis window comprises one or more tabs that correspond to the different simulation analyses performed. Each tab contains a chart that can contain multiple wave plots. A wave plot can have multiple waveforms and a waveform represents the simulation data. From this window, you can display up to four scaled plots simultaneously.

Choosing Source Data

The initial source data consists of all nets taken over during the Signal Integrity setup and listed in the Waveforms section of the SimData panel. You can further define the list of possible source simulation waveforms that can be used in the active chart.

1. Select **Chart » Source Data**, or click on the **Source Data** button in the **Sim Data** panel and the *Source Data* dialog displays. The dialog lists all source simulation waveforms that can be used with the active chart.
2. Clicking the **Create** button will open the *Create Source Waveform* dialog, from where you can define a new waveform by entering a series of X Y value pairs for a series of data points, or create a custom sine or pulse wave.





3. Create a new signal waveform and click on **Create** and the waveform will be added to the available waveform list in the SimData panel.
4. The *Source Data* dialog also enables you to store any of the waveforms as ASCII text files (`WaveformName.wdf`). These waveform files can be recalled (loaded) into the list at any time.

5. You can edit user-defined waveforms, generated using the **Create** button, by clicking on the **Edit** button. See *Editing user-defined waveforms* for more information.

Working with waveforms

Selecting the active chart and plot

Select a chart by clicking on its tab name at the bottom of the Waveform Analysis window. Make a particular plot active by clicking anywhere within the area of the wave plot.

Document Options

If the Number of Plots Visible option is set to **All** in the *Document Options* dialog (**Tools » Document Options** or right-click in the Waveform Analysis window and select **Document Options**), the active wave plot is distinguished by a black solid line around its waveform name section.

If the Number of Plots Visible option is set to 1, 2, 3 or 4, the active wave plot is distinguished by a black arrow at the left hand side of its display area.

Selecting waveforms

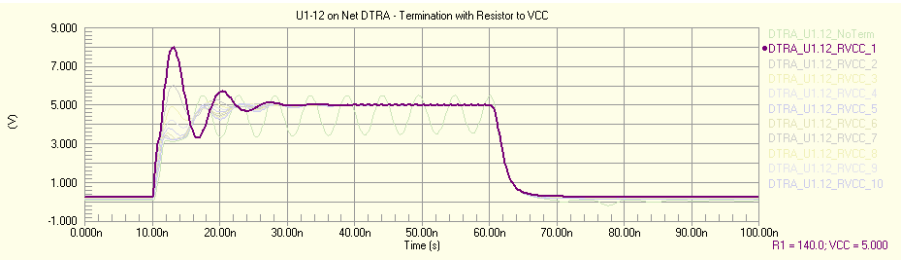
A waveform is selected by clicking on its name in the Waveform Analysis window. A selected waveform will become bolder in color, a dot appears next to the name and the other waveforms will become masked (dimmed). Click on the **Mask Level** button to set the masking contrast and use the **Clear** button (shortcut **Shift+C**, or ESC) to clear any masking and display all for selection.

You can also use the arrow keys or the mouse wheel to move up and down the waveform names. If there are more waveform names than can be displayed on the plot, click on the scrolling arrows that appear to see the entire list.

You can highlight all waves in the same sweep if you enable the **Highlight Similar Waves** option in the *Document Options* dialog.

Zooming in on waveforms

You can drag a selection box around a section of a waveform to zoom in for a closer look. To view the entire waveform again, select **Fit Document** from the right-click menu.



Moving waveforms

If you wish to move a waveform from one wave plot to another, click on the waveform name and drag it to the name area of the required wave plot.

Viewing a waveform in its own wave plot

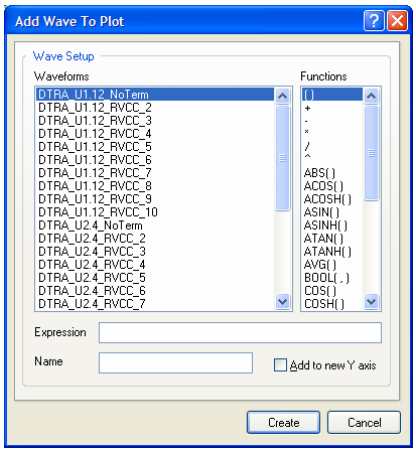
If you wish to view a waveform in its own wave plot:

1. Make sure the Number of Plots Visible is set to **All** (**Tools » Document Options**).
2. Click on the waveform name and drag to either an existing blank wave plot or to a point beyond the last wave plot in the chart. A new wave plot is created.

Adding waveforms to a plot

To add a new waveform into the active wave plot of the current chart:

1. Make the wave plot that you want to add the new waveform to active in the Waveform Analysis window by clicking anywhere within the area of the wave plot.
2. Select **Wave » Add Wave** and the *Add Wave to Plot* dialog displays.
3. Choose a waveform from the list of all available simulation waveforms. If required, you can also create a mathematical expression that uses one or more base waveforms to create a new waveform by adding functions to the expression.



4. Click **Create** and the waveform will be added to the active wave plot.

Editing user-defined waveforms

While you can edit user-defined waveforms that have been manually created using the *Create Source Waveform* dialog, you cannot edit waveforms that have been generated as a result of design simulation. To change these waveforms, you would need to change the circuit, PCB or the setup and rerun the Signal Integrity analysis.

The Edit Wave command allows you to also create new expressions from existing waveforms.

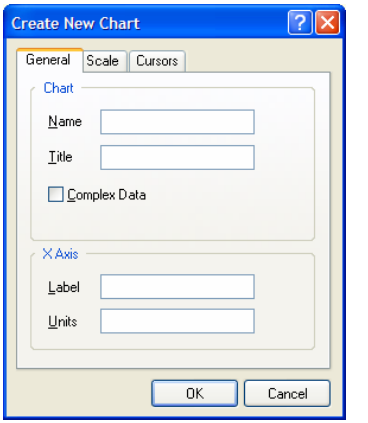
1. Make sure that the waveform you wish to edit is selected in the Waveform Analysis window by clicking on the waveform name.
2. Select **Wave » Edit Wave**. The *Edit Waveform* dialog displays.
3. Use this dialog to either create a new waveform using a mathematical expression involving the selected waveform, or change the waveform completely by choosing a new waveform from the list of all available waveforms.

Saving and recalling waveforms

You can save waveforms as ASCII text files by selecting **Tools » Store Waveform** and saving it as in the format of `WaveformName.wdf`. A `.wdf` file contains the waveform as a series of data points, each represented by an X Y value pair. Please note that once user-defined waveforms have been stored and recalled, they can no longer be edited.

Recall a saved waveform by selecting **Tools » Recall Waveform** and choosing a `.wdf` file from the *Recall Stored Waveform* dialog. The waveform will be recalled and loaded into the list of possible source simulation data waveforms for the active chart.

Creating new charts



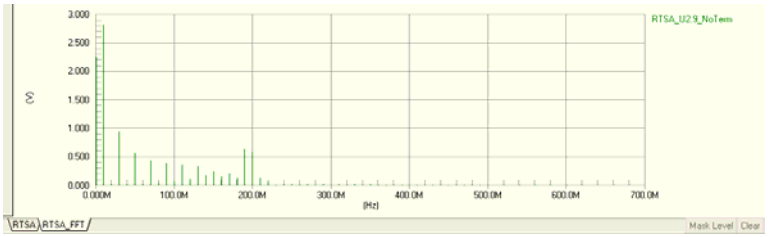
You can create new charts that are added to the current `.sdf` file.

1. Select **Chart » New Chart** to display the *Create New Chart* dialog.
2. Define a name and title for the chart and also the title and units for the X-axis. You can also specify whether or not complex data can be displayed in the chart.
3. Click **OK** and a new blank chart will appear in the Waveform Analysis window, added as a tab after the last chart in the document.

Creating a FFT chart

Performing a Fast Fourier Transform (FFT) on the active chart displays the results in a new chart.

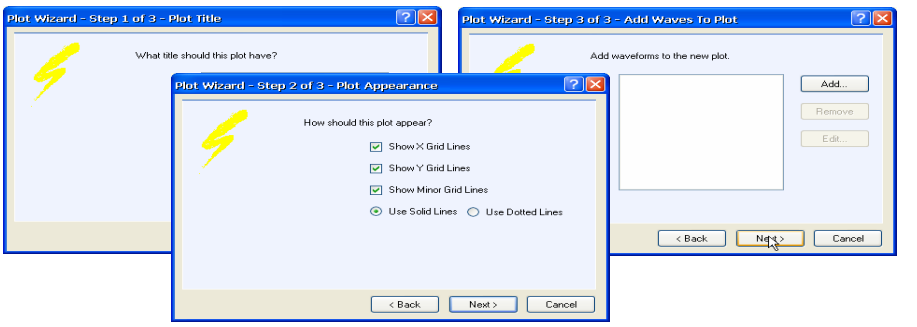
1. Select the chart you wish to perform a Fast Fourier Transform on by clicking on the required analysis tab at the bottom of the Waveform Analysis window.
2. Select **Chart » Create FFT Chart**. The FFT will be performed and the results displayed in a new chart which is added as a new tab (<netname>_FFT) and made the active chart in the window.



Creating new plots

You can add new plots to existing or new charts using the Plot Wizard.

1. Select **Plot » New Plot**. The first page of the Plot Wizard displays. Give the new plot a name and click **Next**.

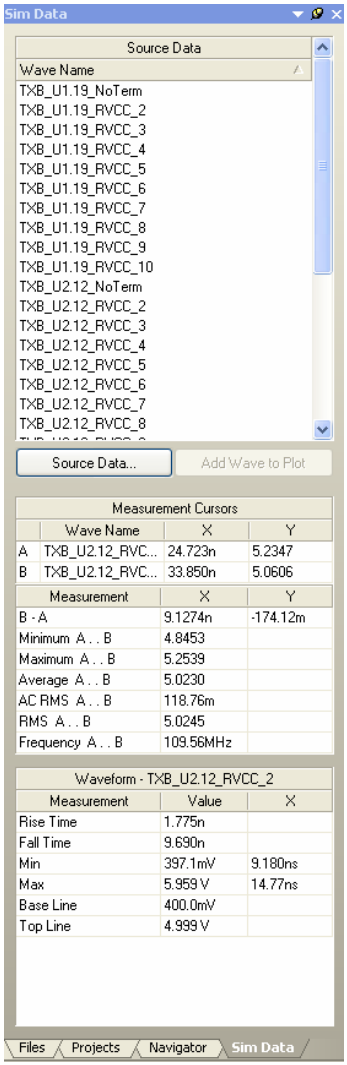


2. Set up the appearance of the plot and click **Next**.
3. Select the waveforms to plot by clicking on the **Add** button in the *Add Wave to Plot* dialog, select the waveform (or add an expression) and click **Create**.
4. Click **Next** to continue and click **Finish** to exit the wizard. The new plot displays in the Waveform Analysis window.

Using the SimData panel

The SimData panel enables you to add waveforms from the available source data to the active wave plot and obtain measurement information based on the selected waveform and measurements calculated using the measurement cursors.

The Waveform section at the top of the panel contains a list of all available source data signal waveforms for the simulation that you have performed. This is the same list that appears in the *Source Data* dialog (**Chart » Source Data**). Click on **Source Data** to open the *Source Data* dialog.



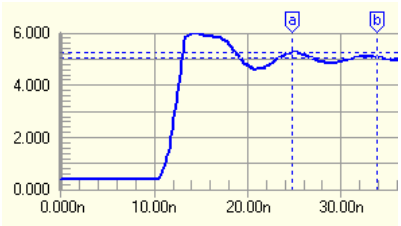
Adding a waveform to a plot from the SimData panel

Click on the **Add Wave to Plot** button in the Sim Data panel to add the selected waveforms to the currently selected plot in the Waveform Analysis window.

Measurement cursors

The Measurement Cursors section of the panel reflects the current and calculated measurements when using one or both of the measurement cursors.

1. The two measurement cursors (A and B) are available by right-clicking on a selected waveform's name in the Waveform Analysis window. Drag the cursors by their tabs to the location required.



2. For both cursors, the name of the waveform the cursor is currently assigned to is shown, as well as X and Y axis data values, dependent on the cursor's position along the waveform.
3. The calculated X and Y values appear in the Measurement Cursors section of the SimData panel.

Waveform measurements

The Waveform Measurements section of the dialog shows various general measurements for the waveform selected in the Waveform Analysis window, such as Rise and Fall times.

After analyzing your results

Once you have analyzed your results, you can experiment, for example, with various terminations to bring down any ringing on the selected nets. You may also need to make changes to your circuit or PCB and rerun your Signal Integrity analyses until the desired results are reached.

Revision History

Date	Version No.	Revision
9-Dec-2003	1.0	New product release
08-Jul-05	1.1	Update for Altium Designer SP4
12-Dec-2005	1.2	Path references updated for Altium Designer 6