KSZ8041NL/RNL

10Base-T/100Base-TX Physical Layer Transceiver

Data Sheet Rev. 1.4

General Description

The KSZ8041NL is a single supply 10Base-T/100Base-TX Physical Layer Transceiver, which provides MII/RMII interfaces to transmit and receive data. A unique mixed signal design extends signaling distance while reducing power consumption.

HP Auto MDI/MDI-X provides the most robust solution for eliminating the need to differentiate between crossover and straight-through cables.

The KSZ8041NL represents a new level of features and performance and is an ideal choice of physical layer transceiver for 10Base-T/100Base-TX applications.

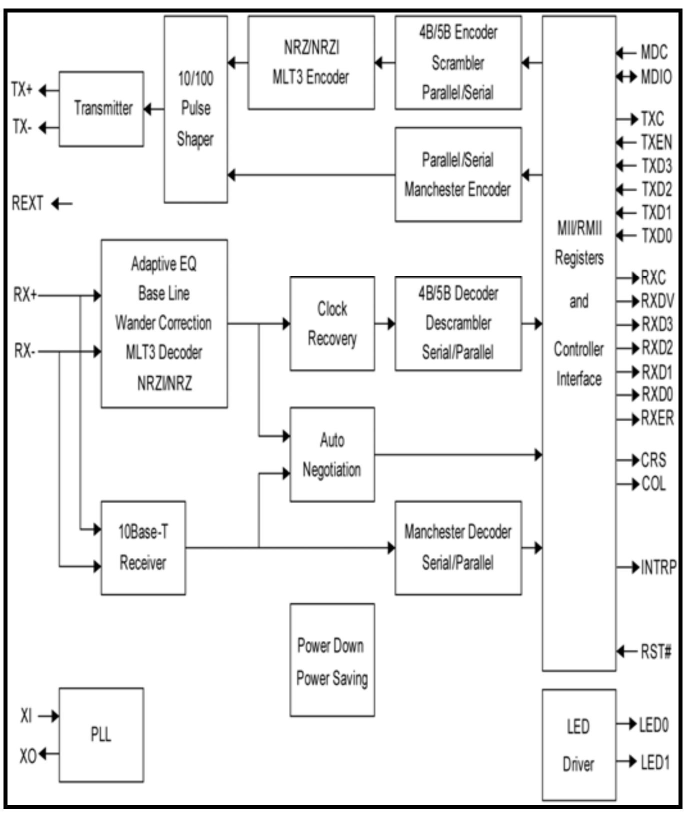
The KSZ8041RNL is an enhanced RMII version of the KSZ8041NL that does not require a 50MHz system clock. It uses a 25MHz crystal for its input reference clock and outputs a 50MHz RMII reference clock to the MAC.

The KSZ8041NL and KSZ8041RNL are available in 32-pin, lead-free MLF® (QFN per JDEC) packages (See Ordering Information).

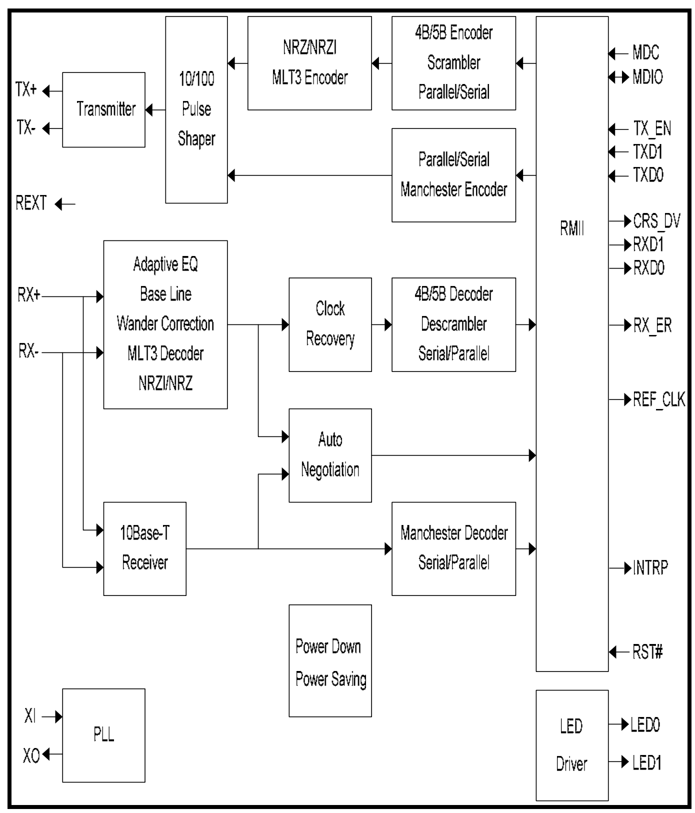
Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Diagram

KSZ8041NL



KSZ8041RNL



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Features

- Single-chip 10Base-T/100Base-TX physical layer solution
- Fully compliant to IEEE 802.3u Standard
- Low power CMOS design, power consumption of <180mW
- HP auto MDI/MDI-X for reliable detection and correction for straight-through and crossover cables with disable and enable option
- Robust operation over standard cables
- Power down and power saving modes
- MII interface support (KSZ8041NL only)
- RMII interface support with external 50MHz system clock (KSZ8041NL only)
- RMII interface support with 25MHz crystal/clock input and 50MHz reference clock output to MAC (KSZ8041RNL only)
- MIIM (MDC/MDIO) management bus to 6.25MHz for rapid PHY register configuration
- Interrupt pin option
- Programmable LED outputs for link, activity and speed
- ESD rating (6kV)
- Single power supply (3.3V)
- Built-in 1.8V regulator for core
- Available in 32-pin (5mm x 5mm) MLF® package

Applications

- Printer
- LOM
- Game Console
- IPTV
- IP Phone
- IP Set-top Box

Ordering Information

Part Number	Temp. Range	Package	Lead Finish	Description
KSZ8041NL	0°C to 70°C	32-Pin MLF®	Pb-Free	MII / RMII, Commercial Temperature
KSZ8041NLI (1)	-40°C to 85°C	32-Pin MLF®	Pb-Free	MII / RMII, Industrial Temperature
KSZ8041NL AM(1)	-40°C to 85°C	32-Pin MLF®	Pb-Free	MII / RMII, Automotive Qualified Device
KSZ8041RNL	0°C to 70°C	32-Pin MLF®	Pb-Free	RMII with 50MHz clock output, Commercial Temperature
KSZ8041RNLI (1)	-40°C to 85°C	32-Pin MLF®	Pb-Free	RMII with 50MHz clock output, Industrial Temperature

Note:

1. Contact factory for lead time.

Revision History

Revision	Date	Summary of Changes
1.0	10/13/06	Data sheet created.
1.1	4/27/07	Added maximum MDC clock speed. Added 40K +/-30% to note 1 of Pin Description and Strapping Options tables for internal pull-ups/pull-downs. Changed Model Number in Register 3h – PHY Identifier 2. Changed polarity (swapped definition) of DUPLEX strapping pin. Removed DUPLEX strapping pin update to Register 4h – Auto-Negotiation Advertisement bits [8, 6]. Set “Disable power saving” as the default for Register 1Fh bit [10]. Corrected LED1 (pin 31) definition for Activity in LED mode 01. Added Symbol Error to MII/RMII Receive Error description and Register 15h – RXER Counter. Added a 100pF capacitor on REXT (pin 10) in Pin Description table.
1.2	7/18/08	Added Automotive Qualified part number to Ordering Information. Added maximum case temperature. Added thermal resistance (θ_{JC}). Added chip maximum current consumption.
1.3	12/11/09	Added Automotive Qualified part number, KSZ8041NL EAM, to Ordering Information. Changed MDIO hold time (min) from 10ns to 4ns. Added LED drive current. Renamed Register 3h bits [3:0] to “manufacturer’s revision number” and changed default value to “Indicates silicon revision.” Updated RMII output delay for CRSDV and RXD[1:0] output pins. Added support for Asymmetric PAUSE in register 4h bit [11]. Added control bits for 100Base-TX preamble restore (register 14h bit [7]) and 10Base-T preamble restore (register 14h bit [6]). Changed strapping pin definition for CONFIG[2:0] = 100 from “PCS Loopback” to “MII 100Mbps Preamble Restore.” Corrected MII timing for t_{RLAT}, t_{CRS1}, t_{CRS2}. Added KSZ8041RNL device and updated entire data sheet accordingly.
1.4	01/19/10	Removed part number (KSZ8041NL EAM) from Ordering Information. Removed chip maximum current consumption.

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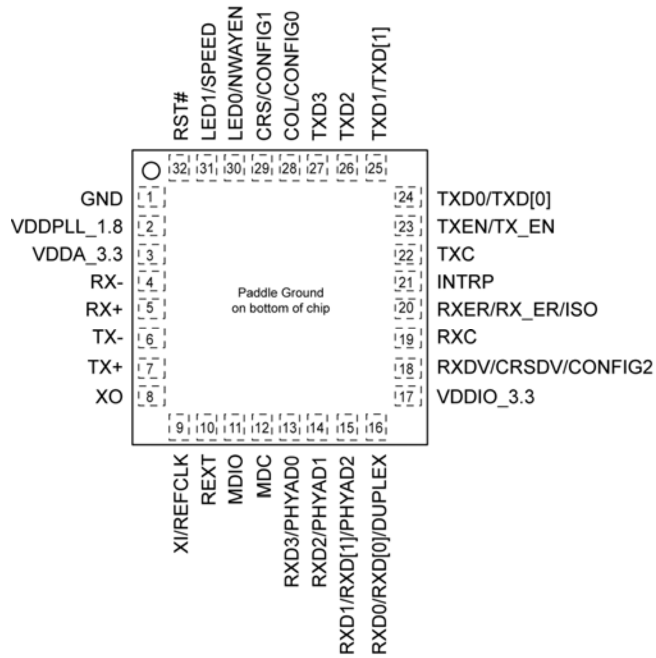
Pin Configuration – KSZ8041NL



32-Pin (5mm x 5mm) MLF®

Pin Description – KSZ8041NL

Pin Number	Pin Name	Type[(1)]	Pin Function
1	GND	Gnd	Ground
2	VDDPLL_1.8	P	1.8V analog V_{DD}
3	VDDA_3.3	P	3.3V analog V_{DD}
4	RX-	I/O	Physical receive or transmit signal (- differential)
5	RX+	I/O	Physical receive or transmit signal (+ differential)
6	TX-	I/O	Physical transmit or receive signal (- differential)
7	TX+	I/O	Physical transmit or receive signal (+ differential)
8	XO	O	Crystal feedback This pin is used only in MII mode when a 25 MHz crystal is used. This pin is a no connect if oscillator or external clock source is used, or if RMII mode is selected.
9	XI / REFCLK	I	Crystal / Oscillator / External Clock Input MII Mode: 25MHz +/-50ppm (crystal, oscillator, or external clock) RMII Mode: 50MHz +/-50ppm (oscillator, or external clock only)
10	REXT	I/O	Set physical transmit output current Connect a 6.49KΩ resistor in parallel with a 100pF capacitor to ground on this pin. See KSZ8041NL reference schematics.
11	MDIO	I/O	Management Interface (MII) Data I/O This pin requires an external 4.7KΩ pull-up resistor.
12	MDC	I	Management Interface (MII) Clock Input This pin is synchronous to the MDIO data interface.
13	RXD3 / PHYAD0	Ipu/O	MII Mode: Receive Data Output[3][(2)] / Config Mode: The pull-up/pull-down value is latched as PHYADDR[0] during power-up / reset. See “Strapping Options” section for details.
14	RXD2 / PHYAD1	Ipd/O	MII Mode: Receive Data Output[2][(2)] / Config Mode: The pull-up/pull-down value is latched as PHYADDR[1] during power-up / reset. See “Strapping Options” section for details.
15	RXD1 / RXD[1] / PHYAD2	Ipd/O	MII Mode: Receive Data Output[1][(2)] / RMII Mode: Receive Data Output[1][(3)] / Config Mode: The pull-up/pull-down value is latched as PHYADDR[2] during power-up / reset. See “Strapping Options” section for details.
16	RXD0 / RXD[0] / DUPLEX	Ipu/O	MII Mode: Receive Data Output[0][(2)] / RMII Mode: Receive Data Output[0][(3)] / Config Mode: Latched as DUPLEX (register 0h, bit 8) during power-up / reset. See “Strapping Options” section for details.
17	VDDIO_3.3	P	3.3V digital V_{DD}
18	RXDV / CRSDV / CONFIG2	Ipd/O	MII Mode: Receive Data Valid Output / RMII Mode: Carrier Sense/Receive Data Valid Output / Config Mode: The pull-up/pull-down value is latched as CONFIG2 during power-up / reset. See “Strapping Options” section for details.
19	RXC	O	MII Mode: Receive Clock Output

Pin Description – KSZ8041NL (Continued)

Pin Number	Pin Name	Type[1]	Pin Function	
20	RXER / RX_ER / ISO	Ipd/O	MII Mode: RMII Mode: Config Mode:	Receive Error Output / Receive Error Output / The pull-up/pull-down value is latched as ISOLATE during power-up / reset. See “Strapping Options” section for details.
21	INTRP	Opu	Interrupt Output:	Programmable Interrupt Output
			Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 9 sets the interrupt output to active low (default) or active high.	
22	TXC	O	MII Mode:	Transmit Clock Output
23	TXEN / TX_EN	I	MII Mode: RMII Mode:	Transmit Enable Input / Transmit Enable Input
24	TXD0 / TXD[0]	I	MII Mode: RMII Mode:	Transmit Data Input[0][4] / Transmit Data Input[0][5]
25	TXD1 / TXD[1]	I	MII Mode: RMII Mode:	Transmit Data Input[1][4] / Transmit Data Input[1][5]
26	TXD2	I	MII Mode:	Transmit Data Input[2][4] /
27	TXD3	I	MII Mode:	Transmit Data Input[3][4] /
28	COL / CONFIG0	Ipd/O	MII Mode: Config Mode:	Collision Detect Output / The pull-up/pull-down value is latched as CONFIG0 during power-up / reset. See “Strapping Options” section for details.
29	CRS / CONFIG1	Ipd/O	MII Mode: Config Mode:	Carrier Sense Output / The pull-up/pull-down value is latched as CONFIG1 during power-up / reset. See “Strapping Options” section for details.

Pin Description – KSZ8041NL (Continued)

Pin Number	Pin Name	Type(1)	Pin Function
30	LED0 / NWAYEN	Ipu/O	LED Output: Programmable LED0 Output / Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up / reset. See “Strapping Options” section for details. The LED0 pin is programmable via register 1Eh bits [15:14], and is defined as follows. **LED mode = [00]** **Link/Activity** / **Pin State** / **LED Definition** No Link / H / OFF Link / L / ON Activity / Toggle / Blinking **LED mode = [01]** **Link** / **Pin State** / **LED Definition** No Link / H / OFF Link / L / ON **LED mode = [10]** Reserved **LED mode = [11]** Reserved

Pin Description – KSZ8041NL (Continued)

Pin Number	Pin Name	Type[(1)]	Pin Function
31	LED1 / SPEED	Ipu/O	LED Output: Programmable LED1 Output / Config Mode: Latched as SPEED (register 0h, bit 13) during power-up / reset. See “Strapping Options” section for details. The LED1 pin is programmable via register 1Eh bits [15:14], and is defined as follows. **LED mode = [00]** **Speed** **Pin State** **LED Definition** 10BT H OFF 100BT L ON **LED mode = [01]** **Activity** **Pin State** **LED Definition** No Activity H OFF Activity Toggle Blinking **LED mode = [10]** Reserved **LED mode = [11]** Reserved
32	RST#	I	Chip Reset (active low)
PADDLE	GND	Gnd	Ground

Notes:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipd = Input with internal pull-down (40K +/-30%).
   Ipu = Input with internal pull-up (40K +/-30%).
   Opu = Output with internal pull-up (40K +/-30%).
   Ipu/O = Input with internal pull-up (40K +/-30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K +/-30%) during power-up/reset; output pin otherwise.
2. MII Rx Mode: The RXD[3..0] bits are synchronous with RXCLK. When RXDV is asserted, RXD[3..0] presents valid data to MAC through the MII. RXD[3..0] is invalid when RXDV is de-asserted.
3. RMII Rx Mode: The RXD[1:0] bits are synchronous with REF_CLK. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent from the PHY.
4. MII Tx Mode: The TXD[3..0] bits are synchronous with TXCLK. When TXEN is asserted, TXD[3..0] presents valid data from the MAC through the MII. TXD[3..0] has no effect when TXEN is de-asserted.
5. RMII Tx Mode: The TXD[1:0] bits are synchronous with REF_CLK. For each clock period in which TX_EN is asserted, two bits of data are received by the PHY from the MAC.

Strapping Options – KSZ8041NL

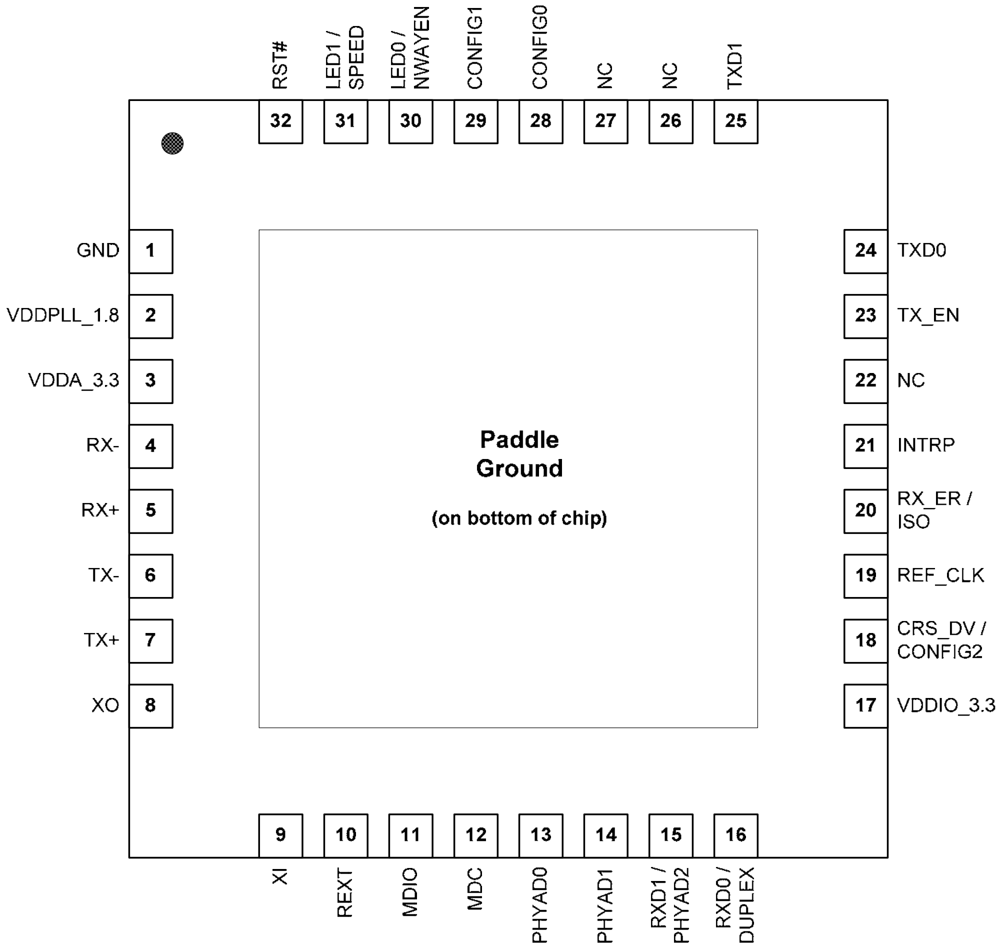
Pin Number	Pin Name	Type[(1)]	Pin Function
15 14 13	PHYAD2 PHYAD1 PHYAD0	Ipd/O Ipd/O Ipu/O	The PHY Address is latched at power-up / reset and is configurable to any value from 1 to 7. The default PHY Address is 00001. PHY Address bits [4:3] are always set to ‘00’.
18 29 28	CONFIG2 CONFIG1 CONFIG0	Ipd/O Ipd/O Ipd/O	The CONFIG[2:0] strap-in pins are latched at power-up / reset and are defined as follows: **CONFIG[2:0]** **Mode** 000 MII (default) 001 RMII 010 Reserved – not used 011 Reserved – not used 100 MII 100Mbps Preamble Restore 101 Reserved – not used 110 Reserved – not used 111 Reserved – not used
20	ISO	Ipd/O	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable During power-up / reset, this pin value is latched into register 0h bit 10.
31	SPEED	Ipu/O	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps During power-up / reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.
16	DUPLEX	Ipu/O	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex During power-up / reset, this pin value is latched into register 0h bit 8 as the Duplex Mode.
30	NWAYEN	Ipu/O	Nway Auto-Negotiation Enable Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation During power-up / reset, this pin value is latched into register 0h bit 12.

Note:

1. Ipu/O = Input with internal pull-up (40K +/-30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K +/-30%) during power-up/reset; output pin otherwise.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may drive high during power-up or reset, and consequently cause the PHY strap-in pins on the MII/RMII signals to be latched high. In this case, it is recommended to add 1K pull-downs on these PHY strap-in pins to ensure the PHY does not strap-in to ISOLATE mode, or is not configured with an incorrect PHY Address.

Pin Configuration – KSZ8041RNL



32-Pin (5mm x 5mm) MLF®

Pin Description – KSZ8041RNL

Pin Number	Pin Name	Type[1]	Pin Function
1	GND	Gnd	Ground
2	VDDPLL_1.8	P	1.8V analog V_{DD}
3	VDDA_3.3	P	3.3V analog V_{DD}
4	RX-	I/O	Physical receive or transmit signal (- differential)
5	RX+	I/O	Physical receive or transmit signal (+ differential)
6	TX-	I/O	Physical transmit or receive signal (- differential)
7	TX+	I/O	Physical transmit or receive signal (+ differential)
8	XO	O	Crystal feedback – for 25 MHz crystal This pin is a no connect if oscillator or external clock source is used.
9	XI	I	Crystal / Oscillator / External Clock Input 25MHz +/-50ppm
10	REXT	I/O	Set physical transmit output current Connect a 6.49KΩ resistor in parallel with a 100pF capacitor to ground on this pin. See KSZ8041RNL reference schematics.
11	MDIO	I/O	Management Interface (MII) Data I/O This pin requires an external 4.7KΩ pull-up resistor.
12	MDC	I	Management Interface (MII) Clock Input This pin is synchronous to the MDIO data interface.
13	PHYAD0	Ipu/O	The pull-up/pull-down value is latched as PHYADDR[0] during power-up / reset. See “Strapping Options” section for details.
14	PHYAD1	Ipd/O	The pull-up/pull-down value is latched as PHYADDR[1] during power-up / reset. See “Strapping Options” section for details.
15	RXD1 / PHYAD2	Ipd/O	RMII Mode: RMII Receive Data Output[1][2] / Config Mode: The pull-up/pull-down value is latched as PHYADDR[2] during power-up / reset. See “Strapping Options” section for details.
16	RXD0 / DUPLEX	Ipu/O	RMII Mode: RMII Receive Data Output[0][2] / Config Mode: Latched as DUPLEX (register 0h, bit 8) during power-up / reset. See “Strapping Options” section for details.
17	VDDIO_3.3	P	3.3V digital V_{DD}
18	CRS_DV / CONFIG2	Ipd/O	RMII Mode: Carrier Sense/Receive Data Valid Output / Config Mode: The pull-up/pull-down value is latched as CONFIG2 during power-up / reset. See “Strapping Options” section for details.
19	REF_CLK	O	50MHz Clock Output This pin provides the 50MHz RMII reference clock output to the MAC.
20	RX_ER / ISO	Ipd/O	RMII Mode: RMII Receive Error Output / Config Mode: The pull-up/pull-down value is latched as ISOLATE during power-up / reset. See “Strapping Options” section for details.
21	INTRP	Opu	Interrupt Output: Programmable Interrupt Output Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 9 sets the interrupt output to active low (default) or active high.
22	NC	O	No connect
23	TX_EN	I	RMII Transmit Enable Input

Pin Description – KSZ8041RNL (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[1]</th><th>Pin Function</th></tr>
<tr><td>24</td><td>TXD0</td><td>I</td><td>RMII Transmit Data Input[0][3]</td></tr>
<tr><td>25</td><td>TXD1</td><td>I</td><td>RMII Transmit Data Input[1][3]</td></tr>
<tr><td>26</td><td>NC</td><td>I</td><td>No connect</td></tr>
<tr><td>27</td><td>NC</td><td>I</td><td>No connect</td></tr>
<tr><td>28</td><td>CONFIG0</td><td>Ipd/O</td><td>The pull-up/pull-down value is latched as CONFIG0 during power-up / reset. See “Strapping Options” section for details.</td></tr>
<tr><td>29</td><td>CONFIG1</td><td>Ipd/O</td><td>The pull-up/pull-down value is latched as CONFIG1 during power-up / reset. See “Strapping Options” section for details.</td></tr>
<tr><td>30</td><td>LED0 /
NWAYEN</td><td>Ipu/O</td><td>LED Output: Programmable LED0 Output /
Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up / reset. See “Strapping Options” section for details.
The LED0 pin is programmable via register 1Eh bits [15:14], and is defined as follows.

LED mode = [00]
<table>
<tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>
LED mode = [01]
<table>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
</table>
<u>LED mode = [10] , [11]</u> Reserved</td></tr>
</table>

Pin Description – KSZ8041RNL (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[1]</th><th>Pin Function</th></tr>
<tr><td>31</td><td>LED1 /
SPEED</td><td>Ipu/O</td><td>LED Output: Programmable LED1 Output /
Config Mode: Latched as SPEED (register 0h, bit 13) during power-up / reset. See “Strapping Options” section for details.
The LED1 pin is programmable via register 1Eh bits [15:14], and is defined as follows.

LED mode = [00]
Speed / Pin State / LED Definition
10BT / H / OFF
100BT / L / ON

LED mode = [01]
Activity / Pin State / LED Definition
No Activity / H / OFF
Activity / Toggle / Blinking

<u>LED mode = [10], [11]</u> Reserved</td></tr>
<tr><td>32</td><td>RST#</td><td>I</td><td>Chip Reset (active low)</td></tr>
<tr><td>PADDLE</td><td>GND</td><td>Gnd</td><td>Ground</td></tr>
</table>

Notes:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Opu = Output with internal pull-up (40K +/-30%).
   Ipu/O = Input with internal pull-up (40K +/-30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K +/-30%) during power-up/reset; output pin otherwise.
2. RMII Rx Mode: The RXD[1:0] bits are synchronous with REF_CLK. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent from the PHY.
3. RMII Tx Mode: The TXD[1:0] bits are synchronous with REF_CLK. For each clock period in which TX_EN is asserted, two bits of data are received by the PHY from the MAC.

Strapping Options – KSZ8041RNL

Pin Number	Pin Name	Type[(1)]	Pin Function
15 14 13	PHYAD2 PHYAD1 PHYAD0	Ipd/O Ipd/O Ipu/O	The PHY Address is latched at power-up / reset and is configurable to any value from 1 to 7. The default PHY Address is 00001. PHY Address bits [4:3] are always set to ‘00’.
18 29 28	CONFIG2 CONFIG1 CONFIG0	Ipd/O Ipd/O Ipd/O	The CONFIG[2:0] strap-in pins are latched at power-up / reset and are defined as follows: **CONFIG[2:0]** **Mode** 000 Reserved – not used 001 RMII 010 Reserved – not used 011 Reserved – not used 100 Reserved – not used 101 Reserved – not used 110 Reserved – not used 111 Reserved – not used
20	ISO	Ipd/O	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable During power-up / reset, this pin value is latched into register 0h bit 10.
31	SPEED	Ipu/O	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps During power-up / reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.
16	DUPLEX	Ipu/O	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex During power-up / reset, this pin value is latched into register 0h bit 8 as the Duplex Mode.
30	NWAYEN	Ipu/O	Nway Auto-Negotiation Enable Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation During power-up / reset, this pin value is latched into register 0h bit 12.

Note:

1. Ipu/O = Input with internal pull-up (40K +/-30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K +/-30%) during power-up/reset; output pin otherwise.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may drive high during power-up or reset, and consequently cause the PHY strap-in pins on the RMII signals to be latched high. In this case, it is recommended to add 1K pull-downs on these PHY strap-in pins to ensure the PHY does not strap-in to ISOLATE mode, or is not configured with an incorrect PHY Address.

Functional Description

The KSZ8041NL is a single 3.3V supply Fast Ethernet transceiver. It is fully compliant with the IEEE 802.3u Specification.

On the media side, the KSZ8041NL supports 10Base-T and 100Base-TX with HP auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

The KSZ8041NL offers a choice of MII or RMII data interface connection with the MAC processor. The MII management bus option gives the MAC processor complete access to the KSZ8041NL control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size.

The KSZ8041RNL is an enhanced RMII version of the KSZ8041NL that does not require a 50MHz system clock. It uses a 25MHz crystal for its input reference clock and outputs a 50MHz RMII reference clock to the MAC.

100Base-TX Transmit

The 100Base-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output.

The output current is set by an external 6.49kΩ 1% resistor for the 1:1 transformer ratio. It has typical rise/fall times of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitter. The wave-shaped 10Base-T output drivers are also incorporated into the 100Base-TX drivers.

100Base-TX Receive

The 100Base-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

PLL Clock Synthesizer

The KSZ8041NL/RNL generates 125MHz, 25MHz and 20MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal or oscillator. For the KSZ8041NL in RMII mode, these internal clocks are generated from an external 50MHz oscillator or system clock.

Scrambler/De-scrambler (100Base-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander.

10Base-T Transmit

The 10Base-T drivers are incorporated with the 100Base-TX drivers to allow for transmission using the same magnetic. The drivers also perform internal wave-shaping and pre-emphasize, and output 10Base-T signals with a typical amplitude of 2.5V peak. The 10Base-T signals have harmonic contents that are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10Base-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RX+ and RX- inputs from falsely trigger the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8041NL/RNL decodes a data frame. The receive clock is kept active during idle periods in between data reception.

SQE and Jabber Function (10Base-T only)

In 10Base-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE Test is required as a test of the 10Base-T transmit/receive path. If transmit enable (TXEN) is high for more than 20 ms (jabbering), the 10Base-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250 ms, the 10Base-T transmitter is re-enabled and COL is de-asserted (returns to low).

Auto-Negotiation

The KSZ8041NL/RNL conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3u specification. Auto-negotiation is enabled by either hardware pin strapping (pin 30) or software (register 0h bit 12).

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation. Link partners advertise their capabilities to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest.

- Priority 1: 100Base-TX, full-duplex
- Priority 2: 100Base-TX, half-duplex
- Priority 3: 10Base-T, full-duplex
- Priority 4: 10Base-T, half-duplex

If auto-negotiation is not supported or the KSZ8041NL/RNL link partner is forced to bypass auto-negotiation, the KSZ8041NL/RNL sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8041NL/RNL to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

The auto-negotiation link up process is shown in the flow chart illustrated as Figure 1.

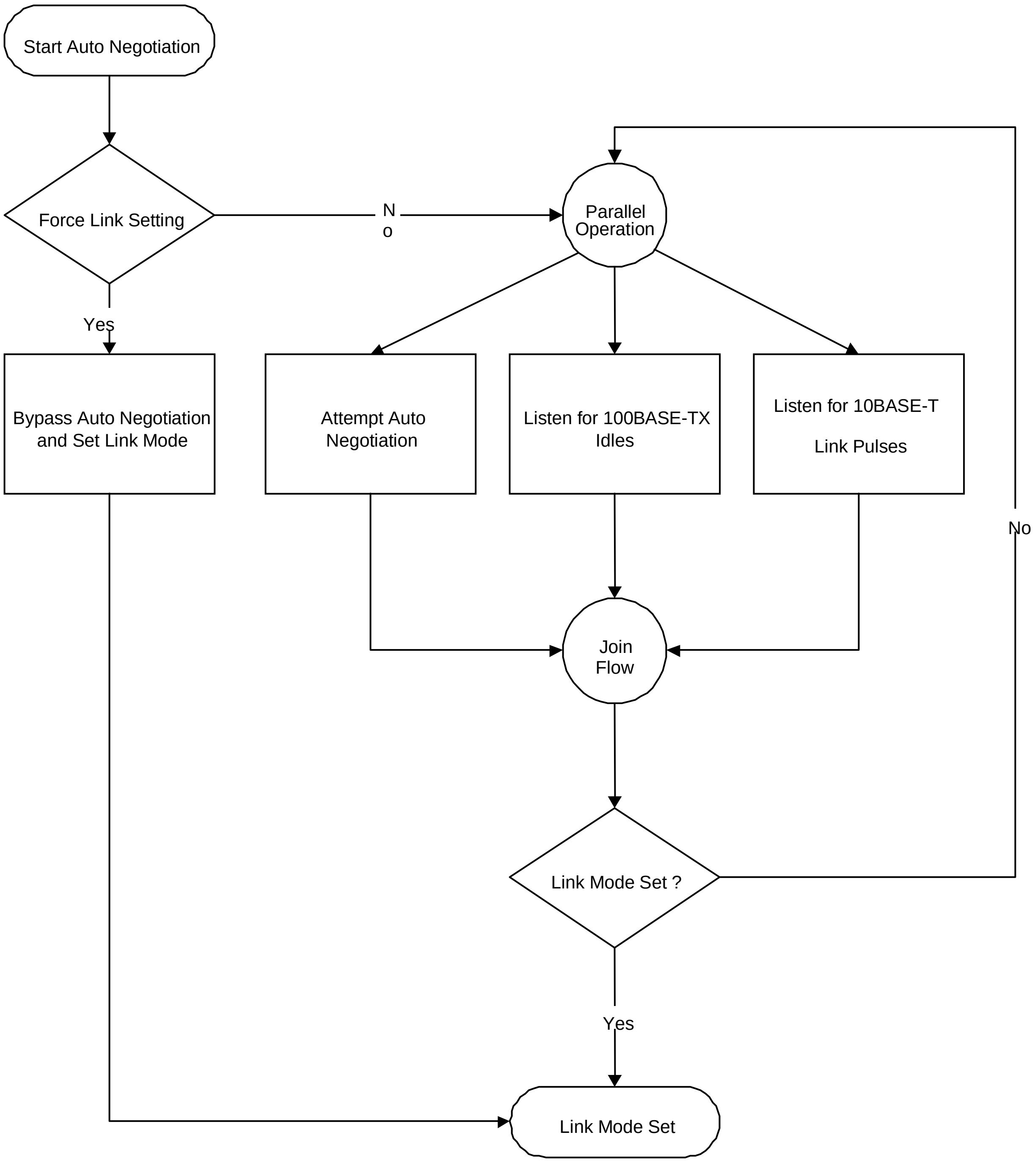


Figure 1. Auto-Negotiation Flow Chart

MII Management (MIIM) Interface

The KSZ8041NL/RNL supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input / Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the KSZ8041NL/RNL. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. Further details on the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows a external controller to communicate with one or more PHY devices. Each KSZ8041NL/RNL device is assigned a unique PHY address between 1 and 7 by its PHYAD[2:0] strapping pins. Also, every KSZ8041NL/RNL device supports the broadcast PHY address 0, as defined per the IEEE 802.3 Specification, which can be used to read/write to a single KSZ8041NL/RNL device, or write to multiple KSZ8041NL/RNL devices simultaneously.
- A set of 16-bit MDIO registers. Register [0:6] are required, and their functions are defined per the IEEE 802.3 Specification. The additional registers are provided for expanded functionality.

The Table 1 shows the MII Management frame format for the KSZ8041NL/RNL.

	Preamble	**Start of Frame**	**Read/Write OP Code**	**PHY Address Bits [4:0]**	**REG Address Bits [4:0]**	**TA**	**Data Bits [15:0]**	**Idle**
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

Table 1. MII Management Frame Format

Interrupt (INTRP)

INTRP (pin 21) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the KSZ8041NL/RNL PHY register. Bits[15:8] of register 1Bh are the interrupt control bits, and are used to enable and disable the conditions for asserting the INTRP signal. Bits[7:0] of register 1Bh are the interrupt status bits, and are used to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 1Bh.

Bit 9 of register 1Fh sets the interrupt level to active high or active low.

MII Data Interface (KSZ8041NL only)

The Media Independent Interface (MII) is specified in Clause 22 of the IEEE 802.3 Specification. It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10Mbps and 100Mbps data rates.
- Uses a 25MHz reference clock, sourced by the PHY.
- Provides independent 4-bit wide (nibble) transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

By default, the KSZ8041NL is configured to MII mode after it is power-up or reset with the following:

- A 25MHz crystal connected to XI, XO (pins 9, 8), or an external 25MHz clock source (oscillator) connected to XI.
- CONFIG[2:0] (pins 18, 29, 28) set to '000' (default setting).

MII Signal Definition (KSZ8041NL only)

The Table 2 describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

MII Signal Name	Direction (with respect to PHY, KSZ8041NL signal)	Direction (with respect to MAC)	Description
TXC	Output	Input	Transmit Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
TXEN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data [3:0]
RXC	Output	Input	Receive Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
RXDV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data [3:0]
RXER	Output	Input, or (not required)	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detection

Table 2. MII Signal Definition

Transmit Clock (TXC)

TXC is sourced by the PHY. It is a continuous clock that provides the timing reference for TXEN and TXD[3:0].

TXC is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

Transmit Enable (TXEN)

TXEN indicates the MAC is presenting nibbles on TXD[3:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the MII, and is negated prior to the first TXC following the final nibble of a frame.

TXEN transitions synchronously with respect to TXC.

Transmit Data [3:0] (TXD[3:0])

TXD[3:0] transitions synchronously with respect to TXC. When TXEN is asserted, TXD[3:0] are accepted for transmission by the PHY. TXD[3:0] is ”00” to indicate idle when TXEN is de-asserted. Values other than “00” on TXD[3:0] while TXEN is de-asserted are ignored by the PHY.

Receive Clock (RXC)

RXC provides the timing reference for RXDV, RXD[3:0], and RXER.

- In 10Mbps mode, RXC is recovered from the line while carrier is active. RXC is derived from the PHY’s reference clock when the line is idle, or link is down.
- In 100Mbps mode, RXC is continuously recovered from the line. If link is down, RXC is derived from the PHY’s reference clock.

RXC is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

Receive Data Valid (RXDV)

RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on RXD[3:0].

- In 10Mbps mode, RXDV is asserted with the first nibble of the SFD (Start of Frame Delimiter), “5D”, and remains asserted until the end of the frame.
- In 100Mbps mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the frame.

RXDV transitions synchronously with respect to RXC.

Receive Data [3:0] (RXD[3:0])

RXD[3:0] transitions synchronously with respect to RXC. For each clock period in which RXDV is asserted, RXD[3:0] transfers a nibble of recovered data from the PHY.

Receive Error (RXER)

RXER is asserted for one or more RXC periods to indicate that a Symbol Error (e.g. a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY.

RXER transitions synchronously with respect to RXC. While RXDV is de-asserted, RXER has no effect on the MAC.

Carrier Sense (CRS)

CRS is asserted and de-asserted as follows:

- In 10Mbps mode, CRS assertion is based on the reception of valid preambles. CRS de-assertion is based on the reception of an end-of-frame (EOF) marker.
- In 100Mbps mode, CRS is asserted when a start-of-stream delimiter, or /J/K symbol pair is detected. CRS is de-asserted when an end-of-stream delimiter, or /T/R symbol pair is detected. Additionally, the PMA layer de-asserts CRS if IDLE symbols are received without /T/R.

Collision (COL)

COL is asserted in half-duplex mode whenever the transmitter and receiver are simultaneously active on the line. This is used to inform the MAC that a collision has occurred during its transmission to the PHY.

COL transitions asynchronously with respect to TXC and RXC.

Reduced MII (RMII) Data Interface

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10Mbps and 100Mbps data rates.
- Uses a 50MHz reference clock.
- Provides independent 2-bit wide (di-bit) transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

The KSZ8041NL is configured in RMII mode after it is power-up or reset with the following:

- A 50MHz reference clock connected to REFCLK (pin 9).
- CONFIG[2:0] (pins 18, 29, 28) set to ‘001’.

The KSZ8041RNL is configured in RMII mode and outputs the 50MHz RMII reference clock to the MAC on REF_CLK (pin 19) after it is power-up or reset with the following:

- A 25MHz crystal connected to XI (pin 9) and XO (pin 8), or a 25MHz reference clock connected to XI (pin 9).
- CONFIG[2:0] (pins 18, 29, 28) set to ‘001’.

In RMII mode, unused MII signals, TXD[3:2] (pins 27, 26), are tied to ground.

RMII Signal Definition

The Tables 3 and 4 describe the RMII signals for KSZ8041NL and KSZ8041RNL. Refer to RMII Specification for detailed information.

RMII Signal Name	Direction (with respect to PHY, KSZ8041NL signal)	Direction (with respect to MAC)	Description
REF_CLK	Input	Input, or Output	Synchronous 50 MHz clock reference for receive, transmit and control interface
TX_EN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data [1:0]
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data [1:0]
RX_ER	Output	Input, or (not required)	Receive Error

Table 3. RMII Signal Description – KSZ8041NL

RMII Signal Name	Direction (with respect to PHY, KSZ8041RNL signal)	Direction (with respect to MAC)	Description
REF_CLK	Output	Input	Synchronous 50 MHz clock reference for receive, transmit and control interface
TX_EN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data [1:0]
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data [1:0]
RX_ER	Output	Input, or (not required)	Receive Error

Table 4. RMII Signal Description – KSZ8041RNL

Reference Clock (REF_CLK)

REF_CLK is a continuous 50MHz clock that provides the timing reference for TX_EN, TXD[1:0], CRS_DV, RXD[1:0], and RX_ER.

The KSZ8041NL inputs the 50MHz REF_CLK from the MAC or system board.

The KSZ8041RNL generates the 50MHz RMII REF_CLK and outputs it to the MAC.

Transmit Enable (TX_EN)

TX_EN indicates that the MAC is presenting di-bits on TXD[1:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all di-bits to be transmitted are presented on the RMII, and is negated prior to the first REF_CLK following the final di-bit of a frame.

TX_EN transitions synchronously with respect to REF_CLK.

Transmit Data [1:0] (TXD[1:0])

TXD[1:0] transitions synchronously with respect to REF_CLK. When TX_EN is asserted, TXD[1:0] are accepted for transmission by the PHY. TXD[1:0] is ”00” to indicate idle when TX_EN is de-asserted. Values other than “00” on TXD[1:0] while TX_EN is de-asserted are ignored by the PHY.

Carrier Sense/Receive Data Valid (CRS_DV)

CRS_DV is asserted by the PHY when the receive medium is non-idle. It is asserted asynchronously on detection of carrier. This is when squelch is passed in 10Mbps mode, and when 2 non-contiguous zeroes in 10 bits are detected in 100Mbps mode. Loss of carrier results in the de-assertion of CRS_DV.

So long as carrier detection criteria are met, CRS_DV remains asserted continuously from the first recovered di-bit of the frame through the final recovered di-bit, and it is negated prior to the first REF_CLK that follows the final di-bit. The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] is "00" until proper receive signal decoding takes place.

Receive Data [1:0] (RXD[1:0])

RXD[1:0] transitions synchronously to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY. RXD[1:0] is "00" to indicate idle when CRS_DV is de-asserted. Values other than “00” on RXD[1:0] while CRS_DV is de-asserted are ignored by the MAC.

Receive Error (RX_ER)

RX_ER is asserted for one or more REF_CLK periods to indicate that a Symbol Error (e.g. a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY.

RX_ER transitions synchronously with respect to REF_CLK. While CRS_DV is de-asserted, RX_ER has no effect on the MAC.

Collision Detection

The MAC regenerates the COL signal of the MII from TX_EN and CRS_DV.

RMII Signal Diagram

The KSZ8041NL RMII pin connections to the MAC are shown in Figure 2.

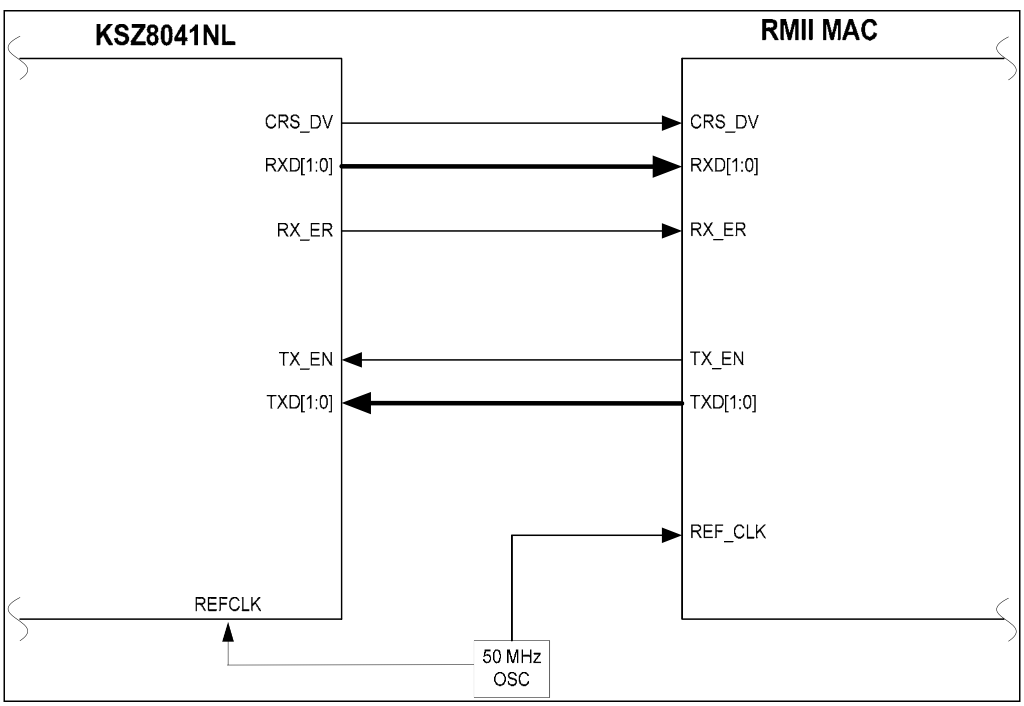


Figure 2. KSZ8041NL RMII Interface

The KSZ8041RNL RMII pin connections to the MAC are shown in Figure 3.

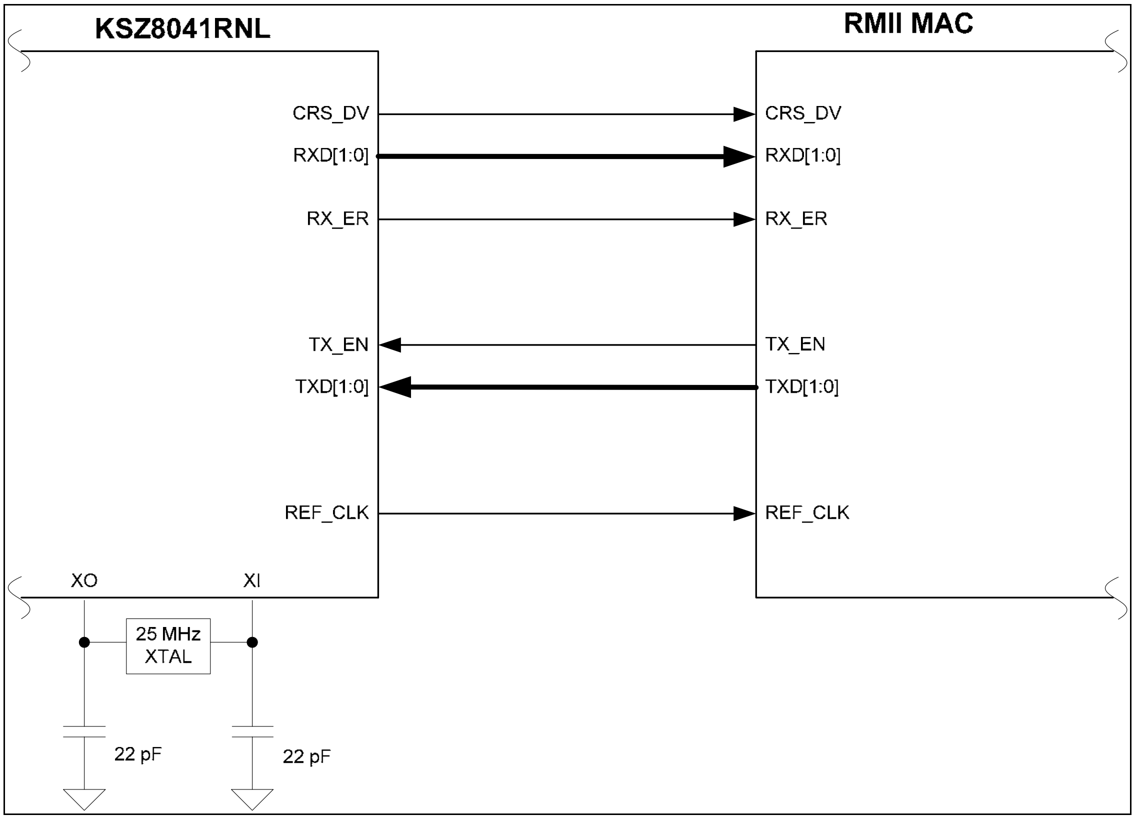


Figure 3. KSZ8041RNL RMII Interface

HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the confusion of whether to use a straight cable or a crossover cable between the KSZ8041NL/RNL and its link partner. This feature allows the KSZ8041NL/RNL to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner, and then assigns transmit and receive pairs of the KSZ8041NL/RNL accordingly.

HP Auto MDI/MDI-X is enabled by default. It is disabled by writing a one to register 1F bit 13. MDI and MDI-X mode is selected by register 1F bit 14 if HP Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support auto MDI/MDI-X.

The IEEE 802.3 Standard defines MDI and MDI-X as follows:

MDI		MDI-X	
RJ-45 Pin	**Signal**	**RJ-45 Pin**	**Signal**
1	TD+	1	RD+
2	TD-	2	RD-
3	RD+	3	TD+
6	RD-	6	TD-

Table 5. MDI/MDI-X Pin Definition

Straight Cable

A straight cable connects a MDI device to a MDI-X device, or a MDI-X device to a MDI device. The Figure 4 depicts a typical straight cable connection between a NIC card (MDI) and a switch, or hub (MDI-X).

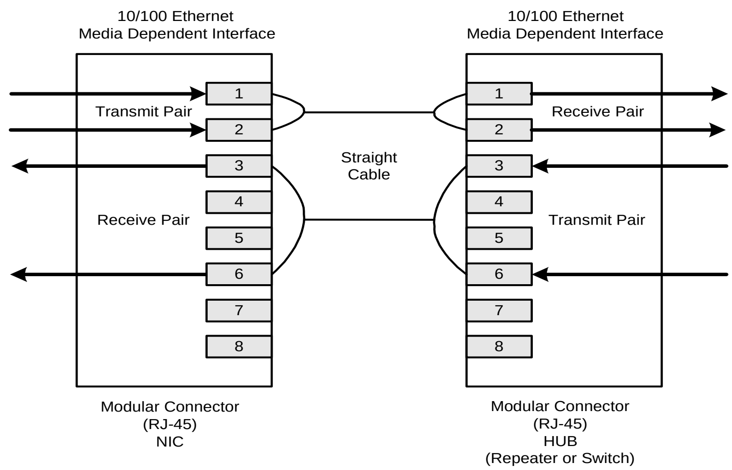


Figure 4. Typical Straight Cable Connection

Crossover Cable

A crossover cable connects a MDI device to another MDI device, or a MDI-X device to another MDI-X device. Figure 5 depicts a typical crossover cable connection between two switches or hubs (two MDI-X devices).

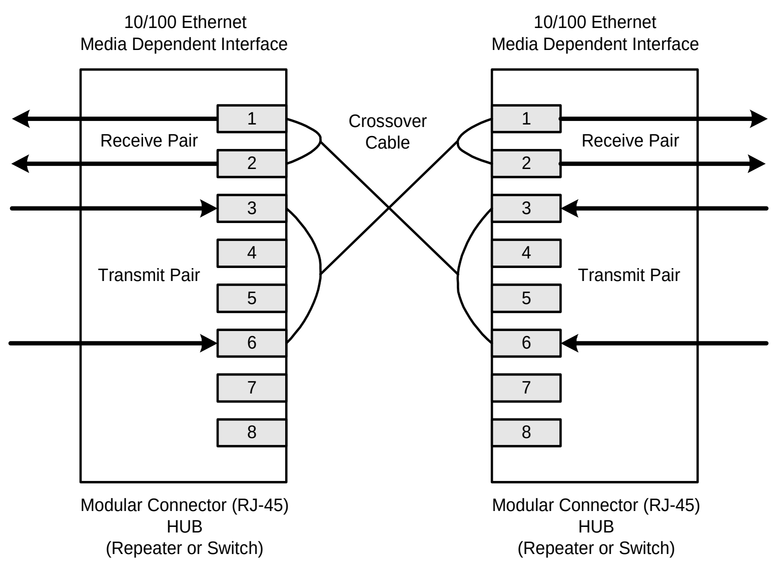


Figure 5. Typical Crossover Cable Connection

Power Management

The KSZ8041NL/RNL offers the following power management modes:

Power Saving Mode

This mode is used to reduce power consumption when the cable is unplugged. It is in effect when auto-negotiation mode is enabled, cable is disconnected, and register 1F bit 10 is set to 1. Under power saving mode, the KSZ8041NL/RNL shuts down all transceiver blocks, except for transmitter, energy detect and PLL circuits. Additionally, for the KSZ8041NL in MII mode, the RXC clock output is disabled. RXC clock is enabled after the cable is connected and link is established.

Power saving mode is disabled by writing a zero to register 1F bit 10.

Power Down Mode

This mode is used to power down the entire KSZ8041NL/RNL device when it is not in use. Power down mode is enabled by writing a one to register 0 bit 11. In the power down state, the KSZ8041NL/RNL disables all internal functions, except for the MII management interface.

Reference Clock Connection Options

A crystal or clock source, such as an oscillator, is used to provide the reference clock for the KSZ8041NL/RNL.

The Figure 6 illustrates how to connect the 25MHz crystal and oscillator reference clock.

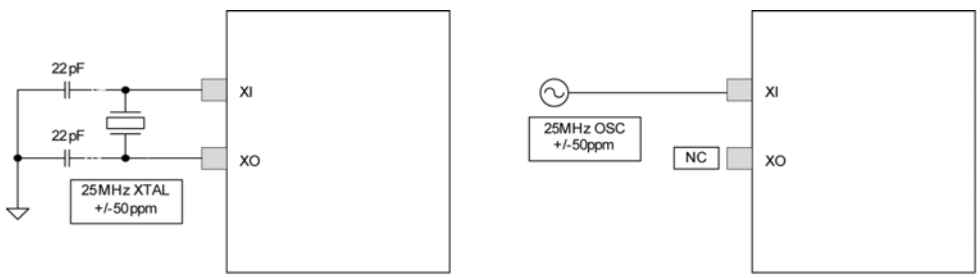


Figure 6. 25MHz Crystal / Oscillator Reference Clock

For the KSZ8041NL, Figure 7 illustrates how to connect the 50MHz oscillator reference clock for RMII mode.

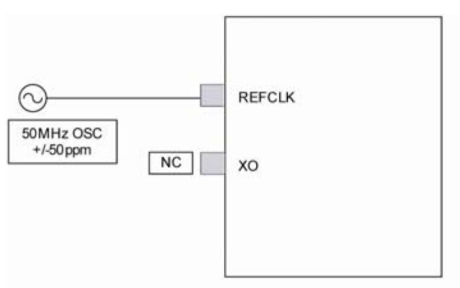


Figure 7. 50MHz Oscillator Reference Clock for KSZ8041NL RMII Mode

Reference Circuit for Power and Ground Connections

The KSZ8041NL/RNL is a single 3.3V supply device with a built-in 1.8V low noise regulator. The power and ground connections are shown in Figure 8 and Table 6.

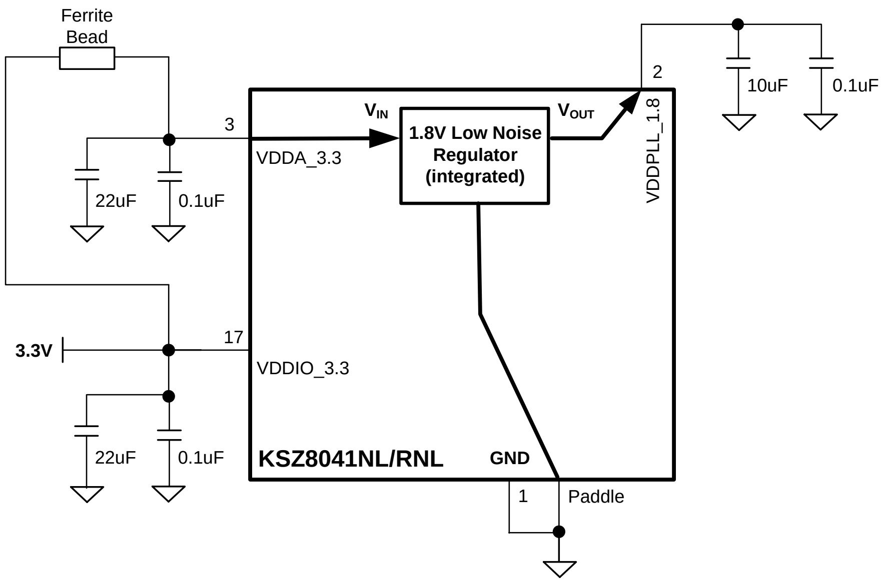


Figure 8. KSZ8041NL/RNL Power and Ground Connections

Power Pin	Pin Number	Description
VDDPLL_1.8	2	Decouple with 10uF and 0.1uF capacitors to ground.
VDDA_3.3	3	Connect to board’s 3.3V supply through ferrite bead.
VDDIO_3.3	17	Connect to board’s 3.3V supply.

Table 6. KSZ8041NL/RNL Power Pin Description

Register Map

Register Number (Hex)	Description
0h	Basic Control
1h	Basic Status
2h	PHY Identifier 1
3h	PHY Identifier 2
4h	Auto-Negotiation Advertisement
5h	Auto-Negotiation Link Partner Ability
6h	Auto-Negotiation Expansion
7h	Auto-Negotiation Next Page
8h	Link Partner Next Page Ability
9h – 13h	Reserved
14h	MII Control
15h	RXER Counter
16h – 1Ah	Reserved
1Bh	Interrupt Control/Status
1Ch – 1Dh	Reserved
1Eh	PHY Control 1
1Fh	PHY Control 2

Register Description

Address	Name	Description	Mode[1]	Default
Register 0h – Basic Control				
0.15	Reset	1 = Software reset 0 = Normal operation This bit is self-cleared after a ‘1’ is written to it.	RW/SC	0
0.14	Loop-back	1 = Loop-back mode 0 = Normal operation	RW	0
0.13	Speed Select (LSB)	1 = 100Mbps 0 = 10Mbps This bit is ignored if auto-negotiation is enabled (register 0.12 = 1).	RW	Set by SPEED strapping pin. See “Strapping Options” section for details.
0.12	Auto-Negotiation Enable	1 = Enable auto-negotiation process 0 = Disable auto-negotiation process If enabled, auto-negotiation result overrides settings in register 0.13 and 0.8.	RW	Set by NWAYEN strapping pin. See “Strapping Options” section for details.
0.11	Power Down	1 = Power down mode 0 = Normal operation	RW	0
0.10	Isolate	1 = Electrical isolation of PHY from MII and TX+/TX- 0 = Normal operation	RW	Set by ISO strapping pin. See “Strapping Options” section for details.

Register Description (Continued)

Address	Name	Description	Mode(1)	Default
Register 0h – Basic Control				
0.9	Restart Auto-Negotiation	1 = Restart auto-negotiation process 0 = Normal operation. This bit is self-cleared after a '1' is written to it.	RW/SC	0
0.8	Duplex Mode	1 = Full-duplex 0 = Half-duplex	RW	Inverse of DUPLEX strapping pin value. See "Strapping Options" section for details.
0.7	Collision Test	1 = Enable COL test 0 = Disable COL test	RW	0
0.6:1	Reserved		RO	000_000
0.0	Disable Transmitter	0 = Enable transmitter 1 = Disable transmitter	RW	0
Register 1h – Basic Status				
1.15	100Base-T4	1 = T4 capable 0 = Not T4 capable	RO	0
1.14	100Base-TX Full Duplex	1 = Capable of 100Mbps full-duplex 0 = Not capable of 100Mbps full-duplex	RO	1
1.13	100Base-TX Half Duplex	1 = Capable of 100Mbps half-duplex 0 = Not capable of 100Mbps half-duplex	RO	1
1.12	10Base-T Full Duplex	1 = Capable of 10Mbps full-duplex 0 = Not capable of 10Mbps full-duplex	RO	1
1.11	10Base-T Half Duplex	1 = Capable of 10Mbps half-duplex 0 = Not capable of 10Mbps half-duplex	RO	1
1.10:7	Reserved		RO	0000
1.6	No Preamble	1 = Preamble suppression 0 = Normal preamble	RO	1
1.5	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	RO	0
1.4	Remote Fault	1 = Remote fault 0 = No remote fault	RO/LH	0
1.3	Auto-Negotiation Ability	1 = Capable to perform auto-negotiation 0 = Not capable to perform auto-negotiation	RO	1
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL	0
1.1	Jabber Detect	1 = Jabber detected 0 = Jabber not detected (default is low)	RO/LH	0
1.0	Extended Capability	1 = Supports extended capabilities registers	RO	1

Register Description (Continued)

Address	Name	Description	Mode[1]	Default
Register 2h – PHY Identifier 1				
2.15:0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). Kendin Communication’s OUI is 0010A1 (hex)	RO	0022h
Register 3h – PHY Identifier 2				
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). Kendin Communication’s OUI is 0010A1 (hex)	RO	0001_01
3.9:4	Model Number	Six bit manufacturer’s model number	RO	01_0001
3.3:0	Revision Number	Four bit manufacturer’s revision number	RO	Indicates silicon revision
Register 4h – Auto-Negotiation Advertisement				
4.15	Next Page	1 = Next page capable 0 = No next page capability.	RW	0
4.14	Reserved		RO	0
4.13	Remote Fault	1 = Remote fault supported 0 = No remote fault	RW	0
4.12	Reserved		RO	0
4.11:10	Pause	[00] = No PAUSE [10] = Asymmetric PAUSE [01] = Symmetric PAUSE [11] = Asymmetric & Symmetric PAUSE	RW	00
4.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
4.8	100Base-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RW	Set by SPEED strapping pin. See “Strapping Options” section for details.
4.7	100Base-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RW	Set by SPEED strapping pin. See “Strapping Options” section for details.
4.6	10Base-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RW	1
4.5	10Base-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RW	1
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	0_0001

Register Description (Continued)

Address	Name	Description	Mode[1]	Default
Register 5h – Auto-Negotiation Link Partner Ability				
5.15	Next Page	1 = Next page capable 0 = No next page capability	RO	0
5.14	Acknowledge	1 = Link code word received from partner 0 = Link code word not yet received	RO	0
5.13	Remote Fault	1 = Remote fault detected 0 = No remote fault	RO	0
5.12	Reserved		RO	0
5.11:10	Pause	[00] = No PAUSE [10] = Asymmetric PAUSE [01] = Symmetric PAUSE [11] = Asymmetric & Symmetric PAUSE	RO	00
5.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
5.8	100Base-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RO	0
5.7	100Base-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RO	0
5.6	10Base-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RO	0
5.5	10Base-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	0_0001
Register 6h – Auto-Negotiation Expansion				
6.15:5	Reserved		RO	0000_0000_000
6.4	Parallel Detection Fault	1 = Fault detected by parallel detection 0 = No fault detected by parallel detection.	RO/LH	0
6.3	Link Partner Next Page Able	1 = Link partner has next page capability 0 = Link partner does not have next page capability	RO	0
6.2	Next Page Able	1 = Local device has next page capability 0 = Local device does not have next page capability	RO	1
6.1	Page Received	1 = New page received 0 = New page not received yet	RO/LH	0
6.0	Link Partner Auto-Negotiation Able	1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation capability	RO	0

Register Description (Continued)

Address	Name	Description	Mode(1)	Default
Register 7h – Auto-Negotiation Next Page				
7.15	Next Page	1 = Additional next page(s) will follow 0 = Last page	RW	0
7.14	Reserved		RO	0
7.13	Message Page	1 = Message page 0 = Unformatted page	RW	1
7.12	Acknowledge2	1 = Will comply with message 0 = Cannot comply with message	RW	0
7.11	Toggle	1 = Previous value of the transmitted link code word equaled logic one 0 = Logic zero	RO	0
7.10:0	Message Field	11-bit wide field to encode 2048 messages	RW	000_0000_0001
Register 8h – Link Partner Next Page Ability				
8.15	Next Page	1 = Additional Next Page(s) will follow 0 = Last page	RO	0
8.14	Acknowledge	1 = Successful receipt of link word 0 = No successful receipt of link word	RO	0
8.13	Message Page	1 = Message page 0 = Unformatted page	RO	0
8.12	Acknowledge2	1 = Able to act on the information 0 = Not able to act on the information	RO	0
8.11	Toggle	1 = Previous value of transmitted link code word equal to logic zero 0 = Previous value of transmitted link code word equal to logic one	RO	0
8.10:0	Message Field		RO	000_0000_0000
Register 14h – MII Control				
14.15:8	Reserved		RO	0000_0000
14.7	100Base-TX Preamble Restore	1 = Restore received preamble to MII output (random latency) 0 = Consume 1-byte preamble before sending frame to MII output for fixed latency	RW	0 or 1 (if CONFIG[2:0] = 100) See “Strapping Options” section for details.
14.6	10Base-T Preamble Restore	1 = Restore received preamble to MII output 0 = Remove all 7-bytes of preamble before sending frame (starting with SFD) to MII output	RW	0
14.5:0	Reserved		RO	00_0001
Register 15h – RXER Counter				
15.15:0	RXER Counter	Receive error counter for Symbol Error frames	RO/SC	0000h

Register Description (Continued)

Address	Name	Description	Mode(1)	Default
Register 1Bh – Interrupt Control/Status				
1b.15	Jabber Interrupt Enable	1 = Enable Jabber Interrupt 0 = Disable Jabber Interrupt	RW	0
1b.14	Receive Error Interrupt Enable	1 = Enable Receive Error Interrupt 0 = Disable Receive Error Interrupt	RW	0
1b.13	Page Received Interrupt Enable	1 = Enable Page Received Interrupt 0 = Disable Page Received Interrupt	RW	0
1b.12	Parallel Detect Fault Interrupt Enable	1 = Enable Parallel Detect Fault Interrupt 0 = Disable Parallel Detect Fault Interrupt	RW	0
1b.11	Link Partner Acknowledge Interrupt Enable	1 = Enable Link Partner Acknowledge Interrupt 0 = Disable Link Partner Acknowledge Interrupt	RW	0
1b.10	Link Down Interrupt Enable	1= Enable Link Down Interrupt 0 = Disable Link Down Interrupt	RW	0
1b.9	Remote Fault Interrupt Enable	1 = Enable Remote Fault Interrupt 0 = Disable Remote Fault Interrupt	RW	0
1b.8	Link Up Interrupt Enable	1 = Enable Link Up Interrupt 0 = Disable Link Up Interrupt	RW	0
1b.7	Jabber Interrupt	1 = Jabber occurred 0 = Jabber did not occurred	RO/SC	0
1b.6	Receive Error Interrupt	1 = Receive Error occurred 0 = Receive Error did not occurred	RO/SC	0
1b.5	Page Receive Interrupt	1 = Page Receive occurred 0 = Page Receive did not occurred	RO/SC	0
1b.4	Parallel Detect Fault Interrupt	1 = Parallel Detect Fault occurred 0 = Parallel Detect Fault did not occurred	RO/SC	0
1b.3	Link Partner Acknowledge Interrupt	1= Link Partner Acknowledge occurred 0= Link Partner Acknowledge did not occurred	RO/SC	0
1b.2	Link Down Interrupt	1= Link Down occurred 0= Link Down did not occurred	RO/SC	0
1b.1	Remote Fault Interrupt	1= Remote Fault occurred 0= Remote Fault did not occurred	RO/SC	0
1b.0	Link Up Interrupt	1= Link Up occurred 0= Link Up did not occurred	RO/SC	0

Register Description (Continued)

Address	Name	Description	Mode[1]	Default
Register 1Eh – PHY Control 1				
1e:15:14	LED mode	[00] = LED1 : Speed LED0 : Link/Activity [01] = LED1 : Activity LED0 : Link [10], [11] = Reserved	RW	00
1e.13	Polarity	0 = Polarity is not reversed 1 = Polarity is reversed	RO	
1e.12	Reserved		RO	0
1e.11	MDI/MDI-X State	0 = MDI 1 = MDI-X	RO	
1e:10:8	Reserved			
1e:7	Remote loopback	0 = Normal mode 1 = Remote (analog) loop back is enable	RW	0
1e:6:0	Reserved			
Register 1Fh – PHY Control 2				
1f:15	HP_MDIX	0 = Micrel Auto MDI/MDI-X mode 1 = HP Auto MDI/MDI-X mode	RW	1
1f:14	MDI/MDI-X Select	When Auto MDI/MDI-X is disabled, 0 = MDI Mode Transmit on TX+/- (pins 7,6) and Receive on RX+/- (pins 5,4) 1 = MDI-X Mode Transmit on RX+/- (pins 5,4) and Receive on TX+/- (pins 7,6)	RW	0
1f:13	Pairswap Disable	1 = Disable auto MDI/MDI-X 0 = Enable auto MDI/MDI-X	RW	0
1f.12	Energy Detect	1 = Presence of signal on RX+/- analog wire pair 0 = No signal detected on RX+/-	RO	0
1f.11	Force Link	1 = Force link pass 0 = Normal link operation This bit bypasses the control logic and allow transmitter to send pattern even if there is no link.	RW	0

Register Description (Continued)

Address	Name	Description	Mode[1]	Default
1f.10	Power Saving	1 = Enable power saving 0 = Disable power saving If power saving mode is enabled and the cable is disconnected, the RXC clock output (in MII mode) is disabled. RXC clock is enabled after the cable is connected and link is established.	RW	0
1f.9	Interrupt Level	1 = Interrupt pin active high 0 = Interrupt pin active low	RW	0
1f.8	Enable Jabber	1 = Enable jabber counter 0 = Disable jabber counter	RW	1
1f.7	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	RW	0
1f.6	Enable Pause (Flow Control)	1 = Flow control capable 0 = No flow control capability	RO	0
1f.5	PHY Isolate	1 = PHY in isolate mode 0 = PHY in normal operation	RO	0
1f.4:2	Operation Mode Indication	[000] = still in auto-negotiation [001] = 10Base-T half-duplex [010] = 100Base-TX half-duplex [011] = reserved [101] = 10Base-T full-duplex [110] = 100Base-TX full-duplex [111] = reserved	RO	000
1f.1	Enable SQE test	1 = Enable SQE test 0 = Disable SQE test	RW	0
1f.0	Disable Data Scrambling	1 = Disable scrambler 0 = Enable scrambler	RW	0

Note:

1. RW = Read/Write.
   RO = Read only.
   SC = Self-cleared.
   LH = Latch high.
   LL = Latch low.

Absolute Maximum Ratings[1]

Supply Voltage
($V_{DDPLL\_1.8}$) .... -0.5V to +2.4V
($V_{DDIO\_3.3}$, $V_{DDA\_3.3}$) .... -0.5V to +4.0V
Input Voltage (all inputs) .... -0.5V to +4.0V
Output Voltage (all outputs) .... -0.5V to +4.0V
Lead Temperature (soldering, 10sec.) .... 260°C
Storage Temperature (T_s) ....-55°C to +150°C
ESD Rating[3] 6kV

Operating Ratings[2]

Supply Voltage
($V_{DDIO\_3.3}$, $V_{DDA\_3.3}$) .... +3.135V to +3.465V
Ambient Temperature
(T_A , Commercial)................................ 0°C to +70°C
(T_A , Industrial) ....-40°C to +85°C
(T_A , AM Automotive Qualified) ....-40°C to +85°C
Maximum Junction Temperature (T_J Max) .... 125°C
Maximum Case Temperature (T_C Max)..................... 150°C
Thermal Resistance (θ_{JA}) ....34°C/W
Thermal Resistance (θ_{JC}) ....6°C/W

Electrical Characteristics[4]

Symbol	Parameter	Condition	Min	Typ	Max	Units
Supply Current[5]						
I_{DD1}	100Base-TX	Chip only (no transformer); Full-duplex traffic @ 100% utilization		53.0		mA
I_{DD2}	10Base-T	Chip only (no transformer); Full-duplex traffic @ 100% utilization		38.0		mA
I_{DD3}	Power Saving Mode	Ethernet cable disconnected (reg. 1F.10 = 1)		32.0		mA
I_{DD4}	Power Down Mode	Software power down (reg. 0.11 = 1)		4.0		mA
TTL Inputs						
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current	V_{IN} = GND ~ VDDIO		-10	10	µA
TTL Outputs						
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 4mA			0.4	V
$\|I_{oz}\|$	Output Tri-State Leakage				10	µA
LED Outputs						
I_{LED}	Output Drive Current	Each LED pin (LED0, LED1)		8		mA
100Base-TX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	100Ω termination across differential output	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	100Ω termination across differential output			2	%
t_r, t_f	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance		0		0.5	ns
	Duty Cycle Distortion				± 0.25	ns
	Overshoot				5	%
V_{SET}	Reference Voltage of ISET			0.65		V
	Output Jitter	Peak-to-peak		0.7	1.4	ns

Electrical Characteristics[4] (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
10Base-T Transmit (measured differentially after 1:1 transformer)						
V_P	Peak Differential Output Voltage	100Ω termination across differential output	2.2		2.8	V
	Jitter Added	Peak-to-peak			3.5	ns
t_r, t_f	Rise/Fall Time			25		ns
10Base-T Receive						
V_{SQ}	Squelch Threshold	5MHz square wave		400		mV

Notes:

1. Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
4. T_A = 25°C. Specification for packaged product only.
5. Current consumption is for the single 3.3V supply KSZ8041NL/RNL device only, and includes the 1.8V supply voltage ($V_{DDPLL\_1.8}$) that is provided by the KSZ8041NL/RNL. The PHY port's transformer consumes an additional 45mA @ 3.3V for 100Base-TX and 70mA @ 3.3V for 10Base-T.

Timing Diagrams

MII SQE Timing (10Base-T)

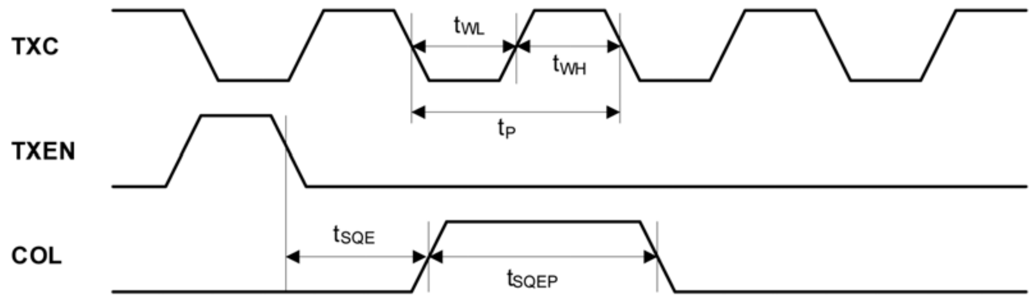


Figure 9. MII SQE Timing (10Base-T)

Timing Parameter	Description	Min	Typ	Max	Unit
t_P	TXC period		400		ns
t_{WL}	TXC pulse width low		200		ns
t_{WH}	TXC pulse width high		200		ns
t_{SQE}	COL (SQE) delay after TXEN de-asserted		2.5		us
t_{SQEP}	COL (SQE) pulse duration		1.0		us

Table 7. MII SQE Timing (10Base-T) Parameters

MII Transmit Timing (10Base-T)

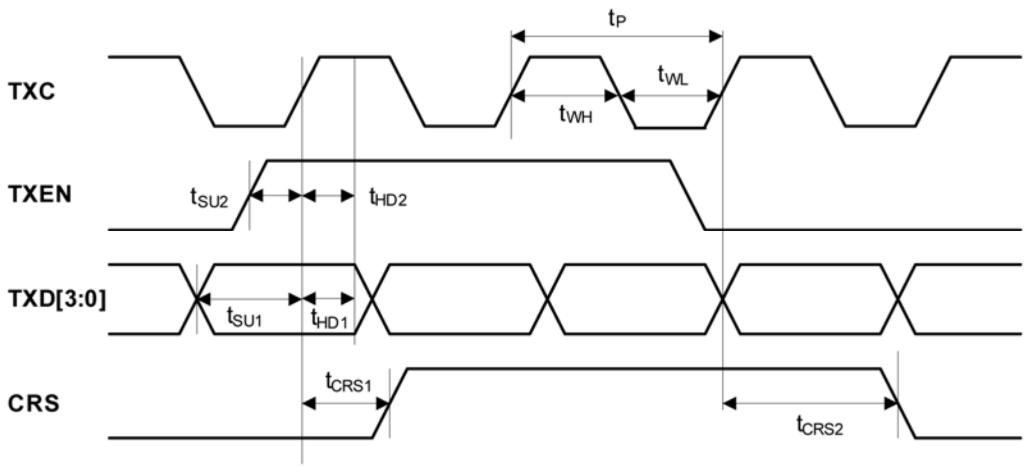


Figure 10. MII Transmit Timing (10Base-T)

Timing Parameter	Description	Min	Typ	Max	Unit
t_P	TXC period		400		ns
t_{WL}	TXC pulse width low		200		ns
t_{WH}	TXC pulse width high		200		ns
t_{SU1}	TXD[3:0] setup to rising edge of TXC	10			ns
t_{SU2}	TXEN setup to rising edge of TXC	10			ns
t_{HD1}	TXD[3:0] hold from rising edge of TXC	0			ns
t_{HD2}	TXEN hold from rising edge of TXC	0			ns
t_{CRS1}	TXEN high to CRS asserted latency		160		ns
t_{CRS2}	TXEN low to CRS de-asserted latency		510		ns

Table 8. MII Transmit Timing (10Base-T) Parameters

MII Receive Timing (10Base-T)

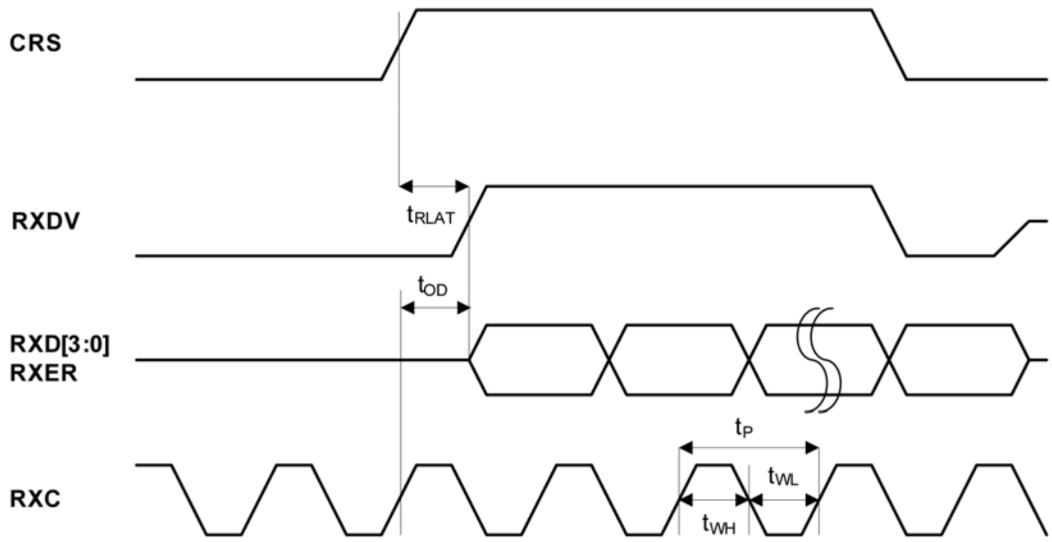


Figure 11. MII Receive Timing (10Base-T)

Timing Parameter	Description	Min	Typ	Max	Unit
t_P	RXC period		400		ns
t_{WL}	RXC pulse width low		200		ns
t_{WH}	RXC pulse width high		200		ns
t_{OD}	(RXD[3:0], RXER, RXDV) output delay from rising edge of RXC	182		225	ns
t_{RLAT}	CRS to (RXD[3:0], RXER, RXDV) latency		6.5		us

Table 9. MII Receive Timing (10Base-T) Parameters

MII Transmit Timing (100Base-TX)

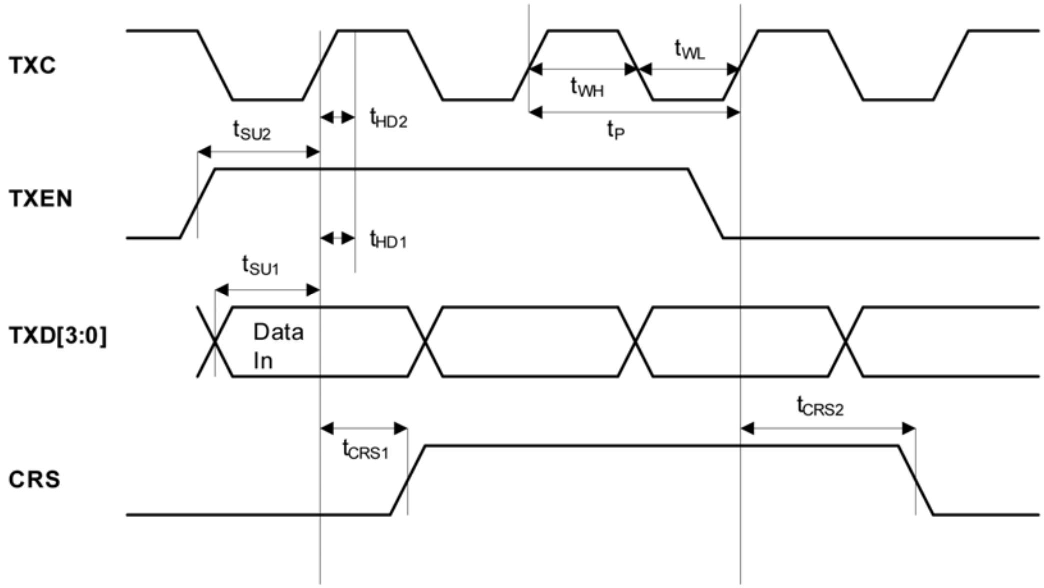


Figure 12. MII Transmit Timing (100Base-TX)

Timing Parameter	Description	Min	Typ	Max	Unit
t_P	TXC period		40		ns
t_{WL}	TXC pulse width low		20		ns
t_{WH}	TXC pulse width high		20		ns
t_{SU1}	TXD[3:0] setup to rising edge of TXC	10			ns
t_{SU2}	TXEN setup to rising edge of TXC	10			ns
t_{HD1}	TXD[3:0] hold from rising edge of TXC	0			ns
t_{HD2}	TXEN hold from rising edge of TXC	0			ns
t_{CRS1}	TXEN high to CRS asserted latency		34		ns
t_{CRS2}	TXEN low to CRS de-asserted latency		33		ns

Table 10. MII Transmit Timing (100Base-TX) Parameters

MII Receive Timing (100Base-TX)

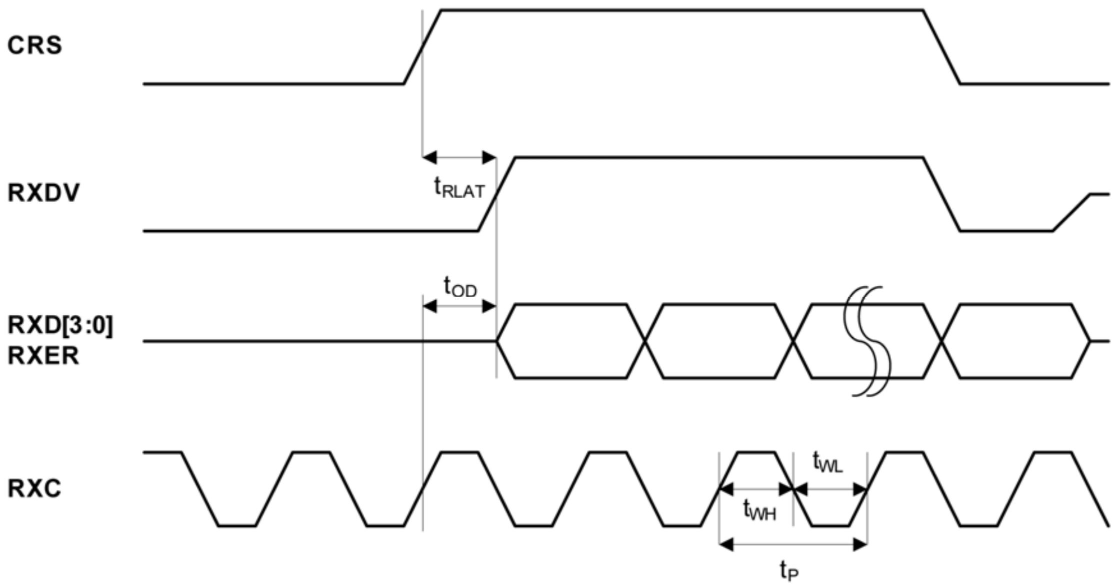


Figure 13. MII Receive Timing (100Base-TX)

Timing Parameter	Description	Min	Typ	Max	Unit
t_P	RXC period		40		ns
t_{WL}	RXC pulse width low		20		ns
t_{WH}	RXC pulse width high		20		ns
t_{OD}	(RXD[3:0], RXER, RXDV) output delay from rising edge of RXC	19		25	ns
t_{RLAT}	CRS to RXDV latency		140		ns
	CRS to RXD[3:0] latency		52		ns
	CRS to RXER latency		60		ns

Table 11. MII Receive Timing (100Base-TX) Parameters

RMII Timing

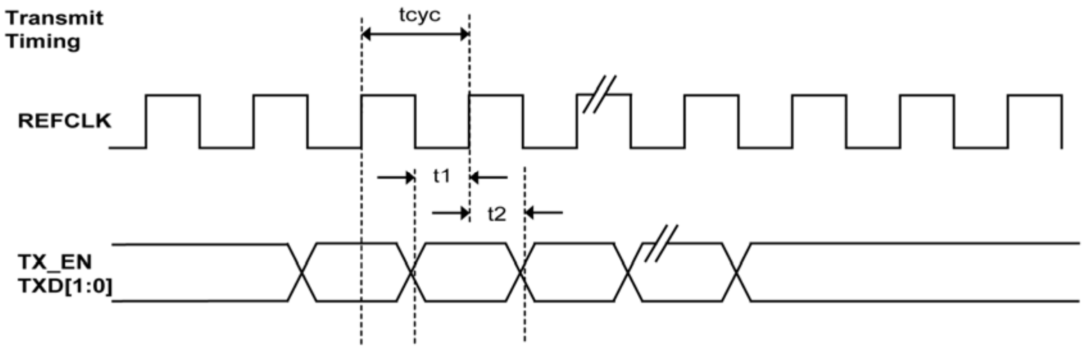


Figure 14. RMII Timing – Data Received from RMII

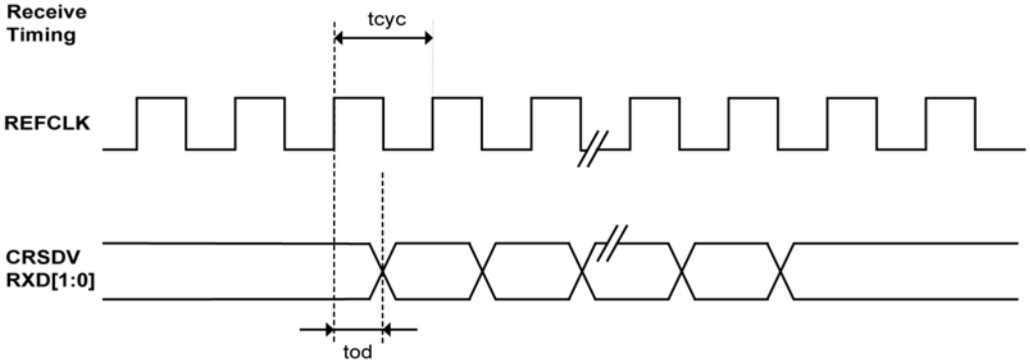


Figure 15. RMII Timing – Data Input to RMII

Timing Parameter	Description	Min	Typ	Max	Unit
t_{cyc}	Clock cycle		20		ns
t_1	Setup time	4			ns
t_2	Hold time	2			ns
t_{od}	Output delay	3		9	ns

Table 12. RMII Timing Parameters – KSZ8041NL

Timing Parameter	Description	Min	Typ	Max	Unit
t_{cyc}	Clock cycle		20		ns
t_1	Setup time	4			ns
t_2	Hold time	1			ns
t_{od}	Output delay	9	11	13	ns

Table 13. RMII Timing Parameters – KSZ8041RNL

Auto-Negotiation Timing

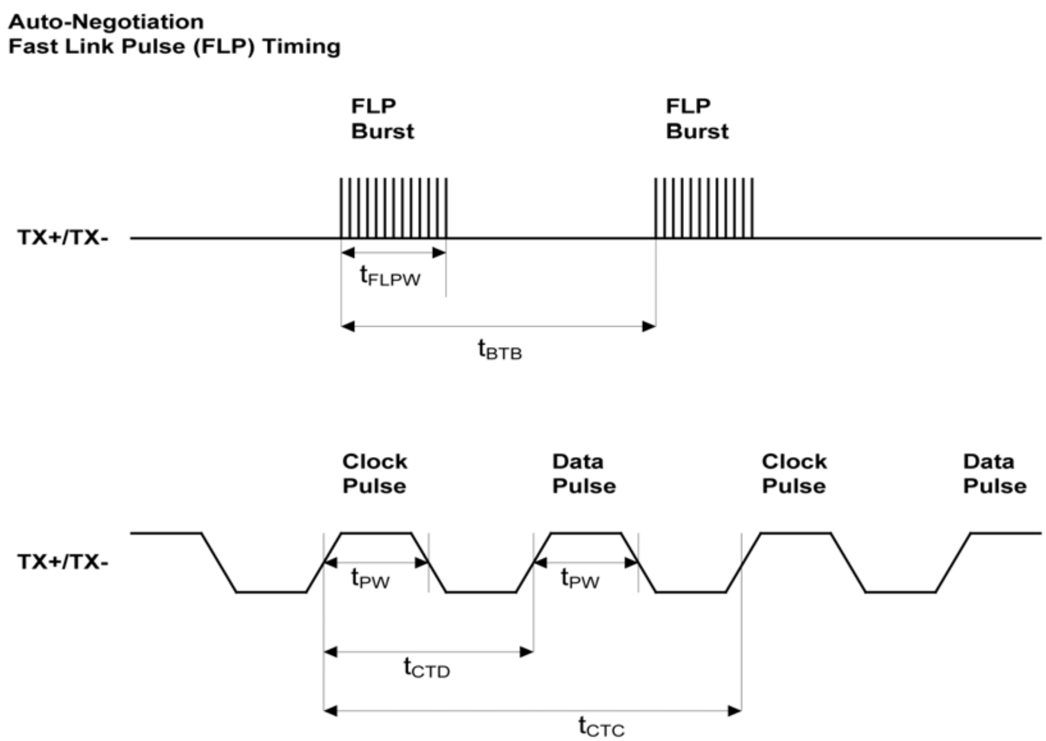


Figure 16. Auto-Negotiation Fast Link Pulse (FLP) Timing

Timing Parameter	Description	Min	Typ	Max	Units
t_{BTB}	FLP Burst to FLP Burst	8	16	24	ms
t_{FLPW}	FLP Burst width		2		ms
t_{PW}	Clock/Data Pulse width		100		ns
t_{CTD}	Clock Pulse to Data Pulse	55.5	64	69.5	µs
t_{CTC}	Clock Pulse to Clock Pulse	111	128	139	µs
	Number of Clock/Data Pulse per FLP Burst	17		33	

Table 14. Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters

MDC/MDIO Timing

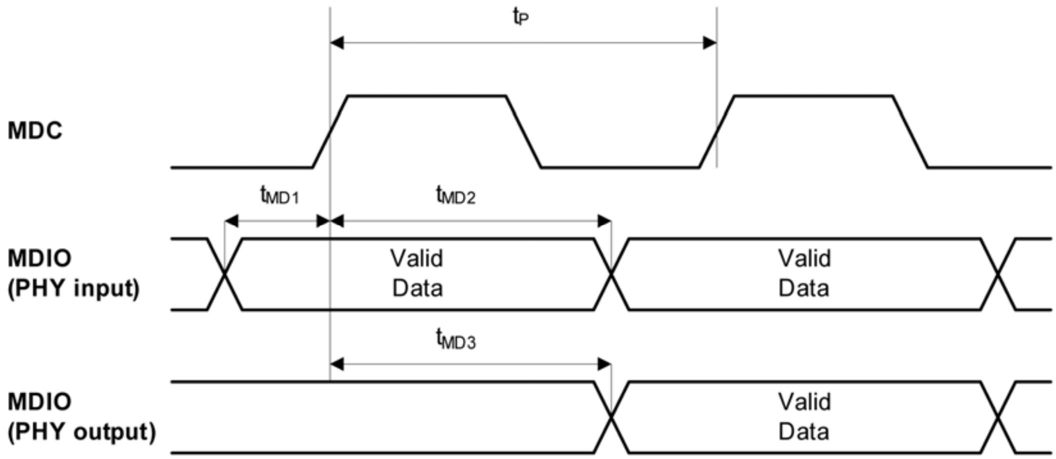


Figure 17. MDC/MDIO Timing

Timing Parameter	Description	Min	Typ	Max	Unit
t_P	MDC period		400		ns
t_{1MD1}	MDIO (PHY input) setup to rising edge of MDC	10			ns
t_{MD2}	MDIO (PHY input) hold from rising edge of MDC	4			ns
t_{MD3}	MDIO (PHY output) delay from rising edge of MDC		222		ns

Table 15. MDC/MDIO Timing Parameters

Reset Timing

The KSZ8041NL/RNL reset timing requirement is summarized in the following figure and table.

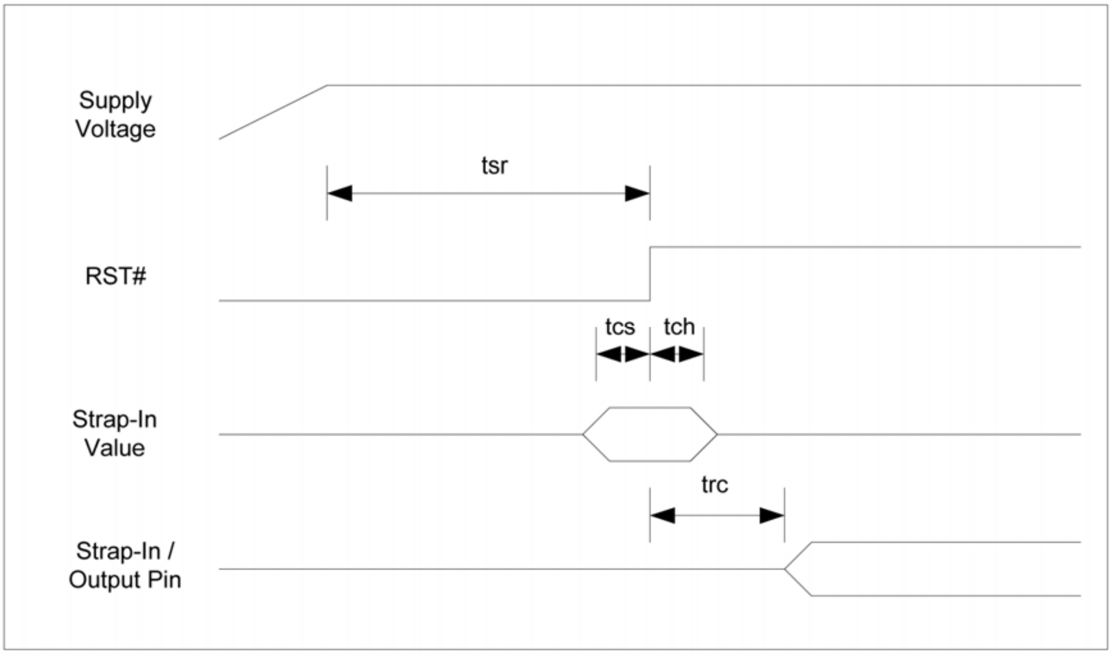


Figure 18. Reset Timing

Parameter	Description	Min	Max	Units
t_{sr}	Stable supply voltage to reset high	10		ms
t_{cs}	Configuration setup time	5		ns
t_{ch}	Configuration hold time	5		ns
t_{rc}	Reset to strap-in pin output	6		ns

Table 16. Reset Timing Parameters

After the de-assertion of reset, it is recommended to wait a minimum of 100 us before starting programming on the MIIM (MDC/MDIO) Interface.

Reset Circuit

The reset circuit in Figure 19 is recommended for powering up the KSZ8041NL/RNL if reset is triggered by the power supply.

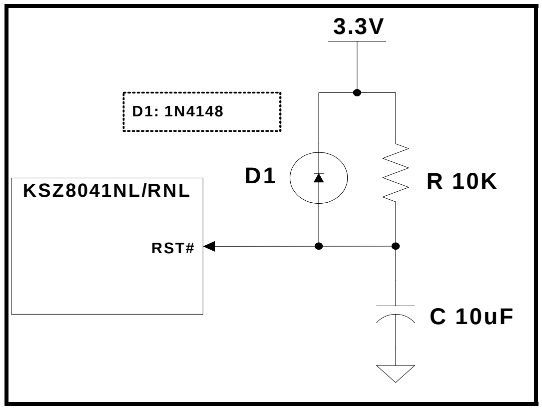


Figure 19. Recommended Reset Circuit

The reset circuit in Figure 20 is recommended for applications where reset is driven by another device (e.g., CPU or FPGA). At power-on-reset, R, C and D1 provide the necessary ramp rise time to reset the KSZ8041NL/RNL device. The RST_OUT_n from CPU/FPGA provides the warm reset after power up.

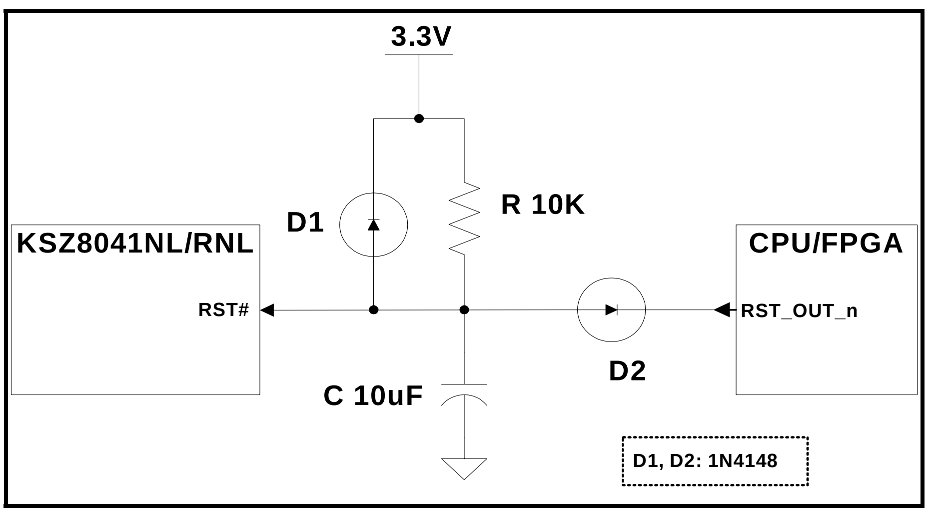


Figure 20. Recommended Reset Circuit for interfacing with CPU/FPGA Reset Output.

Reference Circuits for LED Strapping Pins

The Figure 21 shows the reference circuits for pull-up, float and pull-down on the LED1 and LED0 strapping pins.

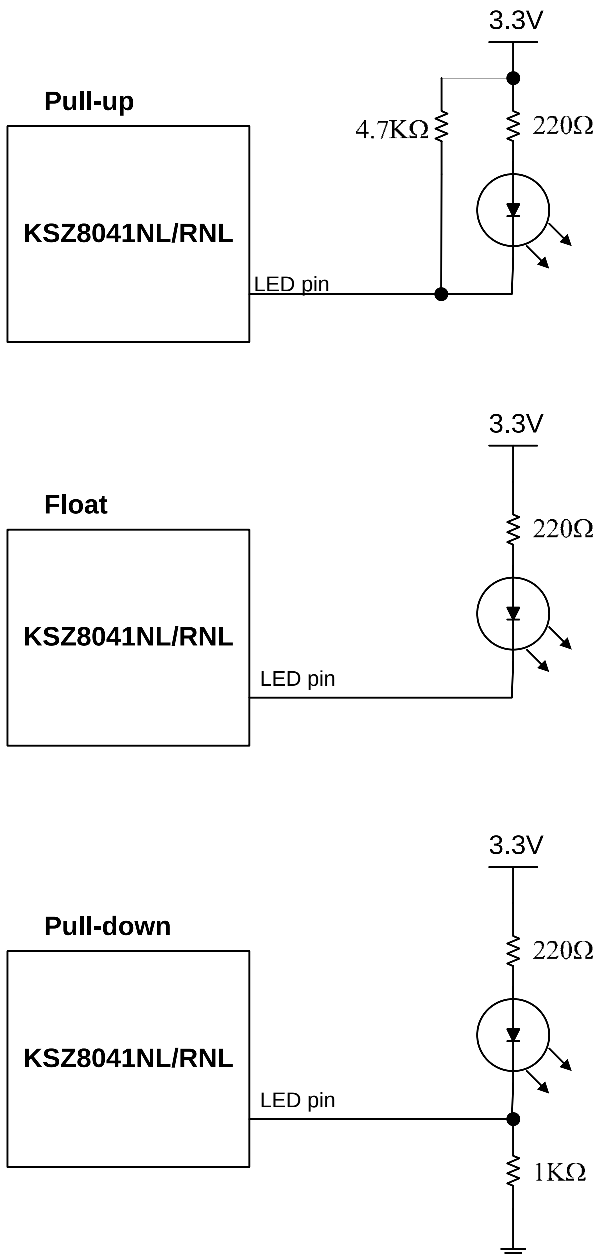


Figure 21. Reference Circuits for LED Strapping Pins

Selection of Isolation Transformer

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode chokes is recommended for exceeding FCC requirements.

The Table 17 gives recommended transformer characteristics.

Parameter	Value	Test Condition
Turns ratio	1 CT : 1 CT	
Open-circuit inductance (min.)	350µH	100mV, 100kHz, 8mA
Leakage inductance (max.)	0.4µH	1MHz (min.)
Inter-winding capacitance (typ.)	12pF	
D.C. resistance (typ.)	0.9Ω	
Insertion loss (max.)	-1.0dB	0MHz – 65MHz
HIPOT (min.)	1500Vrms	

Table 17. Transformer Selection Criteria

Magnetic Manufacturer	Part Number	Auto MDI-X	Number of Port
Bel Fuse	S558-5999-U7	Yes	1
Bel Fuse (Mag Jack)	SI-46001	Yes	1
Bel Fuse (Mag Jack)	SI-50170	Yes	1
Delta	LF8505	Yes	1
LanKom	LF-H41S	Yes	1
Pulse	H1102	Yes	1
Pulse (low cost)	H1260	Yes	1
Transpower	HB726	Yes	1
TDK (Mag Jack)	TLA-6T718	Yes	1

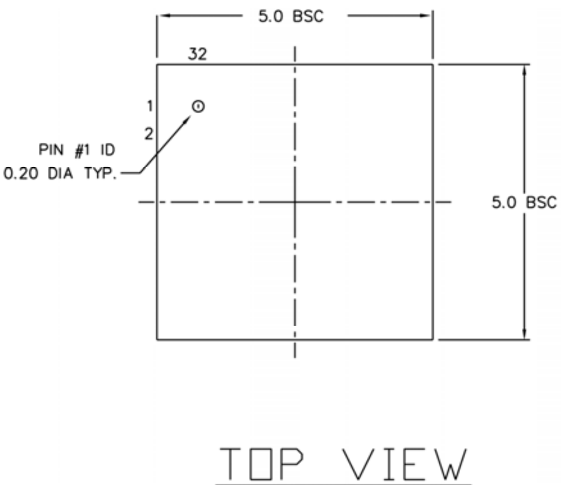
Table 18. Qualified Single Port Magnetics

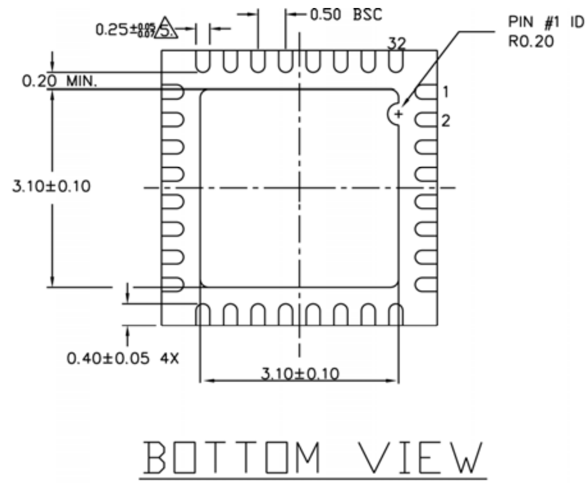
Selection of Reference Crystal

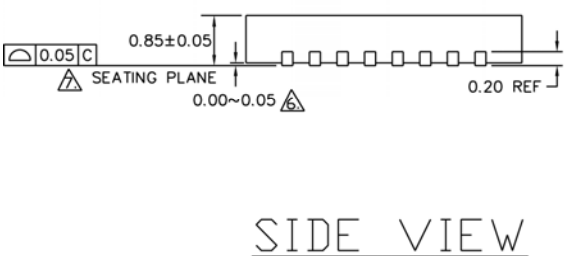
Characteristics	Value	Units
Frequency	25	MHz
Frequency tolerance (max)	±50	ppm
Load capacitance	20	pF
Series resistance	40	Ω

Table 19. Typical Reference Crystal Characteristics

Package Information







NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

32-Pin (5mm x 5mm) MLF® Package

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com