Selecting a Processor for VoIP Solutions

Summary

As VoIP continues to replace analog telephony in the enterprise voice communications marketplace, this technology is also being rapidly adopted in residential environments and small and medium sized businesses (SMBs). The advantages of VoIP—such as multiline, feature-filled voice communications systems using inexpensive digital media and dramatically lower communications rates—that appealed to large businesses are equally attractive to smaller consumers. The demand for VoIP equipment, handsets, IP-PBXs, and gateways continues to grow; and the requirement for higher voice quality is becoming a very clear priority. Market feedback already shows that the mainstream customer is not going to switch to VoIP if it means a lower quality experience than the typical POTS line. The challenge for VoIP hardware developers is to choose a silicon platform that provides the right combination of performance and total BOM cost to provide a winning solution in the very competitive market. The central processor in the VoIP system is a key component in the design, greatly affecting the resulting voice quality, feature set, and bill of materials. This short paper examines the VoIP hardware requirements from several perspectives and the trade-offs that must be considered to choose an effective approach.

VoIP Application Processor Requirements

The major issues facing developers of VoIP hardware products are related to feature set, voice quality, product cost, development effort, and scalability of the design. Developing a common hardware/software platform that can leverage experience across several different products is a desirable approach. However, each end device—IP phone, IAD (integrated access device), residential gateway, IP-PBX—has different requirements. It is a challenge to choose a processor platform that will meet all of the requirements. Most of the end devices also have a very short life cycle, being replaced by updated versions with new or different features, which places a premium on an approach that has greater flexibility and lends itself to rapid design techniques. This will ensure that time to market for new products is minimized.

The table that follows illustrates the available alternatives for VoIP hardware platforms. All of these approaches trade off bill of materials cost, design flexibility, development effort, and time to market for a product with a known performance level and resulting voice quality.

Each different approach has advantages and disadvantages, and the decision must be based on the product and market priorities. A platform based on a microcontroller will offer a familiar and low cost approach for most embedded developers. Microcontrollers offer friendly development environments, are typically a low cost item, and can handle the IP packet processing with ease. However, a microcontroller is not a very good choice for dealing with voice encoding/decoding and signal processing for voice quality enhancement, such as echo cancellation. This is a very limiting platform for an evolving VoIP product. Voice processing is much easier with a DSP architecture that excels in handling streams of data. For that reason, adding a DSP to the design makes a lot of sense. This enables tasks to be assigned to the processor most suited to execute them. This comes at an increase in the BOM, not just for the additional processor, but also for any memory and peripheral devices. Multiple chips (whether MCU plus DSP, or MCU plus ASIC) will lead to higher BOMs and higher engineering effort.

	MCU Only	MCU and DSP	Fixed Function	SoC	Convergent Processor
BOM Cost	Very good	Poor	Very good	Very good	Very good
Feature Flexibility	Fair	Very good	Poor	Poor	Very good
Development Effort/NRE	Easy	Difficult	Easy/difficult	Very difficult	Easy
Time to Market	Very good	Fair	Very good/poor	Poor	Very good

Dedicated, fixed-function hardware is another approach that will definitely have a negative impact on design flexibility. If it is a custom chip design, NRE and time to market suffer. If it is a commercially available ASSP, the ability to build a differentiated product is obviously impacted. Another level of sophistication in this approach is to build/buy an SoC with the MCU and DSP core on a single chip. This will reduce the package count at some loss in flexibility, but does offer programmability. Both the MCU and the DSP code can be tailored to the target application.

The final approach that we discuss is to use a single *convergent* processor to handle the control logic and the voice engine. By a convergent processor, we are referring to a single processor with signal processing performance in the realm of standalone DSPs. Various MCU makers have incorporated some signal processing functionality such as instruction-set extensions and MAC units onto MCU cores, but this approach lacks the essential architectural foundation required for high performance signal processing able to handle advanced voice quality enhancement, such as high performance acoustic echo cancellation and noise reduction. The Blackfin® processor from Analog Devices meets the convergent processor criteria, due to its high performance in both signal and control code execution. The rest of this paper will explore this approach, since convergent processing is the clear leader in hitting all of the critical success factors for a VoIP hardware platform.

Blackfin Convergent Processor Architecture Optimized for Media Processing

ADI's Blackfin single-processor system architecture has DSP features not found on any RISC microcontroller and important microcontroller characteristics not typically on DSPs. All packet processing and media processing are handled inside the same processor core, resulting in a more efficient implementation of an IP media processing solution. In the MCU plus DSP approach introduced previously, there is an important bottleneck for designers implementing a VoIP solution. Data must be transferred between the MCU and DSP subsystems, introducing delay and adding system overhead. The Blackfin processor is also a very high performance flexible processing engine. All of the Blackfin cycles can be assigned to perform control code processing or signal processing. There are not independent limits, such as you would find in an MCU plus DSP design. In addition, Blackfin processors are a fully programmable solution, eliminating the hardware blocks that lock a system designer into a fixed codec or algorithm. Adding or changing features is a software change, and the effort is greatly simplified with the option of stacked flash memory or board mounted flash. Blackfin processors feature a number of solution-oriented peripherals and interfaces that reduce the development effort, complexity, and parts count. Features such as a 10/100 Ethernet MAC, multiple DMA channels, LCD interface, multiple serial, parallel, and audio ports, and low power consumption all drive to the value of the solution.

In addition, the industry-leading application level, system level, and development tool software offerings support Blackfin processors. Leading VoIP solutions from Global IP Solutions and the open-source Asterisk package are optimized for Blackfin processors. Software from ADI (VDK), Unicoi (Fusion) and μClinux all support Blackfin processors with system level kernel and middleware solutions. Development tools from ADI (VisualDSP++® software) and the open-source GNU tools

enable rapid code development and validation. ADI enables different options to meet the customers design requirements for both hardware and software—covering the spectrum of standalone software components to reference designs to a full FOB product at industry-leading performance, power, and price.

ADSP-BF516 Low Power Blackfin Processor with VoIP-Oriented Peripherals

The ADSP-BF516 delivers high performance with available 400 MHz operation. It integrates key peripherals and seamlessly interfaces with other system devices, thus reducing BOM costs. Key features of the ADSP-BF516 include the following:

- Up to 400 MHz Blackfin core and 116 kB L1 on-chip memory for more performance to process high complexity media algorithms

- Ethernet MAC with DMA to provide network connectivity with less processor overhead

- PPI/LCD controller for IP phone user interface

- 2 serial ports (SPORTS) to connect to a codec and SLIC

- 1 removable storage interface (RSI) controller to connect MMC, SD, and CE-ATA devices for IP-PBX

- Up to 40 GPIOs to be used for IP phone keyboard and LED control

- 2 UARTs

- 2 SPI interfaces

- TWI (I²C®) controller

- 8 timers

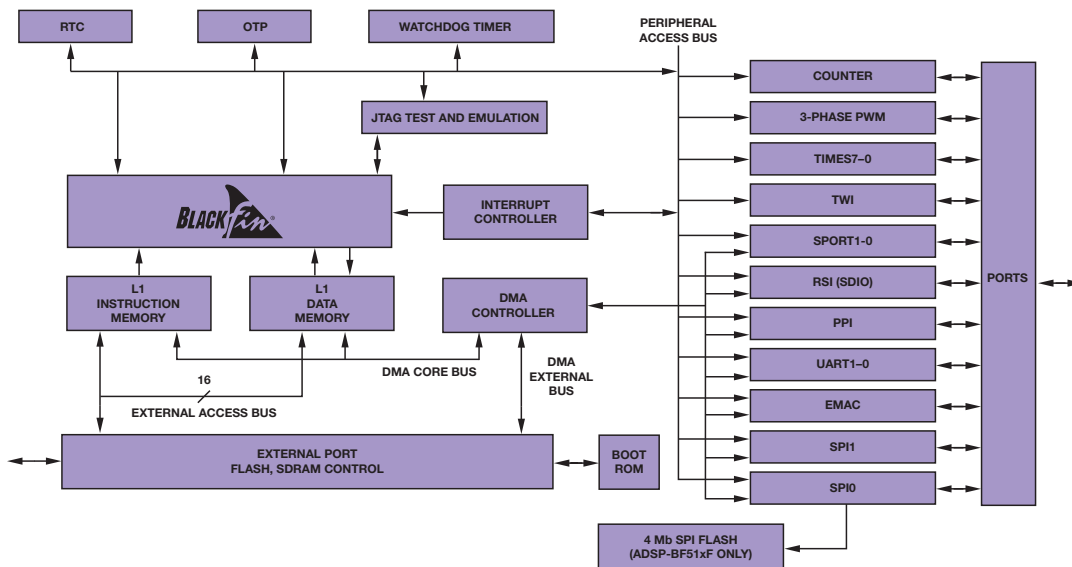- Lockbox™ Secure Technology/OTP 8 kB for security and IP protection

ADSP-BF516 low power Blackfin processor with VoIP-oriented peripherals.

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