Differences Between National Semiconductor 10/100 Mb/s Ethernet Physical Layer Devices

National Semiconductor
Application Note 1425
Brad Kennedy
December 2005

1.0 Purpose

This is an informational document detailing differences between National Semiconductor 10/100 Mb/s Ethernet Physical Layer devices, DP8384x. Some of these points may need to be considered when updating an existing 10/100 Mb/s Ethernet design, using one of National Semiconductor's Ethernet Physical Layer (PHY) products, to the new DP83848 PHYTER™ product. Although the basic functions of the device are similar, differences include feature set, pin functions, package and pinout, and possibly register operation. The impact to a design is dependant on which, and how, features of the previous device are used or implemented.

2.0 Hardware Differences

This section documents differences in the hardware as it relates to features, packages, operating voltages and environments, power requirements, and connections.

TABLE 1. Feature Differences

System Interfaces:	DP83848	DP83847	DP83846	DP83843
MII	3.3V	5V*	5V*	5V
RMII	Yes	No	No	No
SNI	Yes	No	No	Yes
JTAG	Available	No	No	No
100Base-FX Compliant	No	No	No	Yes
Auto-MDIX	Yes	No	No	No
Energy Detect	Yes	No	No	No
LED Outputs	3	6	6	6
INT Output	Yes	No	No	No
CLK-to-MAC Output	Yes	No	No	No
Temperature Range:				
0 to 70˚C	Yes	Yes	Yes	Yes
-40 to 85˚C	Available	No	No	No
-40 to 125˚C	Available	No	No	No
* 5V tolerant				

TABLE 2. Package Differences

	DP83848	DP83847	DP83846	DP83843
Package	48-LQFP	56-LLP	80-LQFP	80-PQFP
Footprint	7x7mm	9x9mm	14x14mm	14x14mm
Package Drawing	VBH48A	LQA56A	VHG80A	VJE80

TABLE 3. Supply Differences

	DP83848	DP83847	DP83846	DP83843
Supply Voltage	3.3v	3.3v	3.3v	5v
Active Power (Typ)	267mW	351mW	495mW	675mW

TABLE 4. Operating Temperature Differences

Temperature Range	DP83848	DP83847	DP83846	DP83843
0 to 70˚C	Yes	Yes	Yes	Yes
-40 to 85˚C	Available	No	No	No
-40 to 125˚C	Available	No	No	No

2.0 Hardware Differences (Continued)

Internal circuitry biasing of the DP83848 has changed from previous devices.

TABLE 5. Configuration Changes

	DP83848	DP83847	DP83846	DP83843
Bias Resistor Value	4.87K Ohm	10K Ohm	9.31K Ohm	4.87K Ohm, 70K Ohm
Bias Capacitor Value	n/a	n/a	n/a	.0033u, .10uF

2.1 Termination and PMD Biasing

Termination of the PMD receive pair (TPRD-/+) on previous Physical Layer devices consisted of a pair of 54.9 Ohms, AC biased to GND. This value, when seen in parallel with the internal receiver circuitry, provided an equivalent 100 Ohms impedance. The DP83848 has changed the internal receiver circuitry and now requires a pair of 49.9 Ohm resistors, DC biased to VDD of the device.

This matching of the termination resistors and common biasing, between the receiver and transmitter of the DP83848, allows the addition of the Auto-MDIX feature to the device.

TABLE 6. Termation and Biasing Differences

	DP83848	DP83847	DP83846	DP83843
TX Termination	49.9 Ohms	49.9 Ohms	49.9 Ohms	49.9 Ohms
TX Bias	3.3V	3.3V	3.3V	AC to GND
RX Termination	49.9 Ohms	54.9 Ohms	54.9 Ohms	49.9 Ohms
RX Bias	3.3V	AC to GND	AC to GND	AC to GND

Refer to the next set of figures for a graphic explanation of this.

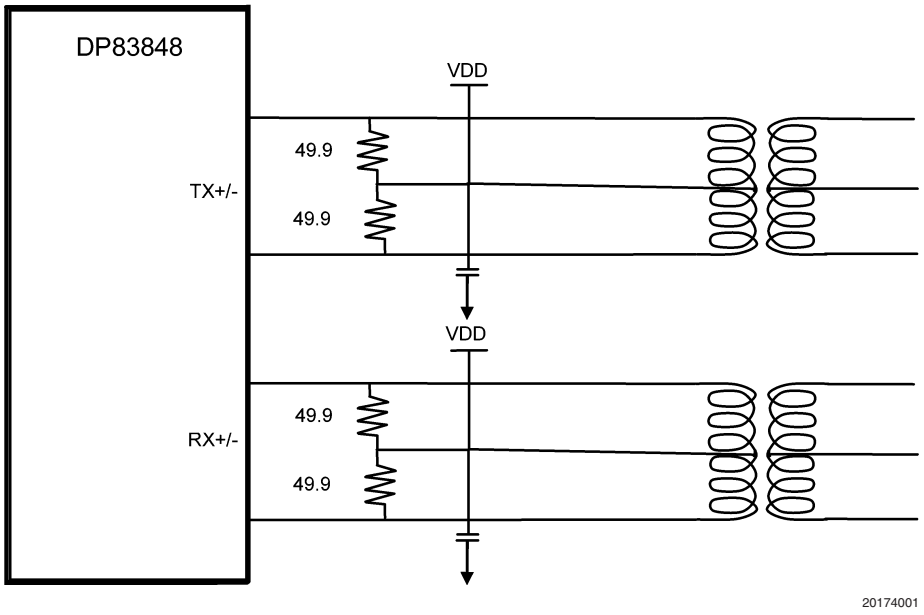

FIGURE 1. DP83848 PMD Connections (Termination & Biasing)

2.0 Hardware Differences (Continued)

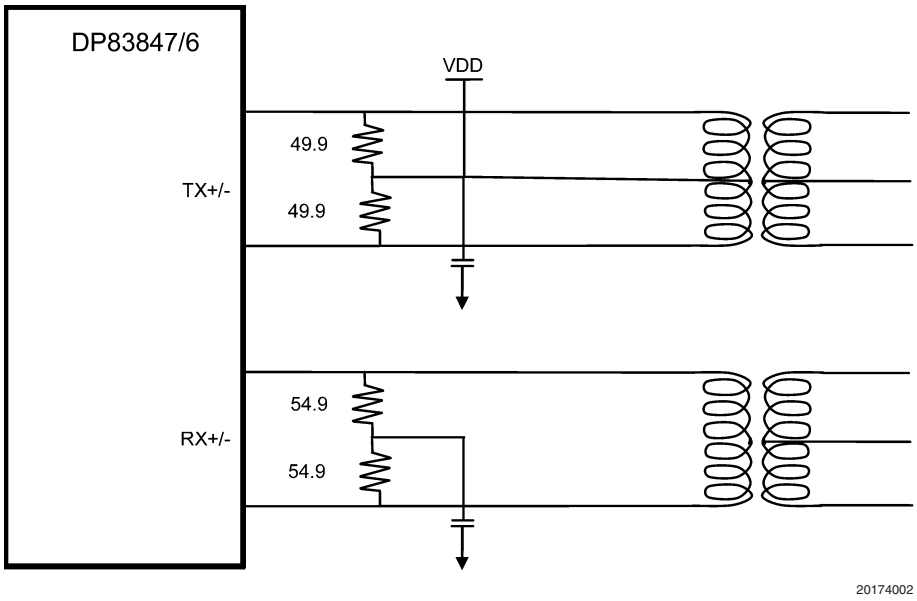

FIGURE 2. DP83847/6 PMD Connections (Termination & Biasing)

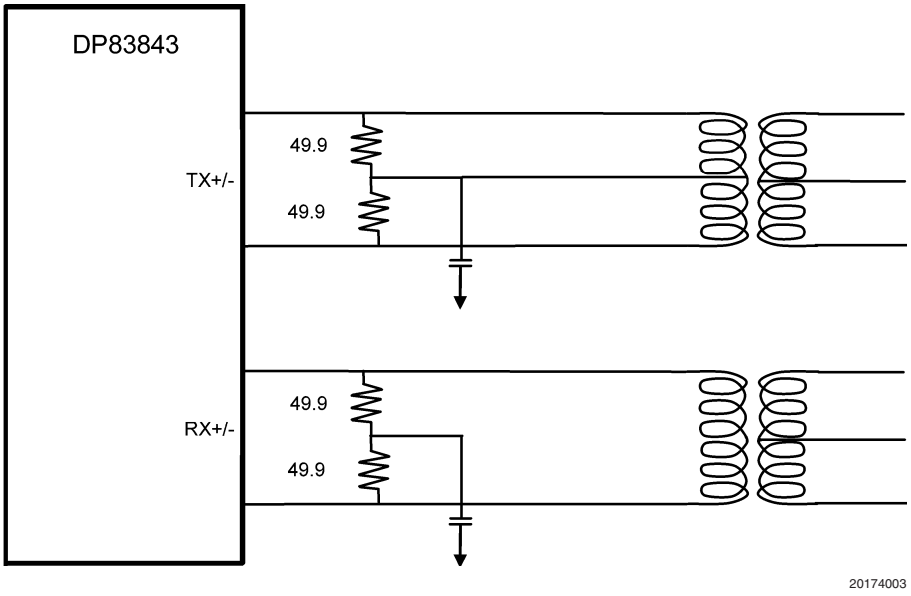

FIGURE 3. DP83843 PMD Connections (Termination & Biasing)

2.0 Hardware Differences (Continued)

TABLE 7. Pinout Differences

NSC Physical Layer Product Pin Comparison

DP83848 Signal Name	848 Pin #	847 Pin #	846 Pin #	843 Pin #	Description
MII Interface Pins					
MDC	31	25	37	35	MGMT DATA CLOCK
MDIO	30	24	36	34	MGMT DATA I/O
RXD0/PHYAD1:4	43,44, 45,46	30,29, 27,26	41,40, 39,38	15,14, 13,12	MII RX DATA
RX_CLK	38	32	45	18	MII RX CLOCK
RX_ER/MDIX_EN	41	33	46	19	MII RX ERROR
RX_DV/MII_MODE	39	31	44	20	MII RX DATA VALID
RX_EN	n/a	n/a	n/a	23	MII RX ENABLE
TXD0:3	3,4, 5,6	38,39, 40,41	54,55, 85,59	31,30, 29,28	MII TX DATA
TX_CLK	1	36	51	24	MII TX CLOCK
TX_EN	2	37	52	33	MII TX ENABLE
TX_ER	n/a	35	50	25	MII TX ERROR
COL/PHYAD0	42	43	60	21	MII COL DETECT
CRS/LED_CFG	40	45	61	22	MII CARRIER SENSE
PMD Interface Pins					
RD-/+	13,14	6,7	10,11	65,67	RX DATA
TD-/+	16,17	11,10	17,16	73,74	TX DATA
FXRD-/+_/AUIRD-/+	n/a	n/a	n/a	49,50	100FX or 10AUI RX DATA
FXTD-/+_/AUITD-/+	n/a	n/a	n/a	44,43	100FX or 10AUI TX DATA
FXSD-/+_/CD-/+	n/a	n/a	n/a	47,48	SIG DET or AUI COL DET
Clock Interface Pins					
X1	34	49	67	9	XTAL/OSC INPUT
X2	33	48	66	8	XTAL OUTPUT
LED Interface Pins					
LED_ACT/COL/AN_EN	26	22	32	42	COL LED STATUS
LED_ACT/COL/AN_EN	26	23	33	38	DUPLEX LED STATUS
LED_LINK/AN_0	28	21	31	39	LINK LED STATUS
LED_SPEED/AN_1	27	18	28	5	SPEED LED STATUS
LED_ACT/COL/AN_EN	26	n/a	n/a	n/a	ACT LED STATUS
LED_RX/PHYAD4	n/a	19	29	40	RX ACTIVITY LED
LED_TX/PHYAD3	n/a	20	30	41	TX ACTIVITY LED
Reset Function Pin					
RESET_N	29	46	62	1	RESET
Strap Pins					
PHYAD0:4	42,43,44, 45,46	23,22,21, 20,19	33,32,31, 30,29	42,41,40, 39,38	PHY ADDRESS
MDIX_EN/RX_ER	41	n/a	n/a	n/a	AUTO MDIX ENABLE
MII_MODE/RX_DV	39	n/a	n/a	n/a	MII MODE SELECT
SNI_MODE/TXD3	6	n/a	n/a	n/a	MII MODE SELECT
LED_CFG/CRS	40	45	61	n/a	LED CONFIGURATION
PAUSE_EN/RX_ER	n/a	33	46	n/a	PAUSE ENABLE
SERIAL10	n/a	n/a	n/a	69	10 SERIAL/NIBBLE SELECT
FXEN/COL	n/a	n/a	n/a	21	FIBER ENABLE
SYMBOL/CRS	n/a	n/a	n/a	22	SYMBOL MODE
THIN/REPEATER	n/a	n/a	n/a	63	THIN AUI/REPEATER

2.0 Hardware Differences (Continued)

TABLE 7. Pinout Differences (Continued)

NSC Physical Layer Product Pin Comparison

DP83848 Signal Name	848 Pin #	847 Pin #	846 Pin #	843 Pin #	Description
Bias Function Pins. Please refer to *Table 5* for additional information on these pins.					
RBIAS	24	3	3	61	BIAS RES CONNECTION
C1	n/a	42	n/a	n/a	REF BYPASS CAP
TXAR100	n/a	n/a	n/a	78	100TX AMP REF CTRL
TWREF	n/a	n/a	n/a	60	TWISTER REF RESISTOR
VCM_CAP	n/a	n/a	n/a	66	CM BYPASS CAP
Test Mode Pins					
TCK	8	n/a	n/a	n/a	JTAG TEST CLOCK
TDI	12	n/a	n/a	n/a	JTAG TEST DATA INPUT
TDO	9	n/a	n/a	n/a	JTAG TEST OUTPUT
TMS	10	n/a	n/a	n/a	JTAG TEST MODE SELECT
TRST#	11	n/a	n/a	n/a	JTAG TEST RESET
AN_0/LED_LINK	28	15	25	4	TEST MODE SELECT
AN_1/LED_SPEED	27	16	26	3	TEST MODE SELECT
AN_EN/LED_ACT/COL	26	17	27	n/a	TEST MODE SELECT
Special Function Pins					
25MHz_OUT	25	n/a	n/a	n/a	25 MHz CLOCK OUTPUT
PWR_DOWN/INT	7	n/a	n/a	n/a	POWER DOWN/INT
PFBIN1,2	18,37	n/a	n/a	n/a	POWER FEEDBACK IN
PFBOUT	23	n/a	n/a	n/a	POWER FEEDBACK OUT
Supply Pins					
VDD	22,32,48	14,28,56, 57,59,63	4,7,12, 14,24,35, 43,49,57, 65,72	6,10,16, 26,36,46, 52,54,68, 72,76,79	3.3V (5.0V FOR DP83843)
GND	15,19,35, 36,47	58,60,62, 64,65	2,6,9,13, 15,18,48, 73,34,42, 53,56,64, 19,76,79	7,11,17,27, 32,37,45, 51,53,57, 64,70,71, 75,77,80	GROUND
Reserved Pins					
RESERVED	12,20	1,2,4, 5,8,9, 12,13,34, 44,47,50, 51,52,53, 54,55, 61	1,5,8, 20,21,22, 47,63,68, 69,70,71, 74,75,77, 78, 80	2,55,56, 58,59,62	RES (N/C FOR DP83843)

3.0 Configuration (Software related) Differences

This section covers differences between the devices as it relates to software configuration of the devices.

3.1 Register Differences

All the IEEE specified registers of NSC Physical Layer devices comply with the respective IEEE standards. Only vendor specific registers have functions that may vary from device to device. If none of the vendor specific registers are modified, for operation in the system application, the devices will have similar operation. In designs that do access or adjust any of these optional registers, the system may use the PHY_ID register, offset 03h, to determine appropriate settings of device registers. Specific functions, of these vendor defined registers, may be available in another register,or possibly in a different bit within the same register location. For additional information, or more specific definitions, please refer to the applicable datasheet(s).

TABLE 8. Register Bit Definitions

Register Address	Register Name	Register Description	Device			
Hex			DP83848	DP83847	DP83846	DP83843
00h	BMCR	Basic Mode Control	No Change			
01h	BMSR	Basic Mode Status	No Change			
02h	PHYIDR1	PHY ID 1	2000h	2000h	2000h	2000h
03h	PHYIDR2	PHY ID 2	5C90h	5c30h	5C23h	5C10h
04h	ANAR	Auto-Neg Adv	11 ASM_DIR	Res	Res	Res
05h	ANLPAR	Auto-Neg Link Partner Ability	11 ASM_DIR 10 Pause	Res	Res	Res
07h	ANER	Auto-Neg Exp	No Change			
08h-Fh	RES		Res	Res	Res	Res
10h	PHYSTS	PHY Status	15:4 Register Changes 3 Loopback Status 2 Duplex Status 1 Speed Status 0 Link Status			
11h	MICR	MII Interrupt Control	2 Test Interrupt 1 Interrupt Enable 0 Int Output Enable	Res	Res	0 Test Interrupt
12h	MISR	MII Interrupt Status	New Register Functions	Res	Res	15 MII Int Pending 14:0 Res
13h	RES		Res	Res	Res	Disconnect Counter
14h	FCSCR	False Carrier Sense Counter	15:8 Res 7:0 FCSR Count	15:8 Res 7:0 FCSR Count	15:8 Res 7:0 FCSR Count	15:0 FCSR Count
15h	RECR	RX Error Counter	15:8 Res 7:0 RxErr Count	15:8 Res 7:0 RxErr Count	15:8 Res 7:0 RxErr Count	15:0 RxErr Count
16h	PCSR	PCS Sub-Layer cfg and sts	15:0 Register Changes	PCSR	PCSR	PCSR
17h	RBR	RMII and Bypass	New Register	Res	Res	LBR
18h	LEDCR	LED Direct Control	New Register	Res	Res	10BTSCR

3.0 Configuration (Software related) Differences (Continued)

TABLE 8. Register Bit Definitions (Continued)

Register Address	Register Name	Register Description	Device			
Hex			**DP83848**	**DP83847**	**DP83846**	**DP83843**
19h	PHYCR	PHY Control	15:5 Register Changes 4:0 PHY Address	4:0 PHY Addr	4:0 PHY Addr	4:0 PHY Addr
1Ah	10BTSCR	10 Base-T Status/Control	15:0 Register Changes	15:9 Unused	15:9 Unused	Res
1Bh	CDCTRL1	CD Test Control	15:0 Register Changes			Res
1Ch	RES		Res	Res	Res	Res
1Dh	EDCR	Energy Detect Control	New Register	Res	Res	Res
1Eh-1Fh	RES		Res	Res	Res	Res

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560