Technical Note

IBIS Behavioral Models

Introduction

The Input/Output Buffer Information Specification (IBIS) is a standard for describing the analog behavior of a buffer. The specification provides a standard parsed file format consisting of current-voltage (I-V) characteristics, voltage-time (V-t) characteristics, device package parasitics, input capacitance, and timing measurement information for several types of I/O structures. IBIS models provide information that accurately models a buffer's behavior without revealing proprietary information about the circuit's structure or fabrication process. Systems designers use IBIS models to perform board level signal integrity simulations and timing analyses.

HSPICE vs. IBIS

Micron provides I/O models both in HSPICE® and IBIS formats, but, unlike IBIS models, HSPICE models must be encrypted to protect Micron's IP, which limits their usefulness to the Synopsys® HSPICE simulator. Distinct advantages to using IBIS models include the following:

- Enables portability between multiple electronic design automation (EDA) software tools—allowing customers greater flexibility in choosing EDA software integrating layout and simulation capabilities
- Provides competitive accuracy
- Completes simulations faster than SPICE models, allowing solution space analysis through sweeps of multiple parameters in a timely manner
- Enables easy integration of package models into simulations
- Provides measurement information, enabling automation of signal integrity and timing verification in EDA software

Structure of an IBIS Model

An IBIS model consists of a series of ASCII-formatted keywords, such as [File Name] and [Model], that are easily parsed by software. Some EDA software uses the keywords directly, and some translate the keywords into its own unique modeling language. The header of an IBIS file contains general information, such as the file name, the IBIS version, the file revision, and notes. The notes section typically includes revision history, information about model limitations, and/or key information about model usage. The rest of the IBIS file includes models of input, output, I/O buffers, and package models.

The elements of a basic CMOS I/O buffer are shown in Figure 1 on page 2. Various keywords in an IBIS file describe the behavioral characteristics of each of these elements. The RLC package parasitics seen in Figure 1 can be included in multiple forms. The minimum, typical, and maximum R, L, and C values for all the signals of a specific package are summarized using the [Package] keyword. Individual R, L, and C

values for the specific pins of a package are listed next to each pin under the [Component] keyword. The [Component] keyword is also where you find Micron part numbers. Many Micron IBIS models contain advanced package models that include multi-segment models or matrices of RLC coupling, which are accessed using the [Package Model] keyword.

When advanced package models containing RLC matrices are present in an IBIS file, the [Pin Mapping] keyword is usually present as well. This keyword indicates the power and ground buses to which a given driver, receiver, or terminator is connected. Including this information improves power integrity simulation.

If a component includes differential pins, such as CLK/CLK# or DQS/DQS#, the differential relationship is declared with the [Diff_pin] keyword. This keyword is found below each [Component] keyword section.

Many output buffers can be configured for multiple drive strengths and may require unique models for specific data rates. Receivers may also include multiple on-die termination (ODT) options. The [Model Selector] keyword is included to link specific buffer model options to specific pins on a component.

Figure 1:   Elements of an IBIS Model
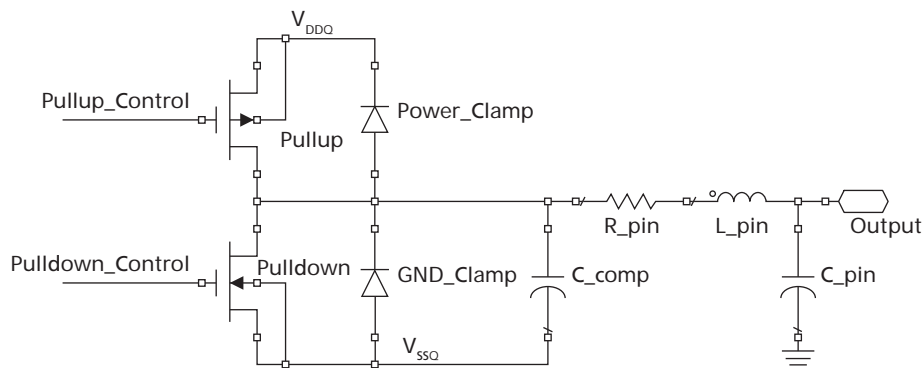
Each [Model] keyword section contains all the data needed to model one configuration of an input, output, or I/O buffer. Input buffers are the simplest model, as they only need to describe the characteristics of the power and ground clamp diodes, the buffer capacitance, and the input receiver switching thresholds. Some input buffers may also include ODT circuits. The I-V characteristics of the ODT circuit may be included in descriptions of the power and ground clamp diodes or may be modeled separately as discussed in the [Submodel] section on the next page.

I-V data tables describing the power and ground clamp diodes are found under the [POWER Clamp] and [GND Clamp] keywords. Data is typically included for three simulation corners: minimum, typical, and maximum. The minimum corner is the combination of process, voltage, and temperature that causes the slowest device operation. The typical corner describes typical device operation, and the maximum corner describes the fastest operation of the device. Including data for all three corners results in worst-case, typical-case, and best-case models. The I-V curve data is also included to provide the full range of voltages a buffer can see in a system environment, from $-V_{DDQ}$ to $2 \times V_{DDQ}$. An example of [GND Clamp] I-V data is shown below.

[GND Clamp]
|
|Voltage   I(typ)   I(min)   I(max)
|
    −1.5   −354.5E-3   −300.2E-3   −399.4E-3
    −1.0   −51.3E-3   −30.2E-3   −73.6E-3
    …
    −0.2   0.0E-3   0.0E-3   0.0E-3
    3.0   0.0E-3   0.0E-3   0.0E-3

I-V data for the pulldown portion of the driver is included with the [Pulldown] keyword. I-V data for the pullup portion of the driver is included with the [Pullup] keyword. [Pullup] and [POWER Clamp] data is entered into the table using the formula $V_{TABLE} = V_{DDQ} - V_{OUTPUT}$ because the current through the pullup device and power clamp diodes is dependent on the voltage between the output and V_{DDQ}. V_{DDQ} voltage is specifically defined in the IBIS model with the [Pullup Reference] and/or the [Voltage Range] keywords.

The C_comp sub-parameter of the [Model] keyword is used to describe the die capacitance. Minimum, typical, and maximum values can be defined. While die capacitance has voltage and frequency dependencies, the C_comp value is a simple capacitance model, so a value of capacitance must be chosen that best represents the die capacitance over the buffer's intended operating range.

While the I-V data described above represents the DC behavior of the buffer, the AC switching behavior of the buffer is modeled with the [Ramp], [Rising Waveform], and [Falling Waveform] keywords. Micron IBIS models contain two [Rising Waveform] tables and two [Falling Waveform] tables to provide the most accurate modeling of the buffer. Each V-t waveform shows the buffer transitioning HIGH or LOW while driving a test load, typically a 50Ω resistor terminated to V_{SSQ} or V_{DDQ}. All four waveforms reference a common input stimulus time. This ensures the data shows the correct turn-on and turn-off relationships of the pullup and pulldown devices during rising and falling edge transitions. An example of a [Rising Waveform] is shown below. The [Ramp] data summarizes the V-t waveform data. It provides a table of rising and falling edge slew rates as measured from the 20% to 80% voltage thresholds of the [Rising Waveform] and [Falling Waveform] data. All tables assume that the effect of die capacitance, C_comp, is included.

[Rising Waveform]
R_fixture = 50.0
V_fixture = 0.0
|
|Time   V(typ)   V(min)   V(max)
|
    −0.00s 0.0E-3   0.0E-3   0.0E-3
    …
    935ps   890.0E-3   856.1E-3   925.8E-3

The [Model Spec] keyword defines parameters that are useful for measuring timing with IBIS models. It provides information to the EDA software about input voltage switching thresholds and timing specification test loads. The [Receiver Thresholds] keyword adds more detailed information about modern input receiver designs, such as those found in DDR devices. [Receiver Thresholds] defines a set of receiver input thresholds as they relate to an external reference voltage, V_{REF} as well as their sensitivity to variations in V_{REF}

The IBIS specification contains many other keywords that are used to model advanced buffer designs, including:

- The [Submodel] keyword is used in Micron models to add the I-V characteristics of ODT circuits. A complete [Submodel] contains [Power Clamp] and [Ground Clamp] I-V data tables.
  - The [Power Clamp] table describes the I-V characteristics of the portion of the ODT circuit tied to V_{DDQ}.
  - The [GND Clamp] table describes the I-V characteristics of the portion of the ODT circuit tied to V_{SSQ}.
  - The combination of I-V data from both tables models the full ODT circuit.
- The [External Circuit] and [External Model] keywords were added in IBIS 4.1 and are multi-lingual model extensions that add support for SPICE, VHDL-AMS, and Verilog-AMS.
- The [Algorithmic Model] keyword was added in IBIS 5.0 to support modeling of serializer/deserializer (SERDES) devices. This keyword defines an algorithmic modeling interface for linking executable shared library files to IBIS.
- The [ISSO PD], [ISSO PU], and [Composite Current] keywords were also added in IBIS 5.0 to improve the modeling of simultaneous switching output (SSO) effects. This significantly improves the ability to analyze power distribution network design with IBIS models.

Support for the multilingual model extensions and AMI and SSO modeling keywords varies among EDA software vendors.

IBIS Open Forum

The IBIS Open Forum is the industry organization responsible for managing the IBIS specification and is comprised of EDA software vendors, model users, and model creators. It is open to individual volunteers, but paid member companies may cast votes regarding specification changes and approvals, financial matters, election of officers, and other organizational issues involving the Open Forum. Its parent organization is TechAmerica. The IBIS 4.2 standard, referred to as ANSI/EIA-656-B, is currently accepted as the national standard. Open Forum members also wrote the "IBIS Cookbook," which describes the recommended steps for creating IBIS files and can be downloaded from the IBIS Web site.

IBIS Model Quality

Model quality is an important topic of interest in the IBIS community. A subcommittee of the IBIS Open Forum, the IBIS Quality Task Group, works to improve model quality throughout the electronics industry. The IBIS Quality Specification 2.0 was released in 2009 and describes in detail the checks that should be performed on IBIS files before they are used. The IBIS Golden Parser, which is a free utility available from the IBIS Web site, can be used to check for proper syntax. Micron supports the work of the IBIS Quality Task Group and follows the recommendations laid out in the IBIS Quality Specification. This includes creation of an IBIS model quality report that is released with every Micron IBIS model.

Future Versions of IBIS

The IBIS 5.0 specification was ratified by the IBIS Open Forum in 2008. Changes to the IBIS specification are proposed through a buffer issue resolution document (BIRD). The Open Forum members vote on inclusion of BIRDs in specific releases of the specification; a majority vote is required to ratify proposed changes. New IBIS specifications maintain backward compatibility with previous versions. Many BIRDs are developed through the work of another IBIS subcommittee, the IBIS Advanced Technology Modeling (ATM) Task Group. The ATM task group, quality task group, and the Open Forum work in concert to improve the capabilities and quality of IBIS models.

Micron Support of IBIS

Micron has been a member of the IBIS Open Forum for many years and fully supports the IBIS specification. IBIS models for most Micron products are available for download from the Micron Web site, www.micron.com. Questions and comments about Micron IBIS models may be e-mailed to modelsupport@micron.com.

More Information

Information about IBIS models and the IBIS Open Forum is available at the IBIS Web site, www.eigroup.org/ibis/. To subscribe to the IBIS users' group reflector, send an e-mail to ibis-users@eda.org. Once subscribed, you can send questions to the ibis-users@eda.org reflector.

Additional resources mentioned in this document include:
• IBIS Quality Specification 2.0
• IBIS 5.0 Specification
• IBIS Cookbook
• IBIS Golden Parser

These and other resources may be found at the IBIS Web site: www.eigroup.org/ibis.

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Revision History