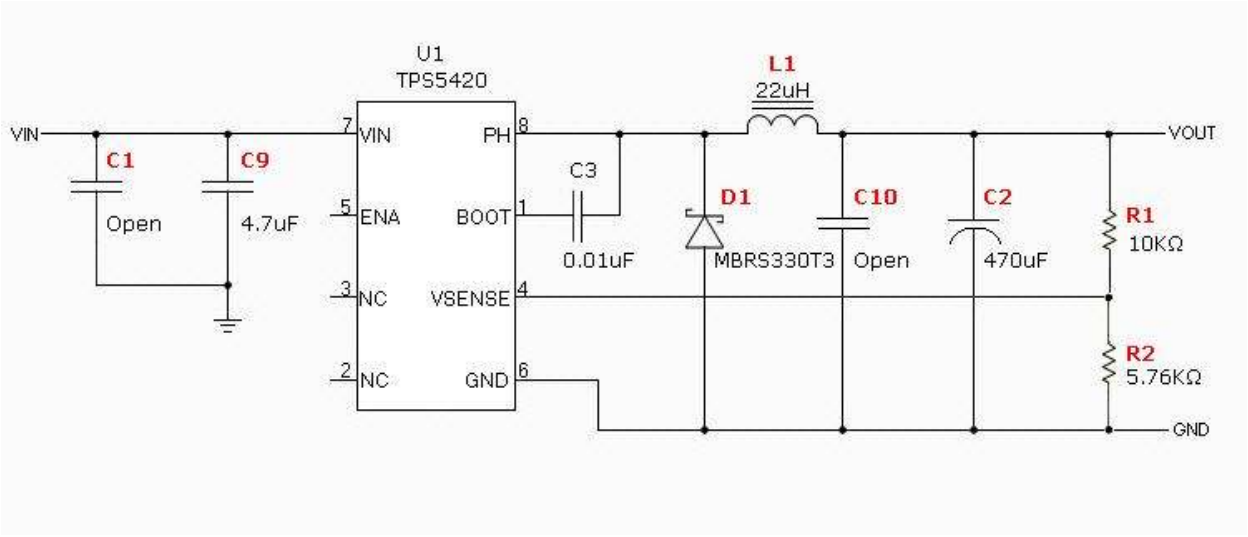
**We recommend selecting 'Landscape' orientation to print this page.**
**In some browsers, the tables and images may get cut off when printing in 'Portrait' mode.**

# Design Summary

Design Name: **Blackfin IP Phone (3V3)**

| | | | |
|---|---|---|---|
| Design ID: | **117079** | Created By User: | **Rômulo Mendes** |
| Creation Date: | **06 Jul 2010** | Design Type: | **PowerSupply** |
| Local Time: | **08:29 AM** | | |

# Schematic


U1
TPS5420
L1
22uH
VIN
C1
Open
C9
4.7uF
7 VIN
5 ENA
3 NC
2 NC
PH 8
BOOT 1
VSENSE 4
GND 6
C3
0.01uF
D1
MBRS330T3
C10
Open
C2
470uF
R1
10KΩ
R2
5.76KΩ
VOUT
GND

# Analysis

## Analysis - Main

| Parameter | User Input Minimum | User Input Nominal | User Input Maximum | Default Input Minimum | Default Input Nominal | Default Input Maximum | Calculated Minimum | Calculated Nominal | Calculated Maximum | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| Input Voltage | 8.00 | - | 10.00 | - | - | - | - | - | - | Volts |
| Input Ripple | - | - | - | - | - | 200 | - | - | 275.2 | mVp-p |
| UVLO(Start) | - | - | - | - | - | - | - | 5.30 | - | Volts |
| UVLO(Stop) | - | - | - | - | - | - | - | - | - | Volts |
| Switching Frequency | - | - | - | - | 500 | - | - | - | - | KHz |
| Slow Start | - | - | - | - | 8.00 | - | - | - | - | ms |
| Estimated PCB Area | - | - | - | - | - | - | - | 428 | - | mm² |
| Max Component Height | - | - | - | - | - | 25 | - | - | 3 | mm |

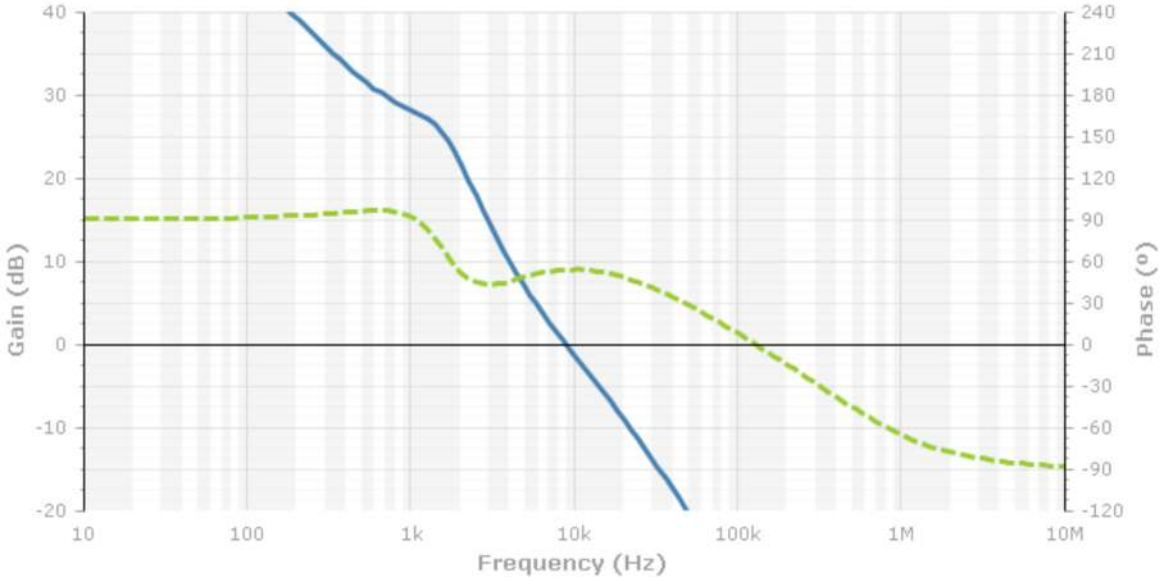
## Analysis - Output1

| Parameter | User Input Minimum | User Input Nominal | User Input Maximum | Default Input Minimum | Default Input Nominal | Default Input Maximum | Calculated Minimum | Calculated Nominal | Calculated Maximum | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage | - | 3.300 | - | - | - | - | 3.298 | - | 3.451 | Volts |
| Output Ripple | - | - | - | - | - | 66 | - | - | 3 | mVp-p |
| Output Current | - | - | 2.000 | 0.100 | - | - | - | - | - | Amps |
| Inductor Peak to Peak Current | - | - | - | - | - | - | 0.223 | - | 0.263 | Amps |
| Current Limit Threshold | - | - | - | - | 3.0 | - | - | - | - | Amps |
| Gain Margin | - | - | - | -10 | - | - | - | -35 | - | dB |
| Phase Margin | - | - | - | 60 | - | - | - | 54 | - | Deg. |
| Upper FET RDSon | - | - | - | - | - | - | 113 | - | 113 | mOhms |
| Duty Cycle | - | - | - | - | - | - | 37.2 | - | 46.3 | % |
| On Time Min(switch) | - | - | - | - | - | - | 619.6 | - | 1158.7 | ns |
| Cross Over Frequency | - | - | - | - | - | - | - | 9 | - | KHz |

# Loop Response

## LoopResponse - Output1

| Switching Freq | Cross Over Freq | LC Corner Freq | ESR Zero Freq | Gain Margin | Phase Margin |
|---|---|---|---|---|---|
| **500Khz** | **9Khz** | **1.6Khz** | **33.9Khz** | **-35 dB** | **54 Deg.** |




Scale Up

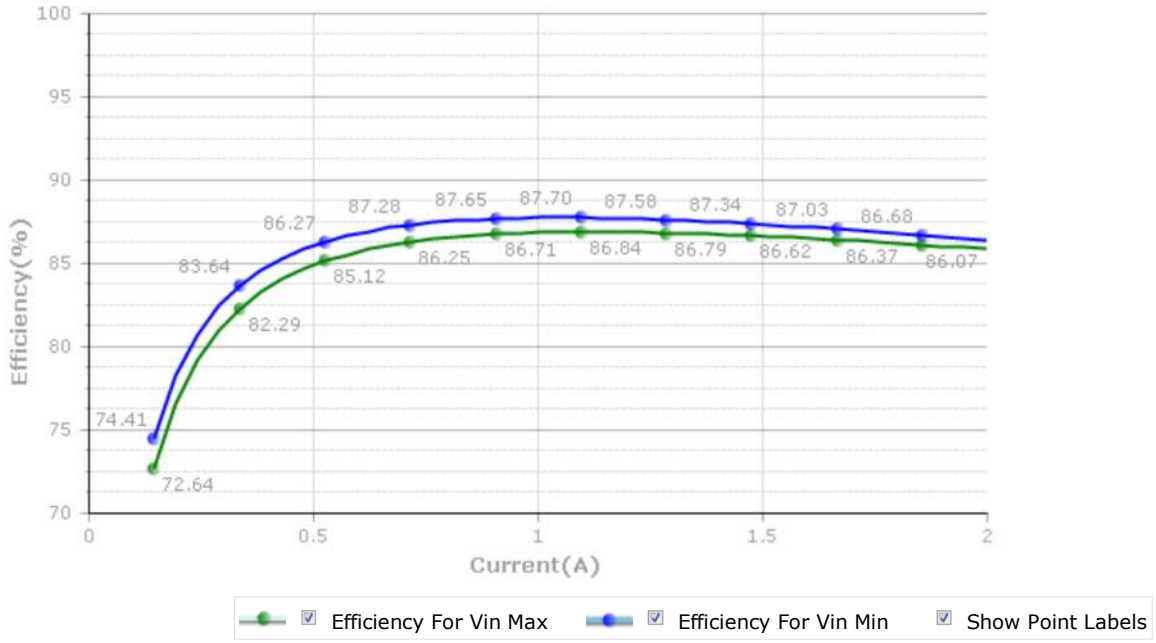
Scale Down

This graph was generated using the following conditions: Nominal Switching Freq, Minimum Vin, Maximum Load, and Maximum Capacitor ESR. To customize conditions use the 'What If Analysis' form

- Open Loop Error Amplifier Gain
- Compensated Error Amplifier Gain
- Compensated Error Amplifier Phase
- Power Stage Gain
- Power Stage Phase
- Total Gain
- Total Phase

# Efficiency

## Efficiency - Output1



# Stress

| Device | Rated Voltage | Calculated Voltage | Rated Current (RMS) | Calculated Current (RMS) | Error Message | Power | Calculated Max Temp |
|---|---|---|---|---|---|---|---|
| C9 (High Freq. Input Cap) | 16V | 10V | 2.5A | 1A | | 5mW | - |
| C2 (Bulk Output Cap) | 6.3V | 3.32V | 4.4A | 76mA | | 58uW | - |
| L1 (Output Inductor) | - | - | 2.5A | 2A | | 224mW | - |
| D1 (Catch Diode) | 30V | 10V | 3A | 1.26A | | 456mW | 61°C |
| U1 (Converter) | 40V | 10V | 2A | 1.36A | | 419mW | 55°C |

Each loss in this view is the worst case calculation for the individual component. The conditions that cause the worst case loss will not all occur at the same time for all components. Therefore adding up the individual worst cases losses to get a total loss of the system is not realistic.

Max Junction Temperature is calculated using Ambient Temperature 25°C along with the resistance (junction to ambient) specified by the manufacturer, with their standards for board layout.

It is recommended that the user review the specifications given by the FET manufacturer for their board layout standards.

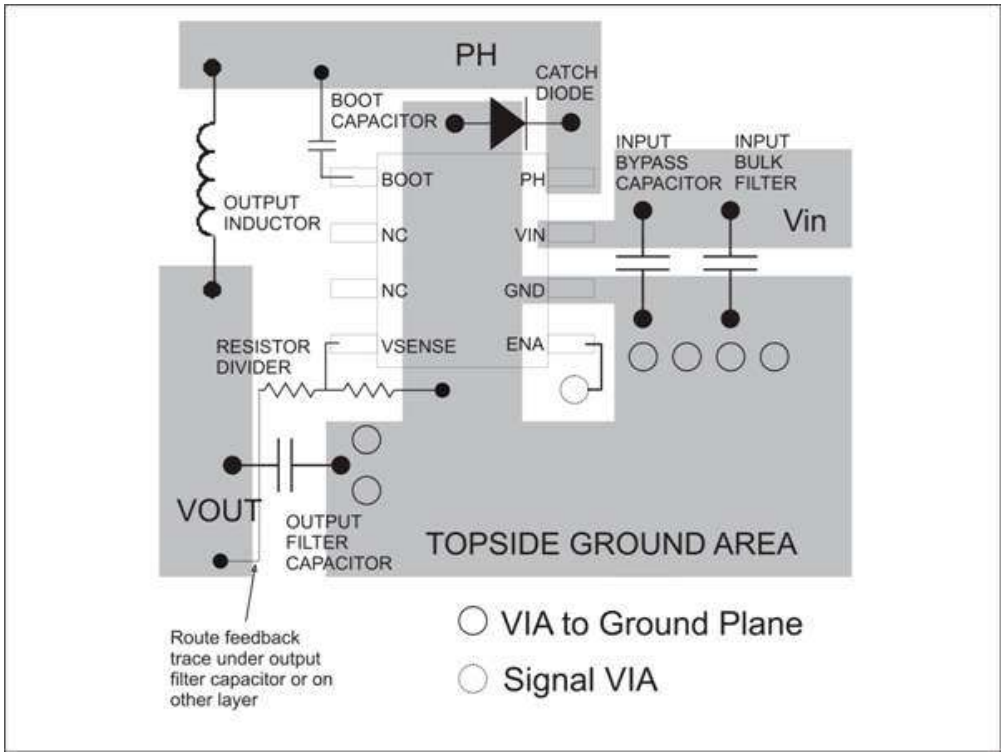
Using a low cost PCB with minimal copper will have a great impact on heat dissapation and could lead to much higher junction temperatures.

Calculated Voltage does not take into account spike voltages caused by various parasitic inductances and capacitances that are factors of board layout

# Bill Of Materials

| Name | Quantity | Part Number | Description | Manufacturer | Package | Area(mm²) | Height(mm) |
|---|---|---|---|---|---|---|---|
| C2 | 1 | 6TPD470M | Capacitor, POSCAP, 470uF, 6.3V, 20% | Sanyo | TPD-D4D | 31 | 3 |
| C3 | 1 | Standard | Capacitor, Ceramic, 0.01uF, 20V, 1% | Standard | 0805 | 3 | 1 |
| C9 | 1 | GRM21BR61C475KA88L | Capacitor, Ceramic, 4.7uF, 16V, 10% | muRata | GRM21B 0805 | 3 | 1 |
| D1 | 1 | MBRS330T3 | Diode, Schottky, 30V, 3A | On-Semi | SMC | 56 | 3 |
| L1 | 1 | 744066220 | Inductor, 22uH, 2.5A, 55.8mΩ | Wurth Electronics | XLH | 100 | 3 |
| R1 | 1 | Standard | Resistor, SurfaceMount, 10KΩ, 100mW, 1% | Standard | 0603 | 2 | 1 |
| R2 | 1 | Standard | Resistor, SurfaceMount, 5.76KΩ, 100mW, 1% | Standard | 0603 | 2 | 1 |
| U1 | 1 | TPS5420 | IC, Converter, 8 pins | Texas Instruments, Inc. | SOIC | 31 | 2 |

# Layout




**Layout Guidelines:**

TPS5420/10

The VIN pins should be connected together on the printed circuit board (PCB) and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS5430 ground pin. The best way is to extend the top side ground area from under the device adjacent to the VIN trace, and place the bypass capacitor as close as possible to the VIN pins. The minimum recommended bypass capacitance is 10 uF ceramic with a X5R or X7R dielectric.

There should be an area of ground one the top layer directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. The GND pin should be tied to the PCB ground by connecting it to the ground area under the device as shown.

The PH pin should be routed to the output inductor catch diode and boot capacitor. Since the PH connection is the switching node, inductor should be located very close to the PH pins and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The catch diode should also be placed close to the device to minimize the output current loop area. Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths The component placements and connections shown work well, but other connection routings may also be effective.

Connect the output filter capacitor(s) as shown between the VOUT trace and GND. It is important to keep the loop formed by the PH pins, Lout, Cout and PGND as small as is practical.

Connect the VOUT trace the VSENSE pin using the resistor divider network to set the output voltage. Do not route this trace too close to the PH trace. Do to the size of the IC package and the device pin-out, the trace may need to be routed under the output capacitor. Alternately, the routing may be done on an alternate layer if a trace under the output capacitor is not desired.

If the grounding scheme shown is utilized, it will be necessary to use a via connection to a different layer to route to the ENA pin.