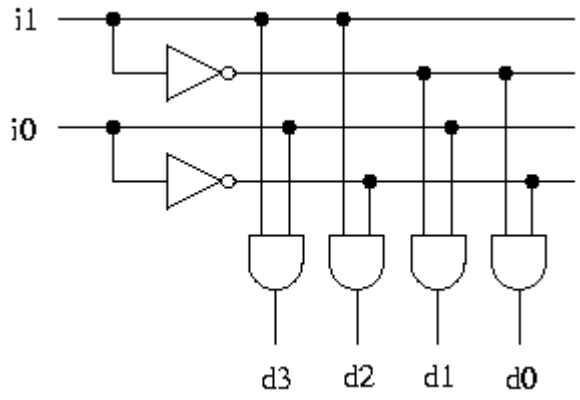
Lab-0

Create a 2x4 Decoder.




```
module jdoodle;
reg I0, I1;
wire A, B, C, D;

   decdr decoder1(I1, I0,  A, B, C, D);

   initial begin
      $display ("(%b %b),  [%b %b %b %b]   --  %d", I1, I0,  A, B, C, D, $time);
         I1=0; I0=0;
      #1  $display ("(%b %b),  [%b %b %b %b]   --  %d", I1, I0,  A, B, C, D, $time);
         I1=0; I0=1;
      #1  $display ("(%b %b),  [%b %b %b %b]   --  %d", I1, I0,  A, B, C, D, $time);
         I1=1; I0=0;
      #1  $display ("(%b %b),  [%b %b %b %b]   --  %d", I1, I0,  A, B, C, D, $time);
         I1=1; I0=1;
      #1  $display ("(%b %b),  [%b %b %b %b]   --  %d", I1, I0,  A, B, C, D, $time);
      $finish;
   end
endmodule

module decdr(i1,i0, a,b,c,d);
input i1, i0;
output a,b,c,d;

* Write Verilog hardware description code here to implement the above  2x4 decoder *

endmodule
```