GaS and GaSe Ultrathin Layer Transistors

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Two-dimensional materials have attracted significant attention from the scientific community in the last few years due to their potential exotic transport physics and prospects for technological applications in various fields. As the first prototype of layered structures, graphene has been widely studied for its unusual electrical, optical, magnetic, and mechanical properties.[1–4] In particular, graphene-based transistors have been explored extensively for their potential use in logic and radio-frequency applications.[5,6] The main advantage of graphene-based field-effect transistors (FET) is the associated carrier high mobility of up to 10^6 cm^2 V^{-1} s^{-1}.[5,6] However, several problems remain with graphene due to absence of a bandgap, which is essential for transistor applications. Subsequently, considerable efforts have been made to "open" the bandgap of graphene, such as with graphene nanoribbons.[7] In this context, there has been an extensive search for other layered materials that are analogous to graphene but with semiconducting characteristics.[8–10]

Single-layers of various layered materials have been obtained using a micromechanical cleavage method.[8,10] Materials such as MoS_2,[9–12] $NbSe_2$,[13,14] h-BN,[15,16] Bi_2Te_3,[17,18] and Bi_2Se_3.[19,20] have emerged as potential materials for nanoelectronic devices due to their useful properties and ease of fabrication. The advantages originate from high surface-to-volume ratio, unconventional electrical, mechanical, magnetic, and optical properties of these layered materials. Transition metal dichalcogenides are inorganic layered materials that exhibit a large variety of electronic properties ranging from semiconductivity to superconductivity making these layered materials potentially useful in next generation nanoelectronic devices.[21] This has provided the motivation to investigate the synthesis of graphene analogues of the layered metal chalcogenides by different chemical approaches.[9,22,23]

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Among the various compounds, MoS_2 has been widely investigated for device applications. Recent reports show that single-layer MoS_2 has a direct bandgap of 1.8 eV.[24] The successful fabrication of FETs with high ON/OFF ratios[11] and NOR logic operation,[25] phototransistors,[12] and gas sensors[26] show the versatility of single layer MoS_2. Recently, we have reported the rapid characterization of various other layered materials including GaS and GaSe by using a micromechanical cleavage as well as their optical contrast on various Si/SiO_2 substrates for high visibility.[10] It is important to fabricate transistors based on these new materials for bench-marking basic transport characteristics towards possible use in device applications.

GaS and GaSe are stable layered metal dichalcogenides semiconducting materials with wide bandgaps (E_g = 3.05 eV and 2.10 eV, respectively). The hexagonal structure of GaS and GaSe has a layered (S-Ga-Ga-S and Se-Ga-Ga-Se) repeating unit built by six membered Ga_3S_3 and Ga_3Se_3 rings. The micromechanical cleavage technique has been used to fabricate single layer sheets of GaS and GaSe by repeatedly peeling the bulk material and transferring this peeled material on top of a SiO_2/Si substrate using adhesive tape. This technique has been proven to be an easy and very fast way of producing highly crystalline and large size (tens of micrometers) sheets of single and few layers. To our knowledge, very few reports are available in literature about the electrical properties of bulk GaS.[27–32] The reason for this can be the high resistivity of these layered material and low mobility of the GaS bulk crystals (bulk mobility ≈ 80 cm^2 V^{-1} s^{-1}) in addition to a difficulty in performing the Hall-effect measurements.[27–32] There are few reports on electrical properties of bulk GaSe crystals (bulk mobility ≈ 215 cm^2 V^{-1} s^{-1}).[31–38] Here, we report for the first time the fabrication and demonstration of the 2D single-sheet GaS and GaSe FETs. Mechanically robust GaS and GaSe material make them perfect candidates for use in FETs enabling substitution of organic-based FETs.

Ultrathin layers of GaS and GaSe were identified first by using optical microscope with the specific color contrast on 500 nm SiO_2/Si and were further confirmed using atomic force microscopy (AFM) and Raman spectroscopy as reported previously.[10] **Figure 1**a shows the schematic of bottom-gate FET device based on single sheet of GaS and GaSe and Figure 1b shows the top view of GaS/GaSe single sheet crystal structure. **Figure 2**a,b show the typical low magnification and high-resolution transmission electron microscopy (TEM; HRTEM) images of thin GaS sheets deposited directly on Quantifoil TEM grid using the adhesive-tape micromechanical method. The as-measured lattice spacings from the HRTEM image for the thin GaS is 3.0 Å. Figure 2c shows the typical selected area electron diffraction (SAED) pattern indicating single crystalline GaS sheets orientated along <100> zone axis. Figure 2d,e depict the low-magnification and HRTEM images of GaSe layered

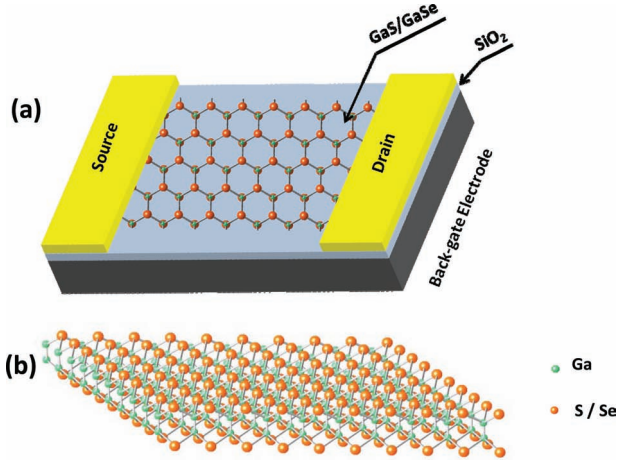

Figure 1. a) Schematic of bottom-gate FET device based on single-sheet of GaS and GaSe. b) Top view of GaS/GaSe crystal structure.

sheets deposited on Quantifoil TEM grid in a similar manner of GaS sheets. The lattice constant for GaSe measured from the HRTEM image is 3.2 Å. The SAED pattern for GaSe layered sheet shown in Figure 2f confirms the hexagonal structure of GaSe and the orientation of the sheets is along <100> zone axis.

Figure 3a shows the typical optical image of single-sheet of GaS deposited on 500 nm SiO_2/Si substrate and Figure 3b shows an optical image after patterning electrode on a GaS sheet using electron beam lithography. The room-temperature FET characteristics of single-sheet of GaS output characteristics (Figure 3c) and transfer characteristics (Figure 3d) carried out by applying a drain-source voltage V_{ds} to a pair of Ti/Au patterned electrodes and gate voltage V_{gs} to the back gate silicon substrate electrode. The back gating characteristics of the FET devices on a single sheet of GaS are typical of an n-type channel conductance. By applying the V_{gs} sweeps repeated on the GaS FET device we did not observe any significant variation, while keeping V_{ds} constant, which indicates the highly stable transistor device. In the inset of Figure 3d we show a typical scanning electron microscopy (SEM) image of the patterned electode on ultathin layer GaS sample.The field effect differential mobilities (μ) of the single-sheet GaS FET devices were calculated using the equation

$$\mu = g_m \left[\frac{L}{W C_i V_{ds}} \right] \quad (1)$$

where g_m is the transconductance that can be obtained from the slope of dI_{ds}/dV_{gs} of the drain-source current I_{ds} versus V_{gs} plot, L is the channel length (5 μm), W is the channel width (20 μm), and C_i (6.9×10^{-5} F cm^{-2}) is the gate capacitance between the channel and the silicon backgate per unit area, which is given by equation $C_i = \varepsilon_0 \varepsilon_r / d$, where ε_0 (3.9) and d (500 nm) are the dielectric constant and thickness of SiO_2, respectively. The typical field-effect differential mobility for GaS single sheet was calculated from two-contact measurement to be ≈0.1 cm^2 V^{-1} s^{-1}. We noted that this value of differential mobility represents lower limit because of the contact resistance of the metal/semiconductor interface. We also noted better contact resistance and ohmic behavior for the device with the Au contact electrode as compared to that of Ti/Au. The on/off current ratio (I_{on}/I_{off}) was determined by taking the ratio of maximum to minimum I_{ds} on the gate voltage axis of the V_{gs} vs I_{ds} plot and was found to be

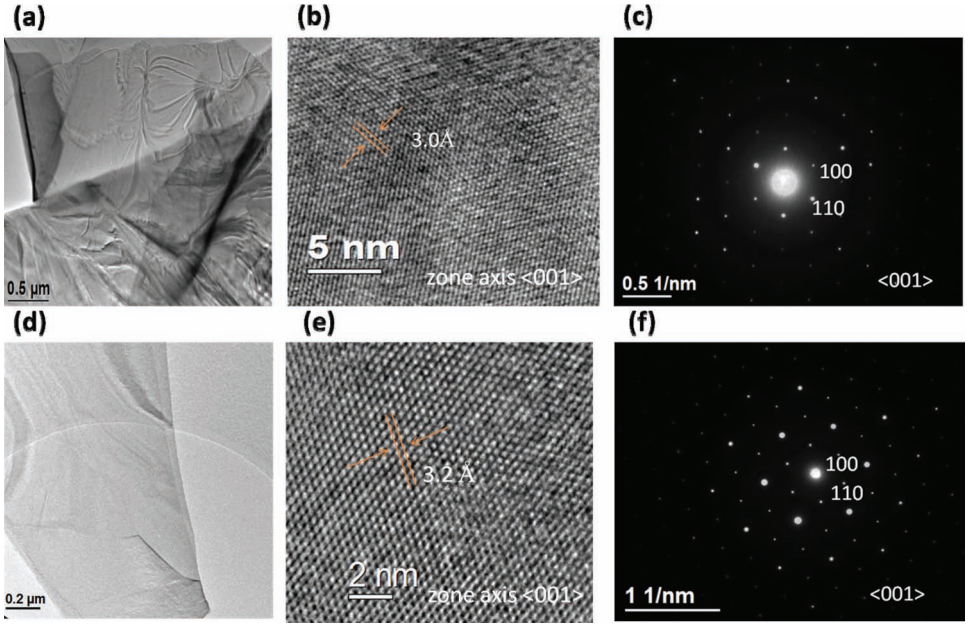

Figure 2. TEM images of few layer GaS sheet a) at low magnification and b) at high resolution. c) Corresponding SAED pattern. TEM images of a few layer GaSe sheet d) at low magnification and e) at high resolution. f) Corresponding SAED pattern.

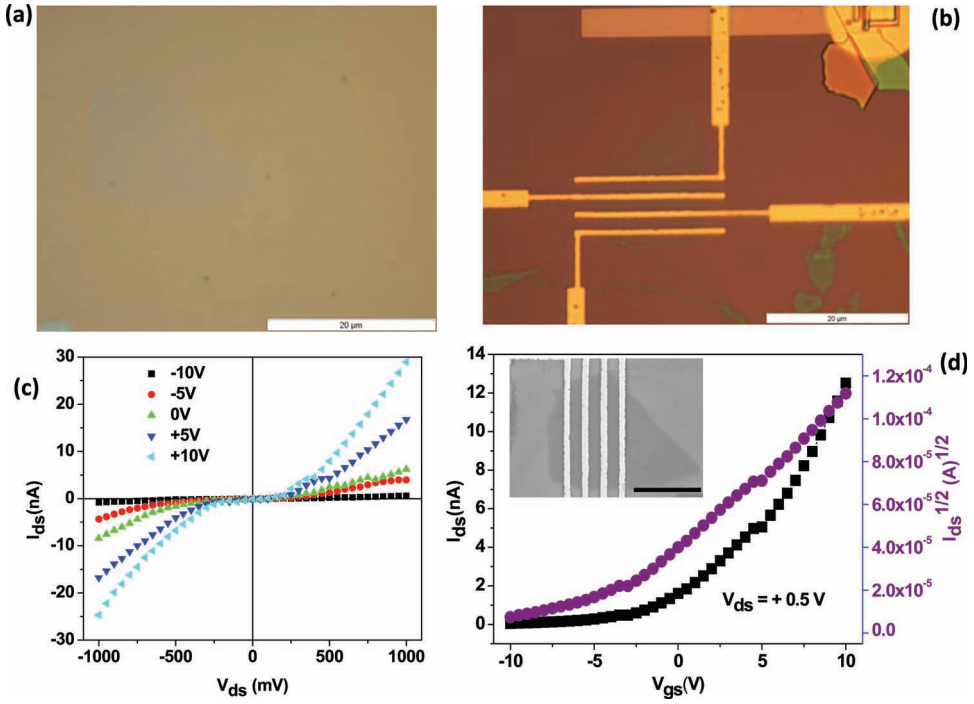

Figure 3. Single-sheet of GaS. a) Typical optical image before patterning and b) optical image after patterning electrodes. c) Gate dependent current–voltage (*I–V*)characteristics of a single-sheet of GaS at room temperature in dark at constant humidity of (22%). d) Transfer characteristics of GaS single-sheet-based FET. Inset of (d) shows an SEM image of the GaS transistor device with a 10 µm scale bar.

≈10^4. The subthreshold swing (SS) was defined as the voltage required to increase the source-to-drain current by a factor of 10 and was calculated by the following equation

$$SS = dV_{gs}/d(\log I_{ds}) \quad (2)$$

SS values were calculated by taking the maximum slope in the transfer curve expressed as a log scale for V_{gs} vs I_{ds}. High subthreshold swings are usually due to existence of surface trap states, leakage currents that are not exponentially dependent on V_{gs}, or incomplete gating effects in the transistor device. Furthermore, it is possible that the subthreshold swing can be improved by surface treatments on the SiO_2/Si gate insulator, including HF cleaning, plasma cleaning, hydrogenation, or annealing the transistor device in Ar + H_2. The ultrathin layer FET based on GaS sheet showed an SS of ≈2.1 V/decade.

Figure 4a shows an optical image of a single sheet of GaSe deposited on 500 nm SiO_2/Si substrate using the micromechanical cleavage technique. Figure 4b shows an optical image of electron-beam patterned electrodes on a GaSe single-sheet. Figure 4c shows the room temperature FET output characteristics of single-sheet of GaSe and Figure 4d shows transfer characteristics. The field-effect differential mobility was calculated for single-sheet of GaSe using Equation (1) and was observed to be 0.6 cm^2 V^{-1} s^{-1}. Additionally, the low conductivity observed in othe transistor devices may be due to adhesive-tape glue, which was stuck to single sheet, interupting the metal–sample contact and which may be responsible for increase in the resistance of the device. We also noted that the devices are sensitive to water absorption, which slowly changes the resistance of the devices. The ON/OFF ratio for the GaSe sheet was observed to be ≈10^5, an order of magnitude higher than that observed for the GaS sheet. Further, we have calculated the SS for GaSe single-sheet FET and it was observed to be ≈1.8 V/decade.

We observed that the calculated differential mobility of the ultrathin layer GaS and GaSe bottom-gate transistor device were ≈0.1 cm^2 V^{-1} s^{-1} and 0.6 cm^2 V^{-1} s^{-1}, respectively, which were equivalent to the previous results from the bottom-gate FET devices reported for single-layer MoS_2.[11] For top-gate single-layer MoS_2 transistor devices, the reported mobility is ≈200 cm^2 V^{-1} s^{-1}, which were obtained using the high-κ gate dielectric material HfO_2 as a top gate electrode on single-layer MoS_2.[11] It is well studied and well known that the trap/impurity states exist at the SiO_2/Si surface in the bottom-gate transistors, and the scattering from these charged impurities degrades the transistor device performance and finally the mobility of the device. Reduction of the surface traps/impurities in the bottom gate dielectric is expected to improve the mobility of GaS and GaSe single-sheet layer based bottom-gate transistor devices. Also it has been reported that the prolonged storage of GaSe sample in air forms a native oxide on surface, which affects the conductivity.[39] We have recently reported the origin of hysteresis in single-layer MoS_2 transistors and also demostarted the techniques to eliminate hysteresis with encapsulating silicon nitride layers.[40,41] **Table 1** summarizes the results

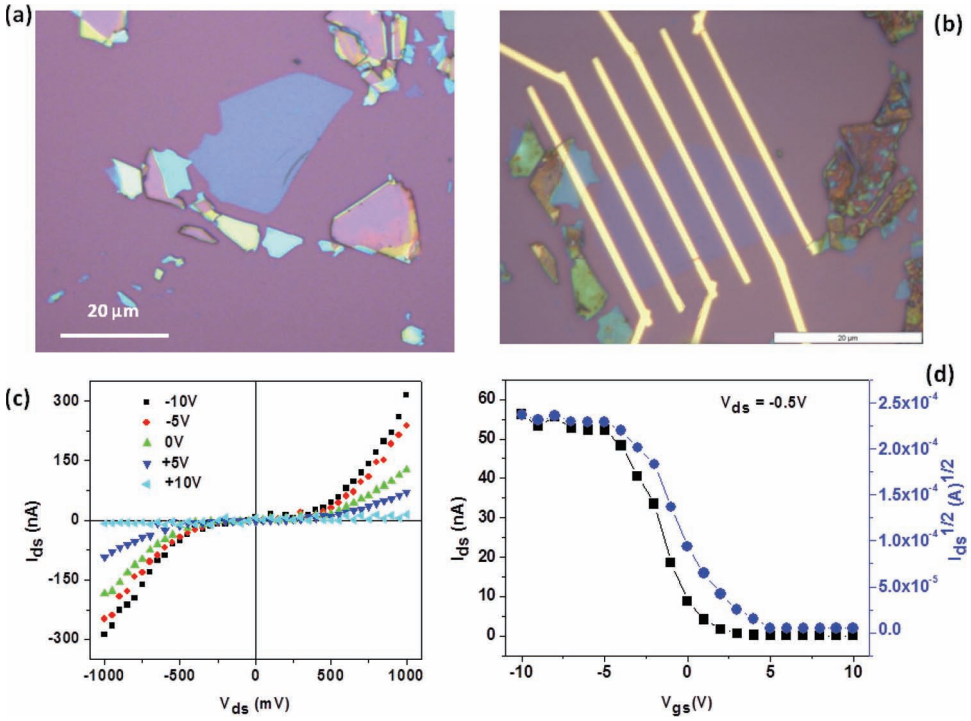

Figure 4. Single-sheet GaSe: a) Typical optical image before patterning electode and b) optical image after patterning electrode. c) Room-temperature FET output characteristics of single-sheet of GaSe in dark at constant humidity (22%) and d) transfer characteristics of a GaSe single sheet FET.

of transistor characteristics of ultrathin layer GaS and GaSe sheet. **Figure 5**a,b shows the *I–V* characteristics of single-sheet GaS and GaSe in dark and in presence of white light. The improvements in the mobility of GaS and GaSe devices were possible by using the high-κ dialectic material as the top gate electrode and with appropriate substrate engineering. It is extremely important to make a four-point probe electrode device or van-der-Pauw structure geometry device (see Supporting Information Figure S3, S5, S8) on these layered materials to perform Hall effect measurements. It may also be interesting to transfer these single sheet on self assembled nanodielectrics and study their FET performance. Extensive future theoretical work on single sheets of GaS and GaSe would be desirable, particularly calculations of scattering rates on phonon and charge impurities for detailed and complete understanding.

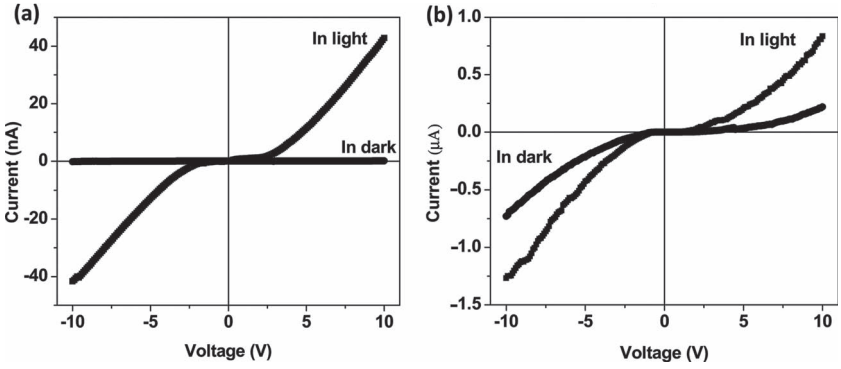

Figure 5. *I–V* characteristics in the dark and in the presence of white light illumination (0.7 mW cm^{-2}) for ultrathin layer sheets of a) GaS and b) GaSe.

In summary, our experimental results demonstrate the basic transport characteristics of single-sheet based transistor of GaS and GaSe fabricated using mechanically exfoliation from bulk crystal, which may offer more opportunities for potential applications as photodetectors, gas sensors, and optoelectronic devices due to the large bandgap in these layered materials, which is an essential property for potential applications. Also, the large area single sheet of GaS and GaSe can also be used as a transparent conductive support for studying biological molecules, nanoparticles, etc. using TEM. We have measured room-temperature bottom-gate geometry transistor characteristics based on single-sheets of GaS and GaSe, which show typical n-type and p-type conductance, respectively. Single-sheet of GaS and GaSe exhibit field-effect respective differential mobilities of ≈0.1 cm^2 V^{-1} s^{-1} and 0.6 cm^2 V^{-1} s^{-1} along with good ON/OFF current ratios in the range of ≈10^4–10^5. These results reveal

Table 1. Summary of GaS and GaSe single-sheet FETs.

FET Device	Conductance Type	ON/OFF Ratio	Mobility [cm^2 V^{-1} s^{-1}]
GaS single sheet	n-type	10^4	0.1
GaSe single sheet	p-type	10^5	0.6

basic transport characteristics and potential for optimization of layered GaS and GaSe as active elements in possible nanoelectronics devices.

Experimental Section:

Preparation of Ultrathin Layers of GaS and GaSe: Ultrathin layers of GaS and GaSe were deposited at room temperature under ambient conditions by mechanically exfoliating bulk GaS and GaSe materials onto degenerately doped silicon wafers with a thermal oxide of thickness of 500 nm. The materials were prepatterned with square markers (distance between each of two neighbor square marker was ≈1500 μm) using shadow mask in thermal evaporator with 1 nm Cr/50 nm Au. Substrates were then cleaned. After preparation of GaS and GaSe thin samples, the thinnest sheet were first identified by optical microscopy and were further characterized using AFM and Raman spectroscopy to confirm the number of layers. The exfoliated flakes had typical dimensions of tens of micrometers. Kokh et al. recently reported the simple method of syntheis of GaS and GaSe bulk crystals using a single-zone heating furnace.[42]

Optical Microscopy: An optical microscope was used to locate ultathin sheets of GaS and GaSe. The optical microscope images were acquired with an optical microscope (Nikon Eclipse ME600) imager M1m with white light illumination (100 W halogen lamp, HAL100) using bright field imaging modes and 100× objectives. In all cases, a Nikon Eclipse ME600 was used for recording the optical images using color view mode with a soft imaging system. For each filter, 100 frames were averaged to produce the final image. Exposure times varied in the range 10–1000 ms depending on the filter.

Ultrathin Layer GaS and GaSe FET Fabrication: After identifying single-sheet of GaS and GaSe, the small marker was fabricated using electron beam lithography near to single-sheet to identify these layer materials during further characterization and measurements process. Contacts were set up using electron beam lithography. For electron beam lithography, the samples were spin coated (4000 rpm for 45 s) first with MMA(8.5)MAA copolymer (8.5) (6% concentration in ethyl lactate), baked at 175 °C for 90 s then spin coated (4000 rpm for 45 s) with overlayer of polymethylmethacrylate (PMMA) (2% concentration in anisole) followed by baking at 175 °C for 90 s and then exposed using an electron beam lithography. Development of sample was done by dipping the sample in methyl isobutyl ketone:isopropyl alchohol (MIBK:IPA) 1:3 solution for 75 s, followed by an IPA rinse for 25 s and drying using a N_2 gun. Contact materials (Ti/Au, 3/70 nm thickness) were evaporated using an electron beam evaporation system followed by lift-off in acetone. For lift-off, devices were kept in acetone for 30 min at 45 °C followed by 5 s ultrasonication. For each, >10 devices were fabricated using single-sheets of GaS and GaSe. The silicon substrate coated 500 nm SiO_2 was used as the back gate. Ti/Au contact patterned devices were annealed before electrical transport measurements. The annealing processes were performed in a home-built furnace system, where the fabricated transistor device in the quartz tube could be quickly moved between a hot zone (center of the furnace) at 200 °C in $Ar + H_2$ for 2 h.

Electrical Characterization of FETs: Electrical characterization of FETs based on ultrathin layers of GaS and GaSe devices was performed by using a Keithley 4200 semiconductor characterization system with a shielded probe station with micromanipulator, optical microscope, and white light source. Leakage current was measured before measuring FET properties for the devices and leakage current swere observed to be below 10 pA.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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[41] In addition to adsorption of water on ultrathin layer sheets, the hysteresis in transistor devices can also be observed with use of polymer such as PMMA for initial marker on the SiO_2 substrate followed by deposition of ultra-thin sheets. It is difficult to remove PMMA completely from the SiO_2 substrate. Hysteresis arising due to this, can be resolve either direct deposition of single-sheets on clean SiO_2 substrates by micromechanical exfoliation technique using scotch-tape or use of shadow mask directly for making initial marker followed by mechanical exfoliation.
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