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Black phosphorus field-effect transistors

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Two-dimensional crystals have emerged as a class of materials that may impact future electronic technologies. Experimentally identifying and characterizing new functional two-dimensional materials is challenging, but also potentially rewarding. Here, we fabricate field-effect transistors based on few-layer black phosphorus crystals with thickness down to a few nanometres. Reliable transistor performance is achieved at room temperature in samples thinner than 7.5 nm, with drain current modulation on the order of 10^5 and well-developed current saturation in the *I–V* characteristics. The charge-carrier mobility is found to be thickness-dependent, with the highest values up to ~1,000 $cm^2 V^{-1} s^{-1}$ obtained for a thickness of ~10 nm. Our results demonstrate the potential of black phosphorus thin crystals as a new two-dimensional material for applications in nanoelectronic devices.

Black phosphorus is a layered material in which individual atomic layers are stacked together by van der Waals interactions, much like bulk graphite[1]. Inside a single layer, each phosphorus atom is covalently bonded with three adjacent phosphorus atoms to form a puckered honeycomb structure[2–4] (Fig. 1a). The three bonds take up all three valence electrons of phosphorus, so, unlike graphene[5,6], monolayer black phosphorus (termed 'phosphorene') is a semiconductor with a predicted direct bandgap of ~2 eV at the Γ point of the first Brillouin zone[7]. For few-layer phosphorene, interlayer interactions reduce the bandgap for each layer added, and eventually reach ~0.3 eV (refs 8–12) for bulk black phosphorus. The direct gap also moves to the Z point as a consequence[7,13]. Such a band structure provides a much needed gap for the field-effect transistor (FET) application of two-dimensional materials such as graphene, and the thickness-dependent direct bandgap may lead to potential applications in optoelectronics, especially in the infrared regime. In addition, observations of a phase transition from semiconductor to metal[14,15] and superconductor under high pressure[16,17] indicate correlated phenomena play an important role in black phosphorus under extreme conditions. We fabricated few-layer phosphorene devices and studied their electronic properties modulated by the electric field effect. Excellent transistor performances were achieved at room temperature. In particular, important metrics of our devices such as drain current modulation and mobility are either better or comparable to FETs based on other layered materials[18,19].

Few-layer phosphorene FET device fabrication

Bulk black phosphorus crystals were grown under high pressure and high temperature (see Methods). The band structure of the bulk black phosphorus was verified by angle-resolved photoemission spectroscopy (ARPES) measurements, as well as *ab initio* calculations. The filled bands of freshly cleaved bulk crystal measured by ARPES are shown in Fig. 1b, and largely agree with screened hybrid functional calculations with no material-dependent empirical parameters (Fig. 1b, dashed and solid lines for filled and empty bands, respectively). The calculated bandgap (~0.2 eV) also agrees reasonably well with previous measurements[8–11], taking into account that screened hybrid functional calculations tend to slightly underestimate the size of the bandgap in semiconductors[20–22].

We next fabricated few-layer phosphorene FETs with a backgate electrode (Fig. 2a). A scotch tape-based mechanical exfoliation method was used to peel thin flakes from bulk crystal onto degenerately doped silicon wafer covered with a layer of thermally grown silicon dioxide. Optical microscopy and atomic force microscopy (AFM) were used to find thin flake samples and determine their thickness (Fig. 2a). Metal contacts were then deposited on black phosphorus thin flakes by sequential electron-beam evaporation of chromium and gold (typically 5 nm and 60 nm, respectively) through a stencil mask aligned with the sample. A standard electron-beam lithography process and other contact metals such as titanium/gold were also used to fabricate few-layer phosphorene FETs, and similar results were obtained in terms of device performance.

FET characteristics of few-layer phosphorene devices

The switching behaviour of our few-layer phosphorene transistor at room temperature was characterized in vacuum (~1×10^{-5} mbar), in the configuration presented in Fig. 2a. We swept the backgate voltage V_g, applied to the degenerated doped silicon, with the source–drain bias V_{ds} across the black phosphorus conductive channel held at fixed values. The results obtained from a device with a 5-nm-thick channel on top of a 90 nm SiO_2 gate dielectric are shown in Fig. 2b. When the gate voltage was varied from −30 V to 0 V, the channel switched from the 'on' state to the 'off' state and a drop in drain current by a factor of ~10^5 was observed. The measured drain current modulation is four orders of magnitude larger than that in graphene (due to its lack of a bandgap) and approaches the value recently reported in MoS_2 devices[18]. Such a high drain current modulation makes black phosphorus thin film a promising material for applications in digital electronics[23]. Similar switching behaviour (with varying drain current modulation) is observed on all black phosphorous thin-film transistors with thicknesses up to 50 nm. We note that the on state current of our devices has not yet reached saturation due to the fact that the doping level is limited by the breakdown electric field of the SiO_2 backgate dielectric. It is therefore possible to achieve even higher drain current modulation by using high-*k* materials as gate

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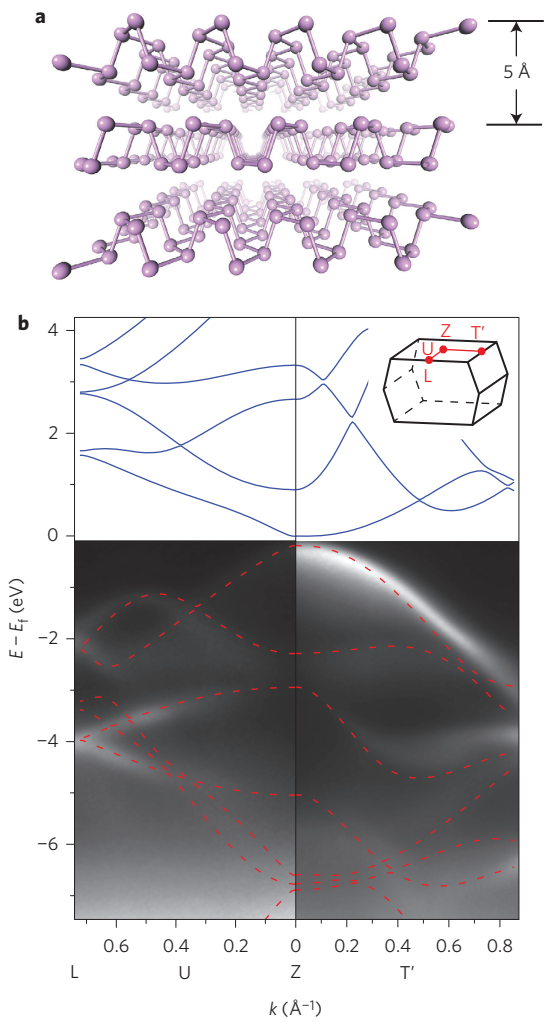

Figure 1 | Crystal and electronic structure of bulk black phosphorus. **a**, Atomic structure of black phosphorus. **b**, Band structure of bulk black phosphorus mapped out by ARPES measurements. A bandgap is clearly observed. Superimposed on top are calculated bands of the bulk crystal. Blue solid and red dashed lines denote empty and filled bands, respectively. The directions of the ARPES mapping are along U (L–Z) and T′, as indicated in the first Brillion zone shown in the inset. E_f is the Fermi energy.

dielectrics for higher doping. Meanwhile, a subthreshold swing of ~5 V per decade is observed, which is much larger than the subthreshold swing in commercial silicon-based devices (~70 mV per decade). We note that the subthreshold swing in our devices varies from sample to sample (from ~3.7 V per decade to ~13.3 V per decade) and is of the same order of magnitude as reported in multilayer MoS_2 devices with a similar backgate configuration[24,25]. The rather big subthreshold swing is mainly attributed to the large thickness of the SiO_2 backgate dielectric that we use, and multiple factors such as insulator layer thickness[26], the Schottky barrier at the subthreshold region[25] and sample–substrate interface state may also have an influence.

The switching off at the negative side of the V_g sweep is accompanied by a slight turn-on at positive gate voltages, as shown in Fig. 2b. To further explore this ambipolar behaviour, we fabricated few-layer phosphorene devices with multiple electrical contacts (Fig. 2c, inset) and performed Hall measurements using two opposing contacts (V_2 and V_4, for example) perpendicular to the drain–source current path to measure the transverse resistance R_{xy}. The Hall coefficient R_H, defined as the slope of R_{xy} as a function of external magnetic field B, reflects both the sign and density of the charge carriers in the sample. As shown in Fig. 2c, a carrier sign inversion is clearly observed in the on states, with positive and negative gate voltages corresponding to hole and electron conduction, respectively. This unambiguously shows that the ambipolar switching of the devices is caused by Fermi level shifting from the valence band into the conduction band.

The nature of the electrical conduction was probed further by performing I–V measurements in a two-terminal configuration (Fig. 2a). As shown in Fig. 2d, the source–drain current I_{ds} varies linearly with V_{ds} in the on state of the hole side, indicating an ohmic contact in this region. Meanwhile, I_{ds} versus V_{ds} is strongly nonlinear on the electron side (Fig. 2d, inset), as is typical for semiconducting channels with Schottky barriers at the contacts. The observed I–V characteristics can be readily explained by workfunction mismatch between the metal contacts and few-layer phosphorene; the high workfunction of the metal electrodes causes hole accumulation at the metal–semiconductor interface, which forms a low-resistance ohmic contact for the p-doped sample, while for the n-doped sample a depletion region is formed at the interface, leading to Schottky barriers and thus nonlinear conduction. This model also explains the observed disparity between conduction at the electron and hole sides in all our samples (Fig. 2b) and is widely accepted to describe the contact behaviour in MoS_2 devices[27].

For potential applications in digital and radiofrequency devices, saturation of the drain current is crucial in order to reach maximum possible operation speeds[23]. By carefully choosing the ratio between channel length and SiO_2 layer thickness, a well-defined current saturation can be achieved in the high drain–source bias region (Fig. 3a). Meanwhile, the electrical contacts remain ohmic in the linear region at low drain–source biases. The results shown in Fig. 3a were obtained in the on state of the hole side of the conduction in a 5 nm sample with a 4.5-μm-long channel on the 90 nm SiO_2 gate dielectric. Such a well-developed saturation behaviour, which is absent in graphene-based FET devices[23], is crucial for achieving high power gains. Coupled with the fact that our channel thickness is on the order of nanometres and thus robust against short-channel effects when the channel length is shrunk to the nanometre scale, our results suggest the high potential of black phosphorus in high-speed field-effect device applications. We note that the on state conductance of our device is relatively low and the threshold source–drain bias is relatively high compared to typical silicon-based devices. Both factors are attributed to the long channel length in our current device. Better device performance, that is, larger saturation current and lower threshold bias, is expected if the channel length and the gate oxide thickness are reduced. Further investigations are needed to test the limit of the device performances of black phosphorus FETs.

Charge transport mechanism in black phosphorus thin flake

We now turn to the characterization of field-effect mobility in few-layer phosphorene devices. Conductance G was measured as a function of V_g and we extracted the field-effect mobility μ_{FE} in the linear region of the transfer characteristics[28]:

$$\mu_{FE} = \frac{L}{W}\frac{1}{C_g}\frac{dG}{d(V_g - V_{th})} \quad (1)$$

where L and W are the length and width of the channel, respectively, C_g is the capacitance per unit area, and V_{th} is the threshold gate voltage. A hole mobility as high as 984 $cm^2\ V^{-1}\ s^{-1}$ is obtained on a 10 nm sample, as shown in Fig. 3b, and is found to be strongly thickness-dependent. Transfer characteristics of two other typical samples of different thicknesses (8 nm and 5 nm, with the 5 nm sample the same as measured in Fig. 3a) are also shown in Fig. 3b. The conductance was measured in a four-terminal

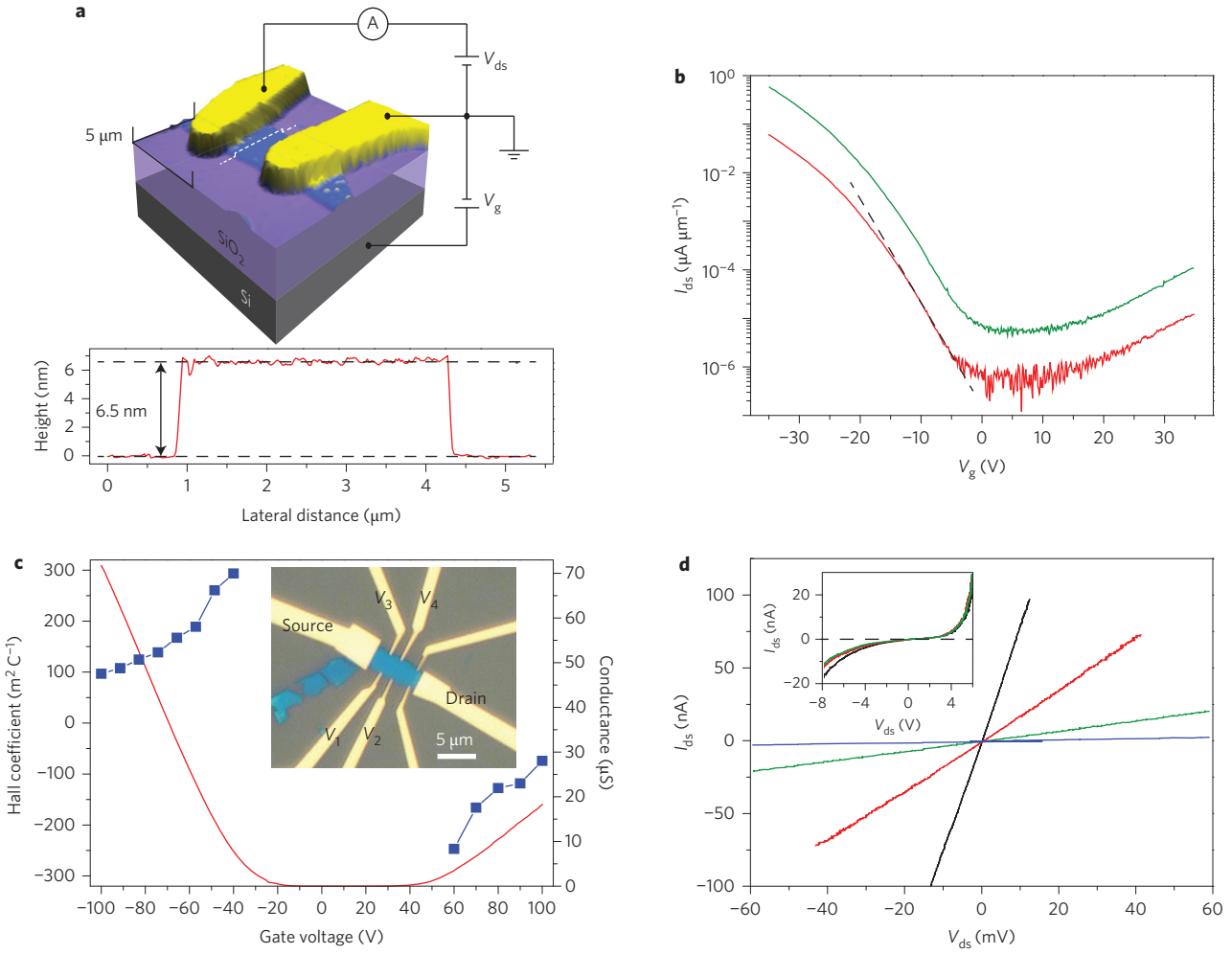

Figure 2 | Few-layer phosphorene FET and its device characteristics. a, Top: Schematic of device structure of a few-layer phosphorene FET. The device profile shown here is the three-dimensional rendering of the AFM data. Electrodes and a few-layer phosphorene crystal are false-coloured to match how they appear under the microscope. Bottom: Cross-section of device along the white dashed line in the schematic. **b**, Source–drain current (on a logarithmic scale) as a function of gate voltage obtained from a 5-nm-thick device on a silicon substrate with 90 nm SiO_2 at room temperature, with drain–source voltages of 10 mV (red curve) and 100 mV (green curve). Channel length and width of the device are 1.6 μm and 4.8 μm, respectively. Drain current modulation up to ~10^5 is observed for both drain–source biases on the hole side of the gate doping, with a subthreshold swing (the slope of the black dashed line) of 4.6 V per decade. A slight turn-on at the electron side is also observed. **c**, Hall coefficient (blue curve) and conductance (red curve) as a function of gate voltage collected from a 8-nm-thick sample on a silicon substrate with 285 nm SiO_2. Carrier type inversion, signified by the sign change of the Hall coefficient, is observed when the polarity of the gate is reversed. Inset: Optical image of a typical multi-terminal few-layer phosphorene device. **d**, *I*–*V* characteristics of the device in Fig. 2b. Linear behaviour is seen at $V_g = -30$ V, −25 V, −20 V and −15 V (black, red, green and blue curves, respectively), indicating ohmic contact on the hole side of the gate doping. Inset: Nonlinear behaviour on the electron side ($V_g = 30$ V, 25 V and 20 V; black, red and green curves, respectively) of the gate doping indicates the formation of a Schottky barrier at the contacts.

configuration to avoid complications from electrical contacts[25]. A two-terminal conductance measurement set-up was also used on some of our devices. This was found to overestimate hole mobility, but still yielded values of the same order of magnitude (Fig. 3b, inset). Such mobility values, although still much lower than in graphene[29–31], compare favorably with MoS_2 samples[18,19,25] and are already much higher than values found in typical silicon-based devices that are commercially available (~500 cm^2 V^{-1} s^{-1})[23].

The thickness dependence of the two key metrics of material performance—drain current modulation and mobility—was further explored to elucidate the transport mechanism of few-layer phosphorene FETs. The experimental results are summarized in the inset of Fig. 3b. The drain current modulation decreases monotonically as sample thickness is increased, while the mobility peaks at ~10 nm and decreases slightly above this. A similar thickness dependence of carrier mobility has been reported in other two-dimensional FETs such as few-layer graphene and MoS_2, where models taking into account the screening of the gate electric field were invoked to account for the observed behaviour[32,33]. Simply speaking, the gate electric field only induces free carriers in the bottom layers as a result of charge screening. So, the top layers still provide finite conduction in the off state, reducing the drain current modulation. The field-effect mobility is also dominated by the contribution from layers at the bottom. Thinner samples are more susceptible to charge impurities at the interface (thus their lower mobilities) that are otherwise screened by the induced charge in thicker samples. This explains the sharp increase in the field-effect mobility below ~10 nm. As the samples become thicker, however, another factor has to be taken into account—because the current is injected from electrical contacts on the top surface, the finite interlayer resistance forces the current to flow in the top layers, which are not gated by the backgate. This

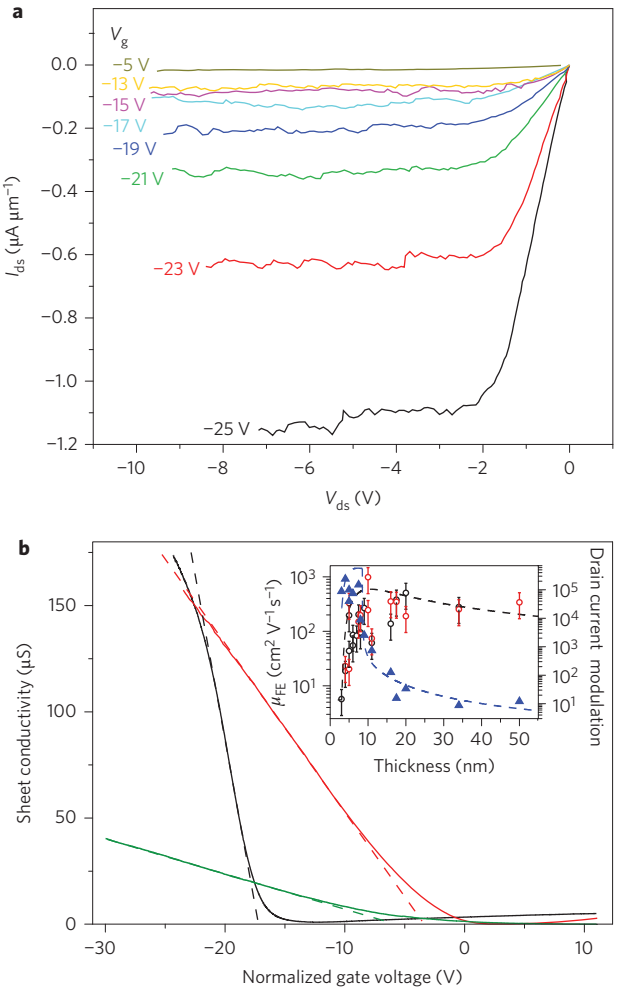

Figure 3 | Current saturation and mobility of a few-layer phosphorene FET. **a**, Drain–source current I_{ds} as a function of bias V_{ds} at different gate voltages collected from a 5-nm-thick device on a silicon substrate with 90 nm SiO_2. Channel length and width are 4.5 μm and 2.3 μm, respectively. A saturation region is observed for all applied gate voltages. **b**, Sheet conductivity measured as a function of gate voltage for devices with different thicknesses: 10 nm (black solid line), 8 nm (red solid line) and 5 nm (green solid line), with field-effect mobility values of 984, 197 and 55 cm^2 V^{-1} s^{-1}, respectively. Field-effect mobilities were extracted from the line fit of the linear region of the conductivity (dashed lines). The 5-nm-thick device is the same as measured in **a**. All gate voltages are normalized to 90 nm gate oxide for easy comparison. Inset: Summary of drain current modulation (filled blue triangles) and carrier mobility (open circles) of black phosphorus FETs of varying thicknesses. Mobilities measured in four-terminal and two-terminal configuration are denoted by black and red open circles, respectively. Error bars result from uncertainties in determining the carrier density, due to hysteresis of the conductance during gate sweep, and the irregular shape of our samples. The upper bound of the those uncertainties is used to estimate the error bars. Dashed lines indicate the models described in the main text.

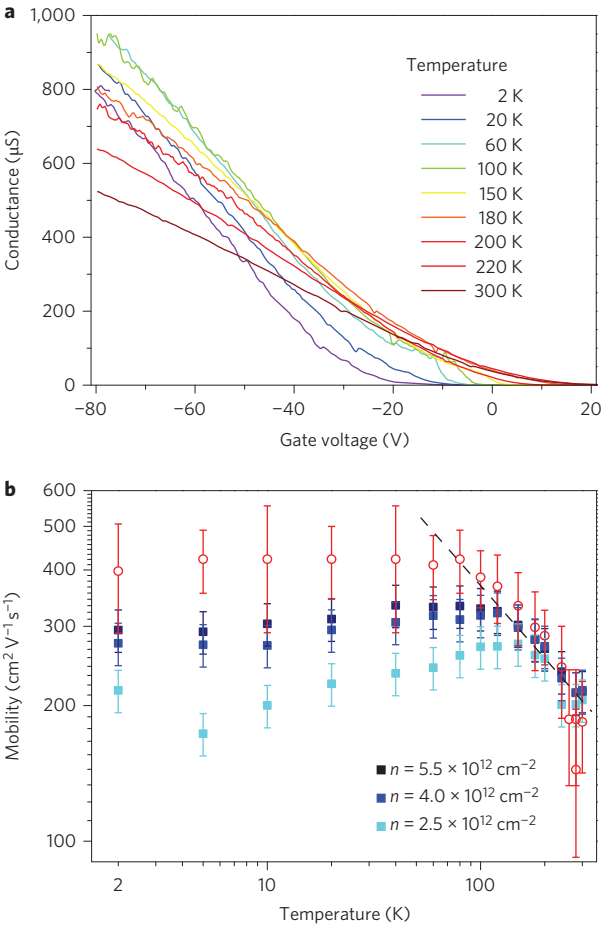

Figure 4 | Temperature-dependent behaviour of a few-layer phosphorene FET. **a**, Four-terminal conductance as a function of gate voltage measured in an 8-nm-thick sample at different temperatures. Channel length and width are 2.6 μm and 8.6 μm, respectively. **b**, Field-effect mobility (red open circles) and Hall mobility (filled squares, three different values of n) as a function of temperature on a logarithmic scale. Data are extracted from the same sample as in **a**. Error bars for field-effect mobility are defined the same way as in Fig. 3b inset. Error bars for Hall mobility represent the uncertainties coming from irregular shape of the sample. A power-law dependence $\mu \approx T^{-0.5}$ (black dashed line) is plotted in the high-temperature region as a guide to the eye.

effect depresses the field-effect mobility for samples thicker than ~10 nm. Based on the above arguments, we modelled the electrical conduction in our samples using a self-consistently obtained carrier distribution (for more details see Supplementary Section 7), and our calculation fits well with the experimental data shown in the inset of Fig. 3b. The model also suggests a way to achieve higher mobility without sacrificing drain current modulation. By using a topgate device structure with a layer of high-k dielectric material as the gate dielectric, one could effectively screen the charge impurities, but leave the drain current modulation intact. In addition, because the top layers where the current flows are now gated by the topgate, the mobility is no longer affected by the interlayer resistance. Such a method has been proven to work in MoS_2 FETs[18,19].

Finally, we examined the temperature dependence of the carrier mobility to uncover various factors that limit the mobility in our FETs. Two types of carrier mobility were measured in the same device, for comparison: the μ_{FE} extracted from the linear part of the gate-dependent conductance (Fig. 4a) according to equation (1), and the Hall mobility μ_H obtained from

$$\mu_H = \frac{L}{W}\frac{G}{ne} \quad (2)$$

where e is the charge of an electron and n is the two-dimensional charge density determined from gate capacitance, $n = C_g(V_g - V_{th})$, which is equal to the density extracted from Hall measurement

$n = 1/eR_H$ if the sample geometry permits an accurate determination of Hall coefficient R_H (Supplementary Fig. 7). The two mobilities in an 8-nm-thick sample as a function of temperature are shown in Fig. 4b. They fall in the vicinity of each other and show a similar trend as the temperature is varied: both decrease at temperatures higher than ~100 K, and saturate (or decrease slightly for low carrier densities) at lower temperatures. The behaviour of the mobility as the temperature is lowered to 2 K is consistent with scattering from charged impurities[32]. We note that in this temperature range the Hall mobility increases as the gate-induced carrier density becomes larger (Fig. 4b). The reduced scattering in the sample points to the diminished disorder potential as a result of screening by free charge carriers. This further corroborates our model in which the charged impurity at the sample/substrate interface is a limiting factor for carrier mobility. On the other hand, the drop in mobility from ~100 K up to 300 K can be attributed to the electron–phonon scattering that dominates at high temperatures[32], and the temperature dependence roughly follows the power law $\mu \propto T^{-\gamma}$, as seen in Fig. 4b. The exponent γ depends on electron–phonon coupling in the sample, and is found to be close to ~0.5 in our 8-nm-thick device (as a guide to the eye, $\mu \sim T^{-0.5}$ is plotted in Fig. 4b as a dashed line). This γ value for few-layer phosphorene is notably smaller than values in other two-dimensional materials[33] and bulk black phosphorus[11], but agrees with that in monolayer MoS_2 covered by a layer of high-k dielectric[19]. The exact mechanism of the suppression of phonon scattering in few-layer phosphorene is not clear at this moment and warrants further study.

Conclusion

We have succeeded in fabricating p-type FETs based on few-layer phosphorene. Our samples exhibit ambipolar behaviour with drain current modulation up to ~10^5, and a field-effect mobility value up to ~1,000 $cm^2\ V^{-1}\ s^{-1}$ at room temperature. The carrier mobility is limited by charge impurity scattering at low temperatures and electron–phonon scattering at high temperatures. The 'on' current is low and subthreshold swing is high, but optimization of the gate dielectric should improve these characteristics. The ability to fabricate transistors, combined with the fact that few-layer phosphorene has a direct bandgap in the infrared regime, makes black phosphorus a candidate for future nanoelectronic and optoelectronic applications.

Methods

Sample growth. Black phosphorus was synthesized under a constant pressure of 10 kbar by heating red phosphorus to 1,000 °C and slowly cooling to 600 °C at a cooling rate of 100 °C per hour. Red phosphorus was purchased from Aladdin Industrial Corporation with 99.999% metals basis. The high-pressure environment was provided by a cubic-anvil-type apparatus (Riken CAP-07). X-ray diffraction (XRD) was performed on a Smartlab-9 diffractometer (Rikagu) using Cu Kα radiation (Supplementary Fig. 1).

Measurements. ARPES measurements were performed at BaDElPh beamline at the Elettra synchrotron radiation facility with a Specs Phoibos 150 electron analyser.[34] The overall energy resolution was set to 20 meV or better and the typical angular resolution was 0.5°. During measurements the temperature was kept at 60 K to avoid the onset of charging. The data shown in Fig. 1b were taken with s-polarized 20 eV photons; no obvious polarization dependence was seen, but a noticeable intensity variation was observed for observed bands.

Transport measurements were mainly performed in an Oxford Instruments Optistat AC-V12 cryostat with samples in vacuum (~1×10^{-5} mbar), with some measurements carried out in an Oxford Instruments Integra a.c. cryostat and Quantum Design Physical Property Measurement System (PPMS) when a magnetic field was required. Data were collected in a d.c. set-up using a DL 1211 current preamplifier with a voltage source, or a Keithley 6220 current source combined with a Keithley 2182 nanovoltmeter. Some Hall measurements were carried out using an SRS 830 lock-in amplifier.

Band structure calculation. Our *ab initio* band structure calculations, based on density functional theory, were performed using the projector augmented wave method[35,36], as implemented in the Vienna *ab initio* Simulation Package (VASP) code[37]. The crystal structure data of black phosphorus were taken from refs 2 and 7. For the exchange-correlation energy, we used the screened hybrid density functional of the Heyd–Scuseria–Ernzerhof type (HSE06)[38]. Details of the calculation are provided in Supplementary Section 5.

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Author contributions

X.H.C. and Y.Z. conceived the project. G.J.Y. and X.H.C. grew bulk black phosphorus crystal. L.L. fabricated black phosphorus thin-film devices and performed electric measurements, and L.L., Y.Y. and Y.Z. analysed the data. Q.G. and D.F. carried out ARPES measurements on bulk black phosphorus crystal. X.O. and H.W. performed *ab initio* band structure calculations. L.L. and Y.Z. wrote the paper and all authors commented on it.

Additional information

Supplementary information is available in the online version of the paper. Reprints and permissions information is available online at www.nature.com/reprints. Correspondence and requests for materials should be addressed to X.H.C. and Y.Z.

Competing financial interests

The authors declare no competing financial interests.