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Multilevel Ultrafast Flexible Nanoscale Nonvolatile Hybrid Graphene Oxide–Titanium Oxide Memories

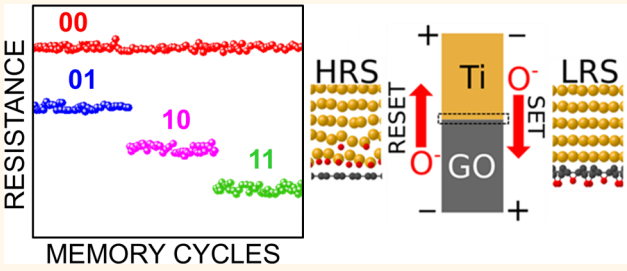
V. Karthik Nagareddy,[†] Matthew D. Barnes,[†] Federico Zipoli,[§] Khue T. Lai,[†] Arseny M. Alexeev,[†] Monica Felicia Craciun,[†] and C. David Wright*[,†]

[†]Centre for Graphene Science, College of Engineering, Mathematics and Physical Sciences, University of Exeter, Harrison Building, North Park Road, Exeter EX4 4QF, U.K.

[§]IBM Research–Zurich, Säumerstrasse 4, 8803 Rüschlikon, Switzerland

Supporting Information

ABSTRACT: **Graphene oxide (GO) resistive memories offer the promise of low-cost environmentally sustainable fabrication, high mechanical flexibility and high optical transparency, making them ideally suited to future flexible and transparent electronics applications. However, the dimensional and temporal scalability of GO memories, *i.e.*, how small they can be made and how fast they can be switched, is an area that has received scant attention. Moreover, a plethora of GO resistive switching characteristics and mechanisms has been reported in the literature, sometimes leading to a confusing and conflicting picture. Consequently, the potential for graphene oxide to deliver high-performance memories operating on nanometer length and nanosecond time scales is currently unknown. Here we address such shortcomings, presenting not only the smallest (50 nm), fastest (sub-5 ns), thinnest (8 nm) GO-based memory devices produced to date, but also demonstrate that our approach provides easily accessible multilevel (4-level, 2-bit per cell) storage capabilities along with excellent endurance and retention performance—all on both rigid and flexible substrates. *Via* comprehensive experimental characterizations backed-up by detailed atomistic simulations, we also show that the resistive switching mechanism in our Pt/GO/Ti/Pt devices is driven by redox reactions in the interfacial region between the top (Ti) electrode and the GO layer.**



KEYWORDS: *graphene oxide, titanium oxide, resistive switching, nonvolatile memory, multilevel memory, flexible memory*

Silicon-based "flash" memory devices are the most prominent and successful nonvolatile memory because of their high storage density and low fabrication costs.[1] However, flash memories, which rely on charge storage for their operation, suffer from a slow programming speed, poor endurance and relatively high operating voltages.[1,2] In addition, their continuous miniaturization (to increase the storage density) is expected soon to reach its fundamental scaling limit due to the difficulty in retaining charge (electrons) in shrinking dimensions.[2]

As an alternative to the conventional silicon-based approach, resistive-switching nonvolatile memory (RRAM or resistive-switching random access memory) devices offer many attractions including a simple two-terminal device configuration, fast operation speed, high endurance, excellent scalability and low-power consumption.[3−5] The basic operating principle of RRAMs is simple, the device is electrically switched between a high-resistance (HRS or RESET) state and a low-resistance (LRS or SET) state by applying appropriate programming voltages; readout is carried out nondestructively at a low voltage. Intermediate resistance states can also be accessed, giving rise to additional functionalities such as multibit storage, logic and arithmetic and neuromorphic (brain-like) processing.[6−10]

To date, a wide range of materials have been found to show resistive switching, the most common being transition-metal-oxides[11−18] (*e.g.*, TiO_2, CuO, NiO, TaO_x, VO_2, HfO_2 *etc.*), perovskite oxides[15,19] (*e.g.*, $Pr_{0.7}Ca_{0.3}MnO_3$, $SrTiO_3$ *etc.*) and chalcogenide phase-change alloys[9,10,20] (*e.g.*, $Ge_2Sb_2Te_5$). Various carbon materials have also shown to exhibit resistive switching properties, including amorphous carbons,[21,22] oxygenated amorphous carbon[23] and graphene oxide.[24,25]

Among these RRAM materials, graphene oxide (GO) is generating considerable scientific and commercial interest due

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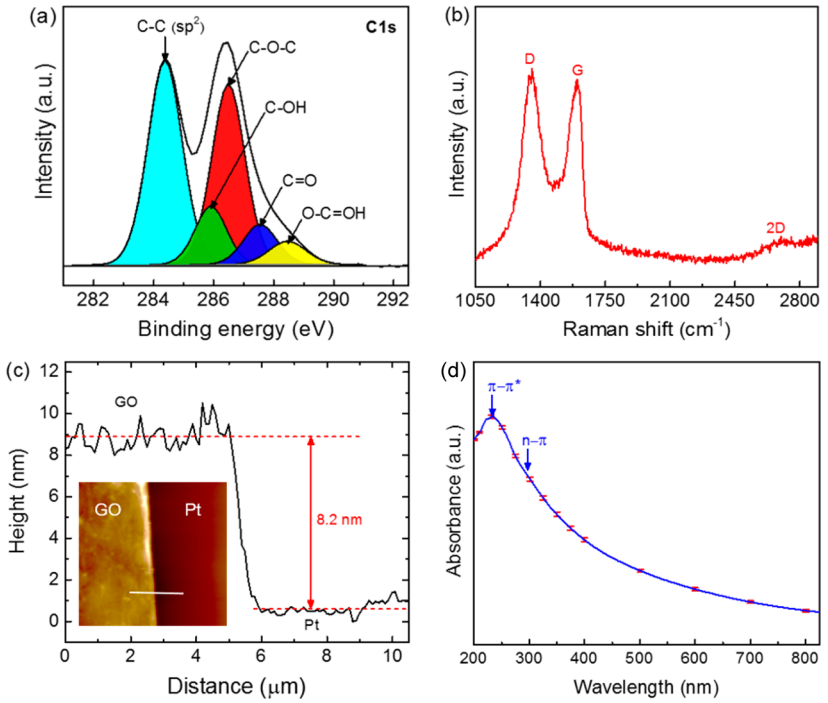

Figure 1. (a) High resolution deconvoluted XPS C1s spectrum of a 20 nm thick GO film showing five major components at 284.4, 285.8, 286.4, 287.7, and 288.5 eV, corresponding to C−C (sp^2) bonding, C−OH (hydroxyls), C−O−C (epoxides), C═O (carbonyls) and O—C═OH (carboxyl) bonds, respectively (b) Raman spectrum of an 8 nm thick GO film (c) AFM surface topography (inset) and line profile measurement and (d) Average absorbance spectrum of 8 nm GO film taken from three regions.

to its potential for low cost fabrication, environmentally sustainable manufacturability and, perhaps most importantly, its high mechanical flexibility and high optical transparency, all of which make it well-suited to future flexible and transparent electronics applications.[24,26−29] However, it is not an overstatement to say that previous studies of GO memory devices have reported a range of often conflicting findings. For example, bipolar resistive switching was observed by some authors in an Au/GO/Pt structure,[30] but not by others.[31,32] Likewise, in some studies an Al/GO/Al stack showed excellent memory characteristics on both flexible and rigid substrates;[24,33] while in other studies no switching was observed for the same structure.[32,34] Discrepancies were also reported for other electrode combinations such as, Ag/GO/ITO,[35,36] Al/GO/Pt,[31,32] Cu/GO/Pt,[30,37] Au/GO/ITO,[32,38] Al/GO/ITO.[31,39]

Unsurprisingly, in light of the varying switching characteristics observed in GO-based memories, a wide range of possible switching mechanisms have been put forward. Some works consider the switching behavior to be related to a bulk effect, meaning a structural modification of the entire GO layer.[28,37,40] Other works, however, associate the switching with interface dominated phenomena. For example, in the Al/GO/Al structure, Jeong *et al.*[24] and Kim *et al.*[33] explained switching in terms of the presence of an AlO_x interfacial layer between the top (Al) electrode and the GO film and in which switching events were caused by the formation and de-formation of Al metallic nanofilaments. However, Hong *et al.*[31] argued that the dominant switching mechanism in the Al/GO/Al structure is due to oxygen-ion migration within the GO layer. Similarly, Khurana *et al.*[41,42] confirmed that the presence of an Al top electrode leads to the formation of an interfacial oxide layer, but argued that this induces oxygen vacancies in the GO film, leading to conducting filament formation through oxygen-ion migration. He *et al.*,[37] on the other hand, proposed desorption/readsorption of oxygen groups from the GO, as well as diffusion of the top metal electrode to explain resistive switching. Wang *et al.*[39] proposed yet another mechanism, based on voltage controlled modulation of the oxygen diffusion barrier height at a Al/GO interface. By employing different top electrodes such as Au, Ti, Cu and Al on a GO/Pt structure, Zhuge *et al.*[30] argued that the reversible switching observed in these devices is predominantly due to the formation and rupture of conductive metallic filaments, irrespective of the electrode type (*i.e.*, reactive or nonreactive). Yet again, and contrary to all these above proposed switching models, Porro *et al.*[36] reported another mechanism as being responsible for switching in a Ag/GO/ITO structure, namely the diffusion of carbon atoms from GO in to the top electrode.

Turning to the dimensional and temporal scalability of GO memories (*i.e.*, how small they can be made and how fast they can be switched), this is an area that has received relatively little attention to date. Indeed, previous studies have invariably concentrated on large-scale devices (tens of micrometers in size) consisting of relatively thick (several tens of nanometers) GO films, typically fabricated using a shadow mask approach.[24,28,30−33,36,37,39,41] Similarly, most studies have reported only on switching in the microsecond or tens-of-microsecond time scales.[39] Consequently, the potential for using graphene oxide to deliver high-performance memories operating on nanometer length and nanosecond time scales is currently unknown.

In summary, in spite of the not inconsiderable number of reports in the literature of studies of GO memories, we have at the present time no clear idea of the performance limits of GO-based devices, nor indeed have we a definitive view of the precise nature of their switching mechanism(s). This is in part due to the plethora of GO device configurations and electrode materials that have been examined to date, which has perhaps

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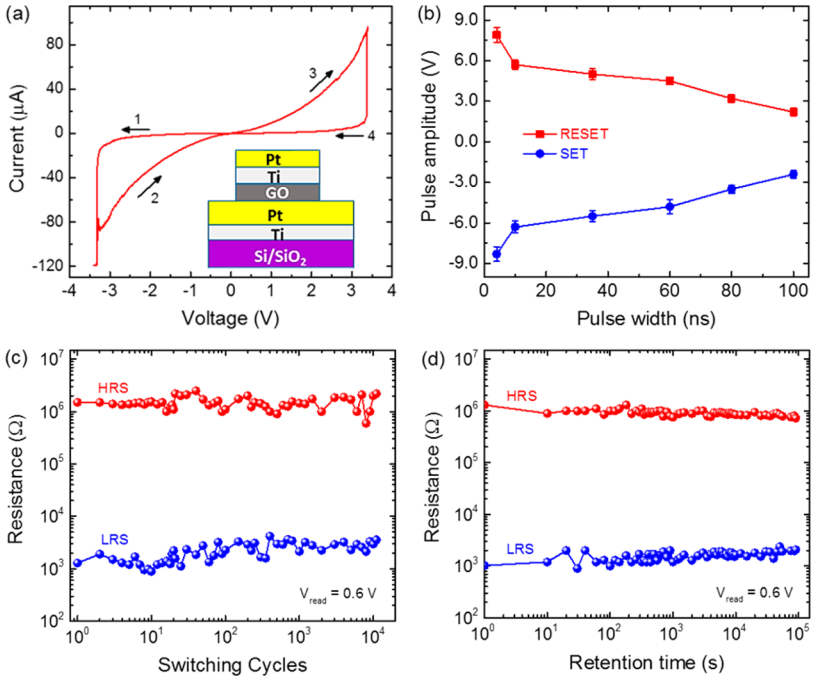

Figure 2. (a) *I*–*V* switching characteristic for a nanoscale GO memory cell (here of 100 nm diameter and with a 20 nm thick GO layer). Inset shows the schematic of fabricated memory cells. (b) Results of switching speed measurements showing pulse amplitudes and durations necessary for successful SET and RESET switching (here for 75 nm diameter cell with 8 nm thick GO layer). (c) Endurance and (d) retention performance of the nanoscale GO memory (again, here for a 75 nm diameter cell with 8 nm thick GO layer).

led to a rather incomplete picture of the potential of GO-based memories. In this work, therefore, we address these shortcomings and present not only the smallest (50 nm), fastest (sub-5 ns), thinnest (8 nm) GO memories produced to date, but also demonstrate that our approach provides easily accessible multilevel (4-level, 2-bit per cell) storage capabilities along with excellent endurance, retention and mechanical flexibility properties. Such performance attributes are, to our knowledge, the best ever reported for GO resistive-switching memories and fairly competitive even when compared to those of other emerging memory technologies such as phase-change, amorphous carbon and resistive-oxide memories.[2−4,11,23] Furthermore, our devices require no preconditioning, or so-called "forming" (a process which is invariably high-voltage/high-power) in order to initiate the reversible switching mode. Finally, *via* comprehensive experimental characterizations backed-up by detailed atomistic simulations, we show that the resistive switching mechanism in our GO devices is driven by redox reactions in the interfacial region between the top (Ti) electrode and the GO layer itself. Our work demonstrates that suitably designed and fabricated GO-based memories have the potential to extend to the demanding applications space of nanoscale, ultrahigh density, ultrafast, multilevel memories, in addition to the more often targeted flexible memories arena.

RESULTS AND DISCUSSION

GO Film Characterization. Large area uniform GO films were prepared by a vacuum filtration approach (see methods) using commercially available GO aqueous dispersions. Unlike conventional GO deposition techniques such as spin-coating,[27,43] drop-casting[44] or dip-coating methods,[45,46] the vacuum filtration approach[47] provides precise control of layer thickness, so enabling the fabrication of ultrathin GO films while maintaining excellent film uniformity and a very low surface roughness. It is also a fast process, shows very high reproducibility and is suitable for wafer-scale GO film deposition and even roll-to-roll manufacturing processes, making it highly attractive for industrial production.[48]

X-ray photoelectron spectroscopy (XPS) measurements were performed to analyze the surface chemical composition of as-prepared GO films. Figure 1a shows the deconvolution of high-resolution XPS C1s spectrum of a 20 nm thick GO film, revealing five major components at 284.4, 285.8, 286.4, 287.7, and 288.5 eV, corresponding to C−C (sp^2) bonding, C−OH, (hydroxyls), C−O−C (epoxides), C═O (carbonyls) and O—C═OH (carboxyl) bonds, respectively.[49] Among the functional groups, C−O−C groups were found to be the major species with ∼47% of the total oxygen concentration, whereas, C−OH, C═O and O—C═OH groups account for ∼6.4%, ∼3.5% and ∼9%, respectively. These results are consistent with the expected chemical composition for typical GO films prepared using wet chemical approach.[49,50]

The structural characteristics of the GO films were characterized by Raman spectroscopy;[50] the acquired spectrum (Figure 1b) showed intense D and G peaks at ∼1360 cm^{-1} and ∼1600 cm^{-1} and a weak 2D peak at ∼2700 cm^{-1}. The D peak in GO originates from structural imperfections created by the attachment of oxygen functional groups and the presence of flake edge sites. The I_D/I_G ratio was calculated as 1.06, a typical value for GO films.[50,51]

The ability of the vacuum filtration method to deliver precisely controlled, ultrathin and ultrasmooth GO films is demonstrated in Figure 1c, where we show the surface topography (inset) and corresponding line profile measurements of an 8 nm thick GO film transferred onto a Pt electrode (on a Si/SiO_2 substrate). We chose Pt as the bottom electrode because, in addition to its nonreactive nature and excellent electrical properties, it has been reported that GO films on Pt

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show very low surface roughness.[31] Indeed, the average root-mean-square (rms) roughness of our GO films deposited onto Pt was very low when compared to GO films reported to date,[24,31,32,34,35,52,53] the film in Figure 1c having an rms roughness of only 1.3 nm, along with excellent uniformity.

The optical properties of our GO films were also analyzed, using UV−vis spectroscopy. Since the absorbance/transmittance of the GO film is proportional to the thickness, any significant variation in film thickness or uniformity across the sample can be easily seen in the corresponding absorbance/transmittance spectra. Figure 1d shows the mean absorbance of an 8 nm thick GO film with a strong peak at ∼230 nm and a weak shoulder peak at ∼300 nm related to the $\pi-\pi^*$ transition of C═C bonds and the $n-\pi^*$ transition of C═O bonds, respectively.[54] The observed deviation in absorbance across the measured area (of 150 × 50 μm^2) was around 2%, confirming the excellent uniformity of our GO films.

Memory Devices. As pointed out in the introduction, previously reported studies of GO-based memories have invariably focused on relatively large device sizes in the tens of micrometer size range. Here, however, we successfully fabricated GO memory cells down to the tens of nanometer size scale. More specifically we fabricated vertical GO memory cells having diameters ranging from 300 μm right down to 50 nm. Devices were fabricated on both Si/SiO_2 and PEN (polyethylene naphthalate) plastic substrates using standard e-beam lithography and laser lithography techniques (see Methods). The lithography process starts by sputter coating blanket Ti(8 nm)/Pt(40 nm) metal films, followed by deposition of blanket GO films on top of the Pt layer. The final memory cell structure is realized by depositing a Ti(8 nm)/ Pt(15 nm) top metal layer, followed by lithographic patterning and reactive ion etching to create vertical GO devices having the structure substrate/Ti/Pt/GO/Ti/Pt, as shown schematically in Figure 2a (inset). Note that Ti layer in our devices plays a dual role; it acts as an adhesion layer for the Pt contacts but is also thick enough (at 8 nm) to ensure that it provides the primary top electrical contact with the GO surface. Thus, from an operational perspective our devices have an asymmetric electrode configuration, with Pt acting as the bottom electrode and Ti the top (the top Pt layer mainly serving as a capping layer for Ti to prevent it from oxidation, ensuring good electrical contact).

Electrical Measurements. The current−voltage ($I-V$) characteristics of the Pt/GO/Ti/Pt memory cells were studied by DC voltage sweep measurements to evaluate the basic resistive switching process of the fabricated devices. The bias voltage was applied to the top electrode and the bottom electrode was grounded. Figure 2a shows a typical $I-V$ characteristic, here for a 100 nm diameter cell with a 20 nm thick GO layer (and on a Si/SiO_2 substrate). The initial, pristine state of the GO cell was the high resistance (HRS or RESET) state. By sweeping the voltage from 0 V to −3.5 V, the device can be seen to switch to a low resistance (LRS or SET) state at about −3.2 V. Sweeping the voltage in the opposite direction results in a switch back to the HRS state at around +3.3 V. Thus, in common with other types of GO memories (and indeed metal-oxide based resistive memories), our devices demonstrate a bipolar, reversible resistive switching mechanism. However, in contrast to many previously reported studies,[30,32,46,55,28,56] our devices do not need any preconditioning *via* a so-called "forming" process in order to operate. This is a significant advantage since the forming process often requires high voltages and powers. (For additional electrical measurement data see Supporting Information Figure S1 and Figure S2 and associated text).

Furthermore, we note that the pristine state in our devices is always the HRS state, and that, under "normal" operating conditions (*i.e.*, for moderate voltages), switching from the pristine to the LRS state can only be achieved if the top electrode is negative with respect to the bottom electrode. Moreover, we found that the electrical transport in both the high and low resistance states corresponds well to a Schottky-emission dominated process (linear in $\ln(I)$ *vs* $V^{1/2}$), and that the resistance of our devices in both states scaled with area (see Supporting Information Figure S3). We also found that we could not achieve any reversible switching if the top Ti layer was missing (*i.e.*, for devices of the form Pt/GO/Pt, see Supporting Information Figure S7). All of these observations point toward a switching mechanism driven in our devices by electrochemical redox (reduction−oxidation) reactions occurring at the top (Ti) electrode/GO interface (as we later confirm).

We now turn our attention to pulsed electrical switching. A key criterion for any new nonvolatile memory technology is the programming (or write and erase) speed, in our case how fast the device can be switched between the SET and RESET states. This was evaluated by applying pulsed excitations of varying durations and amplitudes. Typical results are shown in Figure 2b, in this case for a 75 nm diameter device with an 8 nm thick GO layer. It can be seen that reliable switching between the SET and RESET states can be achieved for pulse durations as short as 4 ns, albeit at the expense of higher pulse amplitudes (*cf.* longer pulses). This is the fastest ever switching, to our knowledge, reported for GO resistive-switching memories and is comparable, or better, than that of other emerging memory technologies such as phase-change, amorphous carbon and resistive-oxide memories, confirming that our devices are well suited to high-speed, high-performance memory applications.[2−4,11,23] The fast switching speeds we observe are, we believe, related to the rate-limiting process in the switching of our devices, which is the diffusion of oxygen ions under the influence of electrical bias. Since the oxygen ions are moving very short distances (from voids in the GO film to the TiO_x layer and back—see later sections on switching mechanism), and since the films themselves and the interface region in particular are thin such that even relatively small voltages lead to high electric fields, we can expect fast switching.

Another key performance criterion for rewritable memories is the endurance, or the number of times the device can be switched between states. In order to investigate the endurance of our memory cells, cyclic pulsed switching measurements were performed. Specimen results are shown in Figure 2c, where +2.1/−2.5 V pulses of 100 ns duration were used to repeatedly switch a 75 nm diameter, 8 nm thick GO cell between the SET and RESET states. Over 10 000 switching cycles were successfully achieved, along with a large resistance-window of around 10^3 Ω. Note that the devices did not fail after 10 000 cycles, it is simply that measurements were stopped at that point. We note that an endurance of 10 000 cycles is already comparable or superior to that achieved in many existing or emerging memories (*e.g.*, current CMOS NAND-Flash devices have an endurance of typically 1000 cycles[1]).

Finally, in this section, we consider the retention performance of our GO memories. As shown in Figure 2d, we found that at room temperature the stable retention of both the LRS

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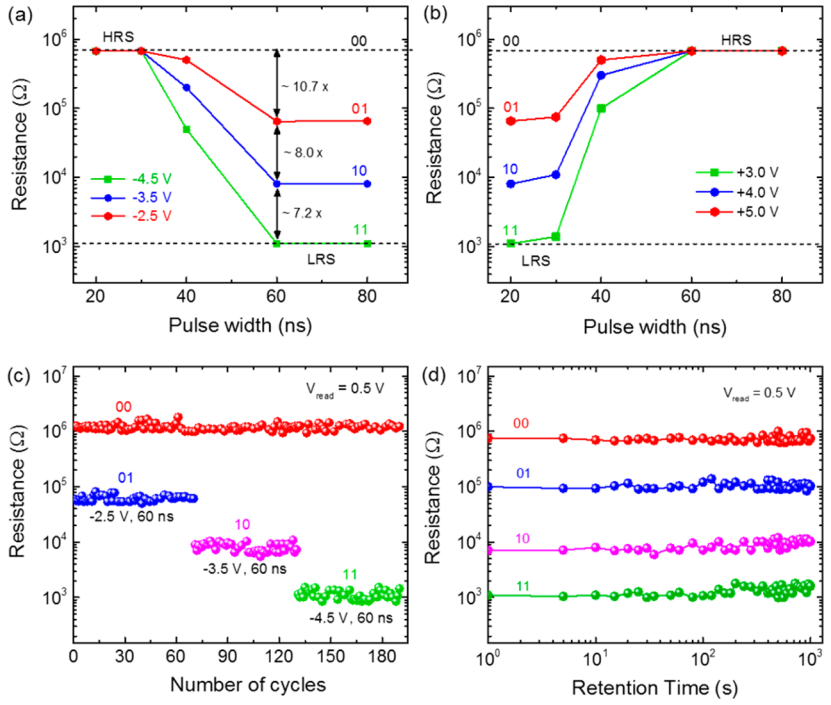

Figure 3. (a) The writing and (b) erasing of multilevel states in a 75 nm diameter GO memory cell (8 nm thick GO layer) *via* control of pulse amplitudes and durations. (c) Endurance and (d) retention behavior of the multilevel, nanoscale GO cell.

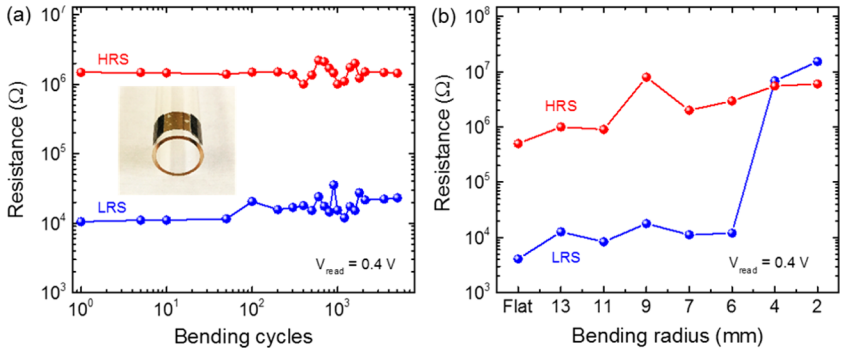

Figure 4. (a) Endurance performance of flexible 2 μm/8 nm GO devices after been subjected to multiple bending cycles at a bending radius of 9 mm. (b) The effect of various bending radii on the resistive switching performance of the GO cells; only extreme bending radii of 4 mm or less led to device failure. Here, for both tests, the sample was relaxed back to its flat state after targeted number of bending cycles/bending radii to measure the HRS and LRS states of the device before continuing with the bending procedure.

and HRS states is sustained for 10^5 s without noticeable change, apart from a slight narrowing of the resistance window. Again, note that the devices did not fail after 10^5 seconds, the measurements simply ceased then. Indeed, devices stored for 6 months after the measurements of Figure 2d still show a large resistance window (see Supporting Information Figure S4), demonstrating that these GO cells have excellent nonvolatile and nondestructive readout properties.

The high quality of the memory characteristics of our devices, as evidenced by the results of Figure 2, is undoubtedly related to the high quality our GO films. For example, by minimizing the variation in film thickness as well as reducing the number of cracks that are often seen within GO films during standard deposition processes, stable and repeatable operation of our memory cells can be achieved without performance degradation (see Supporting Information).

Multilevel Memory States. Memories with the ability to store more than one bit per cell, *i.e.*, having multilevel memory states, are very attractive since they offer a simple and cost-effective route to increased memory capacity (modern CMOS NAND-Flash for example typically stores 2 or 3 bits per cell). Combining such a multilevel storage capability with the extreme scalability that we have demonstrated with our GO memory devices would be particularly effective in terms of realizing memories with ultrahigh storage capacities. We show below that this is indeed possible by providing access to 4 very well-separated and stable memory states in nanoscale GO cells by controlling the write pulse duration and amplitude.

To determine possible conditions for the successful writing and erasing of multilevel memory states in our Pt/GO/Ti/Pt devices, we applied excitation pulses with amplitudes ranging from 2 to 6 V and durations from 20 to 80 ns and monitored the resulting resistance of cell, see Figure 3a and Figure 3b. We found that cells switched perfectly from the RESET state, which can be considered as the 00 state, to the 01, 10, and 11 memory states using pulses of −2.5 V/60 ns, −3.5 V/60 ns and −4.5 V/

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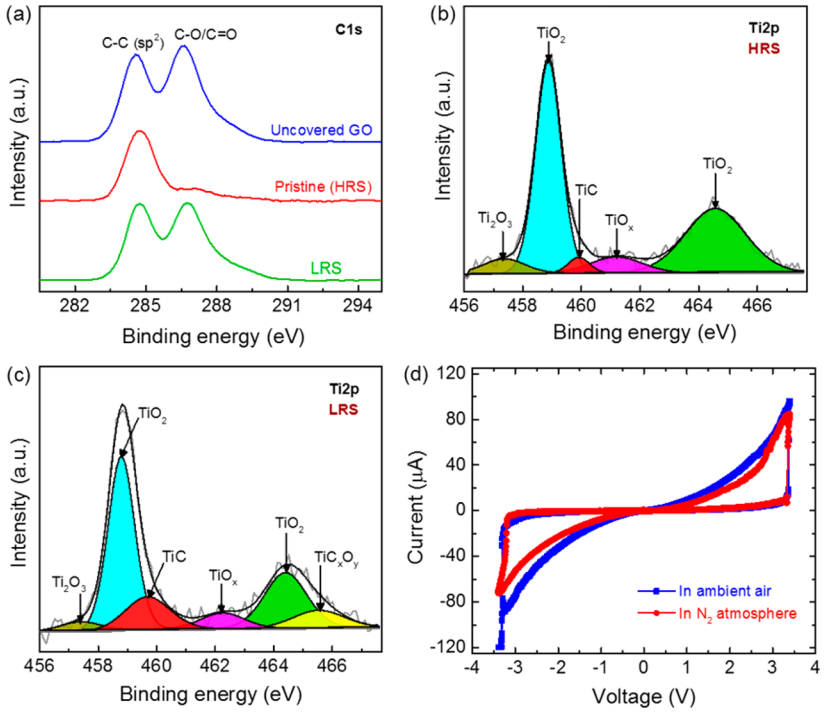

Figure 5. (a) High resolution XPS C1s spectra of GO cells in different states. (b,c) High resolution XPS Ti2p spectra of the GO cells in HRS and LRS states, respectively. (d) Resistive switching characteristics of our GO memory in air and N_2 atmospheres.

60 ns respectively (Figure 3a). The erasing of cells from the 01, 10, and 11 states back to the 00 state was successfully achieved for pulses of +3 V/60 ns, +4 V/60 ns and +5 V/60 ns respectively (Figure 3b). The separation of the intermediate resistance levels was very good (see Figure 3a), facilitating the readout process. The intermediate levels showed excellent endurance (Figure 3c) and were stable with time (Figure 3d).

Although the results of Figure 3 are for memory cells fabricated on Si/SiO_2 substrates, similar multilevel performance was also achieved for cells fabricated on plastic substrates (see Supporting Information Figure S5).

Flexible Memories. For flexible electronics applications, memory devices need to show good mechanical endurance and electrical reliability when subject to repeated flexing and bending. To evaluate the suitability of our GO memory cells for flexible applications, a 1 × 1 cm array of 2 μm memory cells (fabricated on PEN substrates) was repeatedly flexed through a bending radius of 9 mm (the inset of Figure 4a shows the photograph of the sample in a bent or flexed state). After a target number of such bending cycles, the sample was relaxed back to its flat state, cells switched into the HRS and LRS states and their resistances recorded, before recommencing the bending procedure. Figure 4a shows the resistance measured in both resistance states *versus* the number of bending cycles. There is little noticeable degradation even after 5000 bends at the relatively tight bending radius of 9 mm, demonstrating that our GO memories are likely to have excellent electrical reliability in flexible applications (note that devices did not fail after 5000 cycles, it is just that the measurements were stopped at that point).

In a second flexibility test, the substrate was bent from its flat position to increasingly extreme bending radii until device failure. After bending at each radius, the sample was relaxed to its flat position and switching measurements were performed on seven randomly selected devices to obtain an average resistance value for the HRS and LRS states. Figure 4b shows the resistance measured in both states as a function of the bending radius. It can be see that the resistance ratio between the HRS and LRS states is maintained even when the bending radius is reduced to very small values of around 6 mm (which can be considered as an "extremely flexed state"). Further bending, to 4 mm and 2 mm (at which point the sample is almost folded in two) caused the devices to fail, with cells remaining stuck in the high resistance state (upon microscopic inspection of these devices, it was found that this stuck-in-HRS failure was most likely due to cracking in the bottom Pt metal electrodes under extreme bending conditions). The results of Figure 4a and 4b confirm the suitability of our Pt/GO/Ti/Pt memory device structure for flexible electronics applications.

Note that, in tandem with those fabricated on Si/SiO_2 substrates, our GO memories on plastic substrates also showed ultrafast switching and excellent electrical endurance and retention characteristics (see Supporting Information Figure S6).

Resistive Switching Mechanism: Experimental. As discussed in the introduction, various physical mechanisms have been put forward in the literature as being responsible for resistive switching in GO-based materials and devices. The plethora of possible switching mechanisms (*e.g.*, metal filamentation, oxygen ion migration, desorption/readsorption of oxygen, diffusion of carbon atoms) and switching behaviors (bipolar, unipolar, with forming, without forming) reflects the plethora of GO memory materials and device structures investigated to date. And in many cases, conclusive proof of the switching mechanism has been absent. Such aspects have, we believe, hindered progress in GO memory development. We therefore in our work set out to provide evidence of the precise nature of switching for our GO memory devices, both *via* spectroscopic investigations and *via* the use of atomistic modeling.

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Since the results of electrical measurements on our devices indicated that a redox reaction at the top GO/Ti interface was most likely the driving force in the switching process, we investigated the chemical processes occurring at the top GO/Ti interface using X-ray photoelectron spectroscopy (XPS). Figure 5a shows the high-resolution XPS core-level C1s spectra of GO memory cells at different operating states, specifically a cell with the GO layer uncovered (*i.e.*, no top electrode), and in the pristine (HRS) and LRS states (now, obviously, with the top Ti/Pt electrode layer). For all these states, two peaks at 284.6 and 286.1 eV were observed in the C1s spectra, corresponding to (i) carbon−carbon peaks of C═C/C—C in graphene hexagonal rings and related to sp^2 carbon bonding and (ii) carbon−oxygen peaks of C—O/C═O related to sp^3 carbon bonding. However, the intensity of these peaks varied very significantly depending on the cell's operating state. For the cell with the uncovered GO layer, very strong peaks for both C═C/C—C and C—O/C═O bonds are seen, typical for an unmodified GO film. But, upon depositing the Ti top electrode, the oxygen (C—O/C═O) peak diminishes substantially, indicating the strong reduction of graphene oxide. In this condition the GO cell is in its pristine HRS configuration. After electrically switching the cell to the LRS state, it can be seen that the C1s signal shows a dramatic recovery of the oxygen (C—O/C═O) peak that was suppressed when in the HRS state (identical behavior was noted for all cells tested).

We interpret these XPS findings as follows. When the Ti metal is deposited on top of the GO film in order to form the top electrode, Ti atoms take oxygen groups from the first few nanometers of the oxygen-rich GO film, leading to a relatively thick (few nm) TiO_x amorphous interface layer at the GO/Ti interface. Thus, the surface of the GO film will be reduced while the Ti at the GO/Ti interface will be oxidized, resulting in the XPS C1s spectrum of the pristine cell having a reduced oxygen (C—O/C═O) peak intensity (compared to the uncovered cell case). The interfacial TiO_x layer acts as an insulating barrier that dominates the total resistance state of the cell, essentially placing it in the HRS or RESET state. On the application of a negative bias to the top electrode, Ti−O chemical bonds are broken, oxygen ions diffuse back into the GO film and the cell is switched into the LRS or SET state. This transfer of oxygen groups away from the TiO_x layer and back into the GO film results in a large recovery of the C—O/C═O peak. It also lowers the interfacial energy barrier (between the top electrode and the GO) causing the cell resistance to decrease, thus putting the cell in the LRS state.

Note that both TiO_x and GO play a crucial role in the switching process and are essential for reversible operation of our devices. In the absence of either of these layers, the devices reach permanent breakdown condition. Indeed, the extensive Raman spectroscopic studies that we performed before and after switching the device to LRS and HRS states revealed the active participation of both GO and TiO_x layers in the switching process and also confirmed that the switching mechanism in our devices is fundamentally different to that of "conventional" TiO_x-based resistive memories (see Supporting Information Figures S8 and S9 and associated text).

We also carried out high-resolution XPS measurements of the Ti2p spectra to provide additional analysis of the physical processes occurring in the Ti/GO interfacial region as a result of memory switching. Figure 5b shows the Ti2p spectra in HRS state, where strong TiO_2 peaks are observed at 458.8 and 464.5 eV, along with peaks due to other Ti−O species (Ti_2O_3 and TiO_x) at 457.3 and 461.2 eV and a weak peak at 459.8 eV related to TiC.[57,58] When the memory cell is switched to the LRS state, the Ti2p spectrum (Figure 5c) shows a significant reduction in the height of the TiO_2 peaks, along with an increase in the TiC peak and the appearance of a TiC_xO_y peak. These results are consistent with the view that in the HRS state an "insulating" TiO_x barrier is formed at the GO/Ti interface, with oxygen moving away from the GO/Ti interface (and back into the GO film) for a cell in the LRS state. It is well-known that Ti energetically favors bonding with oxygen (Ti−O) first, followed by carbon (Ti−C) and finally Ti−Ti bonds as a last reaction pathway.[58] Hence, in the LRS state, the relative absence of oxygen groups at the Ti/GO interface leads to Ti bonding directly with carbon to form TiC and TiC_xO_y species, as revealed in the XPS spectra.

Note that the reaction pathways in our Pt/GO/Ti type cells are quite different from those in commonly reported Al/GO/Al memories, since in the latter the formation of AlC (aluminum carbide) is not energetically favorable, so Al atoms first prefer bonding with oxygen atoms and then immediately to other Al atoms (Al−Al bonds), resulting in the formation of metal Al filaments at the Al/GO interfacial region, as reported by several groups.[24,33]

Finally, for an additional experimental insight into the switching process in our memory cells we also performed switching in an N_2 atmosphere and compared the results to switching in air. If switching is (as all the evidence presented above points to) due primarily to interface/barrier changes within the cell, rather than being due to any kind of oxygen exchange process with the atmosphere (as reported in other studies[40]) then the changes to the ambient atmospheric conditions should not significantly affect the GO memory cell operation. This is indeed what we found, as shown in Figure 5d, where almost identical switching behavior was observed for the cell operated in air and in an N_2 atmosphere.

Resistive Switching Mechanism: Simulation. To gain a deeper understanding of the precise mechanisms at play during resistive switching in our GO memory we also carried out first-principles calculations based on density functional theory (DFT) to model the chemical reactions occurring at the GO/Ti interface using the PBE (Perdew−Burke−Ernzerhof) exchange-correlation functional and, in selected cases, also the more accurate hybrid functional PBE0. Our modeling approach (see Supporting Information Figure S10) is summarized in the Methods section, with more detail given in the Supporting Information.

We begin by considering three starting atomic configurations for the GO/Ti interface, as illustrated in Supporting Information Figures S11a, S12a, and S13a; each consists of a GO layer in proximity to a clean titanium surface. Upon relaxation of these starting configurations, most of the epoxy and hydroxyl groups (which account for the majority of O-containing species bonded to the graphene, see previous section) that are bonded to the graphene surface facing the titanium surface migrate to that titanium surface, as shown in Supporting Information Figures S11c, S12b and S13b, with most of the O atoms being adsorbed at the Ti surface (though a few diffused between the first and second Ti layers, see Supporting Figure S13b). We found that this oxidation of titanium *via* oxygen transfer from the graphene oxide is an exothermic process with an energy stabilization of around 4.4 to 5 eV/O atom (see Supporting Figure S14). Thus, these simulations corroborate our experimental findings (*via* XPS)

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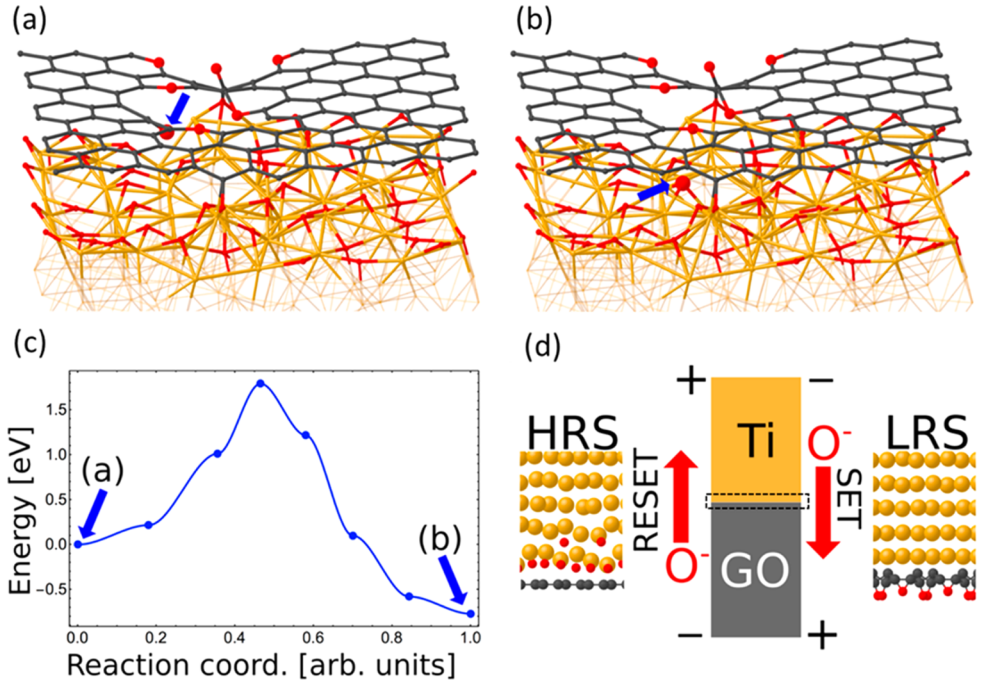

Figure 6. (a) Initial and (b) final configurations of a reversible reactive pathway for oxygen transfer. Titanium, carbon, and oxygen atoms are indicated in orange, dark gray, and red, respectively. The blue arrows indicate the reactive oxygen atom (illustrated *via* the largest sphere). The in-plane oxygen atoms that can undergo reversible switch are indicated *via* larger spheres. (c) The minimum energy pathway for the process computed with the NEB method, see Method section. The activation energy barrier is 1.8 eV (PBE). The continuous blue line represents a cubic interpolation of the energies of the images used in the NEB calculation. The process is exothermic, the energy of the configuration in (b) is 0.77 eV (PBE) lower than the energy of (a). (d) Sketch of the switching mechanism. The RESET step occurs *via* migration of oxygen atoms from GO to titanium. The product is a high resistance state (HRS). The low resistance state (LRS) is restored by migration of oxygen atoms from the oxidized titanium to the graphene-oxide. The polarity is indicated *via* "+" and "−" symbols.

that, during fabrication of the Pt/GO/Ti device, Ti atoms take oxygen groups from the GO layer and form a TiO_x interfacial layer.

However, a process such as that above in which atoms gain many eV of energy is unlikely to be easily reversed, so where might the reversibility lie in our devices? The answer can be found by considering the energetics of oxygen species located in "voids" in the graphene (such "voids" arise naturally in GO films such as ours, which are made up from many entwined nano/microscale GO particles). Prototypical oxygen atoms adsorbed in a void are illustrated in Figure 6a and 6b (and additional void structures modeled in this work are illustrated in Supporting Figure S12 and Figure S13). Within our sampling of the configurational space, the lowest energy sites for oxygen atoms in GO were found to be carboxyl or epoxy groups located in such voids and these O atoms have comparable (within 1 eV) energy to that of O atoms adsorbed on titanium. The activation energy barrier to transfer one of these oxygen atoms from a void in the GO to the titanium surface was found to be only 1.8 eV (PBE), and in this case oxygen transfer brings a stabilization of the energy by 0.77 eV (PBE), see Figure 6c. Given the relatively small energy difference between an oxygen adsorbed at the titanium surface and one adsorbed in a void of GO, we consider that the transfer of oxygen between such sites will be reversible under the presence of an electric field. Furthermore, as we show below, migration of oxygen in this way leads to a modification of conductivity and is therefore, we believe, the origin of the reversible resistive switching we observe in our devices (see Figure 6d).

We now present a comparison of the electronic properties of different GO/Ti interfaces to elucidate the link between the degree of oxidation of titanium and the resistance of the system. For this task we generated five GO/Ti regions containing the same total number of atoms, but differing in the distribution of the O atoms through the whole system. The relaxed geometries labeled with S1, S2, S3, S4, and S5 are illustrated in Supporting Figure S15a. The numbers of oxygen atoms having at least one bond with a Ti atom are 99, 109, 113, 130, and 139 in S1, S2, S3, S4, and S5 respectively. The species-resolved atomic distributions projected along the normal to the interface are illustrated in Supporting Figure S15b. Using the hybrid functional PBE0, we computed the electron density of states and the optical conductivity according to the Kubo−Greenwood formula, (see Methods), which is a joint density of states weighted by the dipole matrix element and which we use here as a proxy for electrical conductivity. In Supporting Figure S15c we plot the optical conductivity along the normal to the interface (z-axis), $\sigma_z(E)$, since it represents the direction along which the resistance is measured in the memory device. We observe a correlation between $\sigma_z(E)$ and the amount of oxygen in the titanium and GO. More specifically, the conductivity decreases (resistivity increases) as O atoms move from GO to titanium, see inset of Supporting Figure S15c.

CONCLUSIONS

We have developed a hybrid graphene oxide−titanium oxide nonvolatile resistive memory that not only offers the attractive features of "traditional" graphene oxide memories, such as the suitability for flexible and transparent electronics applications, a simple and cost-effective production *etc.*, but also allows for a nanometric size-scaling, nanosecond switching speeds and

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multilevel (multibit) operation. Specifically, we have not only presented the smallest (50 nm), fastest (sub-5 ns), thinnest (8 nm) GO-based memory devices produced to date, but also demonstrated that our approach provides easily accessible multilevel (4-level, 2-bit per cell) storage capabilities along with excellent endurance and retention performance—all on both rigid and flexible substrates. *Via* comprehensive spectroscopic (XPS and Raman) and electrical characterization, backed-up by detailed atomistic simulations, we have shown that the resistive switching mechanism in our devices is driven by redox reactions in the interfacial region between the top (Ti) electrode and the GO layer. When the Ti metal is deposited on top of the GO film in order to form the top electrode, Ti atoms take oxygen groups from the first few nanometers of the oxygen-rich GO film, leading to a relatively thick (few nm) TiO_x amorphous interface layer at the GO/Ti interface that acts as an insulating barrier, placing the cell in the HRS or RESET state. On the application of a negative bias to the top electrode, Ti−O chemical bonds are broken and oxygen ions diffuse back into the GO film. This transfer of oxygen groups away from the TiO_x layer and back into the GO film lowers the interfacial energy barrier (between the top electrode and the GO) causing the cell resistance to decrease, thus putting the cell in the LRS state. The switching between HRS and LRS states is electrically reversible and repeatable, the states themselves are stable in air for prolonged durations, and devices fabricated on flexible plastic substrates withstood repeated and extensive bending. Our results will help transform the way in which we view the potential and possibilities for GO memory device development and applications.

METHODS

Material Preparation. The GO films were prepared from commercially available GO flakes dispersed in water (Graphenea Inc., concentration: 4 mg/mL) and diluted to 8×10^{-2} mg/mL. This solution was then filtered using a cellulose-ester membrane with a pore size of 25 nm. Such a small pore size blocks the GO flakes on the membrane while allowing the water to flow through, forming a thin film of GO flakes on top of the filter membrane. The volume of filtered GO dispersion allows control over the final film thickness. Following filtration, the GO film was detached by immersing the membrane in deionized water (see Supporting Figure S16). This is an environmental friendly process without the need for dissolving the membrane in solvents as in conventional vacuum filtration methods.[47] The floating GO film can then be scooped up onto the target substrate. The number of scoops determines the final film thickness, making it an extremely simple process to precisely control the GO layer thickness. This transfer process is highly reproducible with very high yield and as the film size is only limited by the area of the membrane, this approach is capable of producing uniform wafer-scale GO films on a wide range of rigid and flexible substrates.

XPS Characterization. The surface chemical composition of GO films was analyzed by a Kratos AXIS Nova-165 photoelectron spectrometer equipped with a monochromic Al Kα X-ray source (1486.6 eV). The high-resolution XPS C1s and Ti2p spectra were collected under a high vacuum of $\sim 3 \times 10^{-9}$ mbar at room temperature. In order to understand the change, as a result of resistance switching, in the chemical state at the top Ti/GO interface of actual memory cells, special cells with especially thin top electrodes (~4.5 nm Ti layer and ~1.5 nm Pt layer) were fabricated, so allowing direct and nondestructive XPS access to the Ti/GO interfacial region for cells in both the HRS and LRS states and without the need for electrode removal. To improve the signal-to-noise-ratio, Savitzky−Golay smoothing was performed on all the acquired spectra. Each high-resolution C1s and Ti2p scan reported here is an average of 20 scans taken using a pass-energy of 20 eV, an energy step of 0.15 eV and a dwell time of 100 ms. The chemical composition of species was identified by fitting the high-resolution C1s and Ti2p spectra with mixed Gaussian−Lorentzian functions after performing Shirley background subtraction.

Raman Characterization. Raman measurements were performed using a Horiba Scientific Xplora Raman system equipped with an air cooled charge coupled device (CCD) detector and fitted with solid-state diode lasers (532 and 638 nm) for excitation. The spectra were taken at room temperature using a 100× objective lens and 2400 grooves/mm grating with a focused laser spot size of ≈0.70 μm and an incident laser power of <100 μW to avoid damage to the GO film. The peak positions and the I_D/I_G ratios were estimated by fitting the Raman spectra with Lorentzian functions.

UV−Vis−NIR Spectroscopy. UV−vis−NIR measurements were performed using a Jasco MSV-5300 microspectrophotometer equipped with a tungsten halogen visible source, a deuterium arc UV source, a photomultiplier tube UV−vis detector and a thermoelectrically cooled InGaAs NIR photodetector. The resolution was chosen to be at 1 nm and the aperture was set to 50 μm diameter. The GO films were transferred on to Quartz substrates (IDB technologies) to acquire absorbance and transmittance spectra at randomly selected regions of the film (see Supporting Figure S17).

Device Fabrication. The memory devices were fabricated on Si/SiO_2 (300 nm) substrates using e-beam lithography (NanoBeam nB4 e-beam system) and laser lithography (Durham magneto optics laser writer) techniques. First, the bottom electrodes were deposited by sputter coating blanket Pt (40 nm)/ Ti (8 nm) metal films on to Ar plasma cleaned Si/SiO_2 substrates under a base pressure of 5×10^{-7} Torr. Next, GO films of different thicknesses were transferred on top of the bottom electrodes using vacuum filtration method described above. Then, to form top electrodes, another blanket film of Pt (15 nm)/Ti (7 nm) was sputter coated on to the GO film. Finally, this blanket Pt/Ti/GO/Pt/Ti structure was lithographically patterned into an array of circular resist patterns (PMMA or AZ5214E resist) with varying diameters of 50 nm to 300 μm, which acts as the sacrificial mask. Reactive Ion etching was then used to etch away the regions unprotected by the resist, followed by resist mask removal in acetone/IPA, resulting in Pt/Ti-GO-Pt/Ti pillar structure.

Flexible GO memory cells were fabricated on 75 μm thick PEN (Polyethylene-naphthalate) substrates using e-beam lithography. Prior to fabrication, PEN substrates underwent standard chemical cleaning using acetone/IPA solvents for several minutes. Immediately after this cleaning step, a 10 nm thick Pt bottom electrode with 4 nm Ti thick adhesion layer was deposited using DC magnetron sputtering. Next, an 8 nm thick GO blanket film was transferred onto these Pt/Ti coated PEN substrates using vacuum filtration method. Finally, top electrodes of Pt (15 nm)/Ti (7 nm) with 1 to 100 μm diameters were sputter deposited by a single e-beam lithography step.

Electrical Characterization. The electrical switching properties of fabricated GO memory cells were investigated by a Bruker Innova SPM system. Highly conductive, mechanically robust and sharp (~20 nm diameter) PtSi tips and conductive diamond tips (Bruker AFM probes) were used as electrical probes to contact the top electrodes, while the blanket Pt film underneath the GO layer serves as a bottom electrode. The conductive diamond tips and PtSi tips have excellent durability and very high current carrying capacity (unlike conventional C-AFM tips such as Pt/Ir), ensuring prolonged measurement cycles. A Tektronix AFG3101 and Avtech AVMR-2D-B arbitrary pulse function generator were used for ultrafast pulse switching measurements. For more information on the electrical test setup, see ref 10.

Atomistic Simulations. The first-principles (FP) simulations were performed within the framework of DFT in the local density approximation supplemented by generalized-gradient corrections[59] including van der Waals (vdW) Grimme corrections.[60,61] The properties involving virtual states were computed using the well-known DFT hybrid PBE0 exchange-correlation functional to better reproduce the band gap otherwise underestimated in standard DFT. We used the Quantum-ESPRESSO (QE) and CPMD codes.[62] The QE code was used for total energy calculations and geometry relaxation of systems containing at most 160 atoms. For such systems

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we used a simulation cell 5.0808 Å × 8.8002 Å × 29.9766 Å with a 4 × 2 × 1 mesh of k-points for the integration of the Brillouin Zone. We used Goedecker-Teter-Hutter pseudopotentials (GTH)[63] with a plane-wave expansion of the Kohn−Sham orbitals up to a kinetic energy cut off of 100 Ry. For larger systems containing up to 621 atoms, we used the CPMD code. In the Supporting Information we report the box size and the number of atoms of each structure. In order to reduce the computational effort of hybrid calculations (PBE0) we used norm-conserving Martin−Troullier pseudopotentials[64] which allow a lower kinetic energy cut off of 70 Ry, which were tested against the GTH pseudo. For systems with more than 300 atoms, we used only the Γ-point for BZ sampling. We used the nudged-elastic band method (NEB)[65] to compute the energy barriers along two reactive path. To correlate the structural changes to the experimentally observed change in resistance in the material we computed and compared the optical conductivity $\sigma_z(E)$ projected along z-axis, which is the normal to the Ti/GO interface in our setup, of different structures according to the Greenwood−Kubo formula, see Supporting Information.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.6b08668.

Supporting Methods and Results: CAFM electrical switching; memory cell characterization results; switching mechanism and role of GO and TiO_x; graphene oxide preparation and optical characterization; the effect of GO uniformity and roughness on device performance; supporting atomistic simulations (PDF)

AUTHOR INFORMATION

Corresponding Author

*E-mail: david.wright@exeter.ac.uk.

ORCID

C. David Wright: 0000-0003-4087-7467

Notes

The authors declare no competing financial interest.

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