

# **"How could the "Open Source Silicon" movement drive Device and Materials development?"**

<https://github.com/jun1okamura/2024-International-Conference-on-Solid-State-Devices-and-Materials-Short-Course-2>



AIST Solutions  
Producer Jun-ichi OKAMURA

# Biography



- 1986 : Joined SDEL in Toshiba as a researcher for DRAM development
  - 1996 : Worked in the US for IBM/Toshiba/Siemens alliance project
  - 1999 : Joined THine Electronics, startup in Japan (before IPO)
  - 2006 : Established Trigence Semiconductor with two Toshiba colleagues
  - 2009 : Got a grant fund from JST 150M JPY
  - 2012 : Seed fund from INTEL capital 600M JPY
  - 2014 : Series A 840M JPY
  - 2015 : Series B 650M JPY
  - 2018 : Series C Failed Series D fundraising Total 2,480M JPY
  - 2022 : Liquidated Trigence, then join AIST as an invited researcher
  - 2023 : Join AIST Solutions as a producer of semiconductor sector
  - 2024 : Established non-profit OpenSUSI and be representative director
- ※ IEEE Senior member

BIO: LinkedIn

<https://www.linkedin.com/in/jun-ichi-okamura-6b8bb2b/>

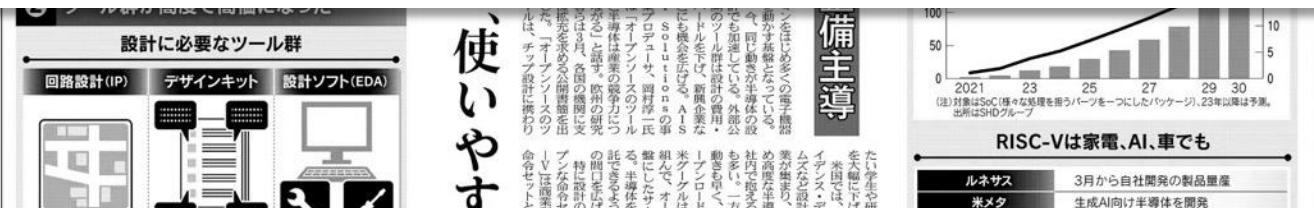
# A new alternative trend of semiconductor design

## 半導体設計、オープン化の波

半導体の設計に、無償で一般公開された「オープンソース」が活用され始めた。高度化によるコスト増や技術者不足などの構造問題の解決に向けて、誰でもアクセスできるツール群を使おうという試みだ。産業技術総合研究所（産総研）や米グーグルは利用環境の整備に動く。オープン規格を採用する企業も増えている。

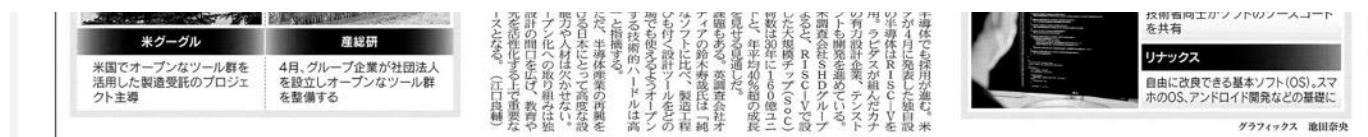
AIST and Google lead semiconductor design “opening” initiative:  
2024/May/10 Nihon Keizai Shimbun, #1 economic newspaper in Japan

<https://www.nikkei.com/article/DGXZQOUC228690S4A420C2000000/>



## Open Source Utilized Silicon Initiatives (OpenSUSI) purpose

OpenSUSI is established to provide an environment for the industry that is long-tail chip users to compete with dedicated semiconductors by Japanese domestic semiconductor assets (chip manufacturing capacity) into a platform that lowers the barriers to entry for original chip design.



# Agenda

---

- What is Open Source Silicon ?
- Why Open Source Silicon is focused on?
- When Open Source Silicon activity was rebooted?
- Why does it focus on the legacy process?
- How is it going to make real evidence?
- How it works in eco-system?
- What is the OpenSUSI intention?
- Open Source Silicon Pros and Cons.
- Summary for Device and Materials.

# What is Open Source Silicon ?



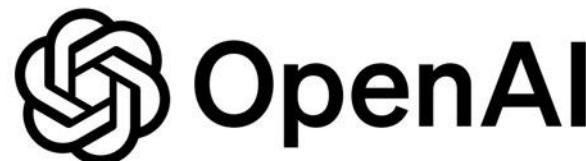
# Open Source Software Development



Android SDK



Visual Studio Code



PyTorch

# Silicon Device Development

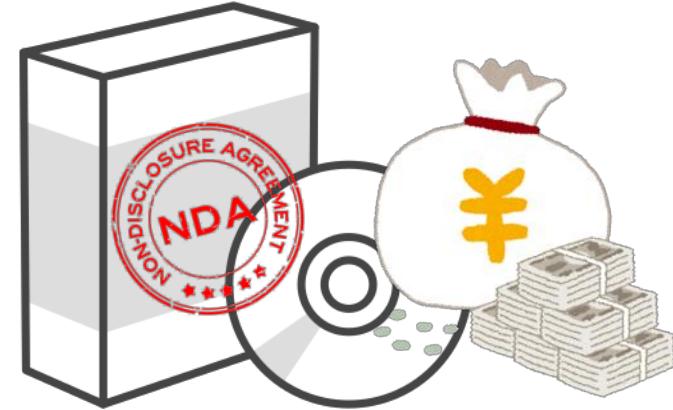
Simulation



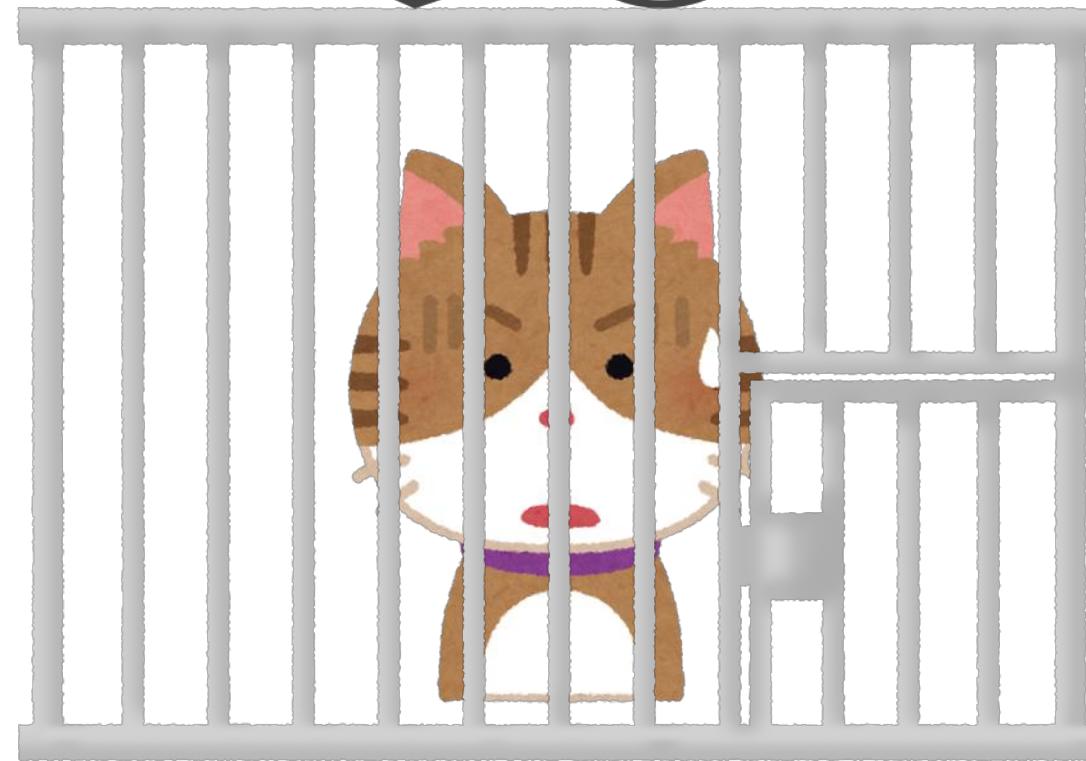
Layout



Test



Synthesis



Prototyping



# High entry wall of semiconductor startup



# Open Source Silicon is ...

---

1. Designing using **Open Source EDA** tools, original design and synthesized data (netlist and GDSII) could be shared within the design community and re-used, transferred, and evaluated without any restrictions if the designer would like to open it.
  
2. Designing utilizing open source process information, **Open Source PDKs**, then design assets (circuit diagrams, custom layouts) and source design files can be made public, verified, improved, and replicated by others and shared within the community.
  
3. A fab service that manufactures and supports **Open Source Silicon devices** designed in (1) and (2) above, and the designed hardware **can be verified by intended real applications.**

# Why Open Source Silicon is focused on?



# Why Open Source Silicon is focused on?

## 【On Educational】

- The increasing cost of semiconductor design and development education is becoming a significant barrier, particularly for undergraduate students at the entry-level. This rising expense limits opportunities and discourages interest among potential future innovators.
- It is important to nurture young students interested in semiconductor design and development. These talented individuals are crucial, not only for passing on knowledge and skills but also for ensuring the creation of secure devices. Additionally, developing domestic expertise is essential to reduce reliance on foreign sources.

# Why Open Source Silicon is focused on?

- Students engaged in semiconductor design must develop proficiency in Linux and VPN connections to secure the use of commercial EDA tools. Additionally, they needed to sign NDAs to access commercial PDKs, which are critical for device design and advancing to the tape-out stages.
- In Japan, the academic licenses for commercial EDA tools are strictly limited to research and development purposes on the licensing agreements. As a result, the availability of licenses for proof of concept (PoC) development for new startups or crowdfunding efforts is quite limited, even within the academic community.

# Why Open Source Silicon is focused on?

## 【On Security】

- Large-scale integrated (LSI) semiconductor devices are crucial for any modern technology, and our daily lives rely heavily on them. It's important to monitor the origins of these devices, including the software versions they employ.
- So, keeping track of the manufacturers and the software of LSI devices is essential. This is not only for preventing errors but also for protecting against security risks like Trojans or backdoors. Strict oversight is vital for ensuring the reliability and security of our semiconductor devices.

# Why Open Source Silicon is focused on?

- The Open Source EDA toolchain offers a viable option for expanding design opportunities, particularly for those just starting in semiconductor design. It not only lowers entry barriers but also nurtures a deeper interest in the field.
- Open Source PDKs facilitate the full transferability of IP and provide significant opportunities for sustainable development within the semiconductor design arena.
- By integrating both Open Source EDA tools and Open Source PDKs, we can spearhead the development of an Open Source Silicon ecosystem. This integration aims to foster transparent design resources and ensure the availability of secure, traceable design assets and the integrity of semiconductor products.

# Why Open Source Silicon is focused on?

USA: 2023/Nov/02

NSF Integrated Circuit Research, Education and Workforce Development Workshop Final Report

<https://arxiv.org/pdf/2311.02055>

EU: 2023/Nov/03

Recommendations and roadmap for the development of open-source silicon in the EU

[https://wiki.f-si.org/images/1/19/Recommendations\\_and\\_roadmap\\_open\\_silicon\\_2023\\_11\\_03.pdf](https://wiki.f-si.org/images/1/19/Recommendations_and_roadmap_open_silicon_2023_11_03.pdf)

EU: 2024/Mar/08

Importance of Open-Source EDA Tools for Academia

<https://open-source-eda-letter.eu/>

# When Open Source Silicon activity was rebooted?



# When Open Source Silicon activity was rebooted?

- 2018 **DARPA** founded Open Source EDA tool development
- 2019 **efabless** approached google to fund the release of the SkyWater's S130 PDK under the Apache 2.0 license.
- 2020 Google and efabless started **OpenMPW** program
- 2021 **IEEE SSCS** sponsored **Chipathon** design contest with Open Source Silicon
- 2023 **OpenMPW** reached **826** applicants and **400** TO projects with **10** shuttle runs.
- 2024 **ChipsAlliance** started new sub-group for Open Source PDKs
- 2024 **OpenSUSI** was established in Japan to support Open Source Silicon eco-system

**Only last 5 years**

<https://www.darpa.mil/program/intelligent-design-of-electronic-assets>

[https://www.darpa.mil/attachments/eri\\_design\\_proposers\\_day.pdf](https://www.darpa.mil/attachments/eri_design_proposers_day.pdf)

<https://github.com/The-OpenROAD-Project>

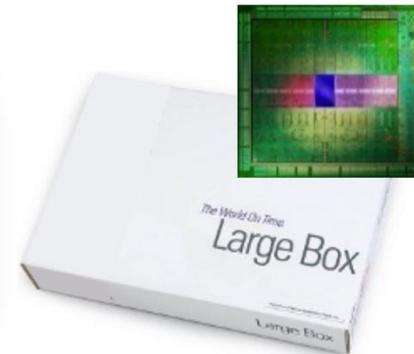
<https://developers.google.com/silicon>

# DARPA@2017 presentation



Are you awake?

```
$ git clone https://github.com/darpa/idea  
$ git clone https://github.com/darpa/posh  
$ cd posh  
$ make soc42
```



Distribution Statement "A" (Approved for Public Release, Distribution Unlimited)

72

# When Open Source Silicon activity was rebooted?

## **[Foundries activity and concerns]**

- 2022 Global Foundries announced to join OpenMPW
- 2023 iHP(Germany) released OpenPDK for their 130nm
- 2024 ChipsAlliances starts OpenPDK sub-group

In the semiconductor industry, fabricators generally do not release Process Design Kits (PDKs) without non-disclosure agreements (NDAs). This practice is primarily due to the confidential nature of semiconductor process technology, which often remains sensitive even years after its development. Fabricators may also hesitate to share these resources because of potential concerns regarding the maintenance quality or the comprehensive documentation of the PDKs.

# When Open Source Silicon activity was rebooted?

## **[ Expanding International User Development**

Open Source PDKs offer the exciting possibility of international user development. With only internet access, individuals and organizations worldwide can engage in chip design and tape-out activities.

## **[Maintenance and Support by the Community]**

The Open Source Silicon Community holds significant potential to maintain and sustainably enhance PDKs, similar to the model followed by Open Source Software. This community-driven approach ensures continuous improvements and support, fostering a robust ecosystem for semiconductor development.

# Why does it focus on the legacy process?



# Components of chip cost

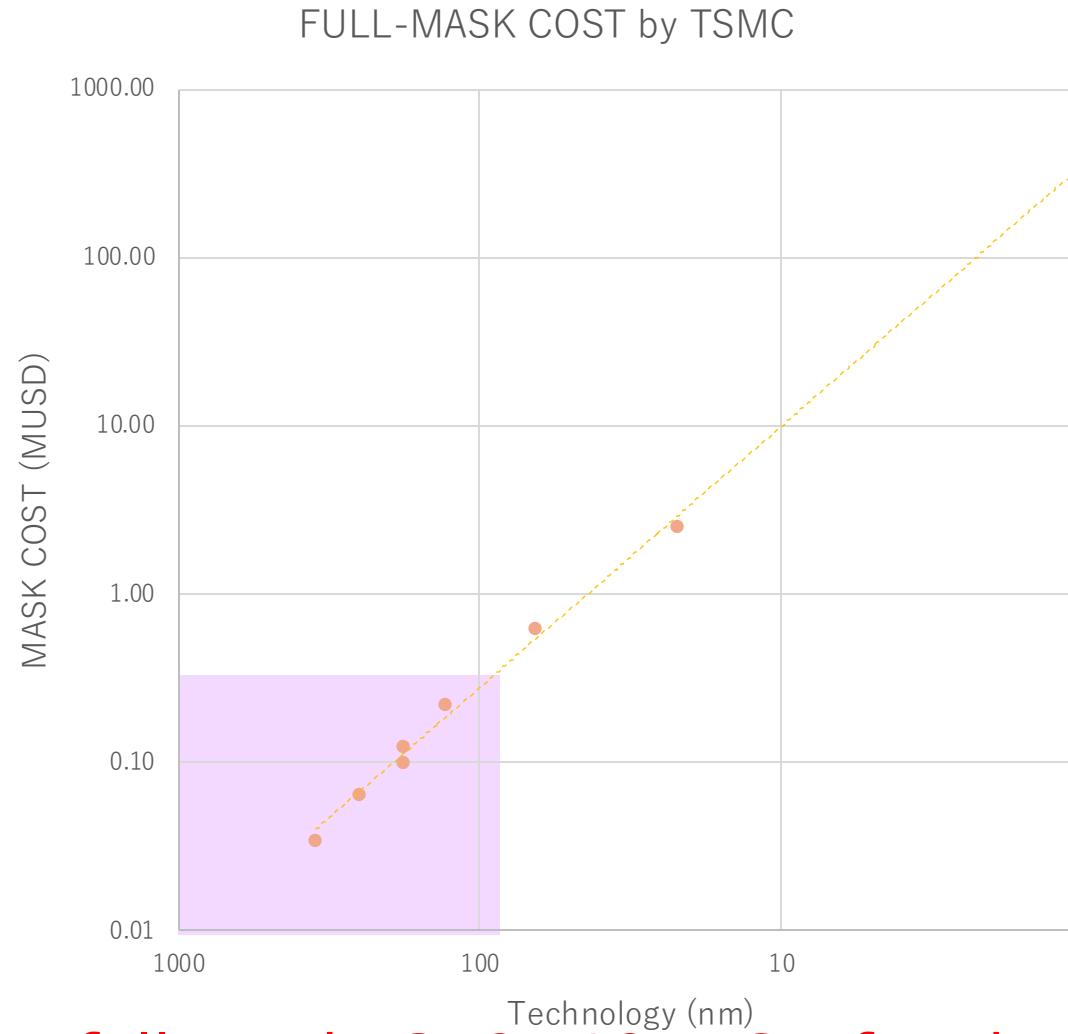
Design cost                          Production cost

Chip cost =  $\frac{\text{EDA tools + IP}}{\# \text{ of products}}$  +  $\frac{\text{mask} \times \text{Layers}}{\# \text{ of products}}$  +  $\frac{\text{Wafer price}}{\text{Gross}}$

$$\alpha \cdot x^{-1.16} \quad \rho \cdot x^{-1.55} \quad \sigma \cdot x^{-0.75}$$
$$\approx 50\% \text{up} \quad \approx 70\% \text{up} \quad \approx 30\% \text{up}$$

Low Volume Production = Design and Mask are major cost

# Mask cost limit for a reasonable budget



NRE COST

10K ~ 400KUSD for full mask, 250~10KUSD for shuttle die (40/reticle)

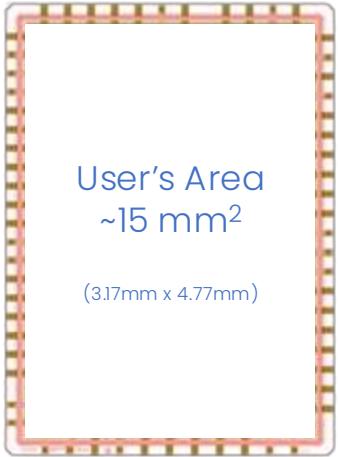
<https://qiita.com/jun1okamura/items/46baa5a35066f18a0801>

<https://github.com/jun1okamura/A-Qualitative-Overview-of-Semiconductor-Costs>

# New ASIC Development Platform, what chipignite is?



40 Dies/Reticle

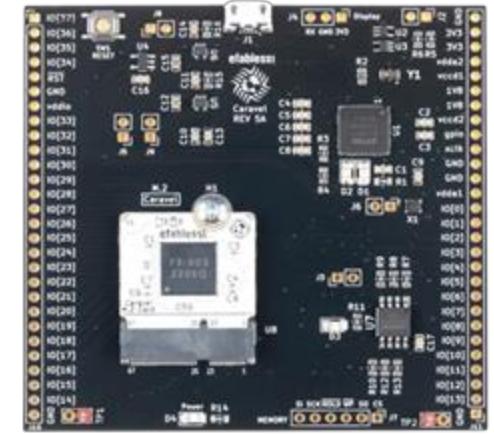


User's Area  
~15 mm<sup>2</sup>  
(3.17mm x 4.77mm)

\$9,750  
100 QFN

+

Evaluation board



Skywater nand2 size  $3.753\mu\text{m}^2 = 3.9\text{M Gates}$   
4KB single port SRAM :  $0.118\text{mm}^2$

Can integrate RISC-V 32 I/E  
~120K Gate + Cache (4~16KB)

# What does chipIgnite drive?

- **Low Cost:**  
130nm/100 QFNs/\$9,750 by chipIgnite prototype service
- **Real experience:**  
RTL design to REAL silicon evaluation
- **Satisfaction:**  
Only one “Chip” in the world by own idea
- **Design Community:**  
No-NDA means open and transferable
- **Easy entry:**  
Just works on your PC, no-VPN and no Servers,

# Can we afford to beyond the legacy process?

## 【Challenge of beyond legacy process】

- **Economic and Security Concerns:** There is a potential risk involving economic security when dealing with proprietary information related to leading-edge process technologies.
- **Rising Costs:** The cost of masks, even for Multi-Project Wafer (MPW) projects, is expensive, which could limit accessibility and feasibility for smaller-scale operations.
- **Design Complexity:** Achieving OPC-ready layout designs and ensuring designs are DRC clean are becoming increasingly complicated, demanding more sophisticated and precise design techniques.

# Can we afford to beyond the legacy process?

## 【Challenge of beyond legacy process】

- **Signal and Power Integrity:** As processes shrink, issues related to signal integrity and power integrity become more predominant, and the lack of Open Source EDA tool support for these advanced concerns can be a significant barrier.
- **Lack of Advanced IP Support:** There is an absence of support for state-of-the-art IPs, such as USB, DDR, and PCIe, within the open-source community, which can hinder the development of fully functional modern devices.

# How is it going to make real evidence?



# Foster an interest in semiconductor design

## Systematic educational approach

Abstraction Layer Sandwich

Software Systems  
Algorithms

Hardware Systems  
Circuits

Devices  
Materials

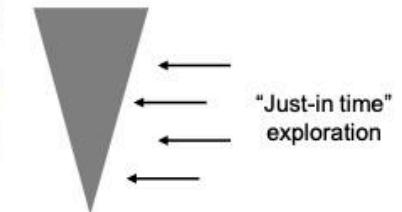


Traditional learning  
trajectory for chip  
designers

Software Systems  
Algorithms

Hardware Systems  
Circuits

Devices  
Materials



- The current education system requires far too many prerequisite courses before exposing students to chip design (especially mixed-signal)
- The field was created bottom-up, but innovation is progressively shifting to higher levels of abstraction
- We must adjust to this trend to re-energize chip design education

B. Murmann

U.S.-Japan Collaborative Workshop on Advanced  
Integrated Circuit Design (Phase 2)

4

B. Murmann

U.S.-Japan Collaborative Workshop  
Integrated Circuit Design

- It is not necessary to understand the entire sandwich to learn the basics of chip design (including mixed-signal ICs)
- Possible approaches for university teaching
  - Follow along as the instructor creates a "template" design
  - Form teams of students with complementary skill sets
    - Some may understand transistors, some excel at software, etc.



## Teaching Mixed-Signal Design Using Open-Source Tools, Boris Murmann, University of Hawaii

[https://github.com/bmurmann/US\\_Japan\\_Semiconductor\\_Workshop/blob/main/Day%201%20-%201100%20-%20Teaching%20using%20OS/slides.pdf](https://github.com/bmurmann/US_Japan_Semiconductor_Workshop/blob/main/Day%201%20-%201100%20-%20Teaching%20using%20OS/slides.pdf)

# Open Source PDKs for Education

## No legal agreements

Access to the foundry technology, chip reference design, EDA tools and design flow are completely open-source.

There are no NDA or other legal agreements required. All content can be downloaded from git repos.

There are no export control restrictions, making it easy to provide access for all your domestic and international students.

## Rapid Design

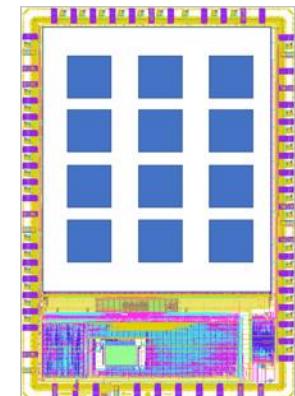
Leveraging reference designs and automated flows enables students to complete a design in a full chip within the time constraints of a single session.

Single session courses can enable students to complete a focused design goal by leveraging an existing template for a full chip.

## Freely collaborate

No NDAs means you can freely share design files across teams and organizations, including GDS final layout files.

Collaborate with universities freely including sharing projects, course content, joint design or support design competitions.



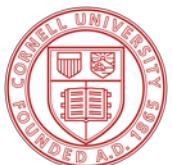
## Aggregate multiple projects into a single tile

Courses with smaller digital or analog student projects can be aggregated into a single project slot making fabrication very cost effective for larger class sizes.

# chipIgnite for Experiential Learning in Action



Georgia Institute  
of Technology



UNIVERSITY  
of DALLAS



The City College  
of New York



W UNIVERSITY of WASHINGTON



清华大学

Tsinghua University



UNIVERSIDAD TECNICA  
FEDERICO SANTA MARIA

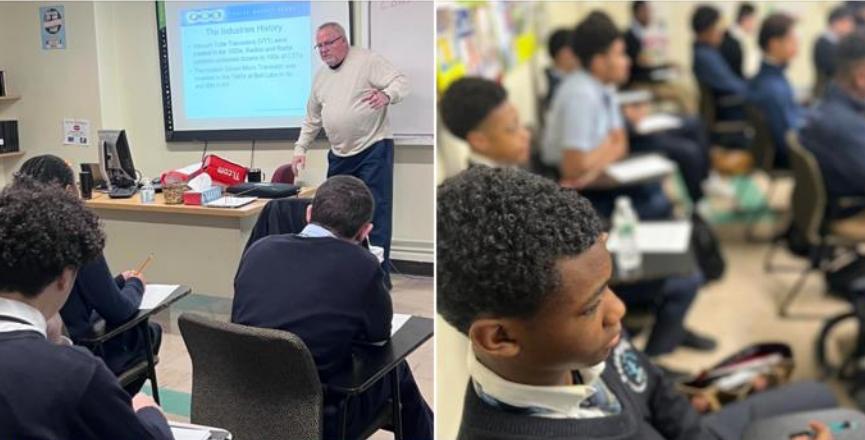


Northwestern  
University



Big things are happening at RCA!  
Lamar Hill, Executive Director of NYDesign and a member of the President's Office of NYCREATES meets with Redemption Christian Academy STEM students for a General session on IC design. This amazing opportunity to partner with NYDesign and NYSTEC for EFabless Chip Ignite, a STEM experiential learning chip design program, will open up high level academic and career pathways for RCA students!

#stemeducation  
#groundbreakers



## High Schools



2024/Sep/01

In other exciting news, Professor JB Koo, our newest Electrical Engineering faculty member who joined us in August 2021 from Intel Corporation, has negotiated with [NYDesign](#). The facility supports microelectronic circuit fabrication for universities through industry partners like Google, IBM, SkyWater and efabless, among others. NYDesign has agreed to provide three tape-outs of 130 nm CMOS technology, one each in January, February, and April of 2023. Each of these individually would cost roughly \$10k so this amounts to nearly \$30k worth of industry-based microelectronic circuit fabrication experience for our electrical engineering students.

Recently, I have focused on securing the necessary funding to launch the new Computer Science Program and several months ago, with the help of Lou Manzione one of our trustees, I began an engagement with Bell Labs. Part of that engagement resulted in their donation of a stereo microscope, several high-performance oscilloscopes, a spectrum analyzer, and a function generator. In addition, the President of Bell Labs, Peter Vetter, will come to Cooper Union on October 27th to engage with faculty and students and give a lecture to the IEEE Student Branch. Additionally, I have had very promising meetings with the Director of the Simons Foundation Flatiron Institute Center for Computational Mathematics and the new head of the machine learning group to discuss the possibility of a joint Computer Science faculty appointment, similar to the one Professor Alice Pisani holds with the Center for Computational Astrophysics at Flatiron.

Finally, I encourage you to take some time to read the articles included in this newsletter. This is by far the largest newsletter to date, an indication of the vibrancy of all that is going on in the School of Engineering.

Thank you again for sharing your valuable time with me on Shoop's Stoop! It's an exciting time to be part of the Albert Nerken School of Engineering. I look forward to sharing additional updates in future editions.

Barry L. Shoop, Ph.D., P.E. | Dean of Engineering

Tags: [Barry L. Shoop](#)

## Universities



Jun-ichi OKAMURA  
SSDM 2024 Short Course 2

## Mohawk Valley students get chance to design future semiconductors

 **Steve Howe**  
Observer-Dispatch  
Published 5:36 a.m. ET June 30, 2022



Some of the Mohawk Valley's bright young minds met for a workshop on microchip design in Rome on June 28.

The event, organized by NYDesign and hosted at New York State Technology Enterprise Corporation headquarters in Griffiss Business and Technology Park, brought in local students, including those from Mohawk Valley Community College, to learn about open source software to design microchips.

While semiconductor fabrication facilities continue to locate in upstate New York, including Wolfspeed in Marcy and Global Foundries in Malta, there's a missing component.

"The element that we don't have a huge amount of capacity around is the design of those integrated circuits," said Lamar Hill, executive director of NYDesign.

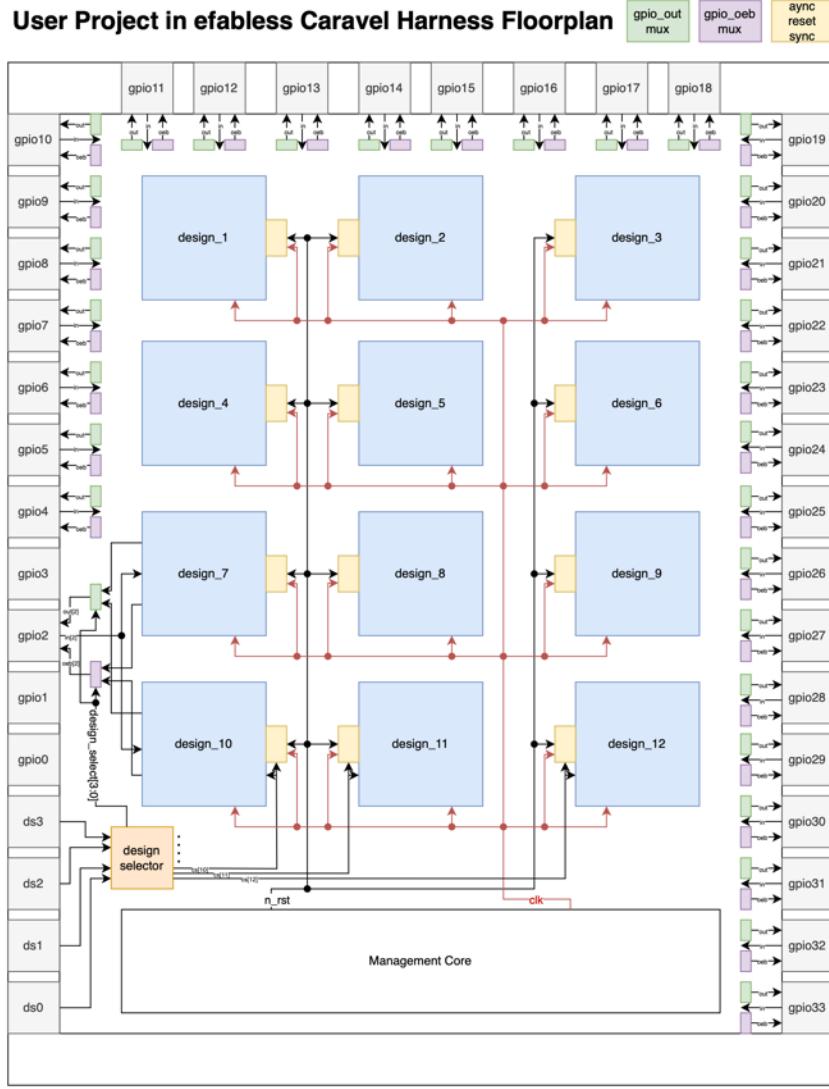


## Community Colleges

Attendees follow along with a live demonstration of open source chip design software at workshop at NYSTEC headquarters in Rome on June 28. Steve Howe / Utica Observer-Dispatch

The research and design aspect accounts for about half of the economic value of the industry, Hill said. The workshop on June 28 included hands-on sessions with efabless, a free chip design software that replicates more expensive programs usually only available at the graduate level.

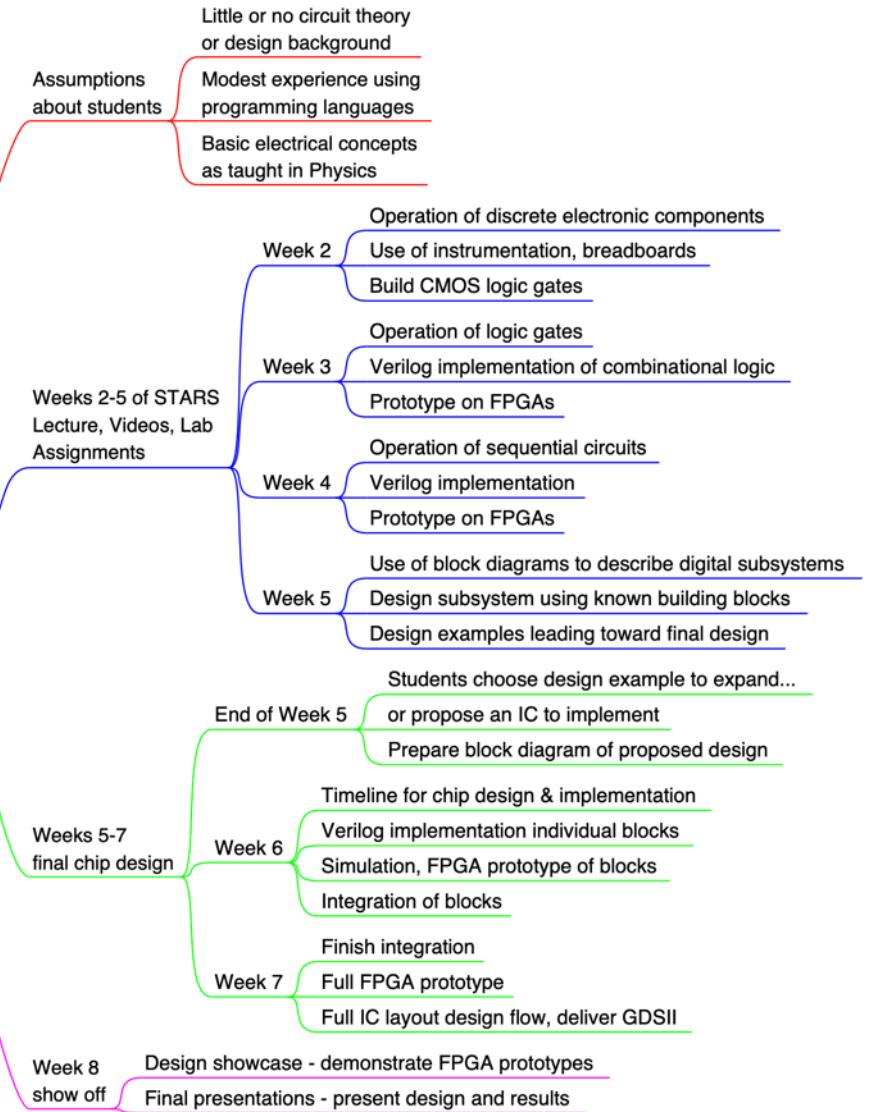
"By participating in this workshop they're going to be able to get access to actually putting designs onto silicon and be able to test them," Hill said.



50 Students  
12 Teams

12 Projects  
1 ASIC

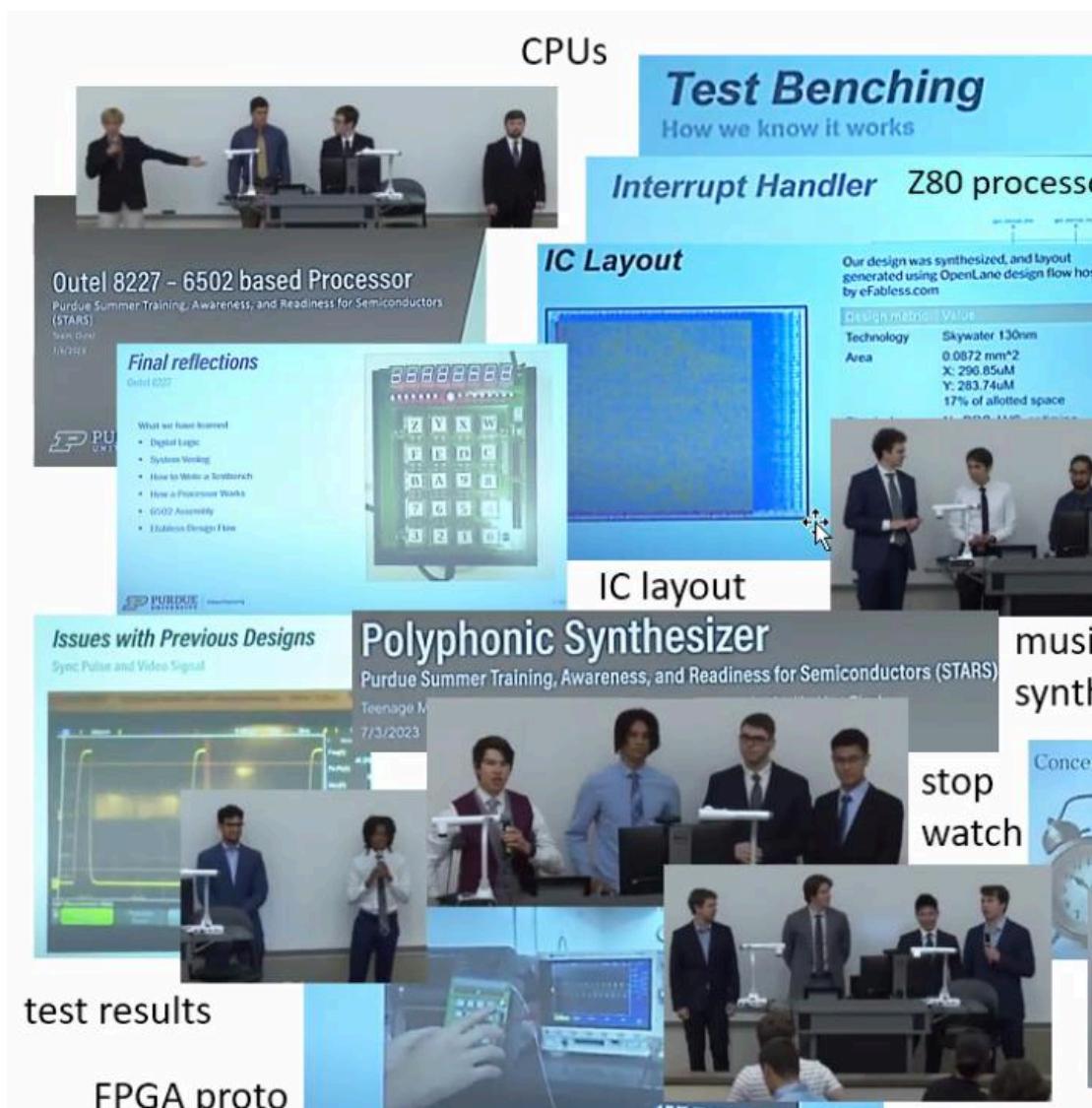
Courtesy of Mark Johnson at Purdue



# STARS

## Students Projects

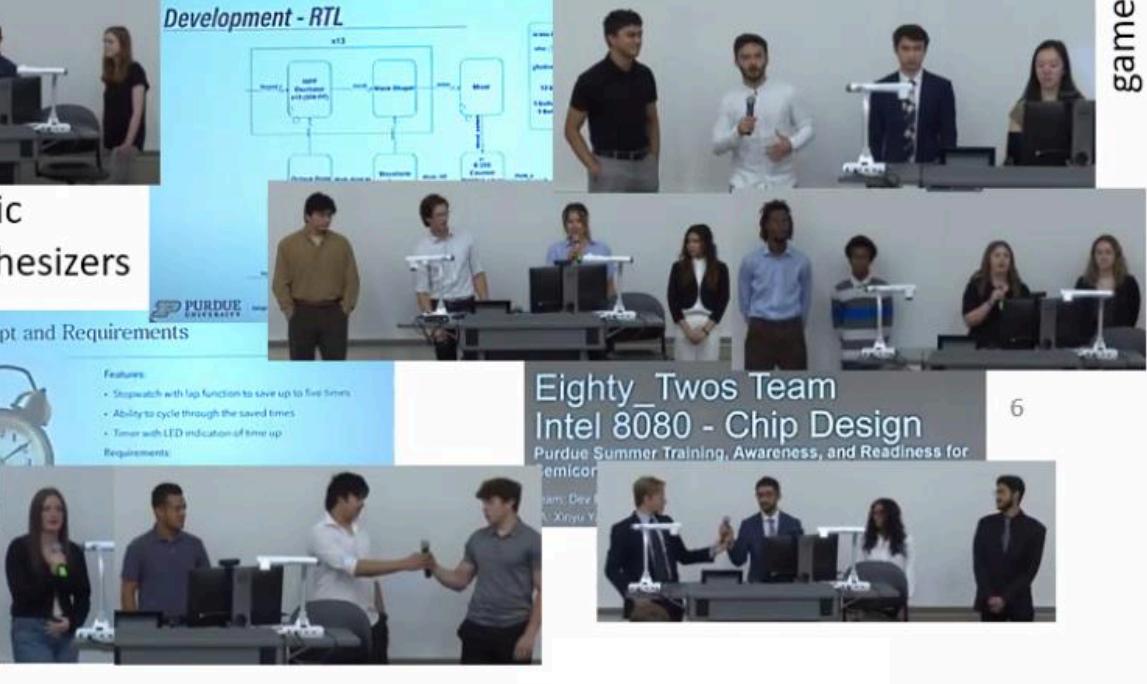
**CPUs**



**Design concept and requirements**



**music synthesizers**



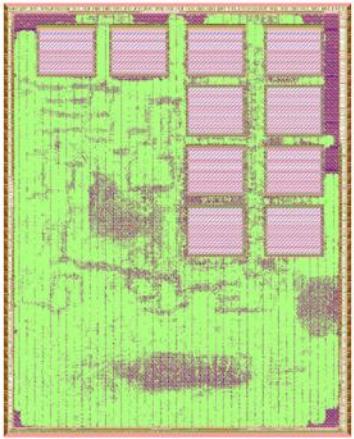
**games**



**test results**

**FPGA proto**

# OPEN SOURCE DESIGNS - STANFORD EE372



## Kairos: A Vector Processor for Error-State Extended Kalman Filter Acceleration

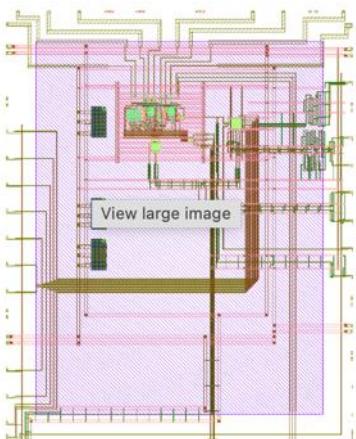
Jeffery Yu, Yuchen Mei

Code: [Design](#), [Caravel User Project](#)

Documentation: [Proposal](#), [Design Review](#), [Final Presentation](#), [Report](#)

Kairos is a SIMD single precision floating point vector processor, with instructions conforming to the RISC-V ISA. It implements operations such as vector fused multiply-add, matrix inversion, and matrix multiply-add, to efficiently accelerate error-state extended Kalman filter (ES-EKF) for trajectory estimation.

<https://priyanka-raina.github.io/ee372-spring2022/>



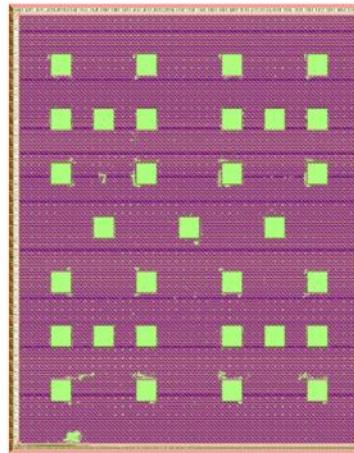
## 12-bit 10-KSPS Incremental Delta-Sigma ADC in Skywater 130 nm

Raymond Yang, Yaqing Xia

Code: [Design](#), [Caravel User Project Analog](#)

Documentation: [Proposal](#), [Design Review](#), [Final Presentation](#), [Report](#)

This project is a 12-bit 10 KSPS incremental delta-sigma analog-to-digital converter (ADC) designed for sensor interface and instrumentation applications. The ADC consists of a second-order incremental modulator and three post-integrators. The total area of the ADC is 0.55 square mm, with 0.53 square mm for analog modulator and 0.02 square mm for digital filter.



## Grapevine: An Asynchronous Numerical Classifier Using Sparse Grids

Leo Liu, Priyanka Dilip

Code: [Design](#), [Caravel User Project](#)

Documentation: [Proposal](#), [Design Review](#), [Final Presentation](#)

Grid-based numerical methods sample N-dimensional functions at regular intervals to produce an N-dimensional set of discrete "grid points". By breaking up grid points into hierarchical subgrids and eliminating subgrids above a certain hierarchy, one can obtain a sparsified grid space that reduces computational complexity.

Grapevine is a hardware accelerator for solving classification problems using the sparse grid approach. It supports up to 6 dimensions and 256 grid points. Each grid point is implemented using a single processing element (PE). An asynchronous network-on-a-chip overlays the PEs to provide low-latency multicast routing.



## Automated Analog Layout of Bandgap Reference Circuit

Yuetong Li, Xingyu Ni

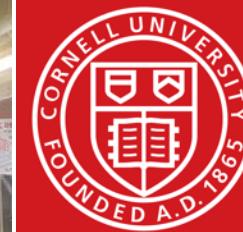
Code: [Design](#), [Caravel User Project Analog](#)

Documentation: [Proposal](#), [Design Review](#), [Final Presentation](#), [Report](#)

This project ports an automatic analog layout generation tool called aloe to work with SkyWater 130 nm technology. Aloe uses a digital place and route tool together with a genetic algorithm to meet different analog layout specifications. Using this tool, we generated several layouts for a bandgap voltage reference circuit on this chip, and we will compare these with a manually laid out version from the previous offering of this course.

# Cornell Custom Silicon Systems (C2S2)

<https://c2s2.engineering.cornell.edu/>



Cornell University®

Silicon CMOS chips are at the heart of every modern computing device from the smallest Internet-of-Things (IoT) device to the largest supercomputer. Unfortunately, undergraduate students currently do not have any opportunity to actually go through the process of fully specifying, designing, implementing, testing, fabricating, and evaluating a computer chip. **Undergraduates leave Cornell thinking that fabricating computer chips is only possible at huge companies like Intel, AMD, NVIDIA, and Apple.** Until recently, there was no realistic hands-on way for students to experience the complete computer chip design process. At the same time, exposing students to the beauty of computer chip design has never been more important, since the slowing of CMOS technology scaling means computer system designers must increasingly rely on specialized computer chips for continued improvements in performance and/or energy efficiency.

How can students (**from freshmen to seniors**) gain hands-on computer chip design experience? **The answer lies in the recent explosion in open-source chip design tools, open-source chip implementations, open-source process design kits, and low-cost computer chip fabrication services.** Just as open-source software has democratized software design, open-source hardware is poised to democratize hardware design.

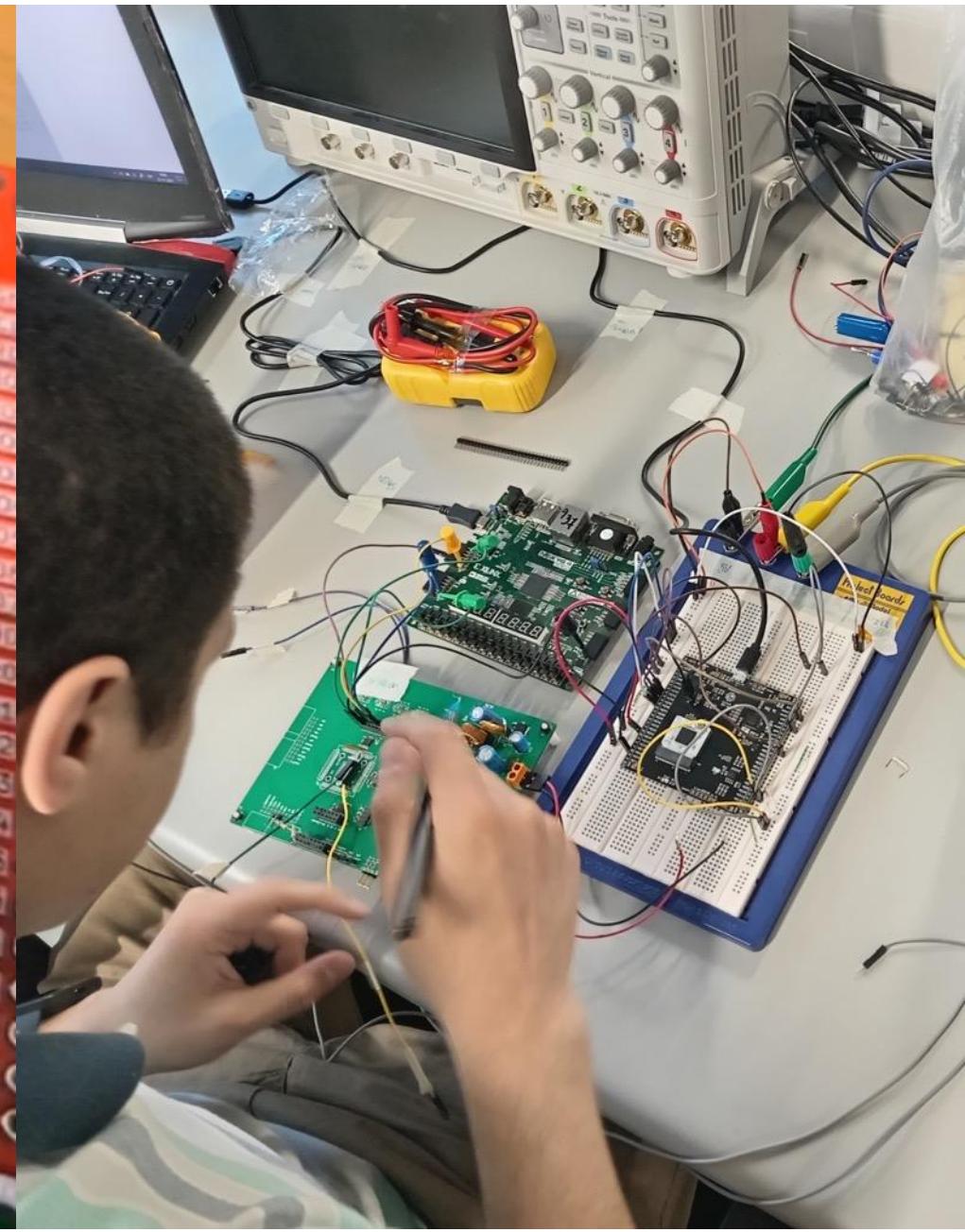
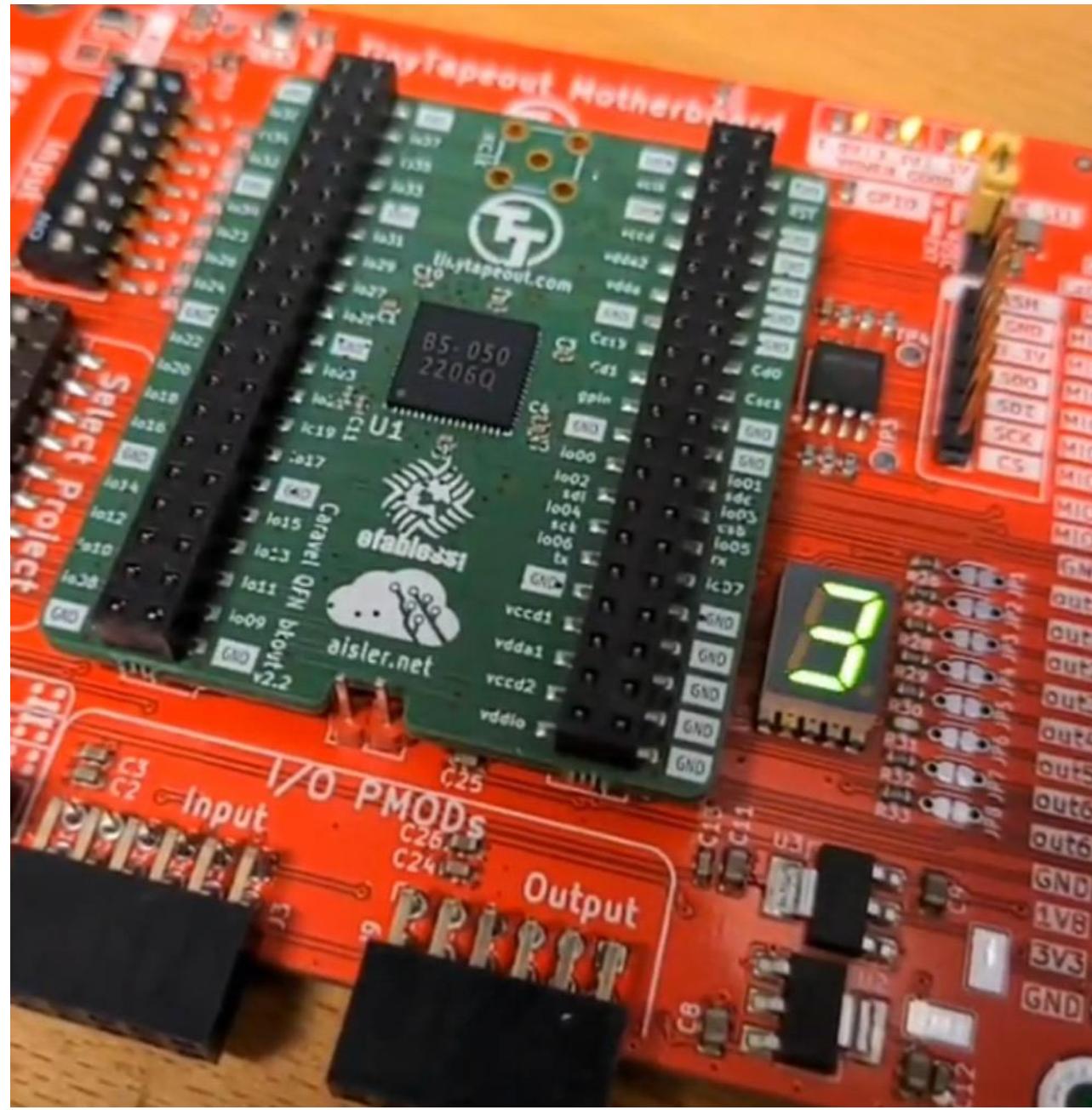
The **Cornell Custom Silicon Systems (C2S2)** Project Team ***leverages this emerging open-source hardware ecosystem to enable undergraduate students to specify, design, implement, test, fabricate, and evaluate custom computer chips.*** The final outcome will be a custom computer chip integrated on a custom circuit board with a complete software stack targeting an important application domain (e.g., ultra-low-power digital agriculture IoT). This ambitious student-led team is likely unique across US universities, and will hopefully inspire a new generation of computer system designers.

## New Course Summer 2023 - MIT Lincoln Labs - Beaver Works

[https://beaverworks.ll.mit.edu/CMS/bw/BWSI\\_Course\\_Listing](https://beaverworks.ll.mit.edu/CMS/bw/BWSI_Course_Listing)

### Microelectronics & Hardware Development *Summer Course*

Beaver Works Summer Institute will offer a brand new course on microelectronics and hardware development this summer. This course will provide students with an overview of how microchips, PCBs, and hardware systems are made and how they run the world. Students will receive hands-on experience on how to design and implement hardware systems using microcontrollers and develop useful electronics that can impact our daily lives. At the start of the summer, students will receive a basic hardware kit and can ask for additional items to be purchased so they can implement their own unique designs. No prior experience with hardware is necessary, and we encourage novices to participate.



# Not only for Google OpenMPW



**MPW-7**

Tapeout: Dec 05, 2022

[Summary](#)

[Projects](#)



**MPW-8**

Tapeout: Dec 31, 2022

[Summary](#)

[Projects](#)



**GFMPW-0**

Tapeout: Dec 05, 2022

[Summary](#)

[Projects](#)



**GFMPW-1**

Tapeout: Dec 11, 2023



**IEEE SSCS Pico 2021**

Tapeout: Jun & November 2021



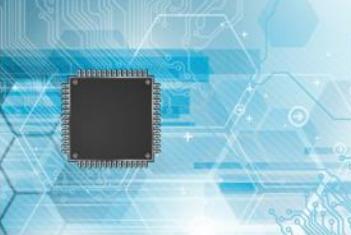
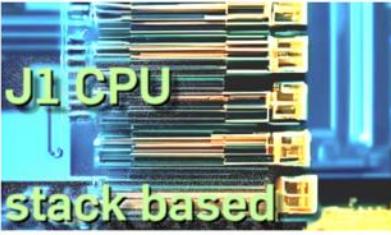
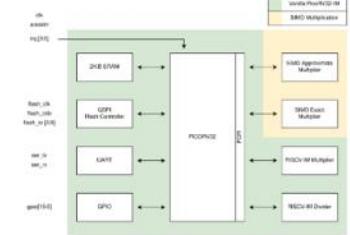
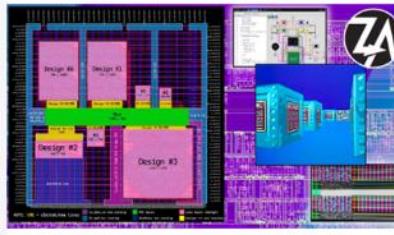
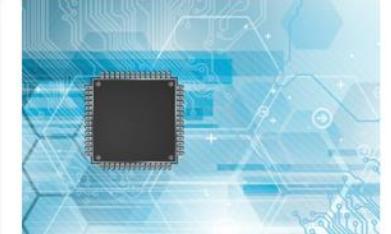
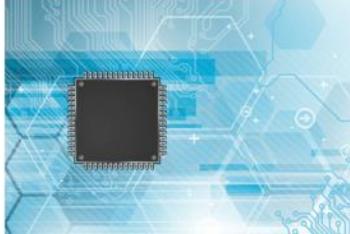
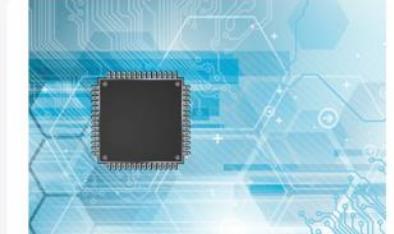
**IEEE SSCS Pico 2022**

Tapeout: Nov 2022

Made possible with Efabless' chipIgnite

ojects

# There are over 700 taped-out projects

			
<b>Encryption_Algorithm</b> <small>public</small>	<b>J1Asic_GF180</b> <small>public</small>	<b>picosoc-w-approximation</b> <small>public</small>	<b>ztoa-team-group-caravel</b> <small>public</small>
MengCheng DES encryption & decryption	Thorsten Knoll   <a href="https://github.com/ThorKn/J1Asic">https://github.com/ThorKn/J1Asic</a> This is the reimplementation of a tiny stack based CPU, named J1. Stack based CPUs were used a...	Luke Vassallo Picorv32-IM with exact and approximate SIMD multiplication extensions. The SIMD modules can be...	Anton Maurovic Multiple muxed designs/experiments assembled by Zero to ASIC Course participants (GFMPW-1)
<small>GFMPW-1 GF180MCUD</small>	<small>GFMPW-1 GF180MCUD</small>	<small>GFMPW-1 GF180MCUD</small>	<small>GFMPW-1 GF180MCUD</small>
			
<b>lfd111x_rvcore</b> <small>public</small>	<b>Multi_Designs_Custom_HW</b> <small>public</small>	<b>Advanced_Encrypti...</b> <small>public</small>	<b>Simple_Filter_Design</b> <small>public</small>
Nicholas Phipps Single Cycle (almost complete) RV32I written in TL-Verilog from LFD111x	M Naveed Coming Soon	Hisham Elreedy Advanced Encryption System (AES) Accelerator	K A Gaganashree   <a href="https://github.com/hw-user0/caravel-efabless.git">https://github.com/hw-user0/caravel-efabless.git</a> Simple Design Implementation of FIR Low Pass Filter and Moving Average
<small>GFMPW-1 GF180MCUD</small>	<small>GFMPW-1 GF180MCUD</small>	<small>GFMPW-1 GF180MCUD</small>	<small>GFMPW-1 GF180MCUD</small>

## Made possible with Efabless' chipIgnite

334

# Activities in Academia

The screenshot shows the ETH Zurich EFCL Summer School website. The main navigation bar includes links for About Us, People, News & Events, Education, Research, Media, and EFCL Summer School. The current page is 'Track 1 - Digital IC Design with Open Source EDA Tools'. The page features a large image of a printed circuit board (PCB) with various electronic components. The text on the page discusses digital IC design with open-source EDA tools.

The screenshot shows the IEEE SSCS "PICO" Open-Source Chipathon page. The header includes the IEEE logo and the text "IEEE Solid-State Circuits Society". The main title is "SSCS ‘PICO’ Open-Source Chipathon". The page has a red header and a white body with text and links related to the chipathon.

The screenshot shows the University of Michigan ECE (Electrical & Computer Engineering) website. The main navigation bar includes links for About, Academics, Research, People, Culture, News, and Events. The article title is "Open-source hardware: a growing movement to democratize IC design". It features a photo of Dr. Mehdi Saligane and quotes from him.

The screenshot shows the IEEE SSCS "Code-a-Chip" Travel Grant Awards page. The main title is "IEEE SSCS ‘Code-a-Chip’ Travel Grant Awards". The page features a large image of a PCB and text about the awards at the 2024 IEEE Symposium on VLSI Technology & Circuits. It also includes a section titled "Program Rules".

## Open-source hardware: a growing movement to democratize IC design

Catherine June • December 22, 2022

**Dr. Mehdi Saligane**, a leader in the open-source chip design community, was among the first researchers to fabricate a successful chip as part of Google's multi-project wafer program.

The University of Michigan is part of a growing movement to make integrated circuits (IC) or chip design more accessible by providing open-source process design kits (PDKs), EDA tools, and building blocks. Chips developed from these design kits are now also invited to be fabricated at no cost to the developer thanks to a [cooperative research agreement](#) between the U.S. Department of Commerce's National Institute of Standards and Technology (NIST) and Google.



"The goal is to lower the barrier and access to silicon," said research scientist Mehdi Saligane, "and at the same time allow people to push the limit of what can be done."

Saligane has been at the forefront of open-source chip design and provides a unique perspective on the program, which is currently funding his own research. Parts of Saligane's research focus on cloud-based data-driven circuit optimization, which leverages modern software practices into chip design. Open-

VLSI Exercises - Antalya

Not Secure antalya.ethz.ch/index.php/VLSI\_Exercises

Google 検証 プライベート Trigence関係 AISOL ニュース 投資・銀行 業務検索 特許関係 規格 設計会社 電気工作 情報源 DnoteLR UJC EDA tools

Antalya VLSI Unix Presentations About

Login / Create Account Search Antalya Edit

## VLSI Exercises

VLSI Lectures

We have prepared a series of exercises for our VLSI course at [ETH Zurich](#).

### Open source vs proprietary tools

Our goal is to deliver this course using *entirely open-source tools*. However there are still some practical challenges and some parts of the flow are not yet (*in our experience*) ready for deployment in teaching. As open source alternatives mature, we will be replacing these gradually.

### Setup

We use the excellent VM for [IIC-OSIC-TOOLS](#) provided by Institute for Integrated Circuits (IIC), Johannes Kepler University (JKU).

If you are using the infrastructure at ETH Zürich, these tools have already been made available.

### Schedule

Exercise	Name	Files	Tools
1	Simulation flow	<a href="#">ex1.tar.gz</a>	Verilator, Siemens/Mentor Questasim
2	RTL, understanding/extending Croc	<a href="#">ex1.tar.gz</a>	
3	Synthesis	<a href="#">ex1.tar.gz</a>	Yosys
4	Block diagrams	<a href="#">ex1.tar.gz</a>	
5	Overview of the flow	<a href="#">ex1.tar.gz</a>	OpenROAD
6	Floorplanning	<a href="#">ex1.tar.gz</a>	OpenROAD
7	Placement / Timing	<a href="#">ex1.tar.gz</a>	OpenROAD
8	Understanding clock tree	<a href="#">ex1.tar.gz</a>	OpenROAD
9	Routing / Finishing	<a href="#">ex1.tar.gz</a>	OpenROAD
10	Power analysis	<a href="#">ex1.tar.gz</a>	OpenROAD
11	DRC / LVS	<a href="#">ex1.tar.gz</a>	Klayout, Siemens/Mentor Calibre

VLSI Lectures - Antalya

Not Secure antalya.ethz.ch/index.php/VLSI\_Lectures

Google 検証 プライベート Trigence関係 AISOL ニュース 投資・銀行 業務検索 特許関係 規格 設計会社 電気工作 情報源 DnoteLR UJC EDA tools

Antalya VLSI Unix Presentations About

Login / Create Account Search Antalya Edit

## VLSI Lectures

VLSI Exercises

The VLSI2 lecture at [ETH Zürich](#) covers aspects of modern digital IC design supported by [VLSI Exercises](#).

### Schedule

Lecture	Name	Topics	Slides
1	Intro	Summary of design flow, cost of IC design, case for open source EDA	<a href="#">ethz_vlsi_lec1.pptx</a>
2	RTL	Refresher on SystemVerilog, a few words on computer architecture, our example design Croc	<a href="#">ethz_vlsi_lec2.pptx</a>
3	Netlist	Logic synthesis, standard cells, other macros, refresher on timing	<a href="#">ethz_vlsi_lec3.pptx</a>
4	ICT	Short summary of IC manufacturing	<a href="#">ethz_vlsi_lec4.pptx</a>
5	LEF	Standard cell structure, routing layers, parasitics	<a href="#">ethz_vlsi_lec5.pptx</a>
6	DEF	Floorplan, I/O ring, ESD structures, packaging	<a href="#">ethz_vlsi_lec6.pptx</a>
7	LIB	Timing, clock trees, corners	<a href="#">ethz_vlsi_lec7.pptx</a>
8	SDF	Parasitics, extraction, issues in timing, crosstalk, noise margins, supply droop, ground bounce	<a href="#">ethz_vlsi_lec8.pptx</a>
9	GDS	Placement, routing, chip finishing, DRC/LVS	<a href="#">ethz_vlsi_lec9.pptx</a>
10	VCD	Power analysis, static vs dynamic power, IR drop, analysis methods, DVFS	<a href="#">ethz_vlsi_lec10.pptx</a>
11	WGL	Motivation for test, Fault models, ATPG, BIST, JTAG	<a href="#">ethz_vlsi_lec11.pptx</a>
12	PPA	Reporting power, performance, area properly	<a href="#">ethz_vlsi_lec12.pptx</a>

The VLSI pages are part of the open source VLSI design course offered by the [Integrated Systems Laboratory](#) of ETH Zürich, by Luca Benini and Frank K. Gürkaynak. See full list of [contributors](#).

Category: VLSI

<http://antalya.ethz.ch/index.php/VLSI>

# OpenPDK Team at iHP



The screenshot shows the iHP website's navigation bar with links to English, Deutsch, and other sections like Research, Services, Joint Labs, News, Career, and About Us. The main content area features a red 'ihp' logo and the text 'Leibniz Institute for High Performance Microelectronics'. Below this, a breadcrumb navigation path leads to the 'Open Source PDK' page.

← Post

 Flo  
@FlorianWoh

Now Frank of IHP a German research Fab who recently provided a new open source PDK is giving an overview how to TO your BiCMOS devices.

#PDK #IHPgmbh #tapeout #germany #coscup

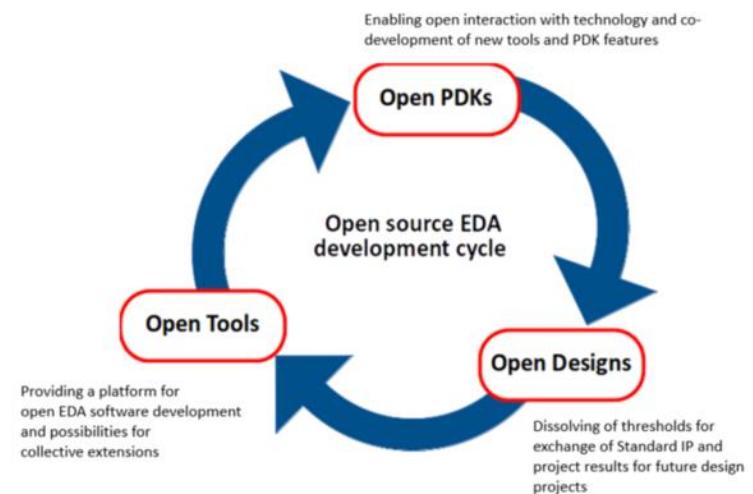
IHP's Open Source PDK

- Internal discussion:
  - > Should we release an open source PDK?
  - > Which technology?
- Announcement on FSCC 2022 to release an open source PDK for IHPs 501302
- 501302 BiCMOS technology: HBT  $f_{T, \text{max}} = 350/450$  GHz and CMOS in 130nm
- First technical data published in March 2023
- Here: [https://github.com/IHP-GmbH/IHP\\_Open\\_PDK](https://github.com/IHP-GmbH/IHP_Open_PDK)
- 362 commits until yesterday

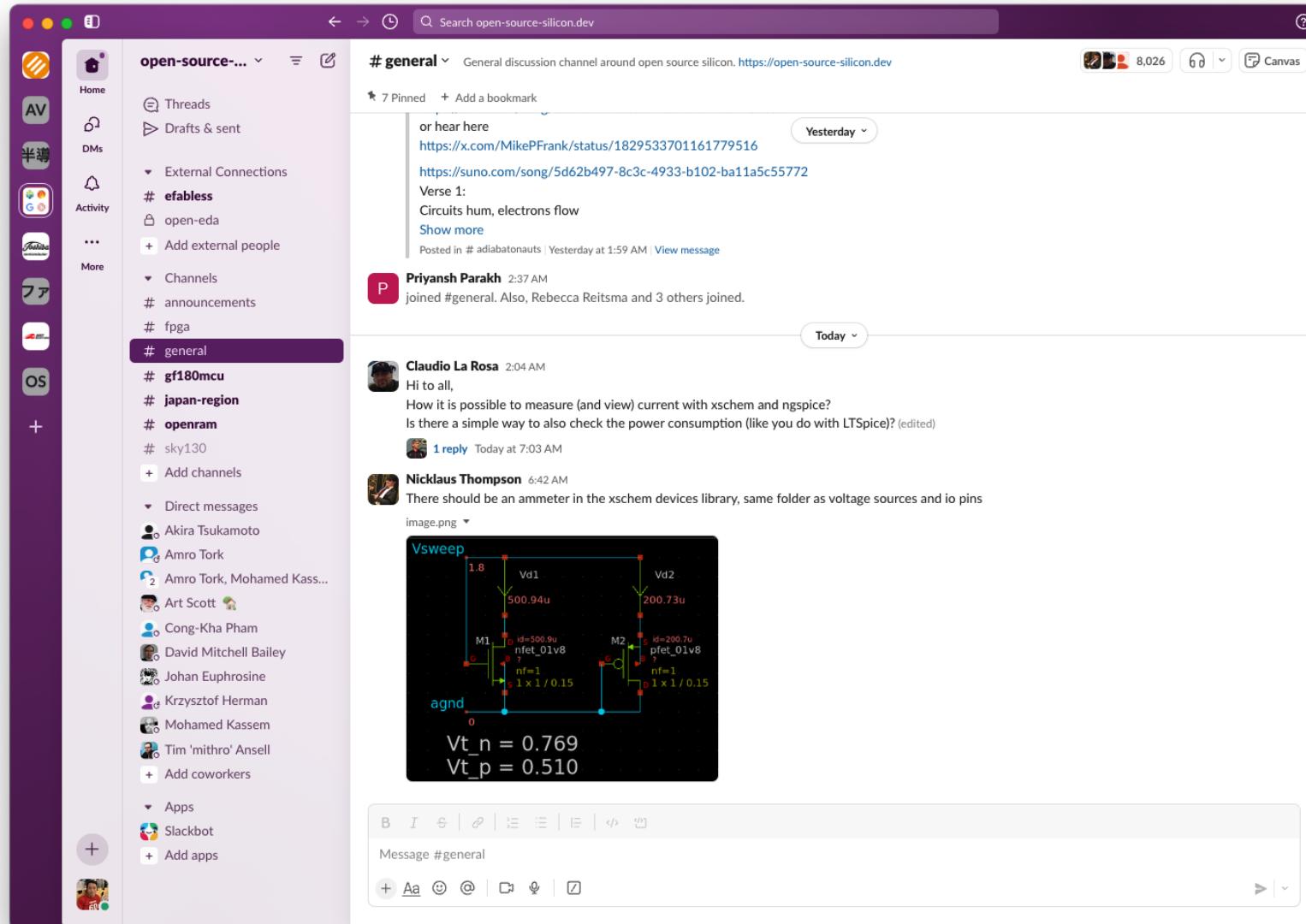
Silicon-Proven IP Cores

- > Development of Standard Cell Library
- > Establishing IP Core Library with silicon-proven designs
- > Offering free MPW runs with first Open Community Run May 2024 (TSMC)
- > Free for designers and developers, funded by funding project
- > Tape Out via European partners
  - > STMicroelectronics
  - > Infineon Technologies
  - > ST Microelectronics
  - > KIT Karlsruhe
  - > Uni Linz Austria
- > GitHub: [https://github.com/IHP-GmbH/IHP\\_Open\\_Designs](https://github.com/IHP-GmbH/IHP_Open_Designs)
- > Next run in November 2024

Open Source PDK in 130nm BiCMOS, developed for Analog/Digital, Mixed Signal and RF ASIC Design



# Slack Community

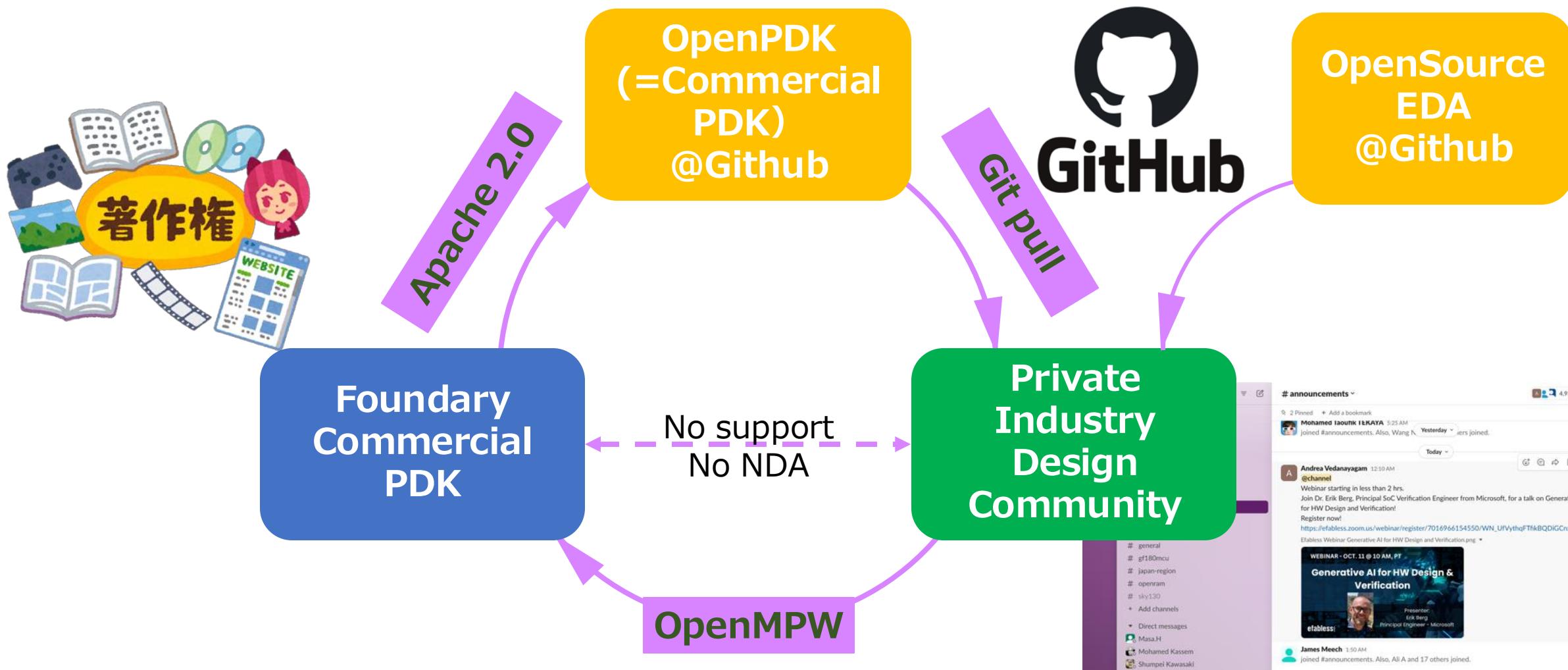


2024/Sep/1  
8,026 members

# How it works in eco-system?

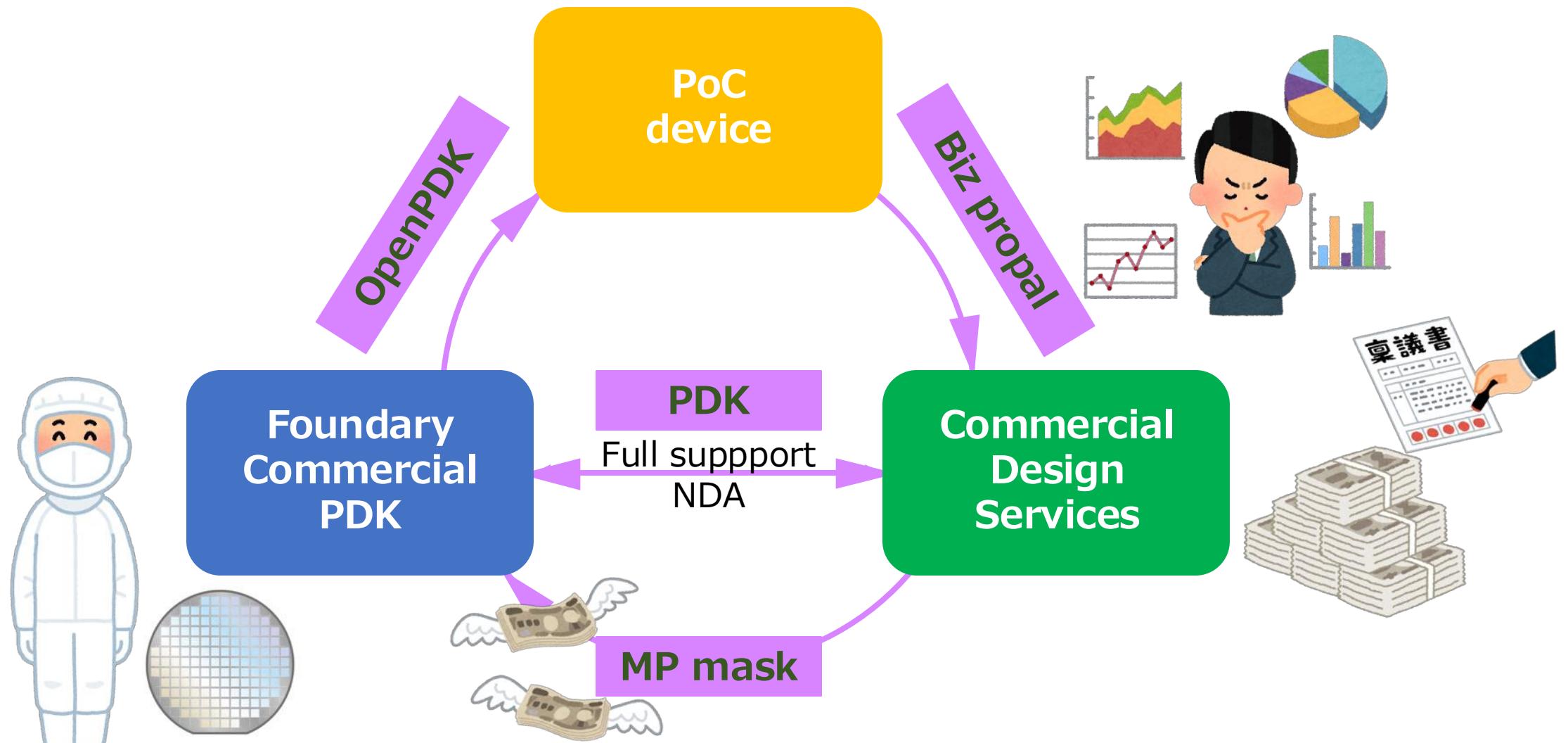


# How Open Source Silicon works in eco-system?



Anyone can freely download the PDK and design chips.  
The fab incurs no new investment or support obligation.

# How Open Source Silicon works in eco-system?



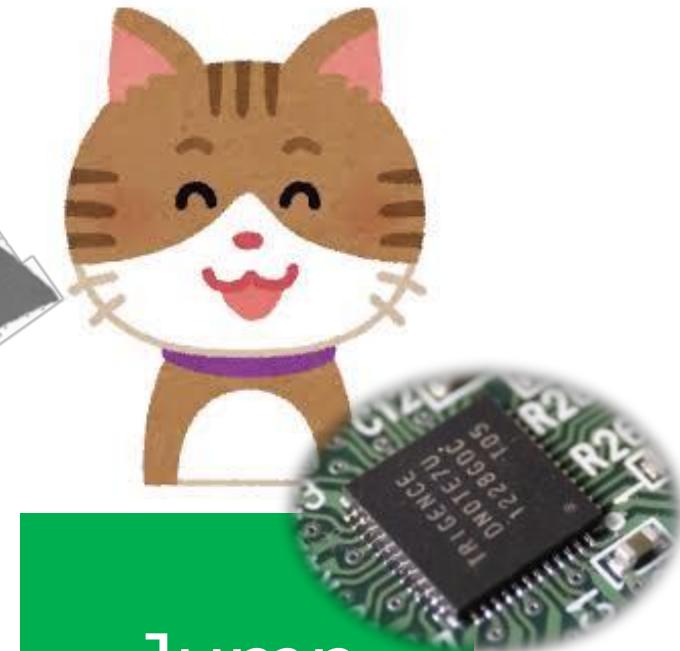
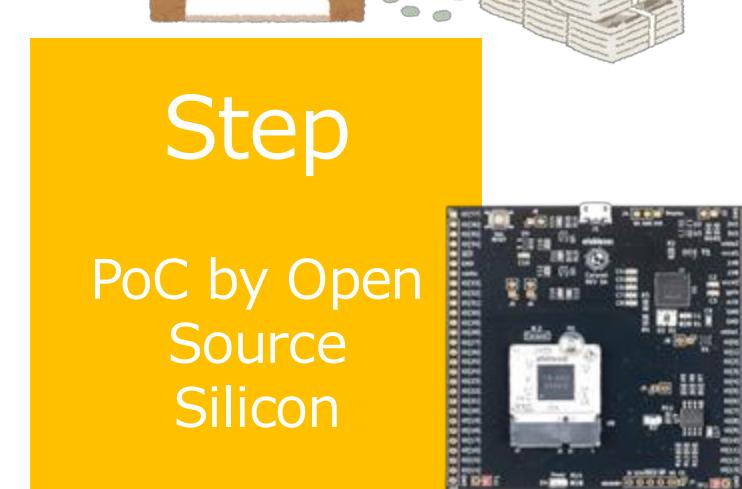
This enables seamless production deployment from PoC products.  
Commercial use of PDK is supported by dual licensing.

# How Open Source Silicon works in eco-system?

This can be lowering the entry wall to encourage chip development and success..



Hop  
Idea



Jump

MP by  
NDA and  
commercial  
tools

# What is the OpenSUSI intention?



# Open Source Utilized Silicon Initiatives

Encouraging **diverse industry sectors** to leverage semiconductor advancements by establishing pragmatic design and manufacturing platforms

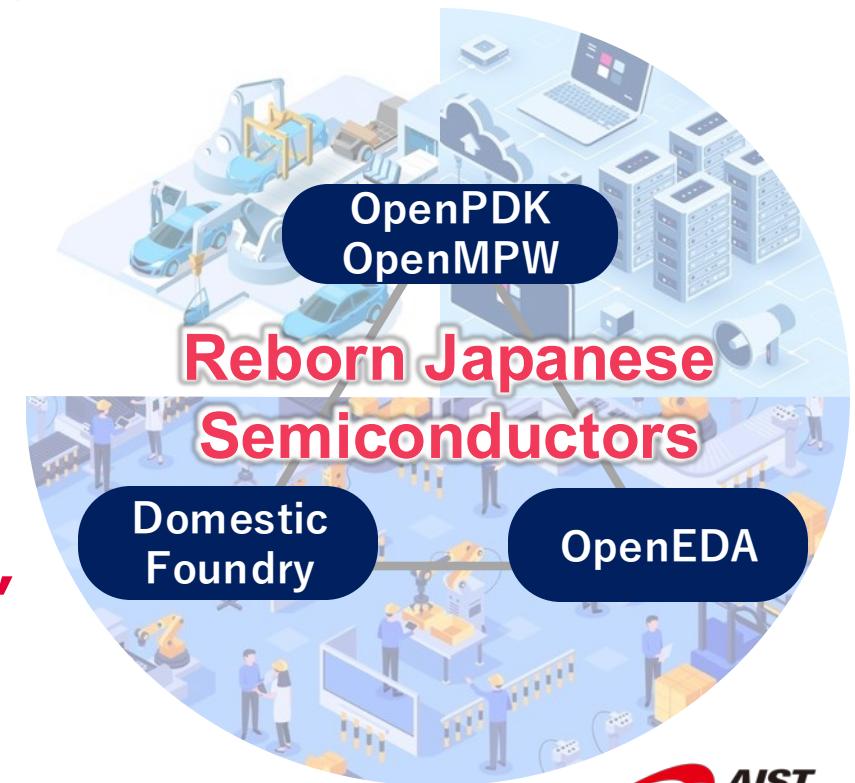


Open Source Silicon for Japan

As an AIST Solutions Business Design platform

**“Accelerate of real users and actual demands”**

Collaborate with domestic foundry + Google to achieve PoC



# Target Users



## Embedded device development company

Board development using commercial semiconductors and FPGAs. Want to convert to ASICs to compete and differentiate from overseas companies, but development costs are an issue

## Software development company

Developing IoT-related software and devices that use CPUs and GPUs. Want to develop ASICs for differentiation through low power consumption and miniaturization, but development costs are an issue.



## Industrial equipment development company

Developing equipment using commercial semiconductors and FPGAs. Want to convert to ASICs to differentiate from overseas companies, hide technology, and improve performance, but development costs are an issue.

The "target" companies are those that are not strong enough to develop their ASICs by installing expensive commercial EDA tools. The purpose is not to change the design method from a commercial to an open tool. It provides a platform that enables organizations or companies that have not been able to afford commercial EDA tools to conduct a PoC to differentiate their products by ASICs.

# Purpose and Article

## Open Source Utilized Silicon Initiatives (OpenSUSI) purpose

OpenSUSI was established to provide an environment for the industry that allows long-tail chip users to compete with dedicated semiconductors by Japanese domestic semiconductor assets (chip manufacturing capacity) into a platform that lowers the barriers to entry for original chip design.

We believe that open-source EDA tools and the Open Source Silicon ecosystem can contribute to the competitiveness, innovation, education, independence, cyber resilience, and environmental sustainability of the semiconductor industry and that the OSS has not only economic benefits but also social benefits that extend throughout the industry. We believe the development and evangelization of this activity is our mission.

### 【Article】

1. Planning, development and provision of open source PDK (design information) for semiconductors.
2. Provision of open source or economically fair price semiconductor prototyping services.
3. Planning and operation of Open Source Silicon design communities and human resource development through these communities.
4. Accumulation and disclosure of semiconductor open source PDK (design information) know-how.
5. Development, management and protection of intellectual property rights related to semiconductors.
6. Planning and operation of lectures, exhibitions, symposiums and seminars, production and sales of books, magazines and printed materials.
7. Exchange of information and cooperation with domestic and foreign institutions, organizations, research institutes, and educational institutions related to semiconductors.
8. Other activities necessary to achieve the objectives of the society.



# The key relationship and eco-system



**efabless**.com

**Google**

**NSW**

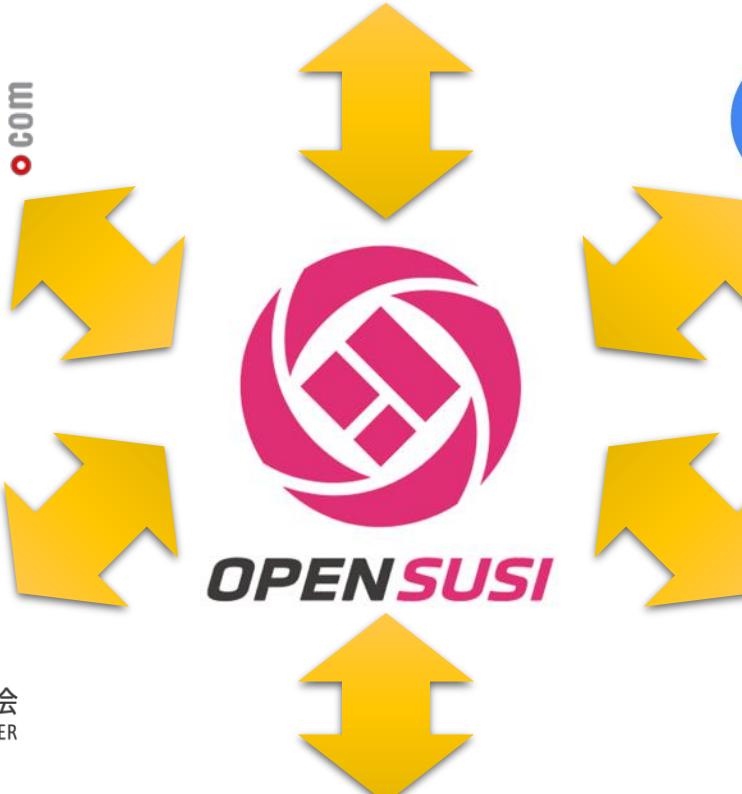
一般社団法人  
**組込みシステム技術協会**  
Japan Embedded Systems Technology Association

**JEITA**

**JEDAT**  
Japan EDA Technologies

ふくおか  
**iST**  
FUKUOKA INDUSTRY, SCIENCE & TECHNOLOGY FOUNDATION  
ふくおかアイスト  
公益財団法人 福岡県産業・科学技術振興財團

公益財団法人 九州経済調査協会  
KYUSHU ECONOMIC RESEARCH CENTER



**AIST**

**経済産業省**  
Ministry of Economy, Trade and Industry

**文部科学省**  
MINISTRY OF EDUCATION,  
CULTURE, SPORTS,  
SCIENCE AND TECHNOLOGY-JAPAN

**AIST  
SOLUTIONS**

**AIST  
SOLUTIONS**

# Domestic Community (ishi-kai.org)

Finished Events



2024/08/11 (Sun) 13:00~

47/72

2024年08月イベント：初めての半導体設計・製造体験 for ISHI会のOpenMPW

Noritsuna Imamura

東京都渋谷区道玄坂1丁目2番3号 渋谷クラス



2024/08/04 (Sun) 13:00~

8/20

ゆるゆるイベント：フェニックスシャトル最終サポート雑談会

Noritsuna Imamura

秋葉原駅



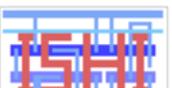
2024/06/22 (Sat) 22:00~

48/100

2024年6月イベント「オープンソースEDA開発者苦労話勉強会」

Noritsuna Imamura

(場所未定)



2024/05/06 (Mon) 13:30~

77/150

2024年5月イベント「ISHI会一周年記念イベント～大討論会～」東京会場&オンライン

Noritsuna Imamura

東京都渋谷区道玄坂1丁目2番3号 渋谷クラス



2024/05/06 (Mon) 13:30~

5/20

2024年5月イベント「ISHI会一周年記念イベント～大討論会～」福岡会場

Noritsuna Imamura

福岡市中央区天神1丁目15-30



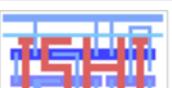
2024/04/04 (Thu) 19:00~

45/130

2024年4月イベント「オープンソースPDK団体」勉強会

Noritsuna Imamura

東京都港区西新橋1-1-10F



2024/03/20 (Wed) 13:00~

11/100

Chipathon2023 ADCチームキックオフイベント

Noritsuna Imamura

(場所未定)

ishikai.org/about/

## の説明

本会は、ISHI会（Inter-linked Society on Homemade IC Kai）と命名されました。オープン化（民主化）されたISHI=石=Silicon=半導体（ASIC/LSI/IC）を扱い、いろいろな分野を繋げていくソサエティー・コミュニティー（会）から発想されたネーミングです。

その先駆けとして登場したOpenMPW（Open Multi Project Wafer）は、Google社がEfabless社に出資して生まれたシャトルプログラムであり、半導体（ASIC/LSI/IC）を作れるうえで必要なツール（EDA/PDK）からファブまでのISHI製造まで含めて、すべてオープン＆無料で半導体（ASIC/LSI/IC）やEDA/PDKを製造することができるプログラムです。これはまさにGNUから始まったオープンソースムーブメント（ソフトウェアの民主化）の「半導体（ASIC/LSI/IC）やEDA/PDKのオープン化」であります！

そこで、本会は、これまでの半導体（ASIC/LSI/IC）の専門家だけではなく、これからの半導体（ASIC/LSI/IC）のオープンソースムーブメントに可能性を見出した人たちと新しい半導体（ASIC/LSI/IC）を作りたい人たちにスポットを当てたユーザソサエティー・コミュニティー（会）として立ち上がりました。

専門家だけが利用可能だったOSやコンパイラ、ライブラリ、アプリ、電子基板、3D CADや3Dプリンターがオープンソースソフトウェア、オープンハードウェア、オープンモデリングなどとして誰もが利用できるようになったように、半導体（ASIC/LSI/IC）やEDA/PDKを誰もが利用できる世界を目指して活動していく所存です。

今後の活動方針としては、他分野の人たちを巻き込んで半導体（ASIC/LSI/IC）分野に革命を起こすという方針で、他分野向けの超初心者向けハンズオンセミナーや専門家向けの濃い内容の勉強会などのイベントを開催したり、チームを作ってOpenMPWシャトルや世界のChipathonに挑戦したり、Maker Faireなどのイベントへの参加をしていきたいと思いますので、よろしくお願ひいたします。

◦ 結成呼びかけ資料

### ISHI会グランドデザイン

#### Our Stars

新規分野を開拓したい  
けどどうすればよいのかわからない

ASIC(LSI)化したい  
けど情報がない

「みんなの経験をチップに！」

ASIC(LSI)業界の現状（閉塞感）

- NDAでなにもしゃべれない
- 最先端は札束の応酬
  - 若者が入ってこない

他業界の現状（限界感）

- 高速・小型・省電力の要求
  - 汎用チップ+ソフトでは限界

OpenMPWの登場！  
すべてがオープン！

コミュニティーの意義

- 成果の再利用が可能。Do It With Others(それ、みんなでやってみよう)の精神
- 日本の利点：地理的に物理的に集まりやすく、勉強会や合宿をやりやすい

ISHI会の意義

- 他（多）分野の知識の統合により、今までになかった研究・開発への期待

2024/Sep/01



2023/05 Start  
~20 members

2024/Sep/1  
288 members

# Tiny Tapeout ( $\sim$ 1K Gate/\$300)

efabless.com

Products Solutions Resources Company Login or Signup

[TYE's Tech Lab.](#)  
TYE's Technology Laboratory

Home Profile Projects Teardown Column Blog

**Tiny Tapeout**  
Design Your First Chip for \$300

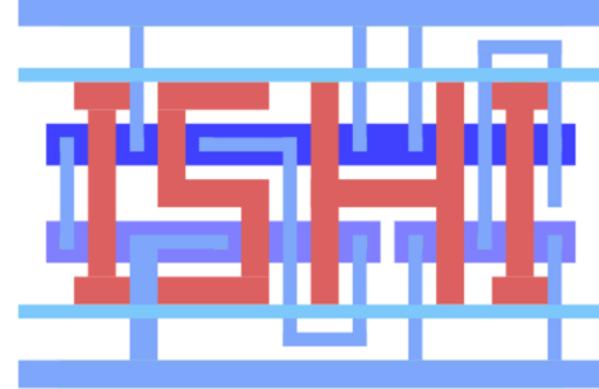
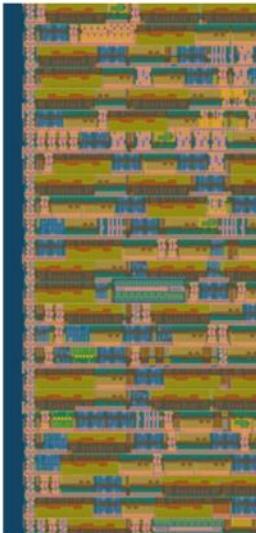
Learn to build your first chip quickly and affordably with Tiny Tapeout. This program is designed for students, makers, university members, or anyone curious about chip design. It provides access to the complex world of chip design and makes it accessible to everyone.

Purchase Tokens for Tiny Tapeout

Affordable Design Submission

Start your chip design journey for just \$300 (larger designs can be accommodated by request). What's included:

- Free Design Tools: Free access to design tools for implementing your project.
- Dedicated Tile Space: Get one tile offering 160x100um of area, and up to 1000 standard cells.
- Fabrication and Packaging: We take care of fabricating and packaging your creation, turning your digital designs into functional silicon. Submitting your design requires a GitHub public repo.
- Development Board: Receive a development board plus carrier board featuring your chip.



TYE's Tech Lab.  
TYE's Technology Laboratory

Home Profile Projects Teardown Column Blog

TinyTapeoutでオレオレICを作ろう

Sep 13 2023年シルバーウィーク特別イベント「TinyTapeout ハンズオン」勉強会

Organizing : ISHI会

Group

ISHI会  
Inter-linked Society on Homemade IC Kai

Number of events 16  
Members 322

Ended  
2023/09/13(Wed)  
21:00 ~ 22:00  
[Google Calendar](#) [iCal](#)

Registration Period  
2023/09/08(Fri) 00:00 ~  
2023/09/13(Wed) 20:00

[Event Organizer Contact](#)

広告

Microsoft Azure Bootcamp  
2024年9月10日(火) - 12日(木) 今すぐ登録

# Open Source Silicon Pros and Cons.



# Open Source Silicon Pros and Cons?

- Open Source EDA does not offer a complete toolchain, yet it provides sufficient functionality for PoC designs and educational purposes. For initial learning stages, understanding pre-manufacturable design readiness, such as DFT, DFM, and BIST, is not crucial. Similarly, detailed verifications including power integrity, signal integrity, and hot-spot detection are not fundamental.
- While these aspects are invaluable for the mass manufacturing of designs and are considered essential expertise within professional domains, gaining a broad understanding and hands-on experience with the basic design processes is more beneficial initially. This foundational knowledge is key for those just beginning in the field and provides a solid base for further specialization.

# Open Source Silicon Pros and Cons?

- As chip design increasingly caters to advanced applications such as AI and ML, traditional design flows using commercial EDA tools and their licensing models often fall short, particularly due to their inability to handle the massive computational requirements needed for building large learning models.
- Open Source EDA and PDK present viable alternatives that are well-suited to AI/ML approaches. The absence of license limitations and the transferable nature of these open-source resources can significantly accelerate the development of innovative design methodologies. This flexibility not only fosters greater creativity but also speeds up the adoption and implementation of new technologies in chip design.

# Open Source Silicon Pros and Cons?

- Open Source EDA offers a user-friendly approach that eliminates the VPN connections to high-performance EWS and license servers since no NDA requirements. This accessibility makes it ideal for individual users and facilitates remote collaboration directory over geometrical distances. Furthermore, Open Source PDKs are transferable and transparent, allowing community members, all designs can be easily downloaded and uploaded from anywhere via the Internet, enhancing global participation.
- Utilizing so-called legacy process technologies, the cost of MPW services remains reasonable, making it accessible for academia and small businesses. This affordability helps to broaden the semiconductor design resource pool, promoting greater innovation and participation in the field.

# Summary for Device and Materials



# Summary for Device and Material

---

- Open Source Electronic Design Automation (EDA) and Open Source Process Design Kits (PDKs) are critical platforms that support **the Open Source Silicon movement, an ongoing alternative trend in chip development.** This movement is gaining maturity, offering significant benefits such as IP portability, design reuse, as well as transparency in chip functionality, and traceability of design sources.
- While it is unclear the full impact this movement will have on device and material development, **I believe it is evident that it is influencing these areas as well.** As this trend evolves, it is crucial to maintain close communication to monitor and understand how it would be innovated.

# Contact



## AIST Solutions, Inc.

Producer, IEEE senior  
Jun-ichi OKAMURA

E-mail: [jun.okamura@aist-solutions.co.jp](mailto:jun.okamura@aist-solutions.co.jp)

LinkedIn:

<https://www.linkedin.com/in/jun-ichi-okamura-6b8bb2b/>

HP:

<https://www.aist-solutions.co.jp>



E-mail: [secretary@opensusi.org](mailto:secretary@opensusi.org)

LinkedIn:

<https://www.linkedin.com/company/opensusi/>

HP:

<https://www.opensusi.org>