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| TCP Title | Verification of AXI-I2S TX |
| Trainee Name | Muhammad Junaid |
| Manager | Rubab Fatima |
| Next Manager | Nouman Akbar |
| Tech Lead | Hassan Ashraf |
| Peer Mentor | Junaid Ahmed |
| Estimated time to complete | 1 month |
| Kickoff Date | |

TCP Description:

This project involves verifying the AXI I2S Transmitter Vivado IP. The trainee will be responsible for verifying all the features outlined in the IP's specification documents. The IP should be generated in Vivado with default parameters.


Acceptance Criteria:

The trainee needs to develop a UVM based testbench for verifying this IP completely. Implement the RAL model for the registers. The other deliverables are follows:

1. Git repository for project
2. Detailed Verification Architecture Document
3. Testplan
4. Coverage Model and Scores

Reference Material / Research Papers:

[Spec Document](#)

 [How to use AMD Vivado's IP Catalog to create a Block RAM](#) (generate your relevant IP similarly)

[Enable UVM in vivado.](#)

[Verification Plan](#)

[VAD workshop](#)

[AXI Spec](#)

[AMBA AXI-Stream Protocol Specification](#)

 [Coding Guidelines](#)