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DLD Project

4 BIT ADDER CIRCUIT

DECLARATION

It is declared that this is an original piece of my own work, except where otherwise acknowledged in text and references. This work has not been submitted in any form for another degree or diploma at any university or other institution for tertiary education and shall not be submitted by me in future for obtaining any degree from this or any other University or Institution.

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ABSTRACT

To create a 4-bit digital adder is the project. The team carefully selected the gates to satisfy the given cost function and made changes to the adder circuit, which was originally designed as a ripple-carry adder (RCA). For example, the initial 1-bit adder is now a Half Adder, which is faster and more energy-efficient. To achieve the necessary performance, gates are implemented using several logic families, taking into account each gate's capability and usage in the circuit.

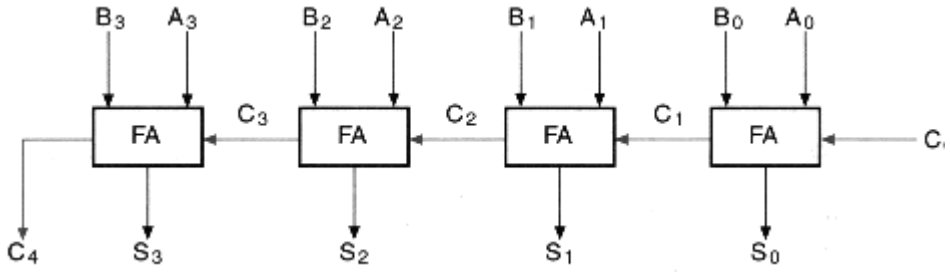
Chapter 1

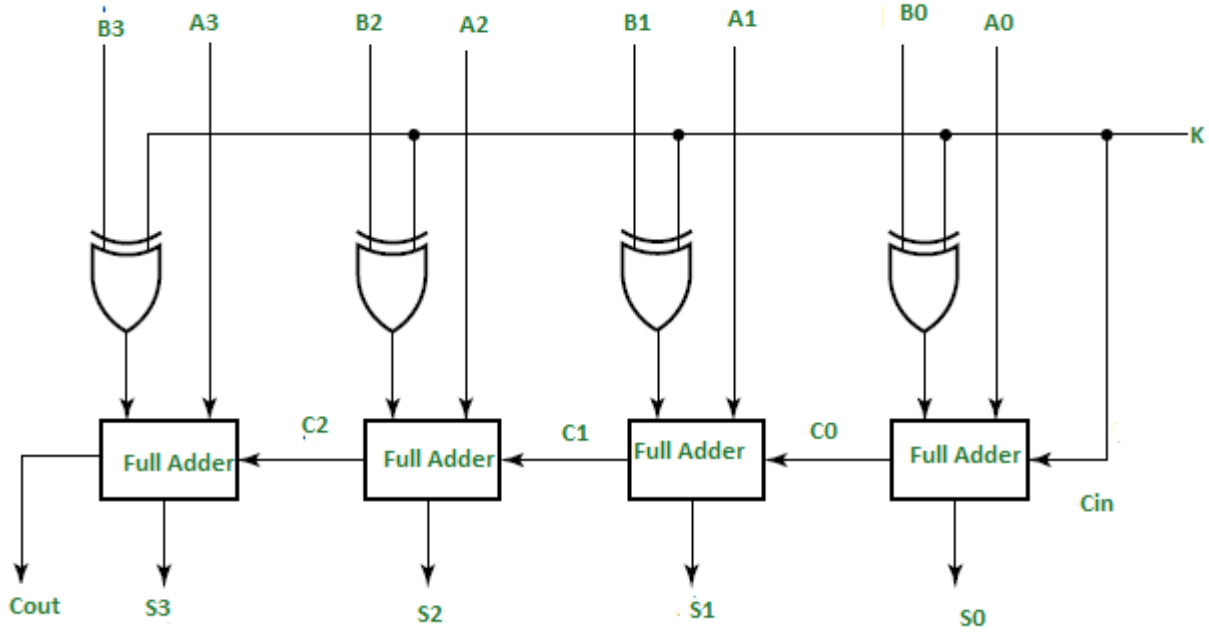
INTRODUCTION

The 'F283 is a complete adder that adds two binary words with a 4-bit length. Each bit has a sum () output, and the fourth bit produces the carry (C4) output as a result. It is possible to carry an end-around without using logic or level inversion.

1. Half Adder.
2. Full Adder.

A four bit complete adder is a logical circuit that accepts a carry signal and two expressions with four bits as inputs and outputs the four bits along with the carry signal at the output terminals.





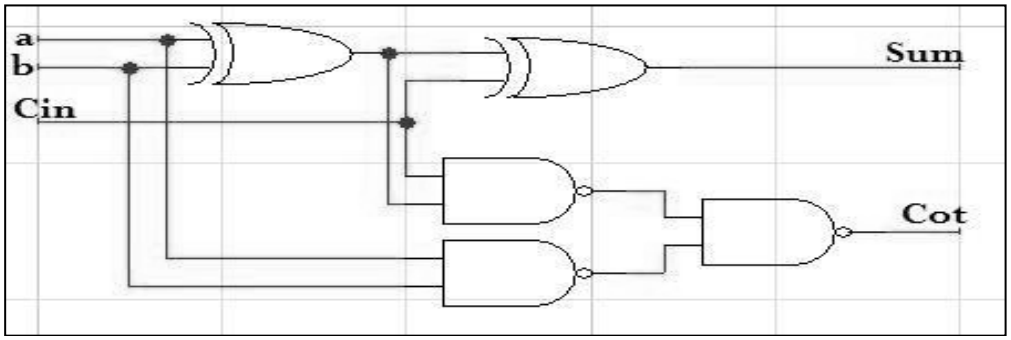
Implementation of the Full Adder at the Gate Level

This section provides a description of the 4-bit ripple carry adder's gate level implementation. It was critical to examine the existing gate level implementations for the complete adder once the group decided to develop the ripple carry adder. Primarily 3 implementations were compared.

The logic of the entire adder is implemented in Implementation 1 using only NAND gates.

Implementation 2 carries out the logic using two XOR gates and three NAND gates.

Implementation 3 carries out the logic using 2 XOR, 2 AND, and 1 OR.



Chapter 2

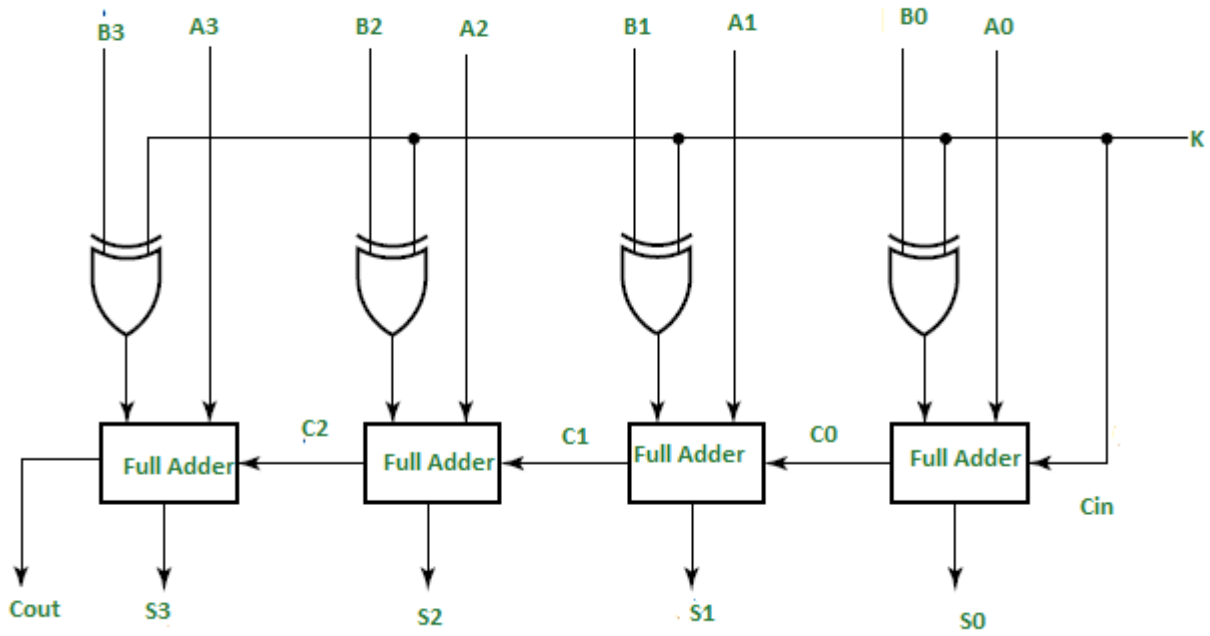
LITERATURE REVIEW

A binary adder-subtractor in a digital circuit is one that can add and subtract binary integers within the same circuit. The binary value that the control signal represents determines the operation that is being carried out. It is one of the ALU's components.

Prior understanding of the Exor Gate, binary addition and subtraction, and full adder is required for this circuit.

As inputs to the digital circuit for the digit operation, let's take two 4-bit binary values, A and B.

Since we are operating on 4-bit numbers, the circuit consists of 4 complete adders. The binary value of the control line K, which is either 0 or 1, indicates whether the operation being performed is an addition or a subtraction.



As shown in the figure, the first full adder has control line directly as its input(input carry Cin), The input A0 (The least significant bit of A) is directly input in the full adder. The third input is the XOR of B0 and K. The two outputs produced are Sum/Difference (S0) and Carry (C0).
If the value of K (Control line) is 1, the output of B0(exor)K=B0′(Complement B0). Thus the operation would be A+(B0′). Now 2's complement subtraction for two numbers A and B is given by A+B'. This suggests that when K=1, the operation being performed on the four bit numbers is subtraction.
Similarly If the Value of K=0, B0 (exor) K=B0. The operation is A+B which is simple binary addition. This suggests that When K=0, the operation being performed on the four bit numbers is addition.
Then C0 is serially passed to the second full adder as one of its outputs. The sum/difference S0 is recorded as the least significant bit of the sum/difference. A1, A2, A3 are direct inputs to the second, third and fourth full adders. Then the third input is the B1, B2, B3 EXORed with K to the second, third and fourth full adder respectively. The carry C1, C2 are serially passed to the successive full adder as one of the inputs. C3 becomes the total carry to the sum/difference. S1, S2, S3 are recorded to form the result with S0.

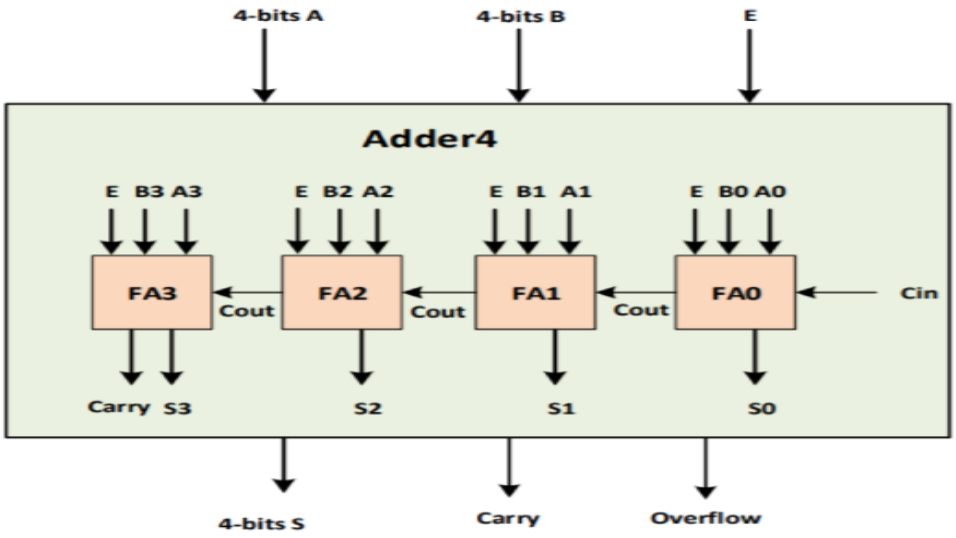
Chapter 3

PROJECT DESIGN AND IMPLEMENTATION

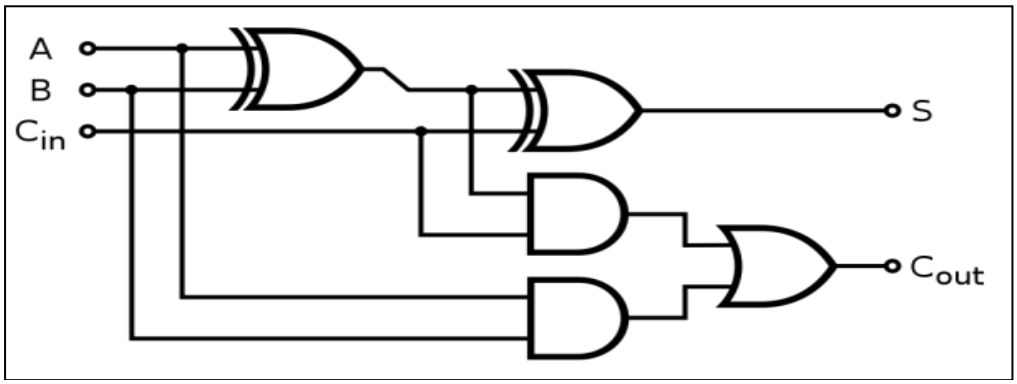
Truth Table for 4-Bit Adder:

A				B				Carry in	Sum				Carry
A3	A2	A1	A0	B3	B2	B1	B0	Cin	S3	S2	S1	S0	Cout
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	1	0	0
0	0	1	0	0	0	1	0	0	0	1	0	0	0
0	0	1	1	0	0	1	1	0	0	1	1	0	0
0	1	0	0	0	1	0	0	0	1	0	0	0	0
0	1	0	1	0	1	0	1	0	1	0	1	0	0
0	1	1	0	0	1	1	0	0	1	1	0	0	0
0	1	1	1	0	1	1	1	0	1	1	1	0	0
1	0	0	0	1	0	0	0	0	0	0	0	0	1
1	0	0	1	1	0	0	1	0	0	0	1	0	1
1	0	1	0	1	0	1	0	0	0	1	0	0	1
1	0	1	1	1	0	1	1	0	0	1	1	0	1
1	1	0	0	1	1	0	0	0	1	0	0	0	1
1	1	0	1	1	1	0	1	0	1	0	1	0	1
1	1	1	0	1	1	1	0	0	1	1	0	0	1
1	1	1	1	1	1	1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

BLOCK DIAGRAM:



Gate Level Implementation of the Full Adder



Chapter 4

CONCLUSION AND FUTURE WORK

All of the ALU's arithmetic operations are built on the adder. Algorithms based on the adder are used to accomplish addition, multiplication, and division. Despite having a more complicated appearance than subtraction, addition may be implemented as a Boolean function using simply AND, OR, and XOR gates. Compared to the other circuits we've looked at so far, the full adder circuit's implementation is more complicated. It required 5 connected gates, 3 distinct chips, and 2 outputs. It took significant consideration and caution to implement and debug this circuit.

References:

- **Introduction:**

https://www.google.com/url?sa=t&source=actor/amp/&ved=2ahUKEwj1ucin9sPxAhUIvRQKHf7iBngQFjAfegQIKRAC&usg=AOvVaw1ZDy9yosE8Stn-KyuozpMU&ampcf=1

- **Gate level Implementation:**

https://www.google.com/url?sa=t&source=web&rct=j&url=http://dar.aucegypt.edu/bitstream/handle/10526/4948/4-Bit%2520Adder.pdf%3

- **Literative Review:**

https://www.google.com/url?sa=t&source=web&rct=j&url=https://www.researchgate.net/figure/Gate-level-implementation-of-a-full-adder