	DATE: 02/05/2024
	Submitted By : Junaid Asif Real No . RRAT-144
	CD-98 : BSAT (IV-Sem)
	Submitted To: Mr. Mehwigh 7ch
	Subject: Coal
	Assignment # 03
Qia	Explain difference between pipelining and parallelism process. Pravide examples of how each technique improves CPU
	of how each technique imprayes CPU
	Postermance.
<u>A.o</u>	Pipelining: Pipelining involves breaking down the execution of inches alice is a
- Pins	Pipelining involves breaking down
	The control of home many into many in 19
	Stages & go that different stages of
	different instructions can be executed
	Simultaneously-Each stage in the pipeline performs a different operation, and multiple
	instructions are overlapped in execution.
	Pipelining improves CPU performance by
	maximising CPU utilisation as it allows
	maximistre CPU utilisation, as it allows multiple instructions to be in different
	Anger a Caccution Simultan county. However
	it may reflex from pipeline bozards such
	as data hosards, central bazards, and
	Structural hazarda, which can reduce officioney.

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	Parallelism:	
	Parallelism involves performing	
	multiple tesks simultaneously using	
	multiple processing units or cores. It	_
	can be classified into TLP and TLP.	
	Parallelism improves CPU performance by	
	increasing throughput, allowing multiple tasks	-
	to be executed concernently. It embles	
	Paster execution de programs by dividing	
	the workload among multiple processing winter	
	and the state of t	
	Example of how each technique improve	
	CPU Performance:	
	The state of the s	
	Piplining: Suppose you have a tack where	
	you need to bake a cake. Pipelining in	,
	This seenavio would insinuolving breaking	
	down the process of baking into multiple	
	Stages, such as mixing ingredients preparing	
	the over baking the cake, and cooling	
	it down. While the cake is being	- Singap
<del></del>	baked you can start mixing the incredie to	
	for the next cake, thereby overlapping the	
	Stages and reducing the overall time	
-	required to bake multiple cakes.	a property.
	A STATE OF THE RESIDENCE OF THE PARTY OF THE	
	Parallelism: Imagine you have a team of	
	chef in a kitchen, each specializing in a	
	different reports of cooking. While one	
	ched is preparing the main course andlar	

ched can complaneously work on apportione, and another other chel can becuse on describe. This division of Johan allows multiple dither the be prepared concurrently, reducing the overall time required to serve a complete month.  Describe stages invalued in instruction execution cycle of pipeline process thou deed pipelining improves (PU performance).  And The instruction execution cycle in a pipeline processor typically consists of several stages, such as each responsible for a specific operation. These stages are designed to exercise improve the increase the throughput and improve CPU performance. Here a depical treatedown of the stages involved in the instruction execution eyelle of ap an instruction fetch: In the stage, the processor pipelined processor:  1. Instruction Fetch: In this stage, the processor enters in the programming program counter. The instruction is then placed into an instruction register (TR)  Per Earther process.  2. Lety alian Decade: In this stage, the		DATE://	
and another that the contents of John allows  Jecerts. This division of John allows  roultiple disher the be prepared  concurrently, roducing the overall time  concurrently, roducing the overall time  required to serve a complete meal.  Describe chases invalued in instruction  execution cycle of pipeline process thou best pipelining improves CPU performances  And The instruction execution cycle in a pipelining processor typically consists of several chages,  each as each responsible for a specific approximation execution execution execution and the stages involved in the instruction execution register (TR)  Processor counter The instruction register (TR)  Per further process.		chef can simultaneously work on appetize	٠٠,
describe. This division of labor allows roultiple disher to be prepared concurrently, reducing the overall time required to serve a complete meal.  Describe stages invalued in instruction excell thow does pipelining improves CPU performances does pipelining improves CPU performances processor typically consists of several stages, each as each responsible for a specific operation. These stages are designed to every and improve CPU performance. Here a a typical increase the throughput and improve CPU performance. Here a a typical treakdown of the stages involved in the instruction execution eyeals of ap and instruction fetch: In this stage, the processor:  1. Instruction Fetch: In this stage, the processor and the instruction is then instruction is then program counter. The instruction is then instruction is then.		and another that the con force on	-
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Concurrently, reducing the overall time  required to lerve a complete meal.  Describe stages invalued in instruction  execution cycle of pipeline process flow  does pipelining improves (PU performance)  Ans The instruction execution cycle in a pipeline  processor typically consists of several stages,  in and each responsible for a specific  approve of the stages are designed to surrius  in order to increase the throughput and  improve of the stages involved in the  instruction execution eyelle as a typical  instruction fetch: In the stage the processor  Petched the instructions from memory using the  address stored in the programming  program counter. The instruction register (TR)  Per further process.		Oliole disher to be prepared	
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program counter. The instruction is then in placed into an inchruction register (TR)  Ear Further process.  2. Test alian Decode: In this stage the		adjuse stored in the tragramming	
Par further process.  2. Tetralian Decade: In this stage the	,	process counter. The instruction is then	
2. Tetralian Decade: In this stage the		placed into an inchrection register (TR)	
2. Tetralian Decade: In this stage the		P. Circler pracelle	
. 1 '0 ' 1	2.	Tetralian Decade: In this stage the	
processor decades the instruction tetched		processor decades the instruction tetched	
in the previous stage-		in the previous stage.	

<u> </u>	Execution: In this stage, the actual operation	
	Secified by the instruction is executed. This	
	could involve orithmetic or logic operations,	
91	memory accesses, or control flow changes.	
	Memory Acress: The stage is responsible	
	Proposition of the state of the	
-	for accepting memory if needed. For instructions	
	I and store instructions data is read	
	from or withen to memory in this page.	
S.	Write Bock: In the final Plage, the results	
	of the executed instruction are written	
	back to the appropriate register. This	
	could be a general-purpose register or	1
	a special-purpose register depending on the	
	type of instruction executed	
	The or word way control	
	Now, Det's discuss how pipelining improves	
•	CPU performances:	
	A Comment of the Comm	
1.	Trereased Throughout: Pipelining allows multiple	
- 1	instructions to be in different stages of	
	execution simultaneously. As a result, the overall	
	throughout of the CPU is increased	
i	because multiple instructions can be processed	
	concurrently.	
- 2	Reduced Latency: By breaking down the instruction	
-	execution eyele indo multiple stages and	
	overlapping them, pipalining reduced the latercy	
	of individual instructions. Even though each	
	instructions takes multiple clock eyales to	
	complete the overall time taken for the ordine instruction	

t	DATE:/	<del>,</del>
	Squerce & reduced.	11
3.	Scalability: Pipelining forilities fecilitates	
	the scaling of CPU performance by	
	enchain the addition as more pipeline	
	slages or by increasing the width of the	
	pipline. This enlability allows for higher	
	dock frequencies and more complex	
	instructions execution without righticoney	
_	significantly increasing the cycle time.	
	Overally pipelining le a hudanestant	
-	technique used in modern CPU design	_
-	to improve performance by increasing throughput, reducing latency, and enhancing	
-	resource utilization	-
-		
-	and the second of the second o	
Que	Discuss the concept of instruction level	
-	garablelism and its importance in	
	TIP technique used in practice.	
	IIP technique used in practice:	
	TIP is a CPU design concept that focuses	
	on executing multiple instructions simultaneously	
	within a single processor care. It aims to	
-	exploit the inherent parallelism present in	
-	performance.	
_	bayer wance.	
	Importance in modern CPU design:	
	Direction for the second secon	

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1,	Performance Improvment: ILP allows CPUs	
	to execute multiple to instructions.	
	concurrently, thereby increasing the overall	
	throughput and performance of the processor	
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٦.	Utilization of CPU Resources: ILP ensures	
	that the CPU's resources, such as	
	forth functional units and execution pipelines	
	ore fully utilized.	
	I'de ide	
٧.	Compensation for Memory Latency: TLP can help	
	militate the import of memory Jalency by	
	allowing the CPU to execute independent	
	instruction while weiting for memory	
	acress to complete.	
-	ACCES TO CAMPOSITE	
ч.	Scalability: TLP techniques can be scaled	
	to accommodate the increasing complexity	المارية المارية
	of modern CPU's-By. Deveraging 28 TLP	
	CRU designers can continue to improve	
	carlange without cignificantly increasing	
	perharmance without eignificantly increasing	
	Caselle Mars - Instrument	
	Frample of ILP Techniques used in Practice	
	1	
	are:	
	P O O C line Constanting on section	
1	Superscalar Grecution: Superscalar processor	
	have multiple execution within a	
	single core, allowing them to execute multiple instructions in parallel.	
	multiple instructions in parallel	