LAB EXERCISE 4

1. a.) What is the tag size for the cache?

Problem: Unified 256 KB, 4-way set-associative cache, 64-byte blocks, 32-bit addresses. CPI = 1.0 if all hits, 50% instructions are data accesses, 2% miss rate, 25-cycle miss penalty.

- Cache Structure:
  - Cache size: 256 KB = 2^{18} bytes.
  - Block size: 64 bytes = 2^6.
  - Sets: $\frac{2^{18}}{2^6 \times 4} = 2^{10} = 1024$.
  - Address: 32 bits.
  - Block offset: $\log_2(64) = 6$ bits.
  - Index: $\log_2(1024) = 10$ bits.
  - Tag: $32 - 6 - 10 = 16$ bits.
- Answer: Tag size = 16 bits.

b. How much faster would the computer be if all memory accesses were cache hits?

- Current CPI:
  - Miss rate: 2% = 0.02.
  - Miss penalty: 25 cycles.
  - CPI with misses: $\text{CPI}_{\text{hit}} + \text{miss rate} \times \text{miss penalty} = 1.0 + 0.02 \times 25 = 1.5$.
- All Hits CPI: 1.0.
- Speedup: $\frac{\text{CPI}_{\text{with misses}}}{\text{CPI}_{\text{all hits}}} = \frac{1.5}{1.0} = 1.5$.
- Answer: 1.5 times faster.

2. a.) The cache is write through.

Problem: Cache: 95% hit rate, 2-word blocks, 10^9 words/s references, 25% writes, 30% blocks dirty. Memory system: 10^9 words/s. Write-allocate cache. Calculate memory bandwidth usage (%).

- Assumptions: Write-through writes directly to memory; read misses fetch 2 words.
- Miss Rate: 5% = 0.05.
- Read Accesses: 75% = $0.75 \times 10^9 = 7.5 \times 10^8$.
- Write Accesses: 25% = $0.25 \times 10^9 = 2.5 \times 10^8$.
- Memory Traffic:
  - Read misses: $0.05 \times 7.5 \times 10^8 \times 2 = 7.5 \times 10^7$ words/s.

- Write misses (write-allocate): $0.05 \times 2.5 \times 10^8 \times 2 = 2.5 \times 10^7$ words/s (fetch block).
- Writes: 2.5×10^8 words/s (all writes to memory).
- Total: $7.5 \times 10^7 + 2.5 \times 10^7 + 2.5 \times 10^8 = 3.5 \times 10^8$ words/s.

- Bandwidth Usage: $\frac{3.5 \times 10^8}{10^9} = 35\%$.
- Answer: 35%.

b.) The cache is write back
- Assumptions: Writes update cache; dirty blocks (30%) written back on eviction.
- Memory Traffic:
  - Read misses: $0.05 \times 7.5 \times 10^8 \times 2 = 7.5 \times 10^7$ words/s.
  - Write misses: $0.05 \times 2.5 \times 10^8 \times 2 = 2.5 \times 10^7$ words/s.
  - Write-backs: Total misses = $0.05 \times (7.5 \times 10^8 + 2.5 \times 10^8) = 5 \times 10^7$. Dirty blocks: $0.3 \times 5 \times 10^7 \times 2 = 3 \times 10^7$ words/s.
  - Total: $7.5 \times 10^7 + 2.5 \times 10^7 + 3 \times 10^7 = 1.3 \times 10^8$ words/s.
- Bandwidth Usage: $\frac{1.3 \times 10^8}{10^9} = 13\%$.
- Answer: 13%.

3. Cache Performance

Problem: Compare write-through (2-cycle write, no buffer stall) vs. write-back (2-cycle write, 50% dirty blocks). Read hit: 1 cycle, miss penalty: 50 cycles, write-back block write: 50 cycles. Instruction cache miss rate: 0.5%, data cache miss rate: 1%. Loads: 26%, stores: 9%.

- CPI Calculation:
  - Instructions: 100%. Loads: 26%, stores: 9%, others: 65%.
  - Instruction Cache: Miss rate = 0.005, penalty = 50.
    - CPI impact: $0.005 \times 50 = 0.25$.
  - Data Cache:
    - Loads: Miss rate = 0.01, penalty = 50.
      - CPI impact: $0.26 \times 0.01 \times 50 = 0.13$.
    - Stores: Depend on cache type.

Write-Through:
- Store hit: 2 cycles.
- Store miss: 2 cycles (write to memory, no stall) + 50 (fetch block, write-allocate).
- Store CPI:

  - Hits: $0.99 \times 2 = 1.98$.
  - Misses: $0.01 \times (2 + 50) = 0.52$.
  - Total: $0.09 \times (1.98 + 0.52) = 0.225$.
- Total CPI: $1.0 + 0.25 + 0.13 + 0.225 = 1.605$.

Write-Back:
- Store hit: 2 cycles.
- Store miss: 2 cycles + 50 (write-back if dirty) + 50 (fetch block).
  - Miss penalty (50% dirty): $0.5 \times (2 + 50 + 50) + 0.5 \times (2 + 50) = 51$.
- Store CPI:
  - Hits: $0.99 \times 2 = 1.98$.
  - Misses: $0.01 \times 51 = 0.51$.
  - Total: $0.09 \times (1.98 + 0.51) = 0.2241$.
- Total CPI: $1.0 + 0.25 + 0.13 + 0.2241 = 1.6041$.

- Performance: Write-back slightly faster ($\frac{1.605}{1.6041} \approx 1.0006$).
- Answer: Write-back CPI = 1.604, write-through CPI = 1.605 Write-back is marginally faster.