Flexible Radio Transceiver (FLRTRX) Interface Control Document

1 Introduction

This document describes the specifications for the flexible radio transceiver (FLRTRX) which is implemented in ECE295. Details regarding the mainboard interfaces, and the interfaces to the various subsystems are provided within this document.

Many modern radio systems, especially those operating in the microwave frequency range (generally defined to be between 1-100 GHz) are implemented using architectures like the one used in this project. In particular, the receiver portion and digital encoding/decoding portions of the transceiver comprise a software defined radio (SDR). SDR is a software implementation of various components traditionally realized in hardware, for achieving radio communication. SDR is a flexible radio platform that allows the functionality of the radio to be reconfigured at any time (like a piece of software). Still, SDRs must be implemented using a significant amount of hardware, particularly the portion that interfaces with the physical radio signal (which is called the "front-end" of the radio system) before operations can be taken over in the software domain. The design of such a radio front-end is the goal of this course. The radio developed in this course will be used for transmitting signals in the High Frequency (HF) radio band (3-30 MHz) and receiving signals in the HF radio band. There are a variety of radio systems that utilize frequencies in these bands. Some notable examples include citizen's band radio systems, shortwave radio broadcasts, amateur radio, aviation air-to-ground communications, maritime services, and radars. The radio developed here will be able to interact with some of these systems.

For ECE295, the complete SDR is made up of 5 discrete subsystems mounted to the mainboard:

1. RX Quadrature Mixer [Subsystem A]
2. Demodulator [Subsystem B]
3. Local Oscillator and User/Computer Interface [Subsystem C]
4. TX Quadrature Mixer [Subsystem D]
5. TX Power Amplifier and Filter [Subsystem E]

This document outlines the mainboard, along with the interface details to the subsystems that will be developed by the students.

2 Radio Principles and Components

If you take a simple radio, like a handheld AM / FM radio, chances are it is implemented as a very specialized piece of hardware: a system that takes in an amplitude-modulated (AM) or frequency-modulated (FM) electromagnetic signal at a specific radio frequency from an antenna,

and transforms it into an audio signal that you can listen to and understand. That radio is responsible for various operations, such as the ability to tune the radio (e.g. so that you can tune precisely to 99.1 MHz if you wanted to listen to CBC Toronto), amplification of a weak radio signal, demodulation of the radio signal into an intelligible form, and further amplification of that signal so that it can drive a speaker or headphones. This is an example of a radio receiver (RX); it is also possible to have radio transmitters (abbreviated as TX, e.g. the hardware that is creating the CBC FM signal in the first place) and transceivers (TRXs) – radio systems that implement both transmitting and receiving functions. Your smartphone and the WiFi card in your computer are examples of systems that contain transceivers for transmitting and receiving digital signals using radio signals. Receive-only radios are also common; in addition to the AM / FM broadcast radio discussed above, the global navigation satellite system (GNSS) receiver in your smartphone or vehicle receives signals from satellites to determine your position without having to transmit information to those satellites.

Modern wireless communication systems are implemented using a combination of hardware and software, unlike the simple handheld AM / FM receiver discussed above. The hardware portion deals with processing the physical electromagnetic signals using in radio communications into a form that is easier to process, and is often referred to as the physical layer of the communication system. In traditional radio systems, like our AM/FM radio example above, hardware components would also handle subsequent processing of these signals to transform them into a form that can be usable by humans, e.g. audio signals to and from the radio unit. Nowadays, in modern implementations of radio systems, intermediate signals are sampled digitally and processed using modern digital signal processing techniques in a software-based platform, such as an embedded processor, application specific integrated circuit (ASIC), or field programmable gate array (FPGA). This allows mathematical operations needed in communications to be implemented more precisely, which is especially important for digital communications, where digital bits are sent back and forth in the system instead of analog audio signals. At the same time, it allows the radio system to be implemented in a flexible way, since a software change can be used to completely redefine how the radio is implemented. This is adaption yields a software defined radio (SDR) system and forms the basis of all modern wireless transceiver implementations.

In ECE295, teams will be responsible for implementing the hardware portion and software-controlled portions of an entire radio transceiver. Since a portion of the radio can be re-defined by software, we call this a flexible radio transceiver (FLRTRX). You will learn in detail how the hardware works, and the platform will also serve to introduce you to important signal processing, communication, and radio communication concepts that you will learn about in more detail in courses such as ECE316, ECE422, and others.

2.1 System Block Diagram

The system block diagram for the FLRTRX is shown in Figure1. Our discussion of the signal flow begins with the antenna on the left-hand side of the diagram, which transmits and receives electromagnetic signals at the frequency of interest. In the receiving mode, the transmit/receive switch (TX/RX switch) is set so that signals from the antenna are directed to the RX portion of the system, in the top half of the diagram; likewise in the other state the antenna is connected to

the TX portion of the system instead. The goal of this portion of the system is to transform the high-frequency electromagnetic signal received by the antenna into a "baseband" signal, which is very low in frequency and suitable for further processing by the software portion of the system. That signal appears at the right edge of the diagram. Similarly, when in TX mode, the signal chain shown in the bottom half of the diagram (with signal flow from right to left) transforms a baseband signal into a powerful high-frequency one that is ultimately applied to the antenna and transmitted. Components of the SDR system are formed into subsystems and described in more detail below.

2.2 Receive Chain

The receive chain is shown in the upper half of Figure 1. The radio frequency (RF) signal received by the antenna first passes through a bandpass filter and limiter. The bandpass filter is responsible for making the receiver selective in the frequency band of interest by filtering out extraneous signals outside the passband. A limiter is built into the front-end of the receiver in case a large signal is accidentally applied (e.g. from leakage from the transmit chain), since the receiver is very sensitive and can be easily overloaded and damaged by large signals.

Next, the filtered RF signal is *downconverted* from the RF carrier frequency to the frequency band of the original message signal. Downconversion refers to the process of shifting the frequency of an RF signal down to a lower one. The downconverter utilizes a three-port device known as a *mixer* (shown as the RX quadrature mixer in Figure 1), which multiplies the incoming signal with a signal at a single frequency f_{LO} generated by the *local oscillator (LO)*. The sum and difference frequencies between those of the RF (f_{RF}) and LO (f_{LO}) signals appear at the output of the mixer ($f_{\mathsf{RF}} + f_{\mathsf{LO}}$) and $f_{\mathsf{RF}} - f_{\mathsf{LO}}$). The higher frequency signal is filtered out by the lowpass filter, and the remaining difference frequency signal is passed on to the next part of the receiver chain.

The receiver mixer is called a *quadrature mixer* because the result of the mixing is a signal that has two components, known as the in-phase (I) and quadrature (Q) components of the signal. If the RF signal was a single sinusoid, the I and Q components would be $90^{\circ\circ}$ out of phase with each other. As you will learn, representing the signal in I/Q form makes it very easy to apply different demodulation techniques to a signal. The purpose of the RX quadrature mixer is to generate these IQ signals. They are subsequently amplified to a more usable level by the IQ amplifier.

Finally, the signal can be demodulated. In ECE295, this is accomplished by sampling the received signal using an analog-to-digital converter (ADC), which is shown as the box with the "A / D" in Figure 1. This digitized signal is processed by an FPGA in real time to perform the demodulation digitally. Finally, the signal is converted back to an analog one using a digital-to-analog converter (DAC) for listening or further processing.

Notice that the conversion from the RF frequency down to baseband in on step yields what is called a *direct conversion receiver*, which is one of many types of radio implementations.

2.3 Transmit Chain

The transmitter portion of the radio is shown in the lower half of Figure 1. The transmitter chain basically works in reverse. A baseband signal, represented in IQ form, is first amplified, since the

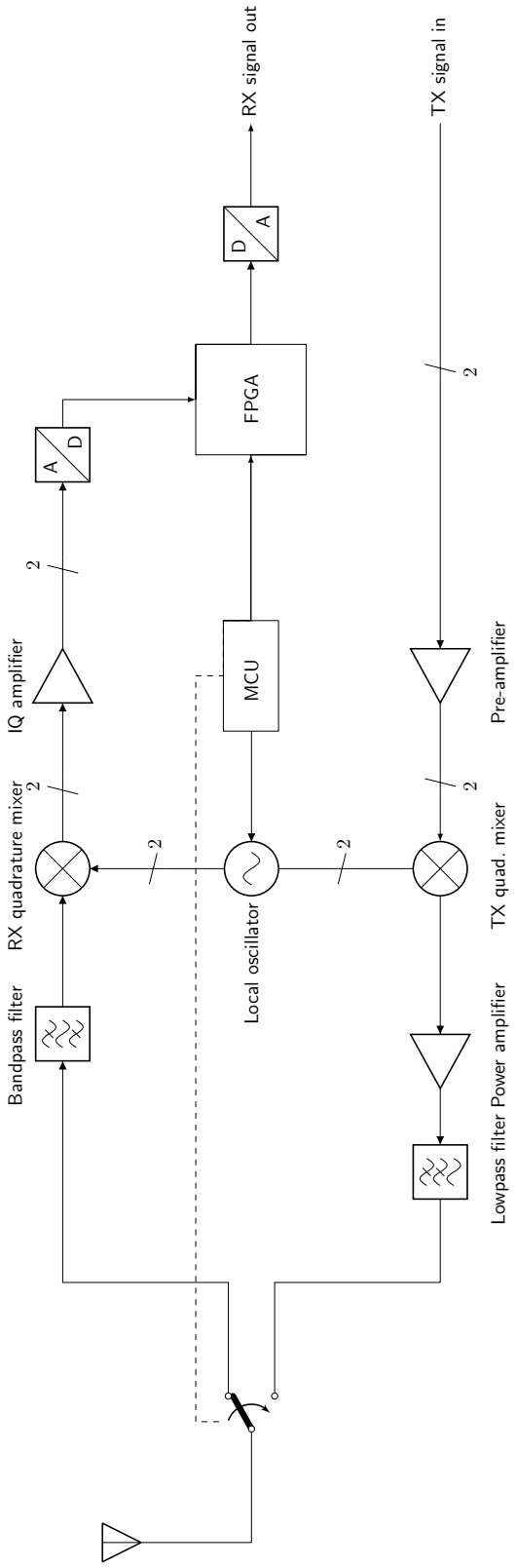

Figure 1: FLRTRX system block diagram

signal amplitude of the TX signal may not be large enough to drive the power amplifier in a later stage. The next stage is an upconverter, essentially taking the IQ signal and translating it to the radio frequency signal, whose frequency is determined by the frequency of the same local oscillator that drove the mixer in the receiver chain. Hence the output of this stage is a signal at the same frequency of the receiver.

At this stage, the signal is still relatively small here in terms of signal power. The signal must pass through a power amplifier (PA) to make it powerful enough to be picked up by distant receivers once it is transmitted by the radio's antenna. The output of the PA must be filtered, to ensure any extraneous frequency products generated by the amplification process are not emitted by the antenna, where they could lead interference with other radio systems.

2.4 Local Oscillator (LO)

The quadrature mixers in the TX and RX chains require an oscillator to generate signals to drive the LO ports on the respective mixers. These signals can be sinusoidal or square-wave signals, but the important thing is that they have a precisely-controlled frequency f_{LO}. For the quadrature mixers, the oscillator generates two output signals such that the two signals are 90° out of phase with each other. The oscillator here is implemented such that it can be controlled either by a human operator through some sort of user interface (UI), and also by a computer through a universal serial bus (USB) port. As such, the oscillator must be under the control of a microcontroller unit (MCU), which facilitates controlling the LO, and coordinating that with human or computer control.

2.5 Functional Subsystems

The functions above have been divided into subsystems as shown in Figure 2. The subsystems are referred to as Subsystems A, B, C, D, and E. Each subsystem will be implemented by a different team, with the exception of Subsystem D, which is provided[1]. A brief description of the subsystems is provided below.

2.5.1 RX Filter, Limiter, and Quadrature Mixer [Subsystem A]

This subsystem filters the signal received by the antenna to remove out-of-band signals. The limiter provides electrical protection to the receiver. After filtering, the signal must be downconverted to the intermediate frequency and filtered. The downconversion requires use of the LO signal at frequency f_{LO} to bring an RF signal of known frequency down to the baseband frequency range of Subsystem B. The signal is filtered to remove extraneous mixer products, and amplified before being passed onto Subsystem B, which acts on the downconverted signal.

2.5.2 Digital Demodulator [Subsystem B]

This is a digital hardware implementation of a demodulator or detector for a prescribed modulation format. Generally, modulation formats include AM, FM, single sideband (SSB), etc. The output is an audio signal that can be connected to a an amplified speaker or headphones for listening purposes. It can also be connected to the sound card of a computer, which is useful in scenarios

[1] Subsystem D accomplishes the reciprocal operation of Subsystem A, and so there is limited value in having teams design this subsystem in addition to Subsystem A.

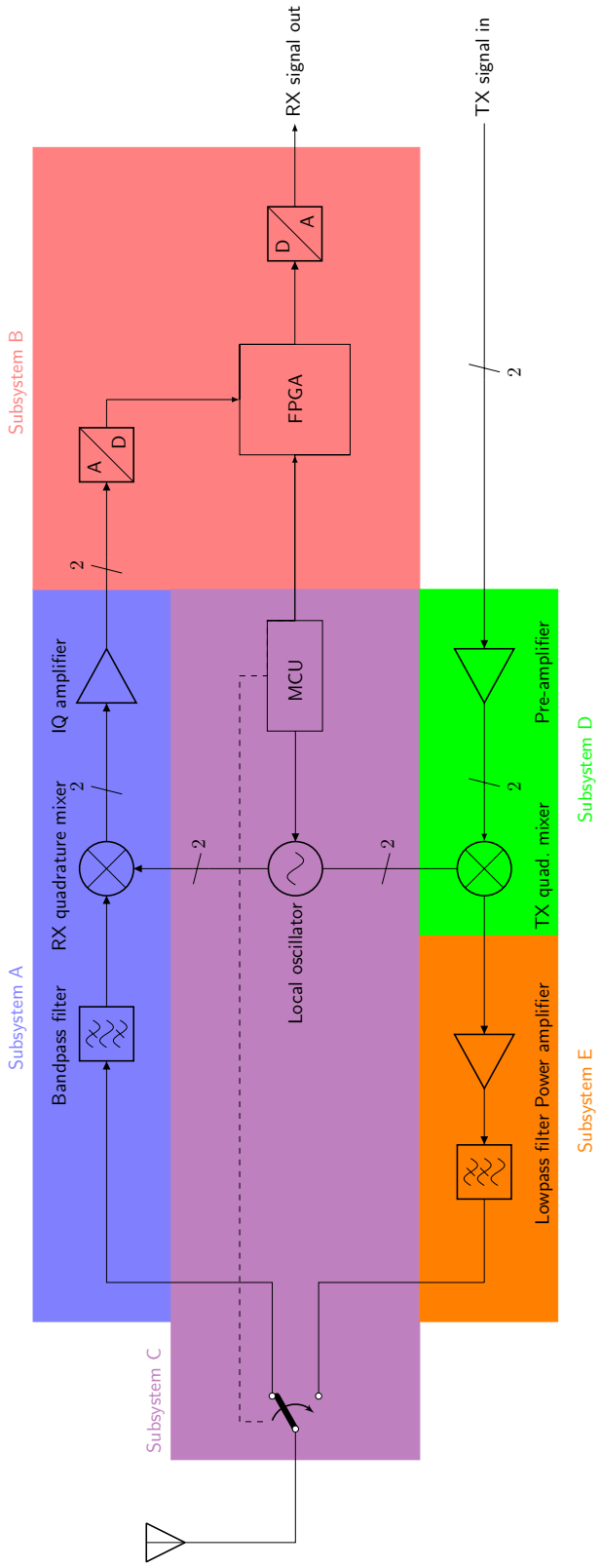

Figure 2: FLRTRX subsystems

where the message is encoded digital information. Subsystem B must be able to demodulate two modulations types: AM and SSB.

2.5.3 Local Oscillator and User/Computer Interface [Subsystem C]

This subsystem supports both the transmitter and receiver portions of the radio. This subsystem is responsible for generating the local oscillator signals driving the transmit and receive quadrature mixers. For the quadrature mixers, two oscillator signals at the same frequency f_{LO} must be generated, 90° out of phase, with the same amplitude. The oscillator must be controllable such that it can be controlled by a student-designed front-panel user interface (UI), as well as by a computer over the USB bus. This subsystem also implements a suitable TX/RX switch that can be controlled by the UI or the computer.

2.5.4 TX Quadrature Mixer [Subsystem D]

This subsystem implements the reciprocal operations of Subsystem B, transforming a suitably modulates pair of IQ signals into a radio frequency signal at frequency $f_{\mathsf{RF}} = f_{\mathsf{LO}}$. This subsystem is not designed by teams, and is already provided.

2.5.5 TX Power Amplifier and Filter [Subsystem E]

This subsystem takes the output from Subsystem D and amplifies it to a powerful signal that can be applied to the radio's antenna and broadcast over a significant distance. A lowpass filter must be included to remove distortion created by the power amplifier in the process.

2.6 Radio Operation

The completed radio system will operate in two ways.

1. **Standalone mode**: When switched on, the radio will be in the receive mode by default. A user can change the receiver frequency through the front-panel user interface and listen to the demodulated signal from the receiver on a speaker or headphones. From the front-panel, a user can also switch the radio to transmit mode, in which case an externally supplied baseband signal supplied to the transmit chain input will be transmitted by the radio and received elsewhere.

2. **Computer-controlled mode**: The entire radio will be under the control of a computer program external to the radio, running on a PC. The radio's operating frequency will be controlled by the computer over the USB bus. Signals received by the radio will be connected to the computer via the sound card, where they will be sampled and demodulated. In transmit mode, outgoing signals are synthesized by the computer's sound card and supplied to the transmit chain. In this mode, the computer has full control over the radio, which is useful when digital information is being exchanged between stations and the TX/RX functionality of the radio must be automated.

3 Mainboard and Subsystem Operation

This section outlines the mainboard and each subsystem that is connected to it. Each subsystem outlines the recommended design approach and the expected testing requirements. This information should guide and put constraints on the design of each subsystem.

3.1 Mainboard

The function of the mainboard is to interconnect all of the subsystems developed by ECE295 teams, provide power, as well as provide an interface to external signals. It accepts subsystems implemented as daughtercards which plug into connectors on the mainboard. The mainboard facilitates the following connections to the outside world:

- RF connection to antenna
- DC power connection
- Baseband IQ inputs for the FLRTRX transmitter
- Numerous intermediate signals between stages for debugging purposes

If all the subsystems of the radio have been implemented properly, the radio as a whole can be test by commanding it to receive signals at known frequencies (e.g. amateur radio frequencies; shortwave frequencies; etc.) and successfully output the message signal or decode it if it is digital (using a PC). Transmission capabilities will be checked by receiving the signals with a reference receiver to check that the transmitter is working as intended.

3.2 RX Bandpass Filter, Limiter and Quadrature Mixer [Subsystem A]

This subsystem accepts the RF signal from the RX pole of the TX/RX switch, applies filtering and limiting of the RX signal, and then downconverts it to the baseband frequency range of the message signal. This process requires the use of an RF filter, a limiting circuit, a quadrature mixer circuit. The quadrature mixer accepts two LO inputs from Subsystem C and uses that to mix with the filtered and limited RF signal. The resulting signal is filtered to reject other frequency products generated in the mixing process, and then amplified for subsequent processing.

3.2.1 Electrical Interface Description

- Input signal 1: Unfiltered HF RX signal (`RX_SIG`) within the 8-16 MHz range.
- Input Signal 2 & 3: oscillator signals from Subsystem C (`LO_F1_0` and `LO_F1_90`), which are two local oscillator signals with 90° of phase difference between them.
- Input signal 3: Active-low transmit-enable signal (`/TXEN`), which is at LVTTL (3.3V) levels. This signal informs the module if the radio is in receive mode (high) or transmit mode (low).
- Output signal 1 & 2: `RX_I` (in-phase) and `RX_Q` (quadrature) signals with a minimum of 30 dB gain applied post-mixing, and at least first order filtering applied with an upper

cutoff frequency at 96 kHz. The downconverted signal's centre frequency should be 10 kHz. Output should be AC-coupled to Subsystem B.

- Power signals: $+$3.3V and $+$5V (either or both can be used).

Information to consider:

- The receive filter must operate with the following specifications: 66% fractional 3 dB bandwidth centered at 12 MHz, maximally flat response (approx. 8–16 MHz).
- The limiter must clip the input signal such that it does not exceed ± 0.7 Vpp.
- IQ signals must be, over the entire input frequency range:
  - Ideally 90 degrees apart in phase [$90^\circ \pm 12.5^\circ$]
  - Amplitude-balanced [within 1 dB]
  - Outputs must not exceed the range 0–5 V.

3.3 Digital Demodulator [Subsystem B]

This subsystem receives a baseband IQ signal from Subsystem A. The signal is sampled by a pair of ADCs and digitally processed by an FPGA to implement a demodulator to extract the message signal. The output of the subsystem is a line-level audio signal from a DAC that can drive amplified speakers or headphones, or be input to the sound card of a computer for further processing.

3.3.1 Behavioural Description

- This module is responsible for implementing SSB and AM demodulation from the sampled I/Q signals. The theory for accomplishing this is not presented in this document, but discussed in the course.
- This module accepts I/Q signals that reside on a 10 kHz carrier (see Section 3.2). Therefore, an additional downconversion is need to recover the baseband I and Q signals.
- The choice of demodulation should be determined by a human operator using the subsystem through some sort of control.

3.3.2 Electrical Interface Description

- Input signals 1 & 2: Baseband I (in-phase) and Q (quadrature) signals from Subsystem A (`RX_I` and `RX_Q`)
- Output Signal 1: A line level audio signal with the demodulated baseband message signal.
- Power signal: $+$5V is provided, but should not be used for powering the FPGA. It should only be used for powering auxiliary circuits, if needed.

3.4 Local Oscillator and User/Computer Interface [Subsystem C]

This subsystem generates all the required LO frequencies for the entire radio, and also controls whether the system operates as a TX or RX and what frequency to use in this process. The block must be controllable by both a human user operating through a front-panel interface, and also remotely controllable by a computer. The human interface can be implemented in a fashion left up to the team, e.g. using a liquid crystal display (LCD), buttons, 7-segment displays, or any other means for a user to interact with the system. The computer interface is standardized and described in more detail below. The LO signals generated by this block are used by Subsystems A and D.

3.4.1 Behavioural Description

- Serial data from computer (via the USB-serial board) using signals `TXD` and `RXD`: serial command supplied over FTDI USB-serial bridge following the CAT specification for controlling the LO frequency and TX/RX mode. See Appendix A for details.
- User interface (UI) should allow the selection of the desired LO frequency, as well as TX/RX mode
- A `DTR` signal from the computer (via the USB-serial board) should be used to control the TX/RX state of the radio when the radio is under computer control. When `DTR` is high, the radio should be in TX mode; when `DTR is low`, the radio should be in RX mode.
- The TX/RX switch is electronically controlled by either the UI or computer interface described above. Only one should be able to control the state of the switch at once. There is no switching speed constraint or control signal power constraints.

3.4.2 Electrical Interface Description

There are two subsystems within Subsystem C: the microcontroller-controlled oscillator and the TX/RX switch. Information is provided for each.

MCU-Controlled Oscillator

- Output signals 1 & 2: quadrature oscillator signals, 90° apart, 3.3 Vpp unipolar at the required frequency f_{LO} [within 100 Hz] (`LO_F1_0` and `LO_F1_90`). These do not need to be perfectly sinusoidal signals or square-wave signals; the mixers that use these signals will act based on the voltage levels defining logic low and logic high to actuate the mixer device.
- Output signal 3: active-low transmit-enable signal (`/TXEN`), which is at LVTTL (3.3V) levels. This signal informs other modules if the radio is in receive mode (high) or transmit mode (low).
- Power signals: $+$5V and $+$3.3V.

TX/RX Switch

- Bidirectional signal 1: signal to/from antenna (ANT)
- Input signal 1: signal from power amplifier (PA_OUT)
- Input signal 2: active-low transmit-enable signal (/TXEN), which is at LVTTL (3.3V) levels. This signal informs other modules if the radio is in receive mode (high) or transmit mode (low).
- Output signal 1: signal to receiver (RX_SIG)
- Power signal: +5V.

3.5 TX Quadrature Mixer [Subsystem D]

NOTE: The information provided below is for informational purposes. Subsystem D is not designed by students and is provided as a complete functional subsystem.

This subsystem accepts two inputs (baseband IQ signal to transmit and two LO outputs from Subsystem D) mixes them to generate the output RF signal. The process is essentially the reciprocal of Subsystem B.

3.5.1 Electrical Interface Description

- Input signals 1 & 2: Baseband I (in-phase, TX_I) and Q (quadrature, TX_Q) signals where 1 Vpp indicates full-scale (1Vpp should produce the full rated output power from the power amplifier in Section 3.6).
- Input signal 3 & 4: LO signals from Subsystem C (LO_F1_0 and LO_F1_90)
- Output signal 1: Modulated signal (PA_IN) with a carrier frequency matching the frequency of the output of Subsystem A ($8-16$ MHz) at an output level sufficient to drive the power amplifier in Subsystem E. Frequency content of the output signal should only reside in the range $8-16$ MHz.
- Power signals: +5V, VCC (unregulated DC)

3.6 TX Power Amplifier and Filter

The signal must be amplified to generate $1-10$ W of continuous (CW) output power into a $50\ \Omega$ resistive load. The required total harmonic distortion (THD) is less than 10%.

3.6.1 Electrical Interface Description

- Input signal 1: Modulated input signal PA_IN from Subsystem D.
- Input signal 2: active-low transmit-enable signal (/TXEN), which is at LVTTL (3.3V) levels. This signal informs the module if the radio is in receive mode (high) or transmit mode (low).

- Output signal 1: Amplified RF signal (PA_OUT) at a level capable of driving a minimum of 1 W and a maximum of 10 W into 50 Ω resistive. Full rated power output should result when input signal 1 is full-scale (see Section 3.5).
- Power signals: +5V, VCC (unregulated DC)

4 Interfaces

This section describes all the interfaces that are present on the mainboard. The mainboard provides interfaces to each subsystem and provides the interconnects between the modules. It also provides intermediate connections for testing the individual subsystems.

4.1 Electrical

The subsystems have been laid out in a hierarchical schematic as seen in Figure 3, which is also available as a PDF file on Quercus. This is the mainboard and it shows how the modules have been broken up into discrete boards. The signal names match what is described in Section 3. Associated pinouts are described in the next section.

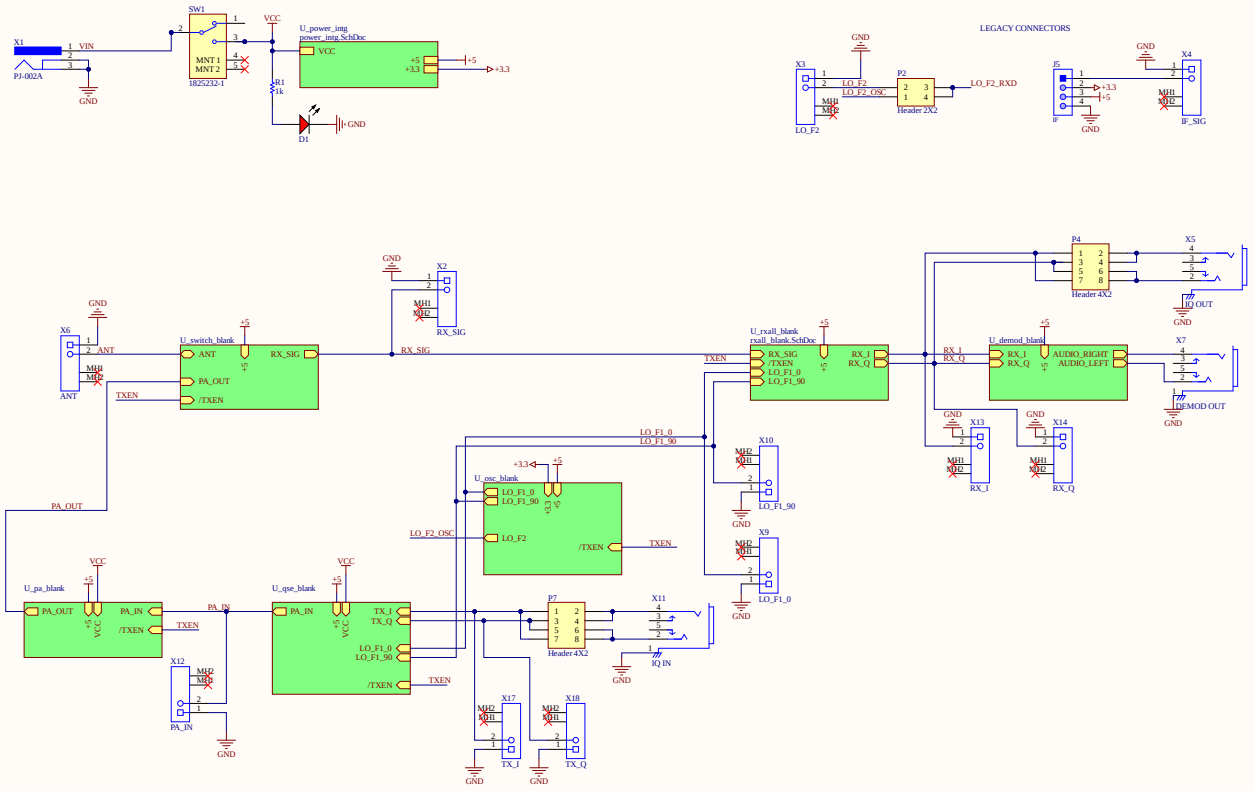

Figure 3: Hierarchical schematic of the FLRTRX. Green boxes are the subsystems; some subsystems are implemented with more than two green blocks.

4.1.1 Connectors

The connectors on the mainboard are outlined in Section 4.1.2. Although the subsystem connectors are on the mainboard as well, for ease of reference, these connectors have been described separately in Section 4.1.3. Subsystems are connected to the mainboard at various points using 4-pin, 2.54 mm pitch rectangular headers, as shown in Figure 4. The prefix `J` is used as the part designator for these connectors, e.g. `J1`. Subsystems will use the male connectors soldered "face down" with the header facing the mainboard, while the mainboard will receive connections using the female connector "face up".

(a) Female connector (b) Male connector (c) Interconnection

Figure 4: Connector stack

When mated together, this creates a *stack height* between the mainboard and a subsystem board of 6 mm (as measured from the top surface of the mainboard to bottom surface of the module board). This means that any components on the bottom side of the subsystem board need to be shorter than this stack height to ensure appropriate mating.

4.1.2 Mainboard External Connectors and Pinouts

There are 5 connectors that are present on the Mainboard that interface to the outside environment. Details of the connector type and the pinout can be found in Tables 1–5.

Please note that that connector `X7` does not need to be used this year, as Subsystem C has 3.5 mm audio jacks on the ADC / DAC daughtercard that can be used for interfacing to the audio signals `AUDIO_L` and `AUDIO_R`. Table 3 is included for historical reasons.

Table 1: `X4` – Antenna

Connector				
Connector Type			BNC	
Connector Part Number			1-1337543-0	
Mating Connector Part Number			N/A	
Pinout				
Contact #	Signal	Type	Voltage	Description
1	`ANT`	Bidirectional	N/A	Antenna signal
2	`GND`	Ground	0 V	Ground

Table 2: `X5` – Subsystem B IQ Output

Connector				
Connector Type	3.5 mm audio jack			
Connector Part Number	35RAPC4BV4			
Mating Connector Part Number	N/A			
Pinout				
Contact #	Signal	Type	Voltage	Description
1	`GND`	Ground	0 V	Ground
2 (LEFT/TIP)	`RX_I`	Output	5 Vpp AC	In-phase component
3	No Connect (NC)			
4 (RIGHT/RING)	`RX_Q`	Output	5 Vpp AC	Quadrature component
5	No Connect (NC)			

Table 3: `X7` – Subsystem C Demodulator Signal Audio Output

Connector				
Connector Type	3.5 mm audio jack			
Connector Part Number	35RAPC4BV4			
Mating Connector Part Number	N/A			
Pinout				
Contact #	Signal	Type	Voltage	Description
1	`GND`	Ground	0 V	Ground
2 (LEFT/TIP)	`AUDIO_L`	Output	-10 dBV AC	Left channel audio
3	No Connect (NC)			
4 (RIGHT/RING)	`AUDIO_R`	Output	-10 dBV AC	Right channel audio
5	No Connect (NC)			

Table 4: `X11` – Subsystem D Transmit Signal Audio Input

Connector				
Connector Type	3.5 mm audio jack			
Connector Part Number	35RAPC4BV4			
Mating Connector Part Number	N/A			
Pinout				
Contact #	Signal	Type	Voltage	Description
1	`GND`	Ground	0 V	Ground
2 (LEFT/TIP)	`TX_I`	Output	5 Vpp AC	In-phase component
3	No Connect (NC)			
4 (RIGHT/RING)	`TX_Q`	Output	5 Vpp AC	Quadrature component
5	No Connect (NC)			

Table 5: X1 – Input Power

Connector				
Connector Type			2.1 mm barrel jack	
Connector Part Number			PJ-002A	
Mating Connector Part Number			N/A	
Pinout				
Contact #	Signal	Type	Voltage	Description
1	VIN	Power	$12 - 18$ VDC	Input power $12 - 18$ VDC
2	GND	Ground	0 V	Ground

4.1.3 Subsystem Connectors and Pinouts

There are 18 connectors that interface with the 6 subsystems. Details of the connector type and the pinout can be found in the following sections.

Subsystem A Connections Historically, Subsystem A was implemented as two daughtercards, which we will refer to as Subsystem A.1 and A.2, with daughtercard A.1 using the connectors described in Table 6 and daughtercard A.2 using those in Table 7. This is because daughtercard A.1 could potentially implement an additional downconversion stage, which is not considered in the current version of the FLRTRX. Therefore, **it is no longer necessary to implement Subsystem A using two daughtercards. Only connectors J1, J5, and J6 need to be used in the design.** All connections (including those no longer needed) are summarized in Tables 6 and 7 for historical completeness.

Subsystem B Connections Subsystem B is implemented using an FPGA that resides on a standalone board residing outside the mainboard. Connections to the ADC on the FPGA connector can be made by using connector J7, which is presented in Table 8. Connector J8 is a legacy connection that allows Subsystem C to connect to the audio jacks on the mainboard described in Section 4.1.2, particularly 3.5 mm audio connector X7. Since the ADC / DAC board used with the FPGA already has 3.5 mm audio jacks on it, there is no need to use these mainboard connectors anymore. Therefore, connector J8 does not necessarily need to be used, and is included in the table for historical reasons.

Subsystem C Connections Subsystem C is implemented using two daughtercards: one for the microcontroller (referred to a daughtercard C.1), and one for the TX / RX switch (daughtercard C.2). The interface for daughtercard C.1, which employs two connectors J9 and J10, is described in Table 9. Note that the LO_F2 connection on J10 is a legacy signal is no longer used.

In addition, the C.1 daughtercard will require the connections in Tables 10–12. on the daughtercard to support programming the microcontroller, connecting the separate PLL module, and serial interface with a PC via a USB-serial module implementing a universal asynchronous receiver-

Table 6: Subsystem A.1 Connectors

Connectors				
Connector Type			Molex 2.54 mm pitch, 4P, TH	
Connector Part Number			PPTC041LFBN-RC	
Mating Connector Part Number			PRPC004SAAN-RC	
J1 Pinout				
Contact #	Signal	Type	Voltage	Description
1	`RX_SIG`	Input	N/A	RX signal
2	`RX_SIG`	Input	N/A	RX signal
3	`GND`	Ground	0 V	Ground
4	`GND`	Ground	0 V	Ground
J2 Pinout (Legacy Connector)				
Contact #	Signal	Type	Voltage	Description
1	`LO_F2`	Input	N/A	LO signal @ f_2 (legacy)
2	`LO_F2`	Input	N/A	LO signal @ f_2 (legacy)
3	`GND`	Ground	0 V	Ground
4	`GND`	Ground	0 V	Ground
J3 Pinout (Legacy Connector)				
Contact #	Signal	Type	Voltage	Description
1	`IF_SIG`	Output	N/A	Intermediate frequency signal
2	`+3.3V`	Power	3.3 VDC	Regulated 3.3 V DC
3	`+5V`	Power	5 VDC	Regulated 5 V DC
4	`GND`	Ground	0 V	Ground

Table 7: Subsystem A.2 Connectors

Connectors				
Connector Type			Molex 2.54 mm pitch, 4P, TH	
Connector Part Number			PPTC041LFBN-RC	
Mating Connector Part Number			PRPC004SAAN-RC	
J4 Pinout (Legacy Connector)				
Contact #	Signal	Type	Voltage	Description
1	IF_SIG	Input	N/A	Intermediate frequency signal
2	+3.3V	Power	3.3 VDC	Regulated 3.3 V DC
3	+5V	Power	5 VDC	Regulated 5 V DC
4	GND	Ground	0 V	Ground
J5 Pinout				
Contact #	Signal	Type	Voltage	Description
1	/TXEN	Input	3.3 V LVTTL	Active-low transmit enable
2	LO_F1_0	Input	3.3 Vpp unipolar	LO signal @ f_{LO}
2	LO_F1_90	Input	3.3 Vpp unipolar	LO signal @ f_{LO} with $90°$ phase shift
4	GND	Ground	0 V	Ground
J6 Pinout				
Contact #	Signal	Type	Voltage	Description
1	RX_I	Output	N/A	In-phase signal
2	+5V	Power	5 VDC	Regulated 5 V DC
3	RX_Q	Output	N/A	Quadrature signal
4	GND	Ground	0 V	Ground

Table 8: Subsystem B Connectors

Connectors				
Connector Type			Molex 2.54 mm pitch, 4P, TH	
Connector Part Number			PPTC041LFBN-RC	
Mating Connector Part Number			PRPC004SAAN-RC	
J7 Pinout				
Contact #	Signal	Type	Voltage	Description
1	RX_I	Output	N/A	In-phase signal
2	+5V	Power	5 VDC	Regulated 5 V DC
3	RX_Q	Output	N/A	Quadrature signal
4	GND	Ground	0 V	Ground
J8 Pinout				
Contact #	Signal	Type	Voltage	Description
1	AUDIO_R	Output	N/A	Audio right channel
2	AUDIO_L	Output	N/A	Audio left channel
3	GND	Ground	0 V	Ground
4	GND	Ground	0 V	Ground

Table 9: Subsystem C.1 Connectors

Connectors				
Connector Type			Molex 2.54 mm pitch, 4P, TH	
Connector Part Number			PPTC041LFBN-RC	
Mating Connector Part Number			PRPC004SAAN-RC	
J9 Pinout				
Contact #	Signal	Type	Voltage	Description
1	/TXEN	Output	3.3 V LVTTL	Active-low transmit enable
2	LO_F1_0	Output	3.3 Vpp unipolar	LO signal @ f_{LO}
2	LO_F1_90	Output	3.3 Vpp unipolar	LO signal @ f_{LO} with 90° phase shift
4	GND	Ground	0 V	Ground
J10 Pinout				
Contact #	Signal	Type	Voltage	Description
1	LO_F2	Output	N/A	LO signal @ f_2 (legacy)
2	+5V	Power	5 VDC	Regulated 5 V DC
3	+3.3V	Power	3.3 VDC	Regulated 3.3 V DC
4	GND	Ground	0 V	Ground

transmitter (UART). **These must be implemented in your PCB design, as these connections do not reside on the mainboard.** Note that the connection `LO_F2` on the PLL connector is not used this year (legacy connection).

Table 10: Subsystem C.1 JTAG Connector

Connectors				
Connector Type			Molex 2.54 mm pitch, 8P, TH	
Connector Part Number			PRPC008SAAN-RC	
Mating Connector Part Number			N/A	
JTAG Connector Pinout				
Contact #	Signal	Type	Voltage	Description
1	No Connect (NC)			
2	`+3.3V`	Power	3.3 VDC	Regulated 3.3 V DC
3	`GND`	Ground	0 V	Ground
4	`TDO`	Output	LVTTL	JTAG test data out
5	`TCK`	Input	LVTTL	JTAG test clock
6	`RST`	Output	LVTTL	Active-low reset signal from programmer
7	`TDI`	Input	LVTTL	JTAG test data input
8	`TMS`	Input	LVTTL	JTAG test mode select

The C.2 daughtercard implements the connections shown in Table 13.

Subsystem D Connections Subsystem D is not implemented by students. The connections in Table 14 are presented for information purposes.

Subsystem E Connections The connections for Subsystem E are summarized in Table 15.

4.2 Mechanical

This section specifies mechanical dimensions for each board, along with the connector locations relative to the centre of the connector. Additional details are provided in PDF drawings provided on Quercus.

4.3 Mainboard Mechanical

The mainboard is 8750 mil $\times$ 6200 mil [222.25 mm $\times$ 157.48 mm]. The layout of the mainboard can be seen in Figure 5. Note that the main board still includes legacy connections for the old implementation of Subsystem A, which used two daughtercards, while this year a single daughtercard will plug into the area for daughtercards A.1 and A.2. A detailed drawing (PDF) can be found on Quercus.

Table 11: Subsystem C.1 PLL Connector

Connectors				
Connector Type			Molex 2.54 mm pitch, 7P, TH	
Connector Part Number			PPTC071LFBN-RC	
Mating Connector Part Number			N/A	
PLL Connector Pinout				
Contact #	Signal	Type	Voltage	Description
1	`+3.3V`	Power	3.3 VDC	Regulated 3.3 V DC
2	`GND`	Ground	0 V	Ground
3	`SDA`	Bidirectional	LVTTL	I^2C data line
4	`SCL`	Output	LVTTL	I^2C clock line
5	`LO_F2`	Output	N/A	LO signal @ f_2 (legacy)
6	`LO_F1_90`	Output	3.3 Vpp unipolar	LO signal @ f_{LO} with $90°$ phase shift
7	`LO_F1_0`	Output	3.3 Vpp unipolar	LO signal @ f_{LO}

Table 12: Subsystem C.1 Serial Interface Connector

Connectors				
Connector Type			Molex 2.54 mm pitch, 7P, TH	
Connector Part Number			PRPC006SAAN-RC	
Mating Connector Part Number			N/A	
UART Connector Pinout				
Contact #	Signal	Type	Voltage	Description
1	`DTR`	Input	LVTTL	DTR signal from UART
2	`TXD`	Input	LVTTL	TXD signal from UART
3	`RXD`	Output	LVTTL	RXD signal to UART
4	`+3.3V`	Power	3.3 VDC	Regulated 3.3 V DC
5	No Connect (NC)			
6	`GND`	Ground	0 V	Ground

Table 13: Subsystem C.2 Connectors

Connectors				
Connector Type			Molex 2.54 mm pitch, 4P, TH	
Connector Part Number			PPTC041LFBN-RC	
Mating Connector Part Number			PRPC004SAAN-RC	
J11 Pinout				
Contact #	Signal	Type	Voltage	Description
1	ANT	Bidirectional	N/A	Antenna signal
2	ANT	Bidirectional	N/A	Antenna signal
3	GND	Ground	0 V	Ground
4	GND	Ground	0 V	Ground
J12 Pinout				
Contact #	Signal	Type	Voltage	Description
1	RX_SIG	Input	N/A	RX signal
2	+5V	Power	5 VDC	Regulated 5 V DC
3	/TXEN	Output	3.3 V LVTTL	Active-low transmit enable
4	GND	Ground	0 V	Ground
J13 Pinout				
Contact #	Signal	Type	Voltage	Description
1	PA_OUT	Input	N/A	TX signal from power amplifier
2	PA_OUT	Input	N/A	TX signal from power amplifier
3	GND	Ground	0 V	Ground
4	GND	Ground	0 V	Ground

Table 14: Subsystem D Connectors

Connectors				
Connector Type			Molex 2.54 mm pitch, 4P, TH	
Connector Part Number			PPTC041LFBN-RC	
Mating Connector Part Number			PRPC004SAAN-RC	
J14 Pinout				
1	`TX_I`	Input	N/A	Baseband in-phase signal
2	`TX_Q`	Input	N/A	Baseband quadrature signal
3	`GND`	Ground	0 V	Ground
4	`GND`	Ground	0 V	Ground
J15 Pinout				
Contact #	Signal	Type	Voltage	Description
1	`/TXEN`	Input	3.3 V LVTTL	Active-low transmit enable
2	`LO_F1_0`	Output	3.3 Vpp unipolar	LO signal @ f_{LO}
2	`LO_F1_90`	Output	3.3 Vpp unipolar	LO signal @ f_{LO} with $90°$ phase shift
4	`GND`	Ground	0 V	Ground
J16 Pinout				
Contact #	Signal	Type	Voltage	Description
1	`PA_IN`	Output	N/A	Signal to be input to PA
2	`+5V`	Power	5 VDC	Regulated 5 V DC
3	`+12V`	Power	$12 - 18$ VDC	Input power $12 - 18$ VDC
4	`GND`	Ground	0 V	Ground

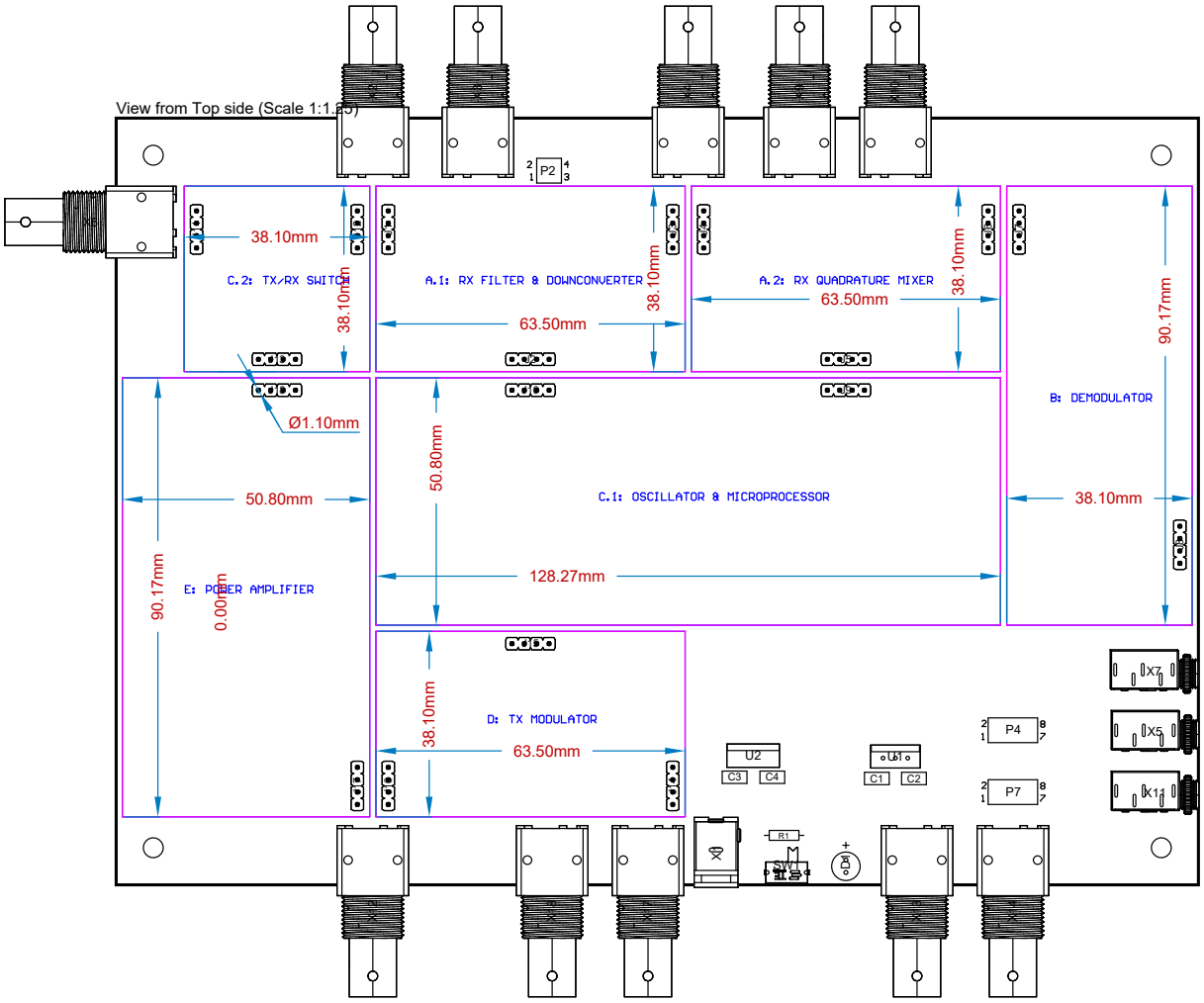

Figure 5: Mainboard mechanical layout with subsystems and connectors presented

Table 15: Subsystem E Connectors

Connectors				
Connector Type			Molex 2.54 mm pitch, 4P, TH	
Connector Part Number			PPTC041LFBN-RC	
Mating Connector Part Number			PRPC004SAAN-RC	
J17 Pinout				
Contact #	Signal	Type	Voltage	Description
1	PA_IN	Input	N/A	Signal to be input to PA
2	/TXEN	Input	3.3 V LVTTL	Active-low transmit enable
3	GND	Ground	0 V	Ground
4	GND	Ground	0 V	Ground
J18 Pinout				
Contact #	Signal	Type	Voltage	Description
1	PA_OUT	Input	N/A	Amplified RF signal, minimum 1 W
2	+5V	Power	5 VDC	Regulated 5 V DC
3	+12V	Power	$12 - 18$ VDC	Input power $12 - 18$ VDC
4	GND	Ground	0 V	Ground

4.4 Subsystem A Mechanical

Recall from Section 4.1.3 that Subsystem A was historially realized on two daughtercards, A.1 and A.2, which were arrayed on the mainboard as shown in Figure 6. These two boards interfaced to the mainboard through six connectors (J1–J6). As discussed in Section 4.1.3, this is no longer necessary. Subsystem A is now to be implemented on a single daughtercard, and **only connectors J1, J5, and J6 need to be used in the design.**

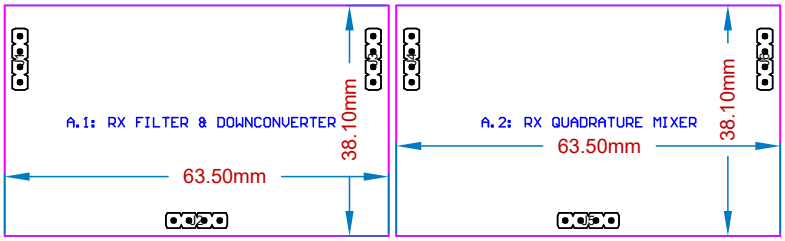

Figure 6: Legacy Subsystem A daughtercard configuration

The new Subsystem A board size must fall within envelope previous occupied by daughtercards A.1 and A.2. Figure 7 provides an envelope of Subsystem A with the connectors indicated. A detailed drawing (PDF) can be found on Quercus. The 3 connections to J1, J5, and J6 should be located according to this drawing. The other connectors shown in Figure 6 do not need to be implemented.

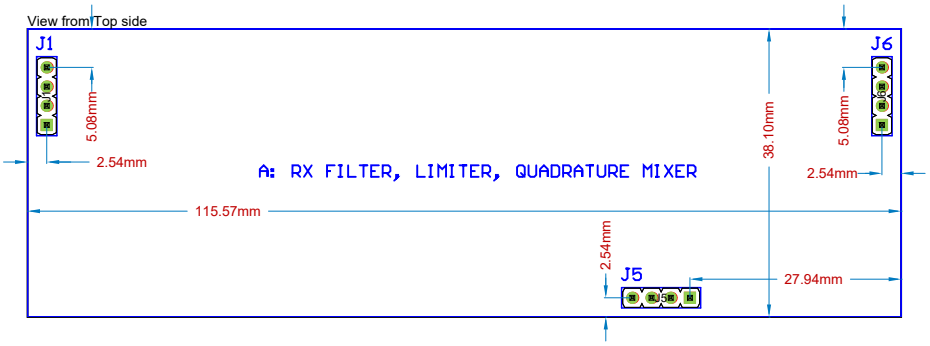

Figure 7: Subsystem A envelope with connector locations indicated

4.5 Subsystem B Mechanical

It is not necessary to design a Subsystem B daughtercard, as you will already have to design an auxiliary board that mates with the DE10-Lite board to facitate connections to peripherals. The recommended way to interface the auxiliary board to the mainboard is through BNC connectors `X13` and `X14`. The BNC connectors can be adapted to RCA jacks for coupling to a stereo audio cable with a 3.5 mm audio connector on the other end for interfacing with the ADC. For audio output from the DAC, amplified speakers will be provided that have a 3.5 mm audio connector to be plugged into the DAC.

If you decide for some reason to build a Subsystem B board that fits on the mainboard, the mechanical details are as follows. The Subsystem B board size must fall within 1500 mil$\times 3550$ mil [38.1 mm $\times$ 90.17 mm]. There are 2 connectors between Subsystem B and the mainboard: J7 and J8. Figure 8 provides an envelope of Subsystem B with the connectors indicated. A detailed drawing (PDF) can be found on Quercus.

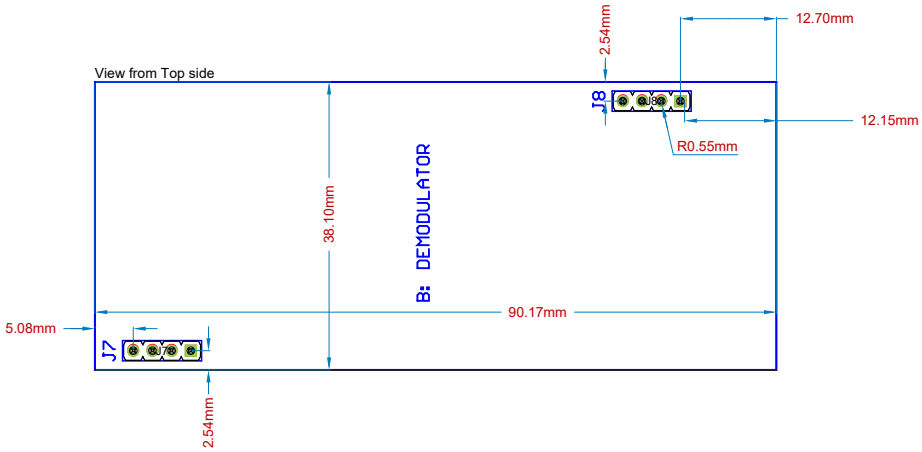

Figure 8: Subsystem B envelope with connector locations indicated

4.6 Subsystem C Mechanical

There are two boards required for Subsystem C: C.1 – Oscillator and Microprocessor, and C.2 – TX/RX Switch board. Both boards are defined below.

4.6.1 C.1 – Oscillator and Microprocessor

The Subsystem C.1 board size must fall within 5050 mil $\times$ 2000 mil [128.27 mm $\times$ 50.8 mm]. There are 2 connectors between Subsystem C.1 and the mainboard: J9 and J10. Figure 9 provides an envelope of Subsystem C.1 with the connectors indicated. A detailed drawing (PDF) can be found on Quercus.

A hole is provided along the bottom edge to mount a standoff to support the board, with the bottom of the standoff resting against the mainboard. There is no corresponding hole on the mainboard for fastening the standoff to the mainboard.

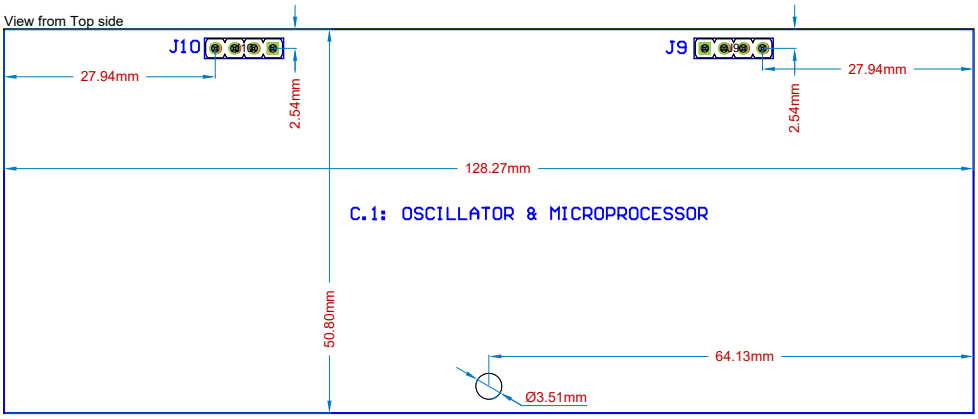

Figure 9: Subsystem C.1 envelope with connector locations indicated

4.6.2 C.2 – TX/RX Switch

The Subsystem C.2 board size must fall within 1500 mil $\times$ 1500 mil [38.1 mm $\times$ 38.1 mm]. There are 3 connectors between Subsystem C.2 and the mainboard: J11, J12, and J13. Figure 10 provides an envelope of Subsystem C.2 with the connectors indicated. A detailed drawing (PDF) can be found on Quercus.

4.7 Subsystem D Mechanical

Subsystem D is not designed by students. Information is provided here for historical purposes.

The Subsystem D board size must fall within 2500 mil $\times$ 1500 mil [63.5 mm $\times$ 38.1 mm]. There are 3 connectors between Subsystem D and the mainboard: J14, J15, and J16. Figure 11 provides an envelope of Subsystem D with the connectors indicated. A detailed drawing (PDF) can be found on Quercus.

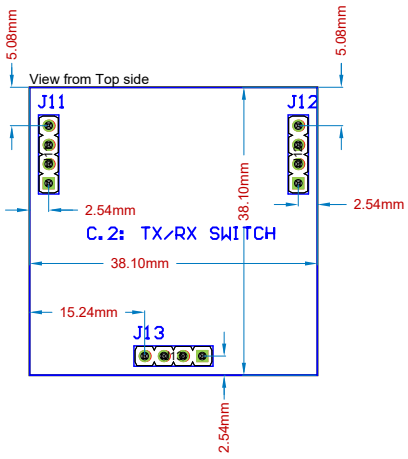

Figure 10: Subsystem C.2 envelope with connector locations indicated

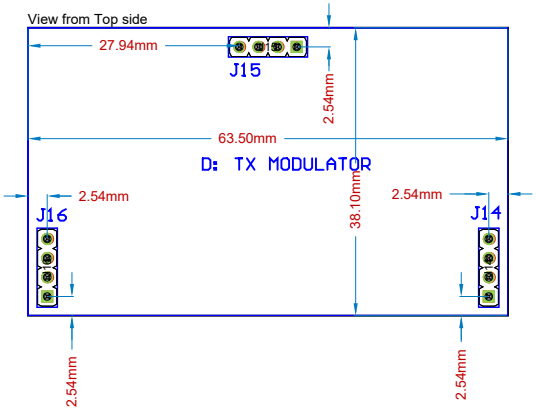

Figure 11: Subsystem D envelope with connector locations indicated

4.8 Subsystem E Mechanical

The Subsystem E board size must fall within 2000 mil $\times$ 3550 mil [50.8 mm $\times$ 90.2 mm]. There are 2 connectors between Subsystem E and the mainboard: J17 and J18. Figure 12 provides an envelope of Subsystem E with the connectors indicated. A detailed drawing (PDF) can be found on Quercus.

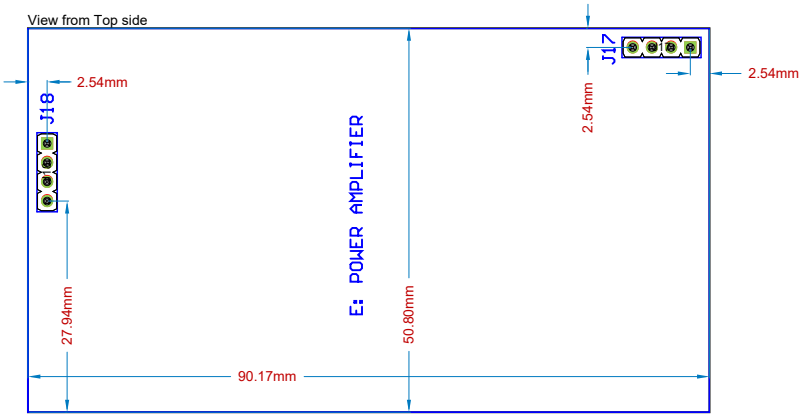

Figure 12: Subsystem E envelope with connector locations indicated

4.9 Power Architecture

Power is regulated and distributed from the power supply through the mainboard to all subsystem boards. Each subsystem board will only be able to draw a limited amount of power to perform the desired function.

The mainboard requires a single DC voltage to power the complete FLRTRX. The mainboard regulates this DC input to two voltage levels that are required by the remaining subsystem circuits. Details are as follows:

+12V Voltage Rails:

Input Power: 12.0 to 18.0 VDC input, 2 A maximum, regulated but variable

Regulated Voltage Rails:

5 V $\pm\, 5\%$ @ 1.5 A maximum output

3.3 V $\pm\, 5\%$ @ 1.5 A maximum output

Appendix: Computer Interface to the FLRTRX Using a UART and CAT Commands

The CAT (computer-aided transceiver) protocol is a text-based system that allows for communication with radio equipment [1]. In ECE295, we will use it to control the FLRTRX using software on a PC. This software allows for adjusting the oscillator frequencies and the transmit/receive state with a GUI (graphical user interface). CAT uses the serial protocol in order to send the ASCII characters making up the text commands. This is then translated to universal asynchronous receiver/transmitter (UART) protocol using the FT232 module for the microcontroller, which is a daughtercard that interfaces with Subsystem C. A diagram showing the basic configuration is shown in Figure 13.

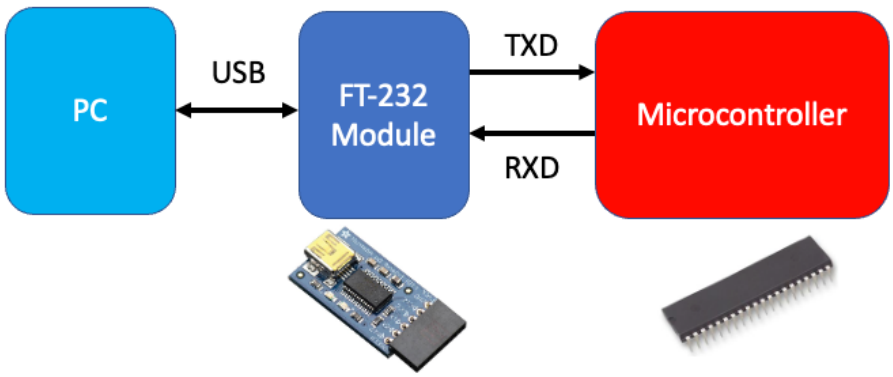

Figure 13: Basic configuration for connecting PC with MCU via the FT232 module [2, 3].

Basics of CAT

Similar to PyVISA that you used in SL3, CAT works on a set and query system. The transmitter (the PC) sets and queries, while the tranceiver (the FLRTRX) performs the actions accociated with the sets and responds to queries. Values, such as the transmit/receive state, are set by including them after the two letter command, such as `TX1;` or `TX0;`. The state can be queried by not including any values and just terminating with a semicolon, such as `TX;`. As such, the FLRTRX needs to be able to

1. receive the incoming string;
2. parse the first two letters to determine the appropriate command;
3. perform the appropriate action (send a response for a query, perform the value change for a command).

A example exchange using CAT is shown below with the "$>$" denoting commands sent by the transmitter.

>TX;
TX0;
>TX1;
>TX;
TX1;

Here, the transmitter is **querying** (`TX;`) the transmit/receive state of the receiver, which is currently in the receive state, denoted by `TX0;`. It then **sets** the receiver to transmit mode with `TX1;`. Following this, the transmitter **queries** (`TX;`) the receiver to confirm that it is indeed in the transmit mode (`TX1;`). Note that each statement **must** be terminated with a semicolon (`;`).

Key Commands

The commands that we will use are that of the Yaesu FT-991A, which can be viewed in the reference manual here. There are many commands, however we will restrict ourselves to `TX`, `FA`, `FB`, and `IF`. Their details can be found in Table 16.

Table 16: Important CAT Commands [1]

Command Name	**TX**
Description	Set the state of the receiver as either transmit (1) or receive (0)
Set	`TX`[1b]`;` where [1b] is a single binary digit equal to `0` or `1` ex. `TX0;` or `TX1;`
Query	`TX;`
Response	`TX`[1b]`;` where [1b] is a single binary digit equal to `0` or `1` ex. `TX0;` or `TX1;`

Command Name	**FA**
Description	Set FA oscillator frequency (LO_F1)
Set	`FA`[9i]`;` where [9i] is a 9-digit integer in Hz. Note that all nine digits must be used so setting FA to 10 kHz would be `FA000010000;`.
Query	`FA;`
Response	`FA`[9i]`;` where [9i] is a 9-digit integer in Hz.

Command Name	**FB**
Description	Set FB oscillator frequency (LO_F2)
Set	`FB`[9i]`;` where [9i] is a 9-digit integer in Hz. Note that all nine digits must be used so setting FB to 10 kHz would be `FB000010000;`. Also note that there are no requirements to output this second frequency, just to respond to queries.
Query	`FB;`
Response	`FB`[9i]`;` where [9i] is a 9-digit integer in Hz.

Command Name	**IF**
Description	Information command to give a status update on the system.
Set	N/A
Query	`IF;`
Response	`IF`[3i]**[9i]**[13i]`;` where **[9i]** is a 9-digit integer in Hz corresponding to frequency the of `FA`. The rest should be left as all zeros.

References

[1] *CAT Operation Reference Manual*, Yaesu. [Online]. Available: https://www.yaesu.com/downloadFile.cfm?FileID=13370&FileCatID=158&FileName=FT%2D991A%5FCAT%5FOM%5FENG%5F1711%2DD.pdf&FileContentType=application%2Fpdf#page=1&zoom=auto,-214,61

[2] Newark. Chip adapter, ftdi friend. [Online]. Available: https://canada.newark.com/adafruit/284/adapter-ftdi-ft232rl-chip/dp/53W5825

[3] element14. Atmega324p-20pu. [Online]. Available: https://my.element14.com/microchip/atmega324p-20pu/mcu-8bit-atmega-20mhz-dip-40/dp/1455110