



T5830P/T5830PES
Memory Test System
Product Description

Manual Number

8703781-02

Applicable Systems
T5830P
T5830PES

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Revision History

Rev.	Date	Relevant item	Change
01	Mar 17/17		
02	Oct 13/17	2.2.1 Algorithmic Pattern Generator	Descriptions have been modified.
		2.7.1 Pin Electronics	Figure 2-20 has been modified.
		2.7.2 Test Head Channel Configuration	Table 2-6 has been modified.
		5.1.2.1 Power Requirements (for T5830P)	Table 5-2 has been modified.
		5.1.3.1 Air Conditioning Requirements (for T5830P)	Table 5-4 has been modified.
		5.1.6 System Weight	Table 5-7 has been modified.
		5.1.10 Cooling Water (T5830P)	Descriptions have been modified. Figure 5-11 has been modified.
		9.1 System Specifications	Table 9-4 and Table 9-6 have been modified.
		9.6.4 PCON Capacitance	Added.

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1. Introduction

1.1 General Overview

The T5830P is a memory test system that mainly targets flash memory devices. This test system adopts a test array architecture to reduce the flash memory device testing time. In addition, this test system can test up to 1152 flash memory devices in parallel in a wafer test, achieving high productivity.

For functional tests at a maximum test rate of 150 MHz (6.67 ns), the T5830P assures high timing accuracy, repeatability, and failure detection capability. Also, a function allowing the testing of flash memory devices in parallel is provided as standard.

In addition to being a high-integrity product, the design of this environmentally friendly test system allows the elimination of toxic substances during the separation and disassembly of test system parts to be disposed of.



Figure 1-1 T5830P Memory Test System

The T5830PES memory test system has achieved miniaturization, noise-reduction, and low power consumption while retaining the functions and performance of the T5830P memory test system.

The T5830PES is an appropriate test system for personal use because it provides performance and functions that are equivalent to those of the T5830P, including functional testing performed at a maximum test rate of 150 MHz (6.67 ns), which is the basic performance of the T5830P, high timing accuracy, repetition accuracy, and high failure-detection performance.

Therefore, the T5830PES can reduce the time required for device development and allows products to be developed that match Time To Market (TTM) without introducing large functional-test equipment for design evaluation.

Just like the T5830P, the T5830PES uses FutureSuite, which allows test programs developed for the T5830PES to be seamlessly developed into parallel test programs for the T5830P. To enhance operability, a GUI (graphical user interface) is employed to facilitate file operations and allow application software to be activated by just clicking desktop icons. For test programs, both the industry standard C language and conventional ATL language can be used.

Connecting to a network is possible as before, which leads to an efficient improvement in device evaluation/analysis and feedback to the production line.



Figure 1-2 T5830PES Memory Test System

1.2 System Features

This test system provides a high degree of test reliability, failure detection capability, and evaluation performance of the overall device characteristics through integration of various software packages that operate on a general-purpose OS.

The main features of this test system are as follows.

1.2.1 Flexible Algorithmic Pattern Generator (ALPG)

When testing VLSI memory devices with increased capacity, a more flexible and powerful algorithmic pattern generator is required for obtaining high failure detection capability while reducing the testing time.

For functional test patterns, enhancement of the failure detection capability and reduction of testing time are in a mutually conflicting relationship. It is therefore important to reduce testing time without deteriorating the failure detection capability, by generating test patterns aimed at internal structures such as the memory circuit structure, memory device structure, and layout of memory cells, or by executing a partial test in which cell blocks are divided.

The algorithmic pattern generation mechanism of this test system can generate complicated test patterns up to 150 MHz without dummy cycles, focused on the partial test and memory internal structure. In addition, various types of patterns (N, N3/2, N2, and N3) can be generated without dummy cycles under microprogram control.

The address space consists of 48 lines, X=24 and Y=24, making it possible to generate 256 terawords of address patterns with X and Y addresses alone.

Data patterns can be generated by using two sets of 36-bit test patterns and address functions, and by inverting data by using address areas.

This test system has a match function that can control a microprogram sequence at high speed depending on the memory device data output status. Therefore, devices such as flash memory with a variable number of data-writing and data-erasing times can be tested at high speed.

1.2.2 Timing System

The test frequency can be set within a range of 10 μ s (100 kHz) to 6.67 ns (150 MHz).

The clock rate and each timing edge can be selected on the fly by selecting one of the 16 preset timing sets.

Every formatter channel has two types of timing clocks (BCLKn and CCLKn) used for independent driver waveforms. Up to 16 of each timing clock can be used.

1.2.3 Waveform Shaping

This test system can generate various types of driver waveforms.

These waveforms are classified into the basic groups: NRZ, RZ, and FIX.

1.2.4 Logical Comparison

In one cycle, logical comparison can be implemented by two edge strobes.

1.2.5 Flash Memory Device Parallel Test Function

This test system has the following functions for each DUT to test flash memory devices easily at high speed:

- Prevention of excessive writing or erasing

When the verification result is Pass for a write or erase test of a flash memory device, driver output signals applied to devices (such as Write enable and Chip enable) and logical comparisons can be prohibited.

- Pass/Fail judgments according to write and erase counts

In this test system, Pass/Fail judgments can be performed by using the retry counter.

The counter (counting and clearing) can be controlled by a pattern program.

Pass/Fail judgments can be easily performed according to the retry counts of write and erase tests of a flash memory device.

- Bad Block management during a test

Logical comparison results in each block of a NAND type flash memory device can be accumulated and managed as Bad Block. Based on the accumulated Bad Block information, logical comparison masking and excessive writing or erasing can be prevented.

By comparing the number of Bad Blocks with the allowable value, PASS/FAIL can be judged for DUTs in real time.

1.2.6 Pattern Selection Function Unlimited for All Pins

The programmable data selector provided for all pins allows unlimited selection of addresses, data, and control signals generated by the ALPG.

This function enables unrestricted interaction between test pins and test data, removes limitations on program creation, and improves program productivity.

Free combinations of multiplexed addresses and data enable a wide variety of device tests.

1.2.7 Test Station

The T5830P uses only one test station, which can be configured with a maximum of 32 sites.

The T5830PES, on the other hand, uses only one test station, which can be configured with a maximum of two sites. One TOM800M module (TOM) and one HVLVDR48 module (HVLVDR) are mounted.

1.2.8 Pin Electronics

Each pin electronics channel has the following feature:

- Driver/single comparator of I/O common configuration (IO CH)

1.2.9 DC Parametric Test for Parallel Testing

Up to 384 DC test units, which test multiple DUTs in parallel, can be installed per test station. This reduces the DC measurement time for parallel testing. These DC test units can be treated as a single unit in a program so parallel testing can be programmed easily.

The T5830PES can be equipped with up to 24 DC test units.

1.2.10 Powerful Failure Analysis System and Memory Repair Analysis Tool

The fail-bit analysis tool for analyzing failed cells of a DUT has a capacity of up to 12 Gb for each site.

The MRA hardware in this system can obtain repair solutions for all test devices at high speed.

Furthermore, powerful optional software support enables the tool to display a bit map according to the layout of the device cells.

1.2.11 Wafer Probing Test

The test station is designed so that it can be connected between the wafer prober and driver/comparator via the shortest route. The Advantest-specific device interface assembly is compatible with major wafer prober products.

1.2.12 Automatic Calibration

With online automatic timing calibration, this test system assures a driver skew of 360 ps p-p, comparator skew of 360 ps p-p, and overall timing accuracy of ± 400 ps. To achieve the highest possible accuracy, they are automatically calibrated for each pin when a test is executed, according to the device structure and test conditions.

The overall timing accuracy includes all of the following timing errors:

- Clock generator nonlinearity error
- Pin-to-pin skew of driver and comparator
- Clock-to-clock skew
- Format skew between drivers
- Jitter including mutual interference between clocks
- Response ambiguity of comparator
- Comparator VOH response error

1.2.13 RASIS (Reliability, Availability, Serviceability, Integrity, and Security)

High serviceability, achieved by adoption of a self-diagnostics concept, has taken the full interchangeability of boards into consideration from the design stage. As a result, faulty boards can be detected among the boards whose number is indicated by the diagnostic program.

To ensure reliable, highly accurate, and stable test system operations, the following parts and functions are contained in the system:

- Temperature monitor
- Standard voltage source for diagnostics
- Standard resistor group for diagnostics
- Quartz clock oscillator for diagnostics
- Time and voltage monitor
- Automatic timing correction function
- Various self-diagnostic functions

2. System Hardware

[Figure 2-1](#) shows a block diagram of this test system.

This test system consists of the following units:

- Algorithmic pattern generator (ALPG)
- Programmable data selector (PDS)
- Timing generator (TG)
- Format control and sense control (FCSC)
- Pin electronics and voltage I/O (PE & VIO)
- DC parametric test unit (DC)
- Programmable power supply for devices (PPS)
- Fail memory (FM)
- Memory repair analysis unit (MRA)

This test system is configured to support a maximum of 32 sites, each of which is controlled by independent test processors.

Because these test processors are collectively controlled by the system controller, they do not need to be controlled individually for each site.

The T5830PES is configured with two sites.

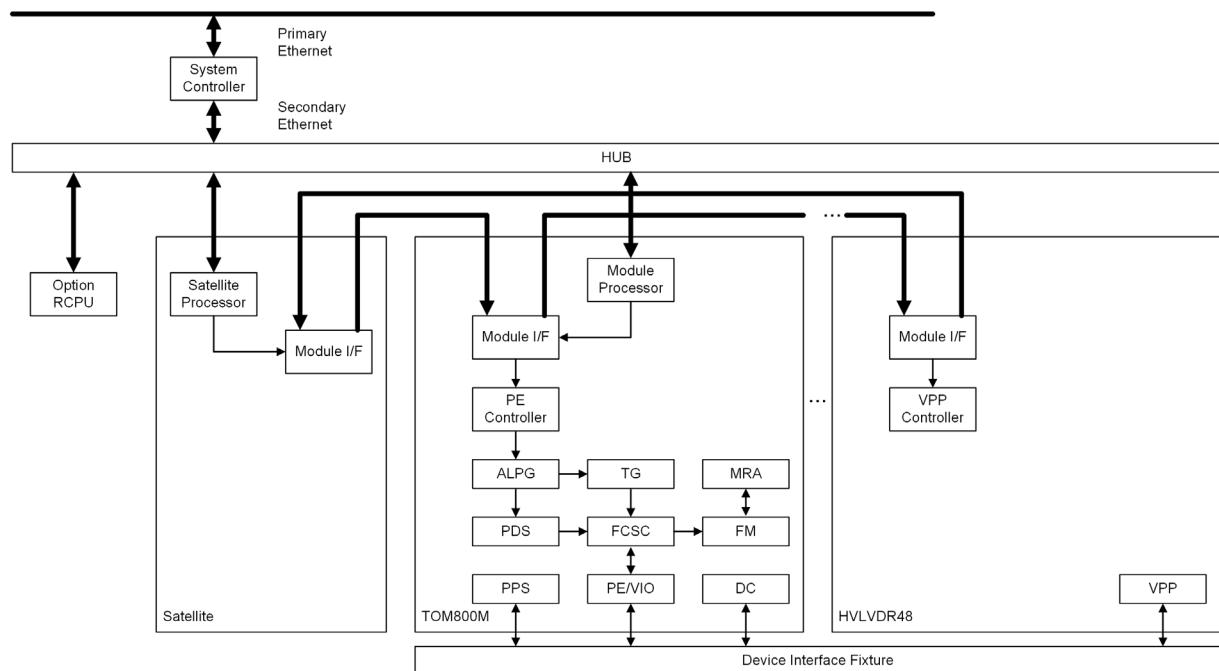


Figure 2-1 Block Diagram (T5830P)

2.1 System Bus

This test system has a universal data bus structure using a high-speed tester control bus.

The high-speed tester control bus is used for controlling data transfer between the tester processor (satellite processor or module processor) and each unit in the test system. It can transfer unit setting data for functional tests, test conditions for DC parametric tests, and results of tests.

All the data, control, and status registers connected to this bus have specific individual addresses. Consequently, the tester processor can handle the transfer of control information and memory test patterns as only data transfers between memory spaces.

2.2 Test Vector Generation

The test vector generator in this test system has the architecture shown in [Figure 2-2](#) which enables it to test high-capacity and complicated memory devices efficiently.

The programmable data selector (PDS) consists of a pin data multiplexer and pin control data multiplexer. It selects the test vectors required for the pin electronics unit.

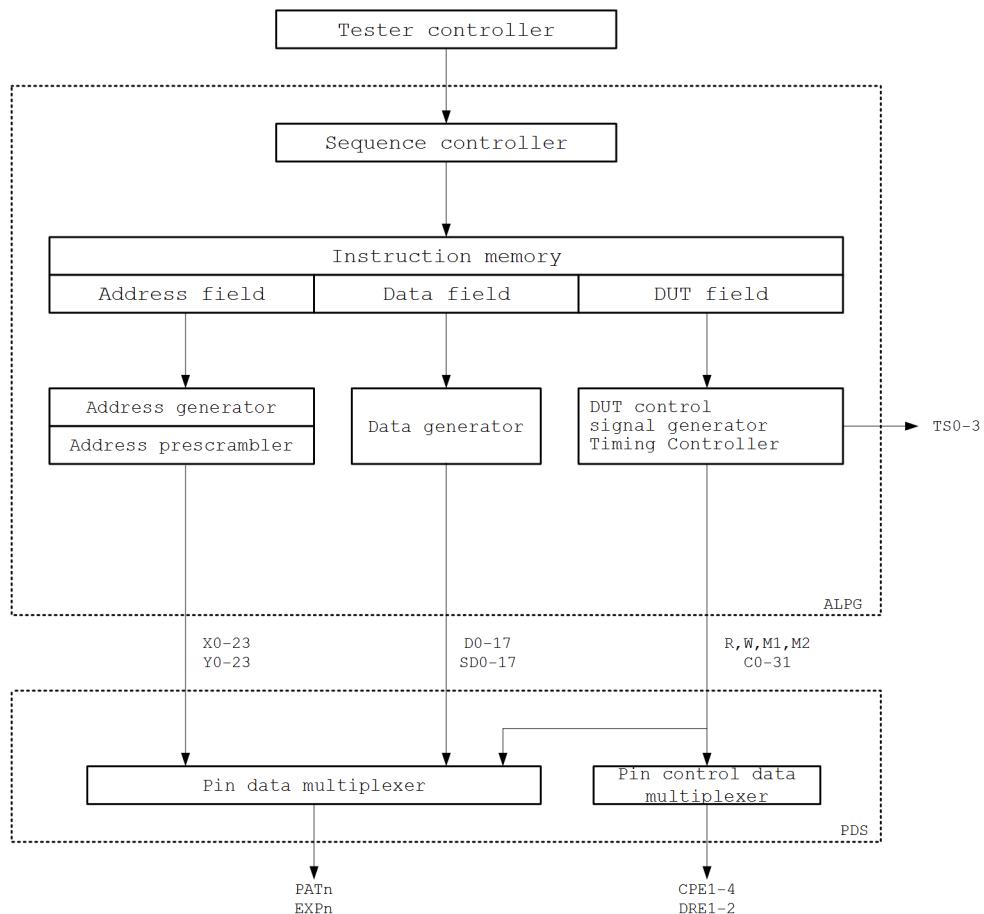


Figure 2-2 Test Vector Generation Mechanism

2.2.1 Algorithmic Pattern Generator

The algorithmic pattern generator (ALPG) consists of the following function blocks ([Figure 2-3](#)):

<ALPG>

- Sequence controller
 - Instruction memory
 - Address generator
 - Address prescrambler
 - Data generator
 - Timing controller
 - DUT control signal generator
 - Tester controller

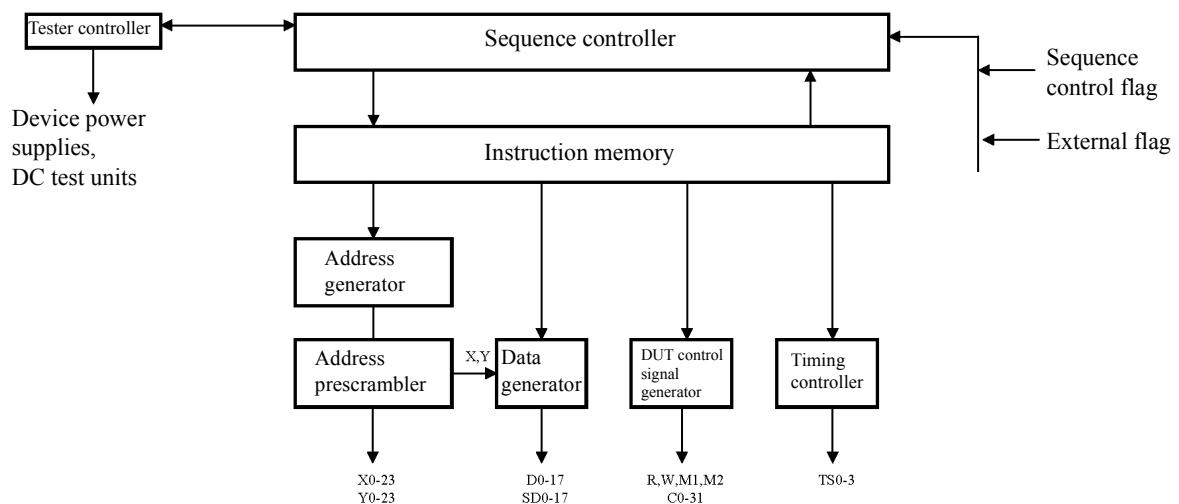


Figure 2-3 Algorithmic Pattern Generator

(1) Sequence controller

The ALPG sequence controller consists of the following registers and instruction memory. It controls a test pattern generation sequence by using instructions such as loop, conditional branch, subroutine jump, and flag sense stored in instruction memory ([Figure 2-4](#)).

WCS	(instruction memory):	4 kilowords
PC	(program counter):	12 bits
STA	(start address register):	12 bits
BAR	(branch address register):	12 bits
JAR	(jump address register):	12 bits
STK	(stack register):	12 bits
IDXRn	(n=1-8) (index register R):	32 bits
IDXWn	(n=1-8) (index register W):	32 bits
IDX	(index register):	32 bits
DFLG	(data inversion flag):	1 bit
CFLGn	(n=1-16) (sequence control flag):	1 bit
FLAG	(match flag):	1 bit

Loops and subroutines can each be nested up to eight levels deep.

The SET instruction can be used to set any data desired for index registers and branch addresses.

The OUT instruction can be used to change setting conditions such as device power supply, synchronizing with pattern generation.

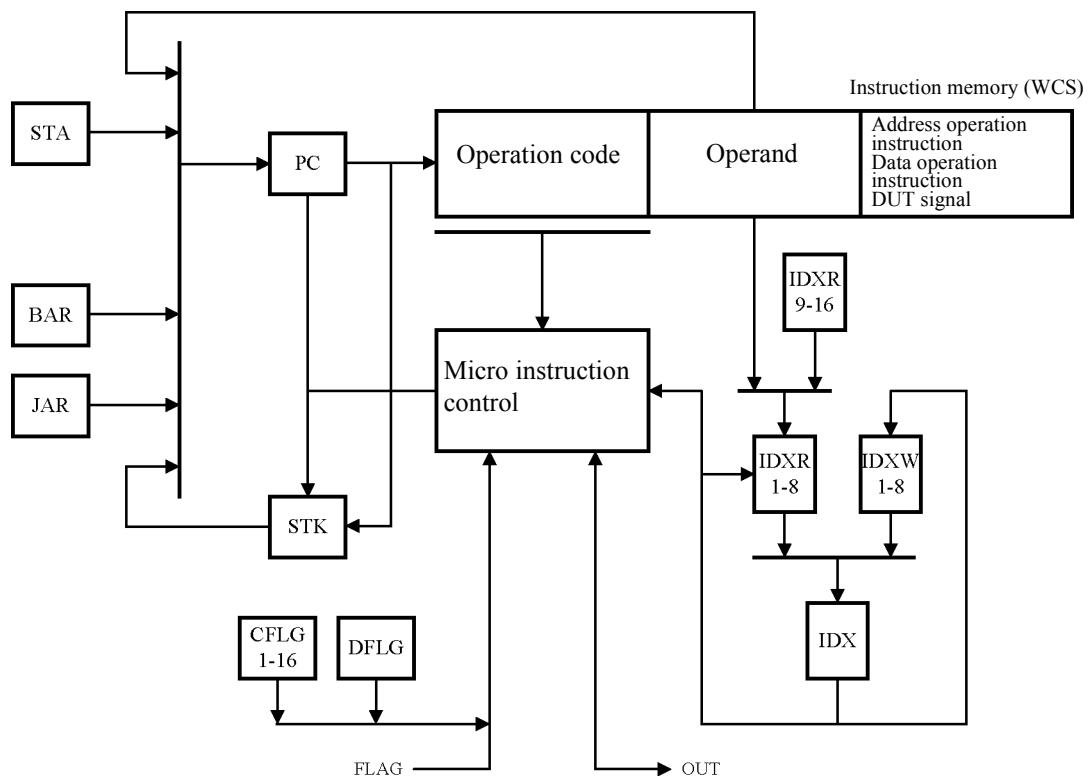


Figure 2-4 Sequence Controller

(2) Address generator

The address generator creates the address patterns applied to DUTs by using address operation instructions stored in instruction memory. It consists of the following registers ([Figure 2-5](#)):

- X (X address): 24 bits
- Y (Y address): 24 bits
- Z (for partial addresses): 24 bits

X registers include XH, XB, XC, XS, XK, XR1 to XR4, XOS, and XT1 to XT15. Y registers include YH, YB, YC, YS, YK, YR1 to YR4, YOS, and YT1 to YT15. X and Y address patterns are generated by executing the operations that use these registers.

In addition, D1A to D1H and D2A to D2D registers are provided as operation registers common to XB, XC, XS, XK, and XR1 to XR4 as well as YB, YC, YS, YK, and YR1 to YR4. Also, D3 and D4 registers are provided as operation registers common to XC, XS, XK, and XR1 to XR4 as well as YC, YS, YK, and YR1 to YR4. The D3 register can perform increment, decrement, and left shift operations. The D4 register can perform right and left shift operations.

Z registers are used to generate block addresses for a partial test. They include the ZH register that initializes Z registers and also include the ZD operation register.

Any bits of the data generated by address operation instructions can be inverted in real time by address inversion instructions by using XCMR, YCMR, and ZCMR.

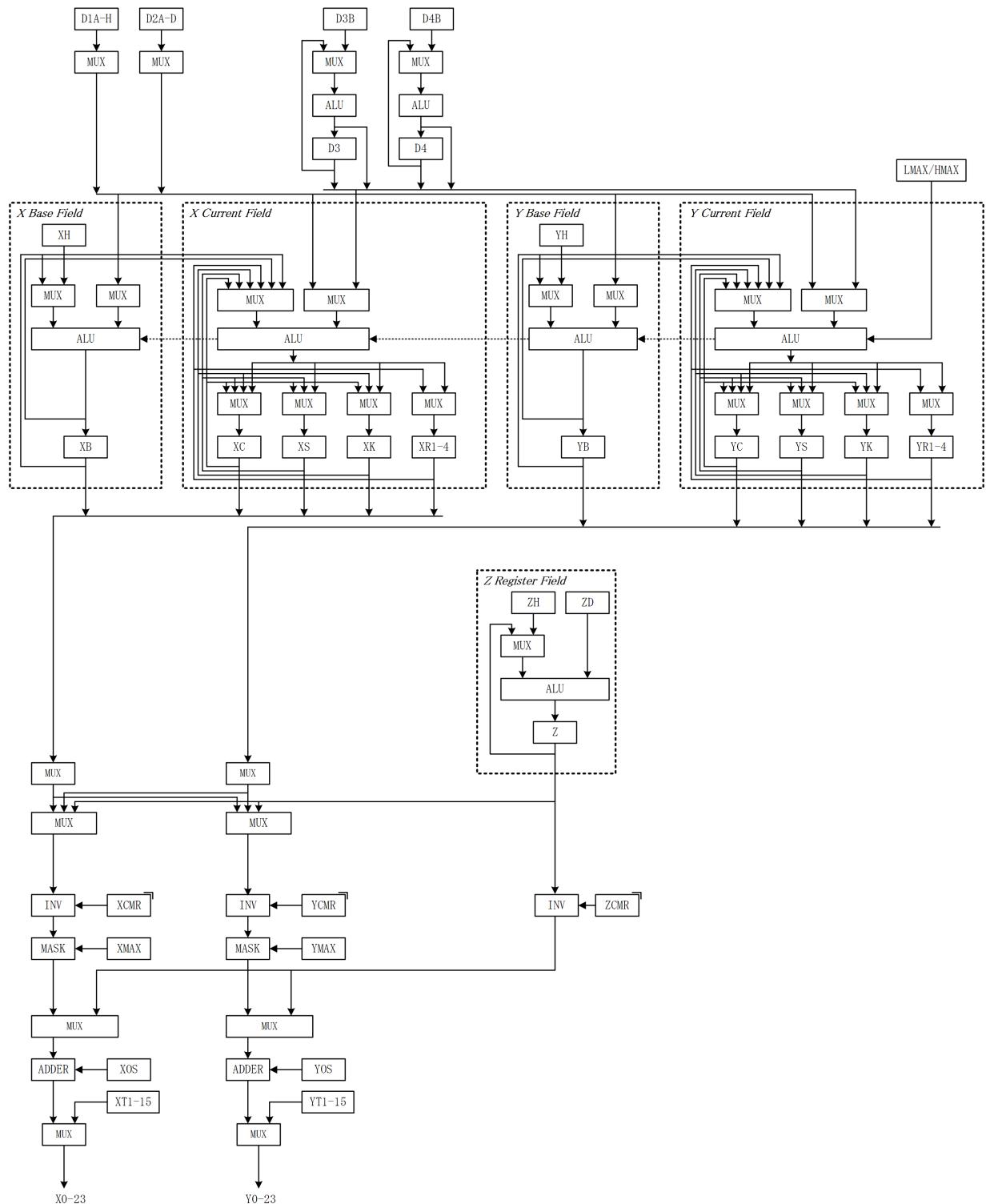


Figure 2-5 Address Generator

(3) Address prescrambler

The address prescrambler consists of the following function blocks:

- X Pre-SCRAM EOR-NOT
- Y Pre-SCRAM EOR-NOT
- Burst-SCRAM ADDER

X Pre-SCRAM EOR-NOT and Y Pre-SCRAM EOR-NOT convert X and Y address patterns by using a combinational circuit of exclusive OR and logical inversion.

Burst-SCRAM ADDER provides a function that generates burst addresses by the adder circuit.

This function adds 1 to the Y address and then outputs it.

(4) Data generator

The data generator creates both write and expected data applied to DUTs, by using data operation instructions stored in instruction memory. The data generator consists of the following registers, area inversion memory, and address function data generator ([Figure 2-6](#)):

- TP1 (data pattern register 1): 36 bits
- TP2 (data pattern register 2): 36 bits
- DCMR1 (data inversion selection register 1): 36 bits
- DCMR2 (data inversion selection register 2): 36 bits

The TP1 register consists of registers TPH1A to TPH1D and D5A to D5D, and the TP2 register consists of registers TPH2A to TPH2D and D6A to D6D. Executing operations that use these registers generates 36-bit two-line data patterns.

When data is generated by data operation instructions, any bits of the data can be inverted in real time by using DCMR1 and DCMR2.

The contents of the TP1 and TP2 registers can be inverted and then output by using data generated as X and Y address functions (FP). Using two FP generators enables individual inversion control of write and expected data in the first and second half of a DDR test. The following 12 types of address functions are provided:

- Fix"0"
- Masked Parity
- Diagonal
- Diagonal2
- Inverted Diagonal
- Inverted Diagonal2
- Masked Diagonal
- Masked Row Bar
- Masked Column Bar
- Checker Board
- AND for Masked Row Bar/Masked Column Bar
- Universal FP

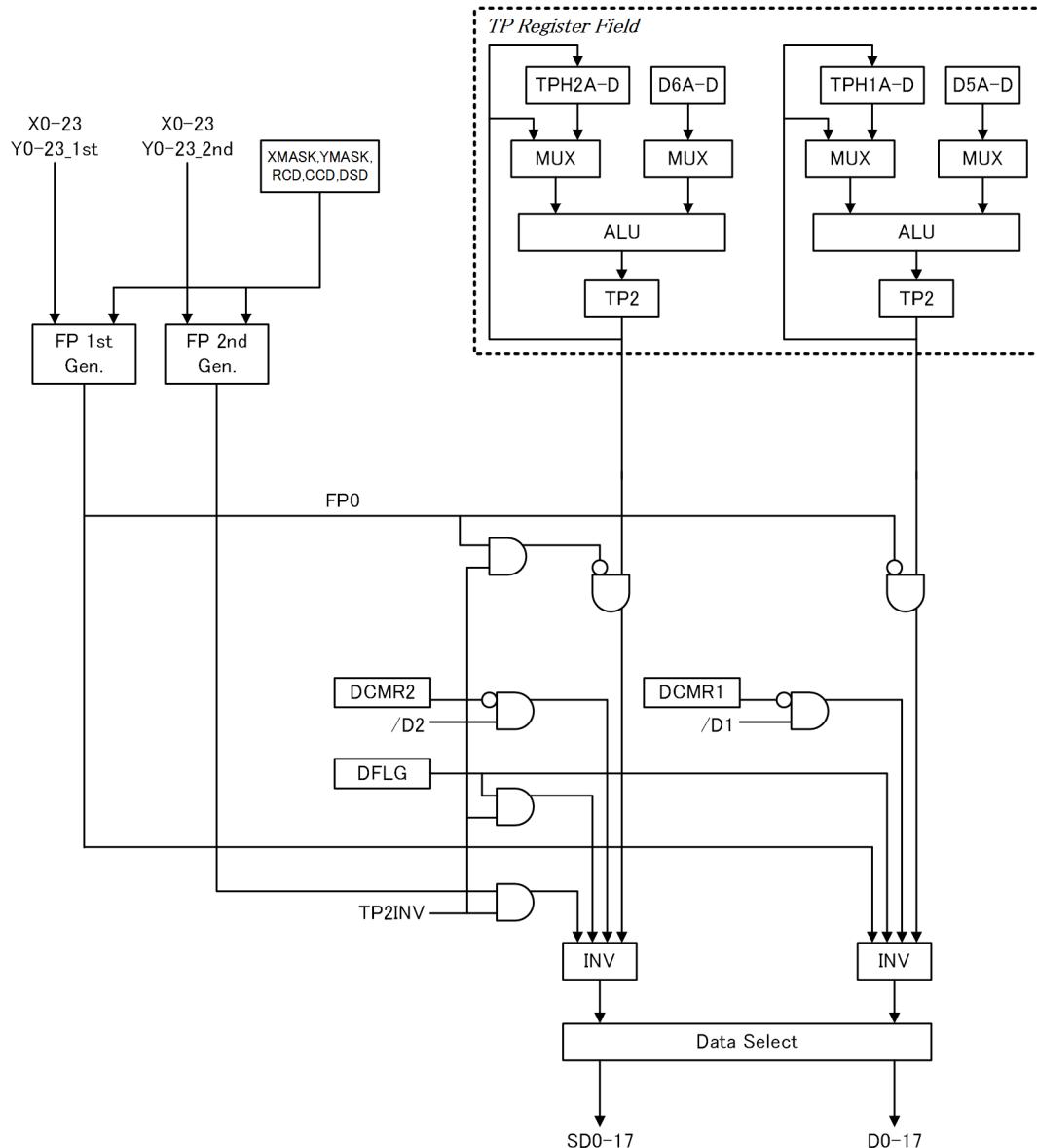


Figure 2-6 Data Generator

(5) Timing controller

The timing controller selects one of the previously set 16 sets of test rates and clock delay values in real time.

(6) DUT control signal generator

The DUT control signal generator creates DUT control terminal signals such as R/W, CS, and OE, comparator comparison control signal, and R, W, M1 to M2, and C0 to C31 DUT control patterns used to switch the driver on and off.

2.2.2 Data Buffer Memory (DBM)

The data buffer memory (DBM) generates patterns for a random logic test.

Table 2-1 DBM Pattern Generation Data

Pattern generation data	Maximum operating frequency	Memory capacity
All pins + DRE2 bit + CPE4 bit	150 MHz	64 megawords

2.2.2.1 Buffer Memory

The buffer memory (BM) generates patterns for a random logic test.

Table 2-2 BM Pattern Generation Data

Pattern generation data	Memory capacity
All pins + DRE2 bit + CPE4 bit	32 kilowords

The relationship between DBM and BM is shown in [Figure 2-7](#).

Even when patterns are generated by the DBM, the data is temporarily stored in the BM. Therefore, the DBM and BM cannot be used as independent memories.

For this reason, the maximum number of words of patterns that can be generated at once is the same as the BM memory capacity.

Patterns for a random logic test, which are stored in the DBM in advance, are stored in the BM by the DB-MXFER instruction specified in the pattern program and then they are generated by the BMINC instruction or X, Y addresses.

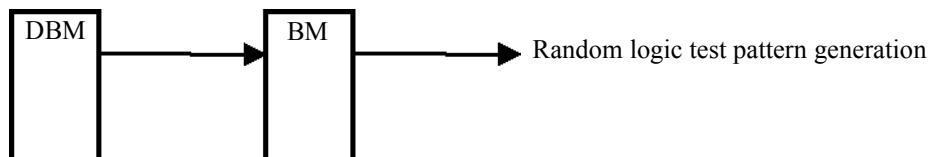


Figure 2-7 Relationship between DBM and BM

2.2.3 Programmable Data Selector

The programmable data selector of this test system consists of the following function blocks ([Figure 2-8](#)):

- Pin data multiplexer
 - Pin control data multiplexer
- (1) Pin data multiplexer

Selects the following data for each pin from patterns such as address data generated by the ALPG:

- Pattern data applied to DUT by the driver (PATn)
- Expected data used when performing DUT-output logical comparison (EXPn)

Sixteen pin data multiplexers exist for each pin. The data to be used can be switched on-the-fly by using the control signal from the ALPG.

- ① Driver pattern data (PATn)

Can be used for all driver and I/O formatter channels.

Pin data multiplexers can select the four pin data items A, B, D, and E from the following address, data, and DUT control signals:

X0-23, Y0-23
 R, W, M1, M2, C0-31
 D0-17, SD0-17
 FIXL, FIXH

Two PAT signals (ports A and B) can be selected for each channel from the signals selected for pin data items A, B, D, and E.

Pin data to be output to ports A and B can be switched on-the-fly by C0, M1, and M2 signals.

- ② Comparator expected data (EXPn)

Can be used in all I/O formatter channels.

In addition to PATn, two EXP signals (ports A and B) can be selected for each channel from pin data items A, B, D, E and PPATn signals.

(2) Pin control data multiplexer

Allows users to select any one of RINV, CPE1 to CPE4, and DRE1 and DRE2 tester control signals common to each pin from the following data:

R
W
M1-2
C0-31
FIXL
FIXH

CPE1 to CPE4 are selected and used for each channel as the enable control signal for DUT output judgment performed by STRBs.

DRE1 and DRE2 are selected and used for each channel as the driver output enable control signal for I/O pins.

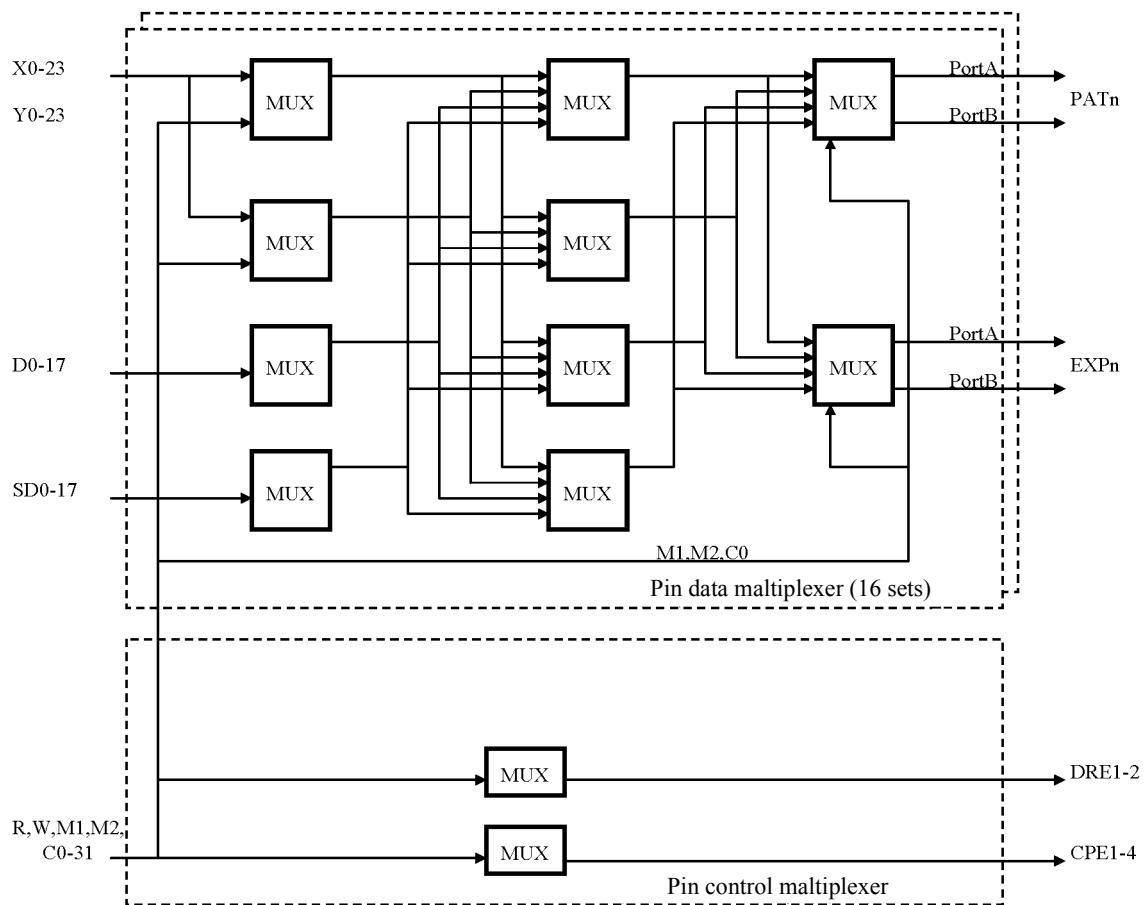


Figure 2-8 Programmable Data Selector

2.3 Special Functional Test Modes

This section describes the special functional test modes.

2.3.1 Match Mode Test

The match mode changes the test vector generation sequence in functional tests in real time when the outputs from DUTs match the expected values.

In this mode, high-speed writing algorithm tests of EPROMs and flash memories can be executed. A match signal is output based on logical AND of PASS results for all DUTs.

For detecting matches and jumping after the detection, many options like the following are provided:

- A match with the expected vector is detected and then a jump is performed.
- A match with the expected vector is not detected and then a jump is performed.
- Match detection is executed for the specified number of times, and if a match is not detected, the test program jumps to the specified address. If matches are not detected for the specified number of times, it jumps again to another specified address.

2.4 Failure Analysis Memory (FM)

Failure analysis memory consists of address failure analysis memory used to analyze the addresses and data bits at which failures occurred during a DUT test, and data memory used to analyze the processes performed until failures occur.

When multiple devices are tested in parallel, fail information for multiple DUTs can be captured simultaneously. For this test system, failure analysis memory is installed in the TOM board as a standard unit.

2.4.1 Address Fail Analysis Memory

Address fail analysis memory contains 12 AFM blocks for each TOM board. An AFM block consists of the following memory and registers:

- Address Fail Memory (AFM)
- Fail cell counter: 31 bits × 16

Fail information for 16 channels can be stored in one block.

The capacity of one block is 2 Gb regardless of frequency.

AFM can be configured according to the number of DUT output bits and the number of DUTs tested in parallel, by using the multiplexer in the input section.

[Table 2-3](#) shows the relationships between the number of DUTs tested in parallel, the number of DUT output bits, and the AFM capacity per DUT. AFM operation mode is as follows:

- (a) Fail information capture (unconditional fail)

AFM can retrieve the addresses where fails occur. For the fail cell counter, one block has 31 bits × 16 counters, and with each one operating in parallel, fails can be counted at high speed.

Table 2-3 Test Frequency, Number of DUTs Tested in Parallel, Number of Output Bits, and FM Capacity

Test frequency	AFM capacity			
	2 bit 96DUT/TOM	4 bit 48DUT/TOM	8 bit 24DUT/TOM	16 bit 12DUT/TOM
≤ 150 MHz (300 Mbps)	256 Mbits	512 Mbits	1 Gbits	2 Gbits

2.4.2 Data Fail Memory

Data failure memory is used to analyze the processes performed until fails occur. It consists of the following memory and registers:

Data Memory	1024 words
Pattern Counter/Fail Counter	39/29 bits

Data Memory includes the following data items:

Fail Address	48 bits	
PC0-11	12 bits	
R	(DUT control signal)	1 bit
W	(DUT control signal)	1 bit
M1-2	(DUT control signal)	2 bits
C0-31	(DUT control signal)	32 bits
TS0-3	(Timing set selection)	4 bits
CYP0-3	(Cycle palette data selection)	4 bits
D0-17, SD0-17	36 bits	
DBM AP	31 bits	
Serial Data	4 × 2 bits	
Pattern Counter	40 bits	
Pin Fail	48 × 2 bits	

Under the following conditions, 1024 patterns of the previously mentioned data are stored:

- (a) 1024 patterns immediately before an arbitrary pattern count
- (b) 1024 patterns immediately before an arbitrary fail count
- (c) 1024 fail patterns generated before reaching an arbitrary pattern count
- (d) 1024 fail patterns generated before reaching an arbitrary fail count

However, the preceding number of fails and that counted by Fail Counter are handled as 1 if one or more fails exist in the same number of steps as 1 WAY interleaves.

2.5 Timing Generator

2.5.1 Timing Characteristics

The timing edges generated by the timing generator have the following features:

(a) Timing Edge

BCLK and CCLK are used as DR waveform timing edges for all IO pins. DREL and DRET are used as I/O switching timing edges for IO pins. STRB is used as comparison judgment timing for IO pins.

With regard to BCLK, CCLK, STRB, DREL, and DRET, up to 128 timing edges each can be used.

(b) Clock/STRB resolution

The timing resolution of BCLK, CCLK, DREL, DRET and STRB is 833 ps at the smallest.

(c) Wide setting range

The timing edge can be set in the following range:

- 0 to 2 μ s and RATE - minimum set resolution

(d) Timing Set

Test rates and timing edges can be selected from 16 timing sets on-the-fly.

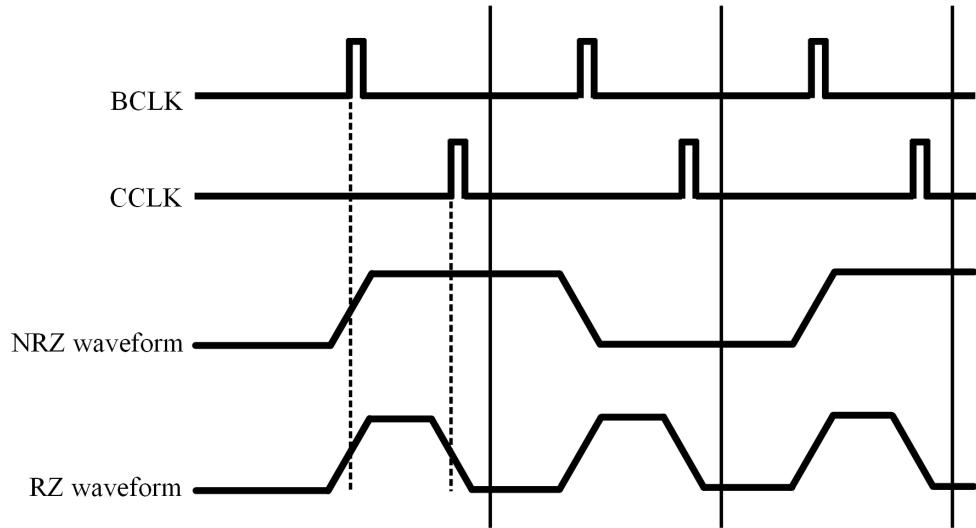
(e) Rate Setting

The functional test cycle can be set in the following range:

- 1Way 6.667 ns to 10 μ s

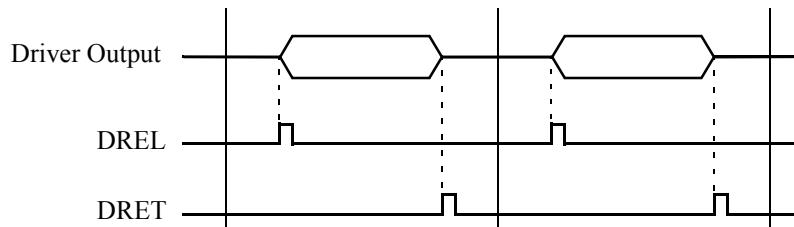
The usages of timing edges BCLK and CCLK for shaping the driver output waveform are as follows.

BCLK is used as the leading edge and CCLK is used as the trailing edge to shape an RZ waveform as shown in [Figure 2-9](#).

**Figure 2-9 Timing Edge Specifications**

As shown in [Figure 2-10](#), DRECLK is used as an I/O switching timing signal to turn on and off the output from the driver in real time.

DRECLK uses one edge (DREL) for the timing of turning the driver on, and another edge (DRET) for the timing of turning the driver off.

**Figure 2-10 DRECLK Specifications**

With this test system, 128 strobes for output judgment are available.

- Edge type strobes (STRB1 to 128)

Two edge type strobes can be set for each IO pin.

When two edge type strobes are set, there is no limit on the proximity that can be set.

[Figure 2-11](#) shows the two edge type strobes.

[Figure 2-12](#) shows an image of switching the strobe without dead band through two test cycles.

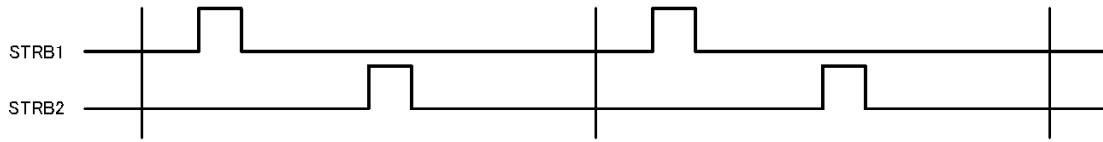
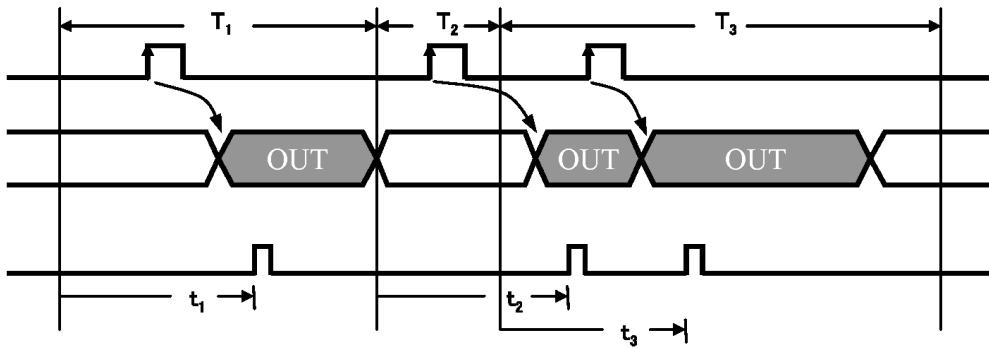


Figure 2-11 Edge Type



T_1, T_2, T_3 : test cycle
 t_1, t_2, t_3 : strobe delay phase

Figure 2-12 Cross Cycle Strobe

2.5.2 On-the-fly Timing Selection

The timing generator of this test system has 16 timing sets. Timings can be selected on-the-fly by using TS0 to TS3 switching control signals from the ALPG.

The timing selection features are as follows:

- (1) Sixteen timing sets are provided for the test rate and all timing edges including B and C clocks, STRB, and DRECLK.
- (2) For 16 timing sets, timings can be selected on-the-fly without any restrictions. (However, some timing restrictions may apply depending on the operation mode.)

2.6 Format Control and Digital Compare

Waveform control is performed based on the pattern data generated by the ALPG and selected by PDS.

2.6.1 Format Control

A waveform is determined by the selection of pattern data and BCLK and CCLK timing edges.

Each pin can generate the waveforms shown in [Figure 2-13](#). These waveforms can be roughly classified into the three basic groups: NRZ, RZ, and FIX.

The DNRZ and /DNRZ modes that output two NRZ waveforms are provided in the same cycle.

Pattern data PATA is output at BCLK timing and PATB is output at CCLK timing.

CLOCK OPEN can be used for real-time switching of a driver waveform without any waveform mode restrictions.

The number of channels of the format control that generates independent waveforms is as follows. The number of format control channels does not depend on the test-station site configuration and the number of CHILD pins.

Table 2-4 Format Control Channel

Format Control channels	Number of channels
I/O channel	48

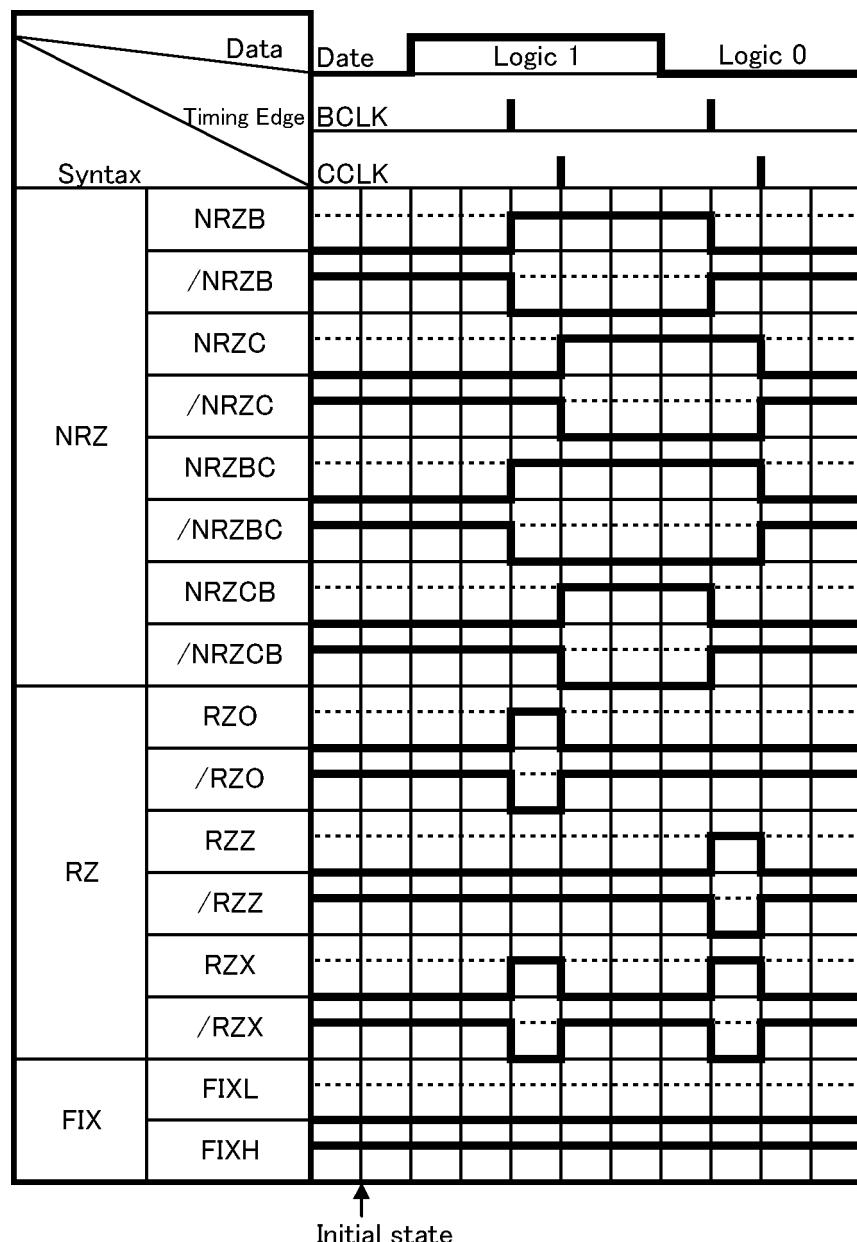


Figure 2-13 Waveform Formatting

2.6.2 I/O Control

I/O control of the driver is performed by using DRE1 and DRE2 selected by PDS. The timing of I/O switching is determined by DRECLK from the timing generator. As shown in [Figure 2-14](#), the timings for when I/O-controlled RZ and NRZ waveforms are switched from off to on and from on to off are respectively determined by DRECLKL and DRECLKT.

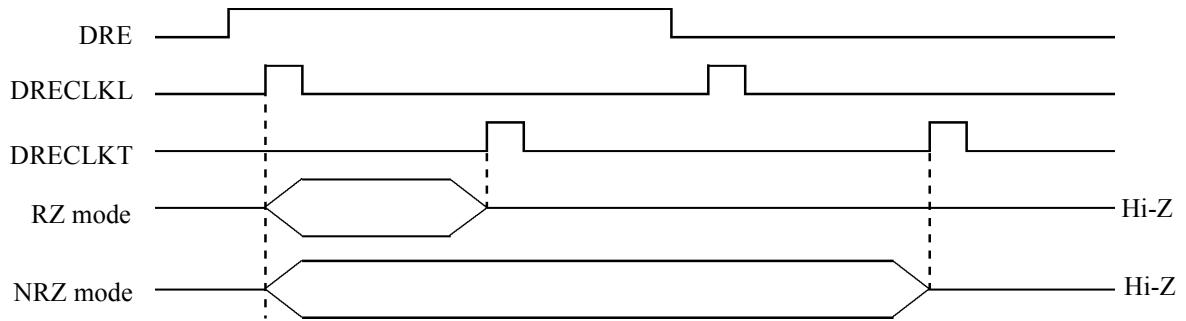


Figure 2-14 Driver I/O Control

2.6.3 Digital Compare

The digital compare logically compares DUT output with its expected value for each pin selected by PDS. This comparison timing is determined by STRB.

Whether comparison is to be performed or not is controlled by CPE1 to CPE4 signals that are generated by the ALPG and selected for each strobe of each pin.

By setting two strobes to one cycle, the device data can be compared with two timings. When doing so, the expected value can be switched between the two strobes.

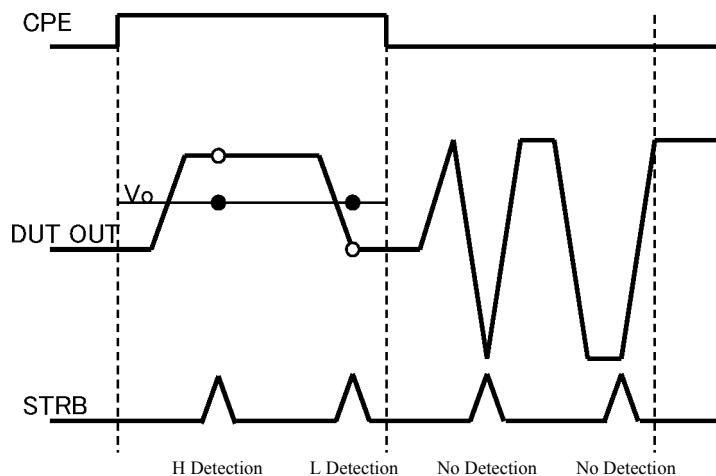


Figure 2-15 Digital Compare

2.6.4 Flash Memory Device Parallel Test Function

This test system has a flash memory parallel test function consisting of the following registers and counter.

[Figure 2-16](#) shows a block diagram of the flash memory parallel test function.

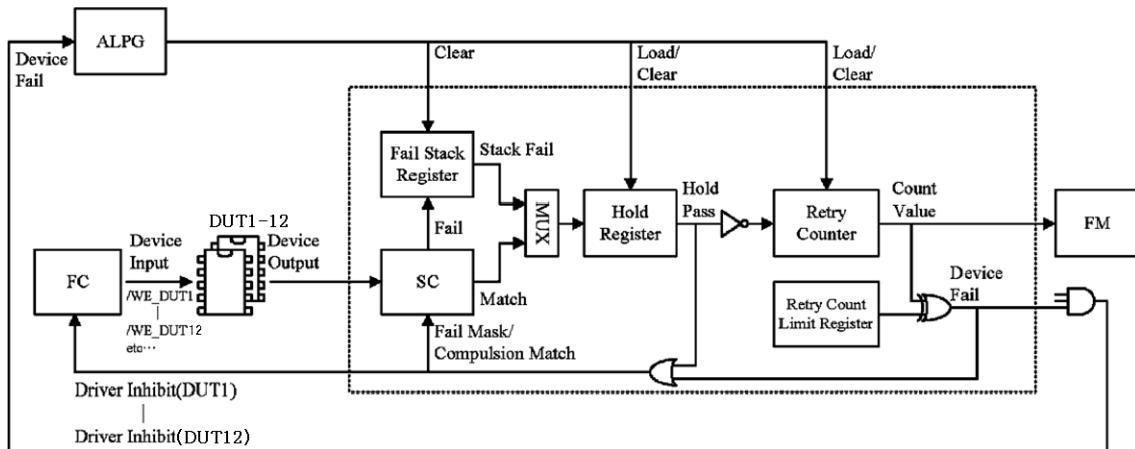


Figure 2-16 Flash Memory Device Parallel Test Function

The hold register retains logical comparison results, takes care of the prohibition of output of driver signals applied to DUTs and the prohibition of logical comparisons, and forcibly performs match operations, allowing users to prevent excessive writing of data into or erasing of data from the flash memory. Storing data in and clearing data from the hold register can be controlled by the pattern program. All I/O pins can be selected to disable driver signals.

The retry counter calculates how many times data is written and erased based on the data stored in the hold register. The retry counter (counting and clearing data) can be controlled by the pattern program. By setting the upper limit of the write/erase count in the retry count limit register and comparing it with the counter value, Pass/Fail judgment of DUTs can be made by using how many times data has been written and erased.

The fail stack register accumulates fail information for each block. Tests can be performed based on this accumulated fail information by operating the hold register and counter. This function facilitates testing for NAND type flash memory devices in which data is written or erased on a block basis.

This test system provides the following types of hardware to be able to handle multi-bank devices:

- Flash hold register One for each I/O pin
- Fail stack register One for each I/O pin

This test system provides the following types of hardware for each function block to be able to perform a parallel test:

- Retry counter: 31 bits × 12
- Retry count limit register: 32 bits × 1

2.6.5 Write Control Function for Individual Data Items

This test system includes universal buffer memory (UBM) as a pattern generator used to write individual data items to memory devices. The UBM can also write individual expected data items. [Figure 2-17](#) shows a block diagram of the write control function.

The address pointer of the UBM is controlled by a MUT signal such as C0 to C31 generated by the ALPG. The UBM can be used to generate addresses in which to write individual data items to bad blocks in the NAND flash memory device. [Figure 2-18](#) shows the operation of writing individual data items to bad block addresses. By using the ALPG PAT in a pattern cycle common to all DUTs and the UBM PAT in an address pattern cycle for an individual DUT, only bad block address data needs to be written in the UBM, which makes the pattern description more efficient.

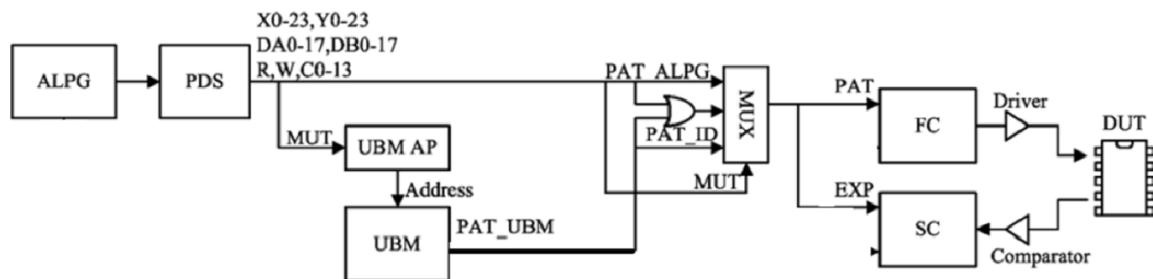


Figure 2-17 Write Control Function for Individual Data Items

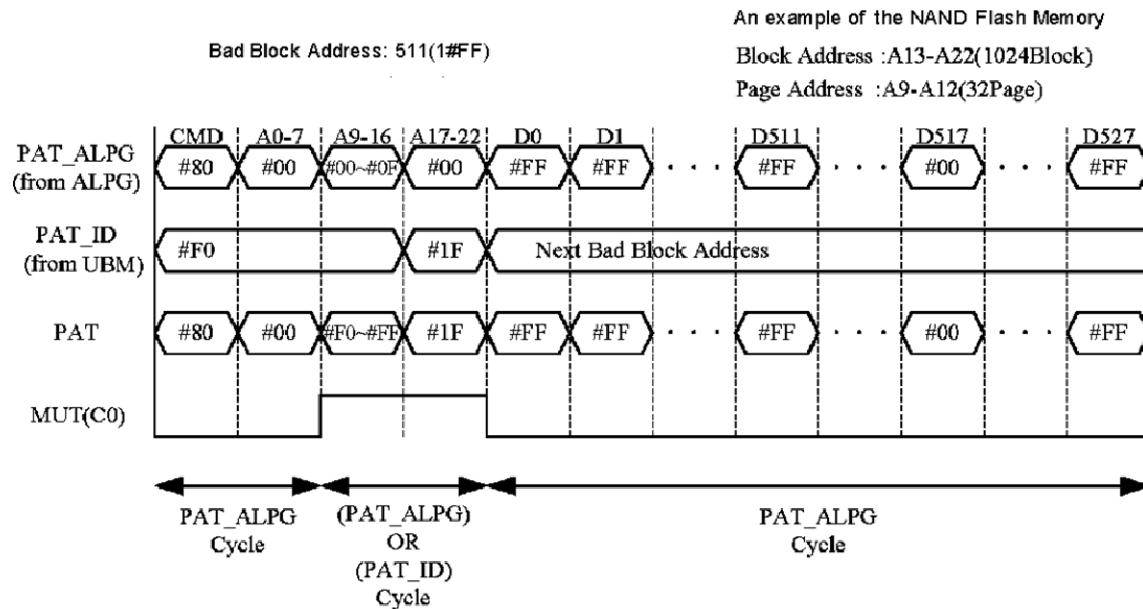


Figure 2-18 Individual Data Items Written to Bad Block Addresses

2.6.6 Block Mask Function

The block mask function masks DUT bad blocks and counts the number of bad blocks by using the bad block memory (BBM). [Figure 2-19](#) shows a block diagram of the block mask function.

The BBM of this test system has a capacity of 256 kilowords \times 4 bits (Note 1) for each function block, and various kinds of information on each block are managed as flags in the BBM. [Table 2-5](#) shows flag assignment in the BBM.

The block mask function generates mask patterns by using fail block information stored in the BBM or the combination of various pieces of flag information as a condition and prohibits logical comparison and driver output on a block basis. This function facilitates masking of NAND type flash memory devices on a block basis and reduces the testing time.

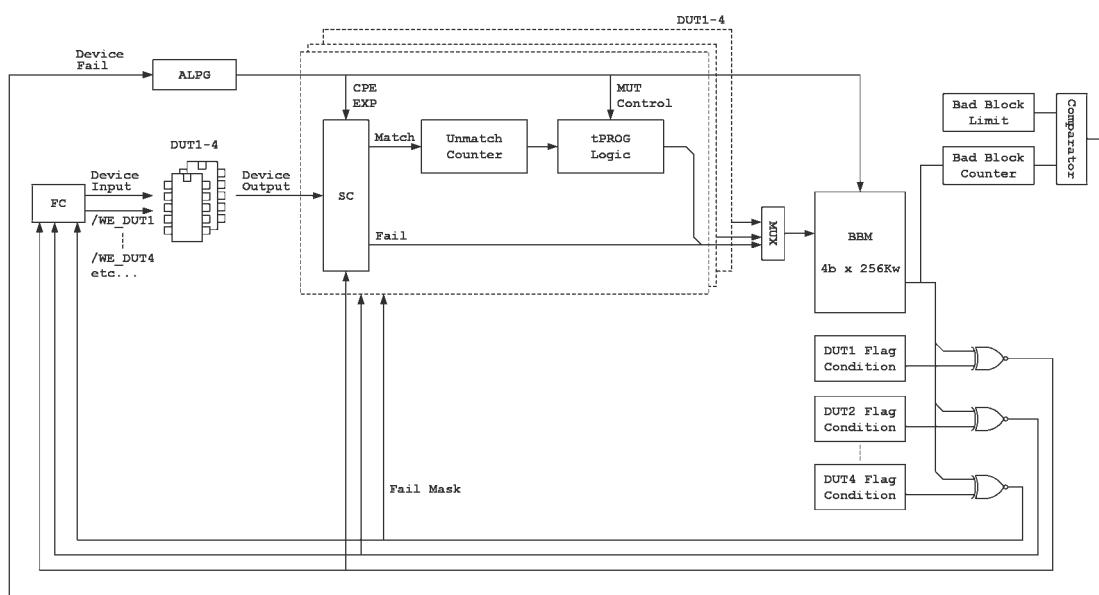


Figure 2-19 Block Diagram of Block Mask Function

Table 2-5 BBM Storage Data

BBM flag	Description
Read Fail	Indicates a fail in the DUT data read cycle. It is synonymous with the conventional bad block flag.

2.7 Test Station

One test station can be connected to this test system.

2.7.1 Pin Electronics

The pin electronics consists of I/O pins only.

- I/O pin electronics

For I/O pin electronics, I/O pins, high-voltage I/O pins, and passive-load I/O pins are provided.

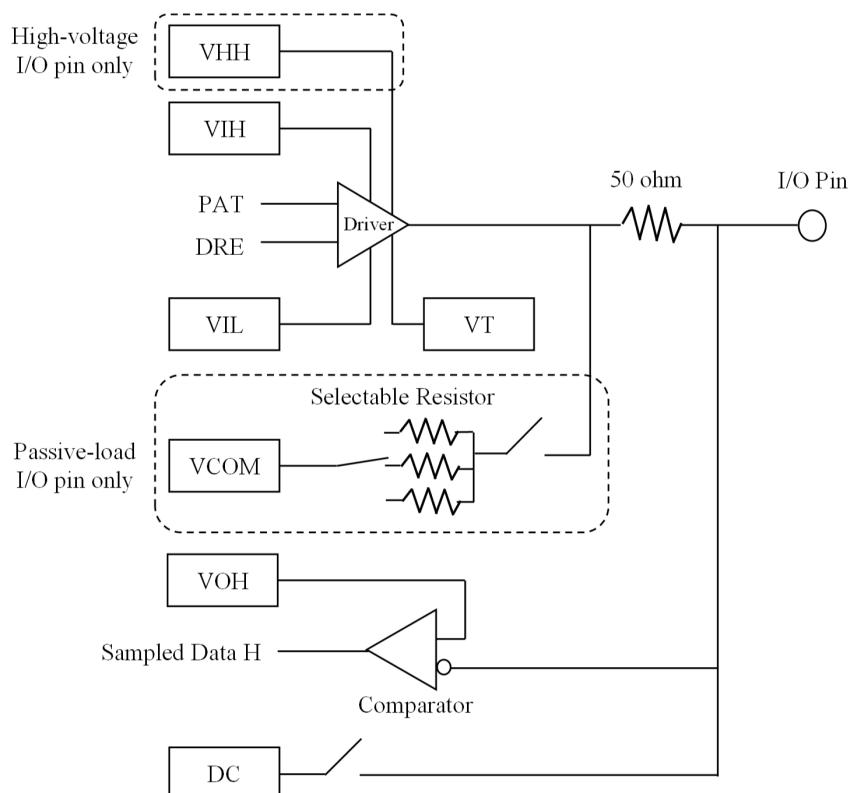
The driver output range for I/O pin electronics is -1.0 V to +6.0 V, which allows an arbitrary pattern to be generated.

The comparator uses programmable VOH as a comparison level. The results of level detection are sent to the sense controller for logical comparison based on strobe timing. There are 16 VOH comparison combinations that can be set under program control. The comparator input range is -1.0 V to 6.0 V. Depending on the device type, termination of output using a resistor may be desirable. In that case, connection to a programmable VTT via a $50\text{-}\Omega$ resistor is possible.

For high-voltage I/O pins, the high-voltage driver from 0 V to +13 V can be switched by the pattern control signal and used in addition to the I/O pin capability.

For passive-load I/O pins, connecting a DUT and a selectable resistor at a user-specified voltage is available in addition to the I/O pin capability. For example, when measuring a Ready Busy pin of the memory device by pulling up with a $1\text{ k}\Omega$ resistor, use of this function eliminates the external circuit. The resistance value can be selected from three types.

[Figure 2-20](#) shows a block diagram of the I/O pin electronics.



[Figure 2-20](#) I/O Pin Electronics

2.7.2 Test Head Channel Configuration

The T5830P uses only one test station, which can be configured with a maximum of 32 sites. Each site is controlled by independent test processors.

[Table 2-6](#) shows channel resources in a test site for parallel tests.

Table 2-6 Test Station Channel Configuration (T5830P)

Site Configuration	I/O	DC	PPS	HVLVDR
32 Site + 4 HVLVDR	4608 ch	384 ch	1152 ch	1152 ch
32 Site + 6 HVLVDR	4608 ch	384 ch	1152 ch	1728 ch
32 Site + 12 HVLVDR	4608 ch	384 ch	1152 ch	1728 ch

The T5830PES, on the other hand, uses only one test station, which can be configured with a maximum of two sites. Each site is controlled by independent test processors.

[Table 2-7](#) shows channel resources in a test site for parallel tests.

Table 2-7 Test Station Channel Configuration (T5830PES)

Site Configuration	I/O	DC	PPS	HVLVDR
2 Site + 1 HVLVDR	288 ch	24 ch	48 ch	32 ch

[Table 2-8](#) shows I/O pin numbers and types for the T5830P/T5830PES.

Table 2-8 I/O Pin Numbers and Types (T5830P/T5830PES)

PinNo.*1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
I/O pin	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
High-voltage		○		○		○		○		○		○		○		○		○		○		○		○
Passive-load			○			○			○			○			○			○			○			○
PinNo.*1	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
I/O pin	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
High-voltage		○		○		○		○		○		○		○		○		○		○		○		○
Passive-load			○			○			○			○			○			○			○			○

*1: Child A, B, and C pins are provided for each pin number in each site.

2.8 DC Parametric Test

A DC parametric test measures the current in DUTs (devices under test) by applying a voltage and measures the voltage in DUTs by applying a current to the DUTs.

The multiple DC test units mounted in this test system are connected to the pins used for a parallel test, and a DC parametric test for all of them can be executed simultaneously.

If the number of DUTs tested in parallel is larger than the number of DC units, one DC unit is assigned to multiple DUTs and the measurement is performed while DC connections are switched automatically.

When creating a parallel testing program using DC test units, the program can be described as a measurement program for one DUT.

For the T5830P, up to 384 DC test units can be mounted in each station.

For the T5830PES, up to 24 DC test units can be mounted in each station.

2.9 Device Power Supply

The T5830P can have up to 1152 PPS channels to supply power to DUTs in a configuration with the maximum number of sites. (For three-branch output in a module)

When a multiple-device parallel-test program is created, the same value is automatically specified by the program for the power supply connected to the same power supply pins of the DUTs.

The PPS output voltage range is -1 V to +13 V.

All of the PPS channels have a current measurement function.

The T5830PES has 48 available PPS channels. (For two-branch output in a module)

Just like the T5830P, all of the PPS channels have a current measurement function.

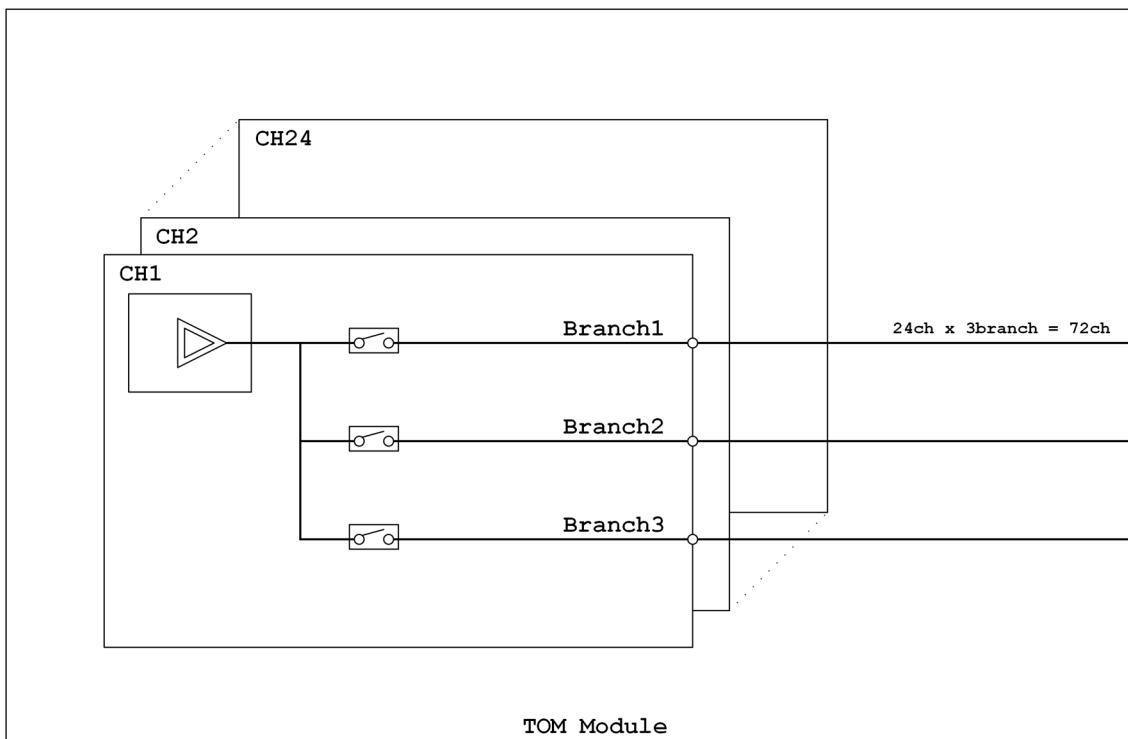


Figure 2-21 Number of PPS Channels and Branches of TOM Module

2.10 High Voltage Level Driver (HVLVDR)

This system optionally provides the high voltage level driver (HVLVDR) module.

A device test can be executed by using the HVLVDR that requires high-voltage source or high-voltage measurement.

The HVLVDR output voltage range is -10 V to +32 V. The voltage measurement range is -10 V to +32 V.

For the T5830P, the HVLVDR has a maximum of 1728 available channels. (For six-branch output in a module)

For the T5830PES, the HVLVDR has a maximum of 32 available channels. (For two-branch output in a module)

All the HVLVDR channels have a current measurement function.

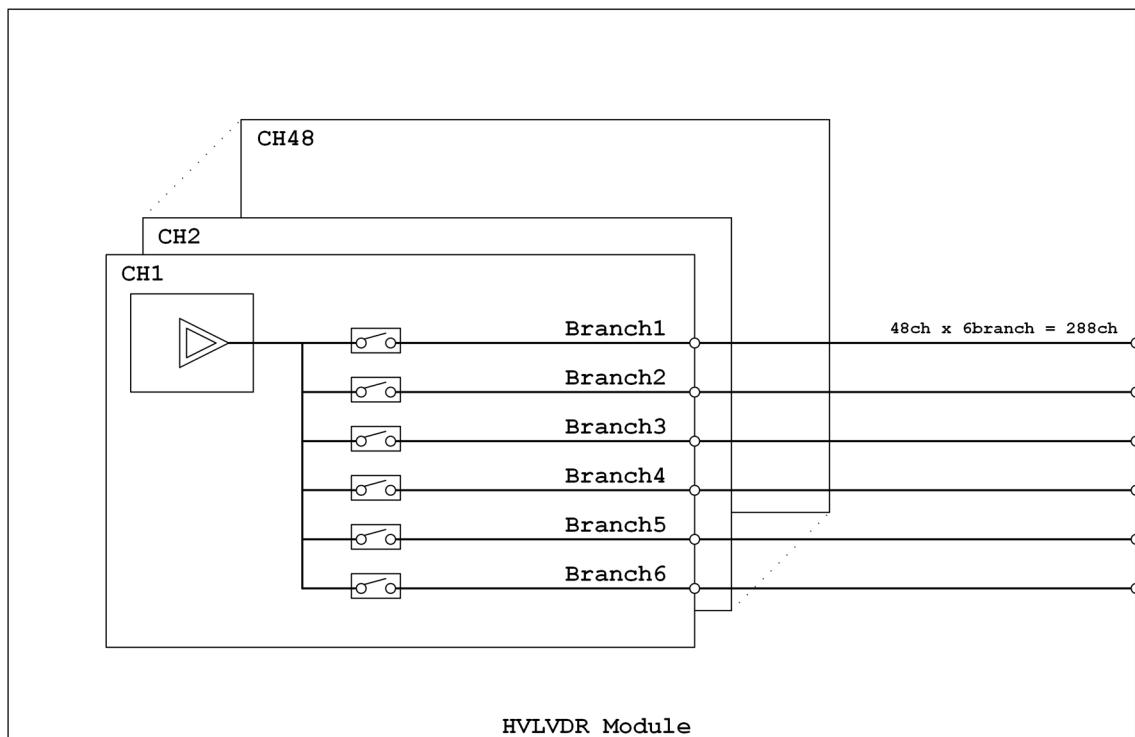


Figure 2-22 Number of Channels and Branches of HVLVDR Module

2.11 DUT Interface

2.11.1 Manual Test Performance Board

To test DUTs manually, attach a DUT socket to the performance board supplied by Advantest. Connect the pin electronics output of the test head and socket pins by wiring them.

[Table 2-9](#) shows the major I/O signal terminals on the performance board and their usage.

Table 2-9 Control Signals on Performance Board

Type	Usage
PIN	Output points of test head pin electronics. DUT socket pins are wired to these points.
LBCTRL	Can be set as an SPI bus (CLK, /CS, DIN, DOUT, /RST) or a parallel bus that has four outputs and one input.
Device power supply output	Output points of device power supplies. These points are wired to DUT power supply pins.
Utility power supply	+3.3 V and +5 V are output. It can be used on the performance board as necessary.

Table 2-10 LBCTRL Specifications

Parameter	Identifying symbol	Conditions	Specifications	
			Minimum	Maximum
High input voltage	LB_VIH		2 V	
Low input voltage	LB_VIL			0.8 V
High output voltage	LB_VOH	LB_IOH=-100 μ A	3 V*1	
Low output voltage	LC_VOL	LB_IOH=100 μ A		0.2 V*1
Input current	LB_II	VI = 5.5 V or GND	-10 μ A	10 μ A
Output resistance	LB_RO		45 Ω	55 Ω

*1: The LBCTRL output is terminated at 50 Ω . The output voltage varies according to the load current.

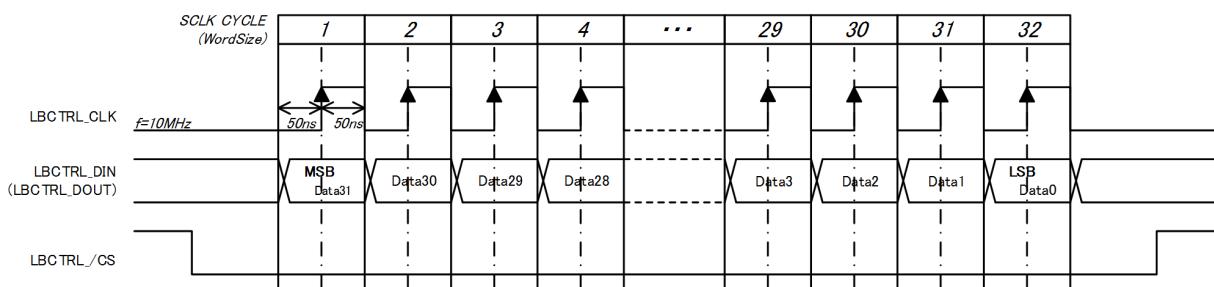


Figure 2-23 LBCTRL Timing Chart

2.11.2 Wafer Test

This test system includes a complete wafer prober interface. It allows users to perform high-accuracy wafer tests.

To ensure compatibility with various types of wafer probers on the market, Advantest provides a complete interface package that includes electrically calibrated cables, connectors, mechanical housings for easy wafer prober tests, and other necessary items.

2.12 Automatic Calibration System

This test system has a calibration system. This calibration system corrects the voltage, current, and timing accuracies, allowing users to improve the reliability and accuracy of tests.

This test system provides calibration that depends on a test program and one that does not.

2.12.1 Calibration that Does Not Depend on Test Programs

Calibration that does not depend on a test program is executed by the system initialization program. It is designed to calibrate items that do not depend on conditions set in a test program. Thirty minutes after the test system power is turned on, the system software automatically starts the system initialization program.

The system initialization program calibrates the following items:

- (a) Linearity and offset of voltage and current of the DC parametric test unit and those of device power supplies
- (b) Linearity of each edge generated by the timing generator
- (c) Linearity and offset of the driver output level
- (d) Linearity and offset of the comparator comparison level
- (e) Linearity and offset of the termination level

2.12.2 Calibration that Depends on Test Programs

Calibration that depends on a test program is executed by the calibration program (UTL_ExecCalb/CALL CALB).

The following items are calibrated based on conditions set in a test program:

- (a) Skew between driver pins
- (b) Skew between comparator pins
- (c) Skew between the driver and comparator
- (d) Driver I/O timing

2.12.3 Overall Timing Accuracy

The overall timing accuracy is specified by totaling the amounts of error that the test system has and is ensured when both the test program independent calibration and test program dependent calibration are complete.

The overall timing accuracy includes both the timing accuracy of signals input into devices and the timing accuracy that compares and judges signals output from devices. The timing accuracy of signals input into devices includes elements such as the driver skew, clock linearity, and jitter. The timing accuracy that compares and judges signals output from devices includes elements such as the comparator skew, strobe linearity, and jitter. The overall timing accuracy also includes the skew between the driver and comparator.

This test system ensures the overall timing accuracy of ± 400 ps by executing automatic calibration including all preceding elements at 0 V to 1 V 50%.

2.13 Memory Repair Analyzer MRA5 Lite

The memory repair analyzer 5 (MRA5 Lite) unit analyzes repair addresses of memory devices with a redundant repair function at high speed.

Conventional MRAs such as MRA4 (MRA4 through MRA4ev3) shortened the repair analysis processing time by performing analysis for each DUT using multiple controllers. MRA5 Lite has improved the parallel-processing ability by changing a part of the analysis algorithm to a hardware-based one, so that it has achieved a higher analysis processing speed compared with MRA4.

As with MRA4, the MRA5 Lite hardware includes the MRA unit and the FM unit to process each individual DUT in parallel.

2.13.1 Block Diagram

MRA5 Lite consists of AFM (address fail memory) and the two blocks described below. Every AFM block (function block) has this configuration.

- ① MRA5acc (MRA5 accelerator)
- ② RCPU

When MRA5 Lite starts an analysis, the workstation is used to set up the conditions for repair analysis according to the device redundancy and to send these conditions to each RCPU. The workstation is used to set up the conditions for repair analysis according to the DUT redundancy and to send these conditions to each RCPU. The tester processor sends the start instruction for the repair analysis to each MRA5acc, and this starts the repair analysis. The RCPU produces a repair solution using the analysis data obtained from MRA5acc. Each RCPU sends the analysis result to the workstation.

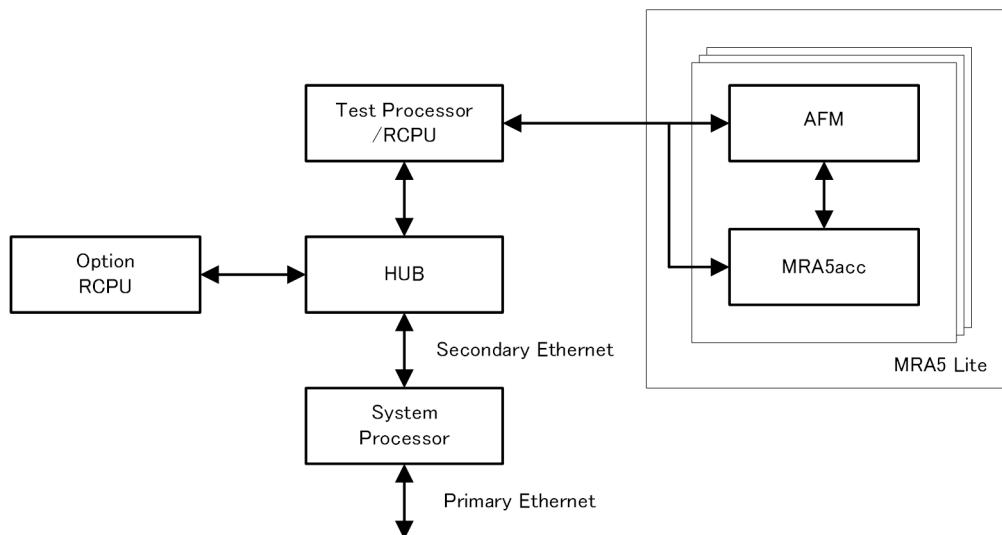


Figure 2-24 Block Diagram of MRA5 Lite Functions

2.13.2 MRA5 Lite Hardware

The MRA5 Lite hardware consists of the MRA (MRA5 accelerator) and RCPU (MRA controller) units, which have the following functions:

- After a device test, MRA5 Lite accesses the AFM to perform an analysis operation.
- The MRA and RCPU units in the MRA5 Lite are prepared for each DUT. Each DUT is analyzed independently and simultaneously.

2.13.3 MRA Unit (MRA Accelerator) in MRA5 Lite

The MRA unit in an MRA5 Lite has one MRA5 accelerator (MRA5acc) per 32 bits of AFM data. The MRA accelerators operate in parallel so that memory repair analysis data can be obtained at high speed.

2.13.4 RCPU Unit (Repair Controller) in MRA5 Lite

The RCPU unit in an MRA5 Lite has one repair controller per six MRA5 accelerators (MRA5acc). The repair controllers operate in parallel so that repair analysis can be performed at high speed.

By adding an exterior optional RCPU, analyses can be performed at higher speeds.

2.13.5 Software for MRA5 Lite

For more information on MRA5 Lite software, refer to the reference manual of FutureSuite MRA.

2.14 Safety Devices

Various types of safety devices are provided for this test system to ensure safety.

2.14.1 Abnormal Temperature Detection

The mainframe and test head are equipped with temperature sensors.

When an abnormal temperature is detected, the main power switch automatically turns off and a message is displayed on the monitor screen. However, this only occurs when communication with the system controller is possible.

2.14.2 Power Failure Detection

If an abnormal output is detected from the DC power supply used in the test system, the main power switch automatically turns off and a message is displayed on the monitor screen.

2.14.3 Smoke Detection

A smoke detector is installed to detect smoke in the mainframe and test head. If smoke is detected, the main power switch automatically turns off.

2.14.4 EMO Switch

This test system is equipped with an EMO switch that turns off the power if an abnormality occurs in the test system installation location. One EMO switch is provided as standard.

2.14.5 Fan Abnormality Detection

Each fan in the test head is equipped with a rotation sensor.

If a fan stops due to an abnormality, the main power switch automatically turns off and a message is displayed on the monitor screen.

2.14.6 Tester Cooling Unit Abnormal Detection

The tester cooling unit is equipped with sensors to detect various abnormalities.

When an abnormality is detected, the main power supply is automatically turned off and a message is displayed on the monitor. However, the message is displayed only when the system controller and system monitor board can communicate with each other.

The message displayed on the monitor indicates that the tester cooling unit is in an abnormal state.

Details of abnormalities

- Fluorinert temperature is too high or too low.
- Fluorinert flow rate is too low.
- Water has entered the Fluorinert tank.
- Liquid level of the Fluorinert tank is too low.

Table 2-11 Presence of Sensors to Detect Abnormalities in Tester Cooling Units

No.	Details of abnormalities	Presence of sensor	
		T5830P	T5830PES air exchange cooling unit
1	Internal transformer temperature exceeded 100°C.	<input type="radio"/>	-
2	Fluorinert temperature is too high or too low.	<input type="radio"/>	-
3	Fluorinert flow rate is too low.	<input type="radio"/>	<input type="radio"/>
4	The differential pressure of the external cooling water is too low.	<input type="radio"/>	-
5	The output pressure of Fluorinert is high.	<input type="radio"/>	-
6	Malfunction of the Fluorinert pump.	<input type="radio"/>	-
7	Water has entered the Fluorinert tank.	<input type="radio"/>	<input type="radio"/>
8	Water has mixed with Fluorinert in the heat-exchange unit.	<input type="radio"/>	-
9	Liquid has accumulated at the base of the system.	<input type="radio"/>	-
10	Liquid level of the Fluorinert tank is too low.	<input type="radio"/>	<input type="radio"/>
11	The front panel is open.	<input type="radio"/>	-
12	The DC power source voltage is too high or too low.	<input type="radio"/>	-

3. Computing Architecture

3.1 Overview

This test system uses a multiprocessor as the computing architecture. One processor is for controlling the test system and one is for measuring devices. This makes it possible to achieve high-speed device testing times and high-repeatability device characteristic evaluations. [Figure 3-1](#) shows basic components.

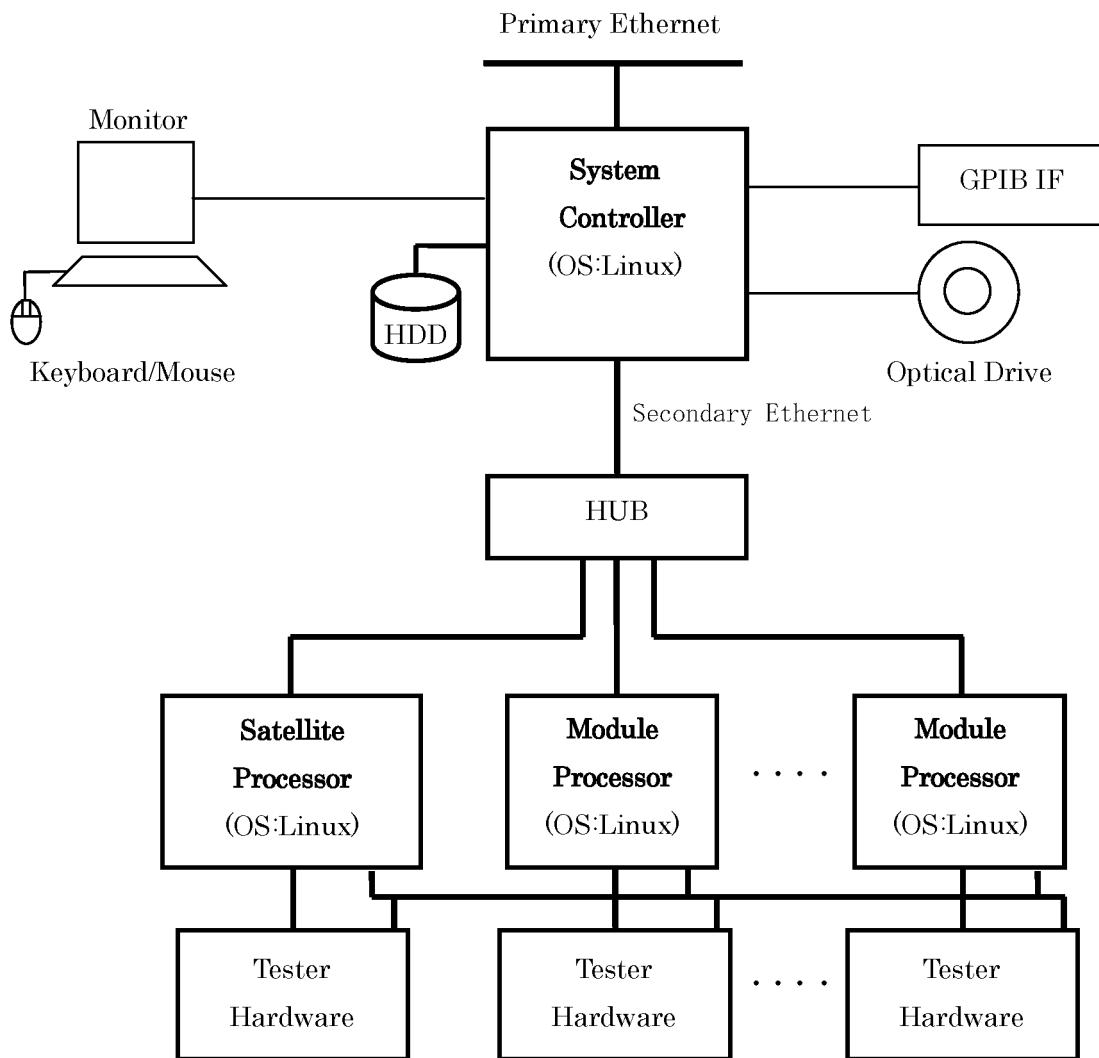


Figure 3-1 Basic Components

3.2 System Controller

The system controller is an interface between the user and test system. It controls all test system functions, downloads the test program to be executed to the satellite processors and module processors, and collects returned test results.

Table 3-1 System Controller Function

Function	Specification
OS	Linux
CPU	Xeon E3-1225v2 3.2 GHz
Memory	4 GB
I/O	Primary Ethernet: 10/100/1000Mbps × 1 Secondary Ethernet: 10/100/1000Mbps × 1 GPIB × 1
Hard disk drive	1 TB
Optical drive	Compatible format: DVD-R, DVD-RW, DVD-ROM, CD-R, CD-RW, CD-ROM
Graphic monitor	19-inch LCD monitor with 1280 × 1024 pixel resolution
Keyboard	104 English, connector: PS/2
Mouse	Mouse with a scroll wheel, connector: USB

3.3 Satellite Processor

The satellite processors execute the program loaded into the satellite processor memory by the system controller.

Table 3-2 Satellite Processor Specifications

Function	Specification
OS	Linux
CPU	Atom 1.6 GHz single core
Memory	1 GB
I/O	Ethernet: 10/100/1000Mbps × 1 Tester control bus: 100 MB/s data rate

3.4 Module Processor

The module processor executes the program loaded into the module processor memory by the system controller. The test program can independently execute a parallel test of DUTs.

Table 3-3 Module Processor Specifications

Function	Specification
OS	Linux
CPU	ARM 1.2 GHz dual core
Memory	4 GB
I/O	Ethernet: 10/100/1000base-TX × 1 Tester control bus: 100 MB/s data rate

4. Software

4.1 General Description

This test system is controlled by the FutureSuite system software.

The FutureSuite system software controls test, performs automatic calibration, collects and analyzes test data, and controls the system diagnostic program.

4.2 FutureSuite System Software

The FutureSuite system software includes the following software:

- LINUX operating system
- GCC compiler and DDD debugger
- ATL compiler and LIB DEBUG
- FutureSuite test system kernel
- FutureSuite tester utility
- Diagnostic program
- Automatic calibration program

4.2.1 FutureSuite Test System Kernel

The FutureSuite test system kernel provides the following services as C language libraries.

- Test configuration setup
- Test flow control
- Event hook
- Test results
- Test system status
- Error processing

4.2.2 FutureSuite Tester Utility

The FutureSuite system software provides various utilities to evaluate or analyze devices.

4.2.3 Diagnostic Program

The diagnostic program allows test systems to perform self-diagnostics.

4.2.4 Automatic Calibration Program

The automatic calibration program automatically calibrates the timing, voltage, and current accuracies.

4.3 Test Program

The test program consists of the test plan program, socket program, memory pattern program, and scramble program.

Each program is used after compiled by using a dedicated compiler.

- Test plan program
Sets test conditions of the test plan program and controls a sequence.
- Socket program
Defines the relationship between pin names that are used in the test plan program and pin numbers of the test systems. Also defines information for testing multiple devices in parallel.
- Memory pattern program
Defines the pattern program test vectors.
- Scramble program
Replaces address vectors of the scramble programs X, Y, and Z.

4.4 Test Language

This test system use the standard C language and Advantest test language (ATL) as a test plan programming language.

4.5 Operating System

This test system, the test processor and system controller use the LINUX operating system.

5. Specification for Installation and Acceptance

5.1 Installation Plan

5.1.1 Environmental Requirements

This test system assures its operations and specifications within the environment shown below.

Install the test system in an environment which satisfies the following conditions:

Table 5-1 Environmental Requirements

Ambient temperature (Note 1)	When operating	20°C to 30°C Temperature change must be 2°C or less per hour.
	When not operating	-20°C to 60°C (Note 2) (Note 7)
Relative humidity	When operating	40% to 65% (Note 3)
	When not operating	20% to 90% (Note 8) No condensation
Vibration		2 m/s ² or less (5 Hz to 50 Hz) 5 m/s ² or less (50 Hz to 500 Hz)
Shock (Note 4)		30 m/s ² or less
Ambient atmosphere		Must be free of salinity, iron, or corrosive gases.
Amount of dust		0.1 mg/m ³ or less (Note 5)
Magnetic field strength (Note 6)		1 µT or less (0.8 A/m or less)
Overtoltage category		III (Applicable standard: IEC 60364-44)
Altitude		2000 m or lower
Pollution level		3 (Applicable standard: IEC 60664-1)

Note 1: *The intake-air temperature of the test system mainframe and test station must be within the temperature range used during operation.*

Note 2: *Completely drain the coolant from the cooling unit when storing the test system. The cooling unit may be damaged by freezing in low temperature.*

Note 3: *Charged voltage of static electricity rapidly becomes high when the relative humidity becomes less than 50%. This causes stress to devices to be tested and pin electronics, which may lead to electrostatic discharge failure. To keep the electrostatic generation voltage low, an environment with a relative humidity of approximately 50% is recommended.*

Note 4: *This test system features precision instruments. If excessive vibrations or shocks are applied to the system, it may be damaged or may malfunction. To avoid damaging the system, use a truck that is equipped with air suspension when transporting.*

Note 5: *Do not install a printer or any of its peripherals in a clean room.*

Note 6: *If the magnetic field intensity of the system installation location is greater than the above value, the measurement accuracy of voltage and current values may degrade. To prevent degradation of the measurement accuracy, ensure that the magnetic field intensity of the system installation location is appropriate before installing the system.*

Note 7: *The system controller ambient temperature when the system is not operating is 0°C to 50°C.*

Note 8: *The system controller relative humidity when the system is not operating is 20% to 80%.*

5.1.2 Power Requirements

5.1.2.1 Power Requirements (for T5830P)

- Mainframe and Dual Satellite test head
Input: 180 VAC to 220 VAC three phase 50/60 Hz $\pm 0.5\%$ $\times 4$ lines
- A power supply for the RCPU is also required. For the input, single phase 200 V or 100 V can be selected.
- Common Mode surges should not exceed 2000 V for the AC power supply input. If there is any possibility that Common Mode surges exceeding 2000 V can occur, appropriate countermeasures must be taken.
- Differential Mode surges should not exceed 1000 V for the AC power supply input. If there is any possibility that Differential Mode surges exceeding 1000 V can occur, appropriate countermeasures must be taken.
- Common Mode conductive interference voltage should not exceed 10 V for the AC power supply input. If there is any possibility that Common Mode conductive interference voltage exceeding 10 V can occur, appropriate countermeasures must be taken.
- Voltage interruptions must not be longer than 10 ms.
- Electrical fast transient/burst voltage must be less than 2000 V for AC power supply or appropriate countermeasures must be taken.
- Electrical fast transient/burst voltage must be less than 1000 V for external interface cables or appropriate countermeasures must be taken.
- Voltage and frequency stability requirements are as follows:
180 VAC to 220 VAC three-phase 50/60 Hz $\pm 0.5\%$
If voltage fluctuations are outside this range, a regulator must be used.
Each power supply must be connected via a 30-mA circuit breaker having a grounded terminal.

The ground resistance for ground connections must be 100Ω or less. Prepare the power cable (4 lines in [Figure 5-1](#)) and use the following crimp-terminals for connection to the tester.

Crimp-terminal: Outside diameter: 12 mm

Screw hole diameter: 5.3 mm

(However, the line for the frame ground of the feed cable is not used.)

To connect the frame ground (grounding bar: PE on the rear), use the following crimp-terminals and wire:

Wire conductor: AWG4 green/yellow spiral (equivalent to UL1283)

Crimp-terminal: Outside diameter: 12 mm

Screw hole diameter: 5.3 mm

Connect power supply cables to the test system breaker power supply input terminals in the order R → S → T (U → V → W) from the left side of the operation panel.

AC power supply cable

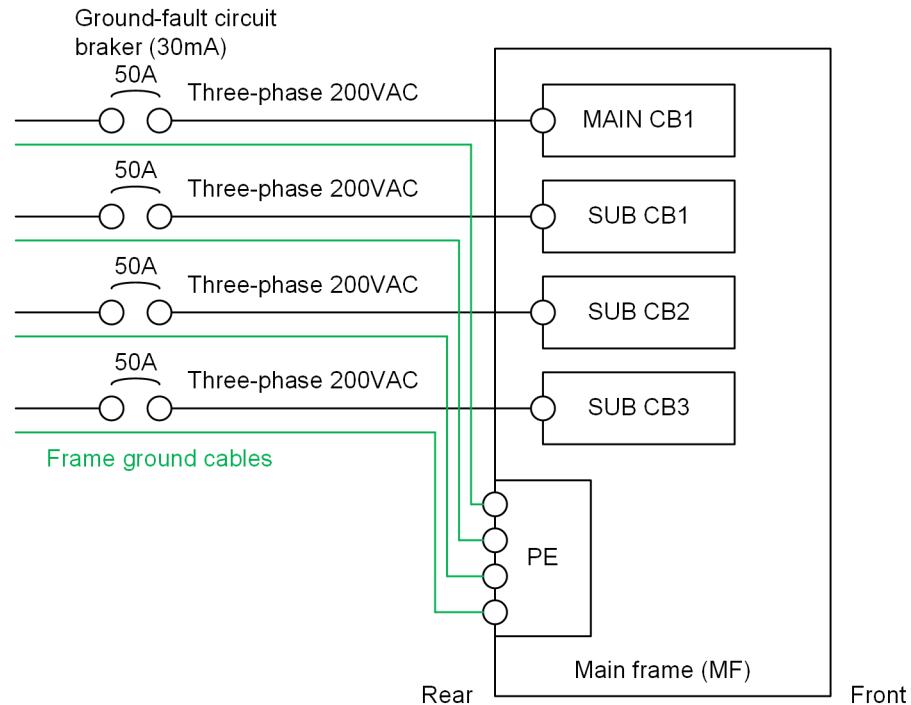


Figure 5-1 Power Supply

Table 5-2 Power Consumption of Full Configuration

MAIN CB1	SUB CB1	SUB CB2	SUB CB3	Total
5.9 kVA	8.1 kVA	8.1 kVA	8.1 kVA	30.2 kVA

Main circuit breaker short circuit current rating: 10 kA

Main Frame AC cable Routing

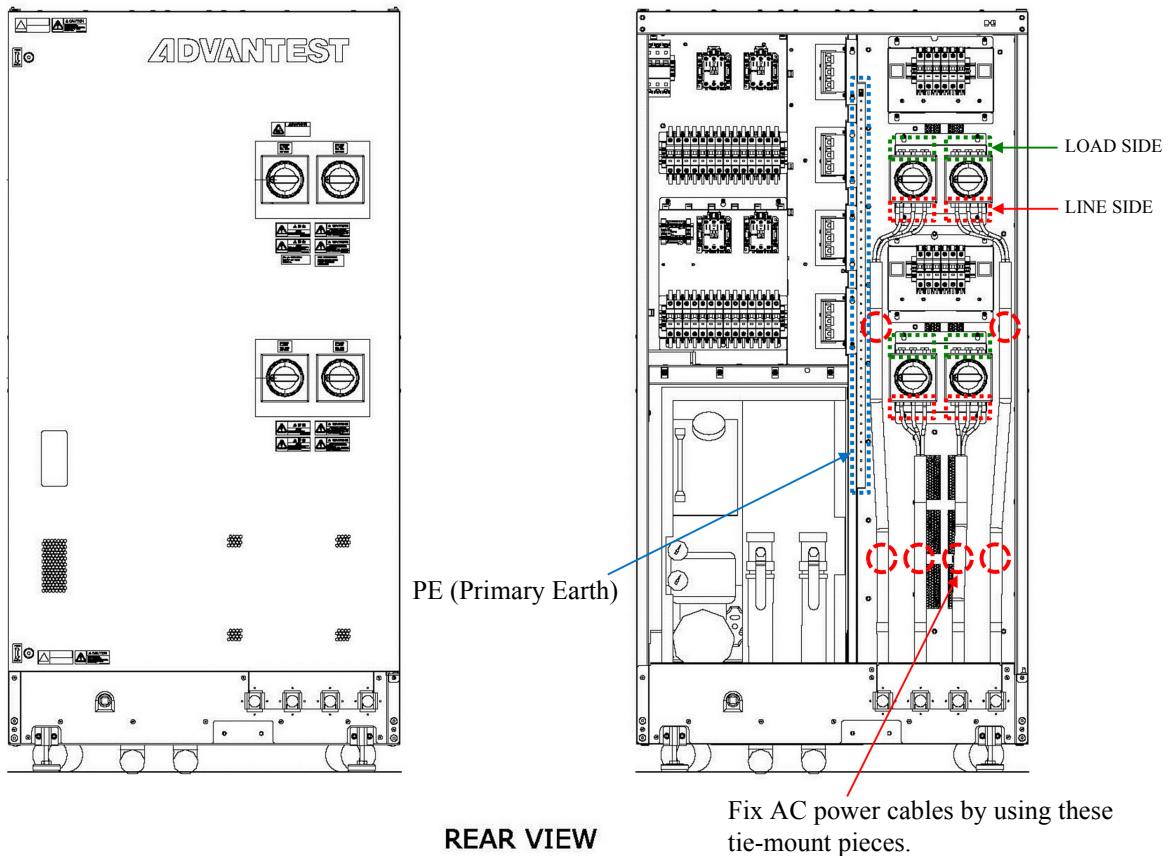


Figure 5-2 AC Power Supply Cables Routing

5.1.2.2 Power Requirements (for T5830PES)

- ES mainframe Input: Single phase 200 V 20A × 1 line
- Note: When shipping to Japan, China, Taiwan, Korea, and India, a 16-A rated power cable is included. Therefore, the power supply to the test system must be connected via a 16-A circuit breaker.*
- Air exchange cooling unit Input: Single phase 200 V 15A × 1 line
 - Power supplies for the system controller and LCD monitor are additionally required. For the input, single phase 200 V or 100 V can be selected.
 - For AC power supply input, the surge voltage in Common mode should not exceed 2000 V. If there is a possibility that a surge voltage in Common mode exceeding 2000 V could be generated, an appropriate countermeasure must be taken.
 - For AC power supply input, the surge voltage in Differential mode should not exceed 1000 V. If there is a possibility that a surge voltage in Differential mode exceeding 1000 V could be generated, an appropriate countermeasure must be taken.
 - The conductive interference voltage of the AC power supply should not exceed 10 V in Common mode or appropriate countermeasures must be taken.
 - The AC power supply momentary power loss must be 10 ms or less.
 - The electrical fast transient/burst voltage of the AC power supply should not exceed 2000 V or appropriate countermeasures must be taken.
 - The electrical fast transient/burst voltage of external interface cables should not exceed 1000 V or appropriate countermeasures must be taken.
 - The voltage requires the following stability:
Single phase 50/60 Hz ±0.5%
 - A protective earth (PE) must be connected to the power supply.

For more information on power consumption, refer to [Table 5-3](#).

Table 5-3 T5830PES Power Consumption

System	Power consumption
T5830PES	3.8 kVA

Rated interrupting capacity of power supply: 1.5 kA

5.1.3 Air Conditioning

5.1.3.1 Air Conditioning Requirements (for T5830P)

Table 5-4 shows the heat value of the T5830P. Consider the heat value when planning the air conditioning. Be sure to install air conditioning equipment in rooms where test systems are installed.

The specifications for the fan on the Test Head side and the quantity of exhausted air are shown in Table 5-4 and Figure 5-3.

Table 5-4 T5830P Generated Heat

System	Heat quantity
T5830P	106,020 kJ/h

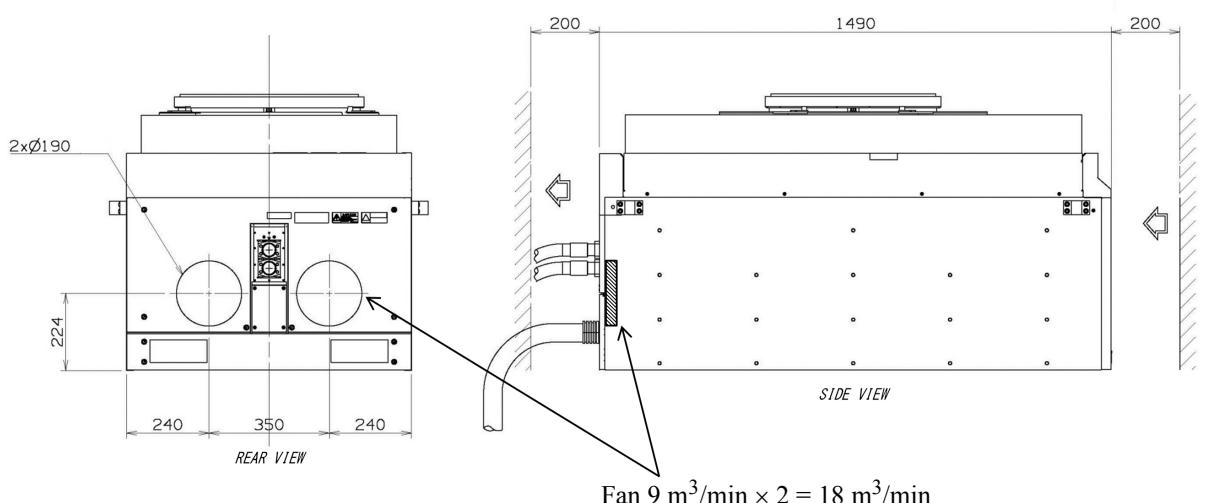


Figure 5-3 TH Fan

5.1.3.2 Air Conditioning Requirements (for T5830PES)

Table 5-5 shows the heat value of the T5830PES. Consider the relevant heat value when using air conditioning. An air conditioner must be installed in the room where the test system is installed.

Table 5-5 T5830PES Generated Heat

System	Heat quantity
T5830PES	12,928 kJ/h

5.1.4 Compressed Air

- (1) This test system requires the following air source for mounting and unmounting the performance board:

- Air Source: 0.49 MPa to 0.69 MPa dry air
- Air consumption: 30 L/min to 40 L/min (ANR)
- Air pressure dew point: -10°C or less

This test system requires two air source lines when using a test head stand.

- (2) Air supply hoses and hose clamps must be prepared by the customer.

Air hose connectors are provided by Advantest.

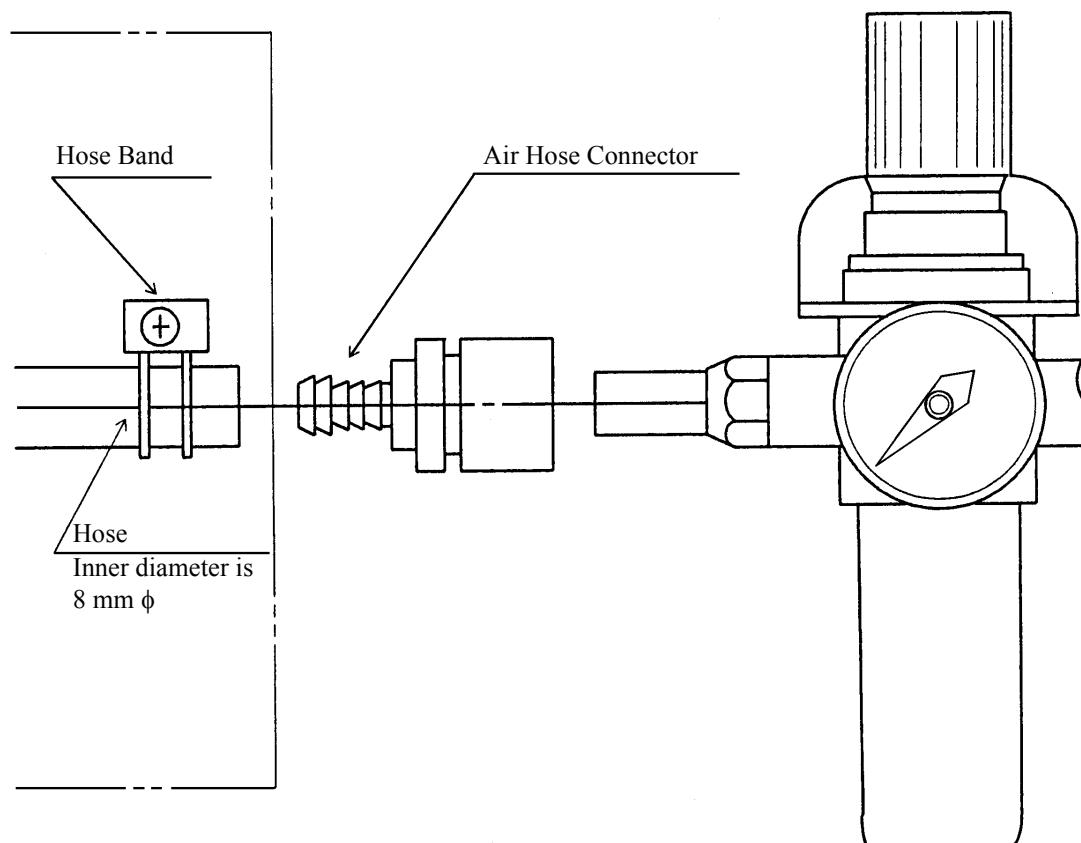


Figure 5-4 Connection

(3) To perform a wafer low temperature test^{*1} when the WMB has a center clamp mechanism, an air source such as the following one is required:

- 1. Air source: 0.49 MPa to 0.69 MPa dry air
- 2. Air consumption: 100 L/min (ANR) or more
- 3. Atmospheric pressure dew point: -70°C or lower
- 4. Input air grade: ISO8573 grade 1

Note: *If condition 4 is not satisfied, install a micro mist separator (rated filtration 0.01 µm).*

If conditions 1 to 4 are not satisfied, an Advantest dry air unit is required. In that case, contact Advantest.

*1: The low temperature test refers to a test using a wafer cooling function.

When the WMB does not have a center clamp mechanism, the air source described previously is not required.

5.1.5 Floor Plan

5.1.5.1 Floor Plan (for T5830P)

Figure 5-5 shows a standard floor plan for the T5830P.

Secure space for maintenance approximately 1 m between the rear surface of the mainframe and the wall.

The height of the room from floor to ceiling must be at least 2.4 m.

The outer dimensions (height × width × depth) of the mainframe and test head are as follows:

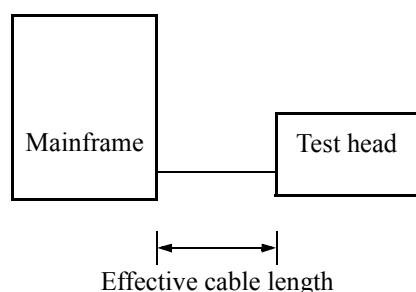
- MF: 1650 mm × 850 mm × 1050 mm
- TH: 640 mm × 830 mm × 1490 mm
- Monitor desk (option): 680 mm × 650 mm × 900 mm
- RCPU (option): 450 mm × 220 mm × 570 mm

Table 5-6 shows the movable distance of each part.

Table 5-6 Movable Distance

Unit name	Starting point	Effective cable length
Test head	Mainframe	Approx. 6.0 m
Monitor desk (option)	Mainframe	Approx. 6.0 m

Note: "Effective cable length" in the table refers to that shown below.



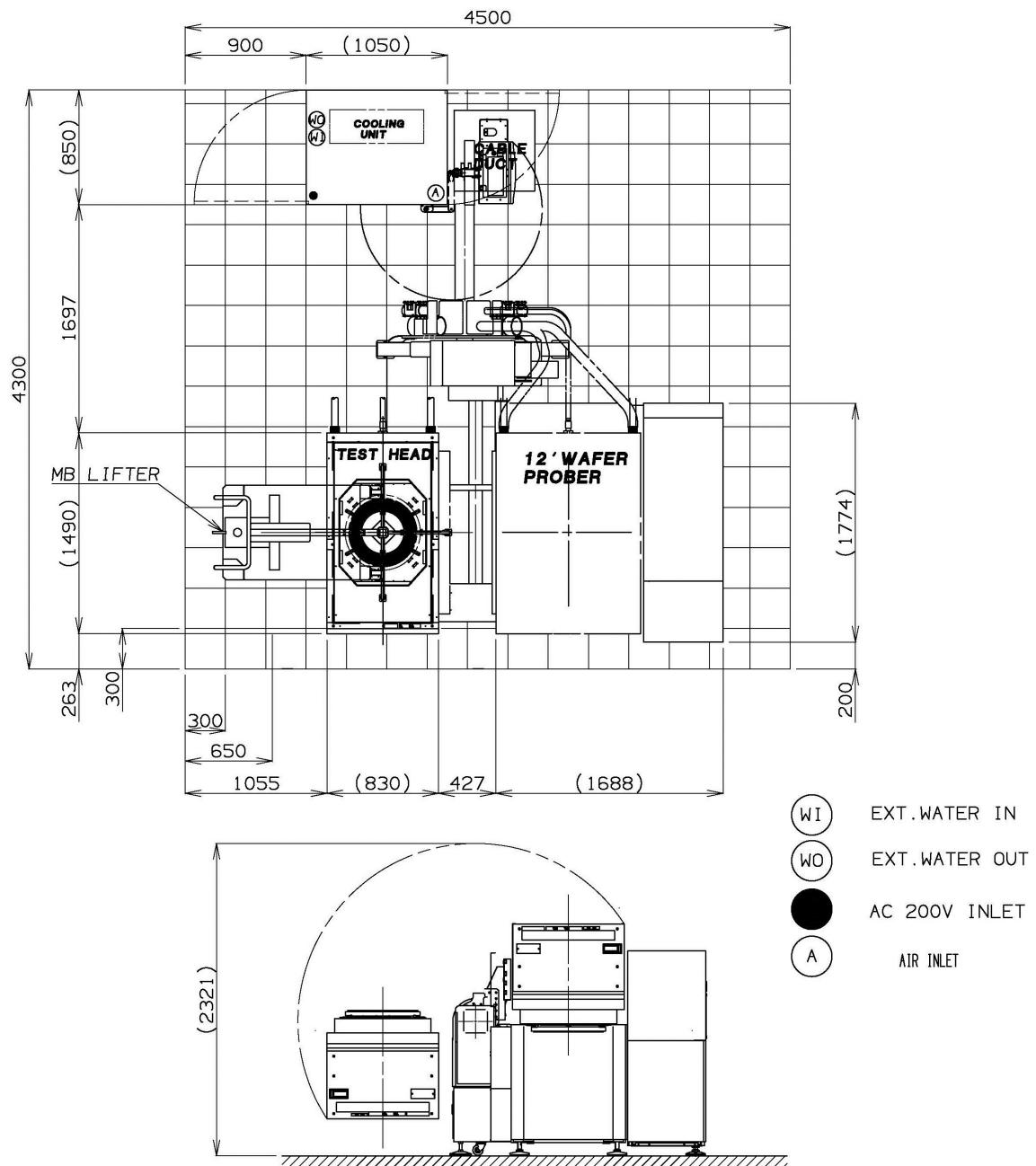


Figure 5-5 T5830P + Prober Specification Floor Plan

5.1.5.2 Floor Plan (for T5830PES)

[Figure 5-7](#) shows a standard floor plan for the T5830PES.

The T5830PES and its air exchange cooling unit use the following air intake and exhaust system.

- (1) The ES mainframe takes air from the left and right sides and releases heat to the back and underside.
 - (2) The cooling unit takes air from the front and releases heat to the left and right sides and the back.
- Do not use the T5830PES where the exhausted heat circulates internally.

As shown in [Figure 5-6](#), do not place any obstacles within 200 mm on each side of the ES mainframe and 250 mm on each side of the cooling unit so it can intake and exhaust air.

Also, note the following when moving the T5830PES for installation.

Do not move the T5830PES over an uneven floor on its casters.

When it is necessary to move the T5830PES over an uneven surface, prepare an appropriate ramp beforehand and then move the system. The system can only be moved on a flat floor.

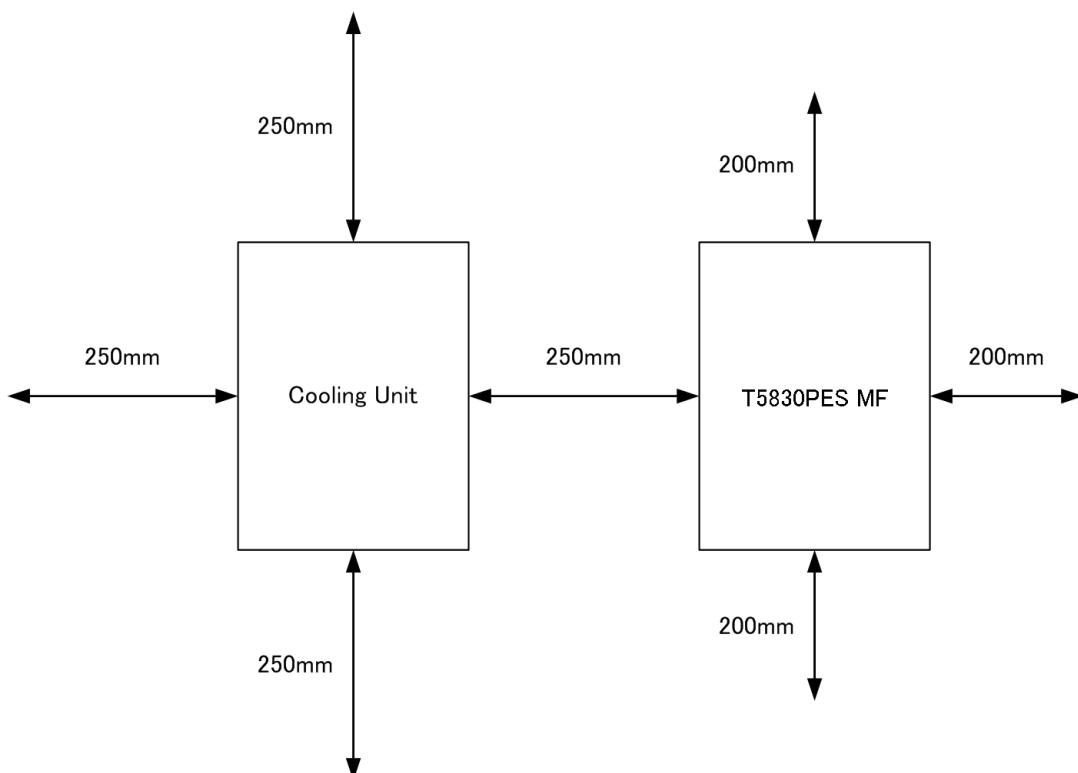


Figure 5-6 T5830PES Layout Restrictions

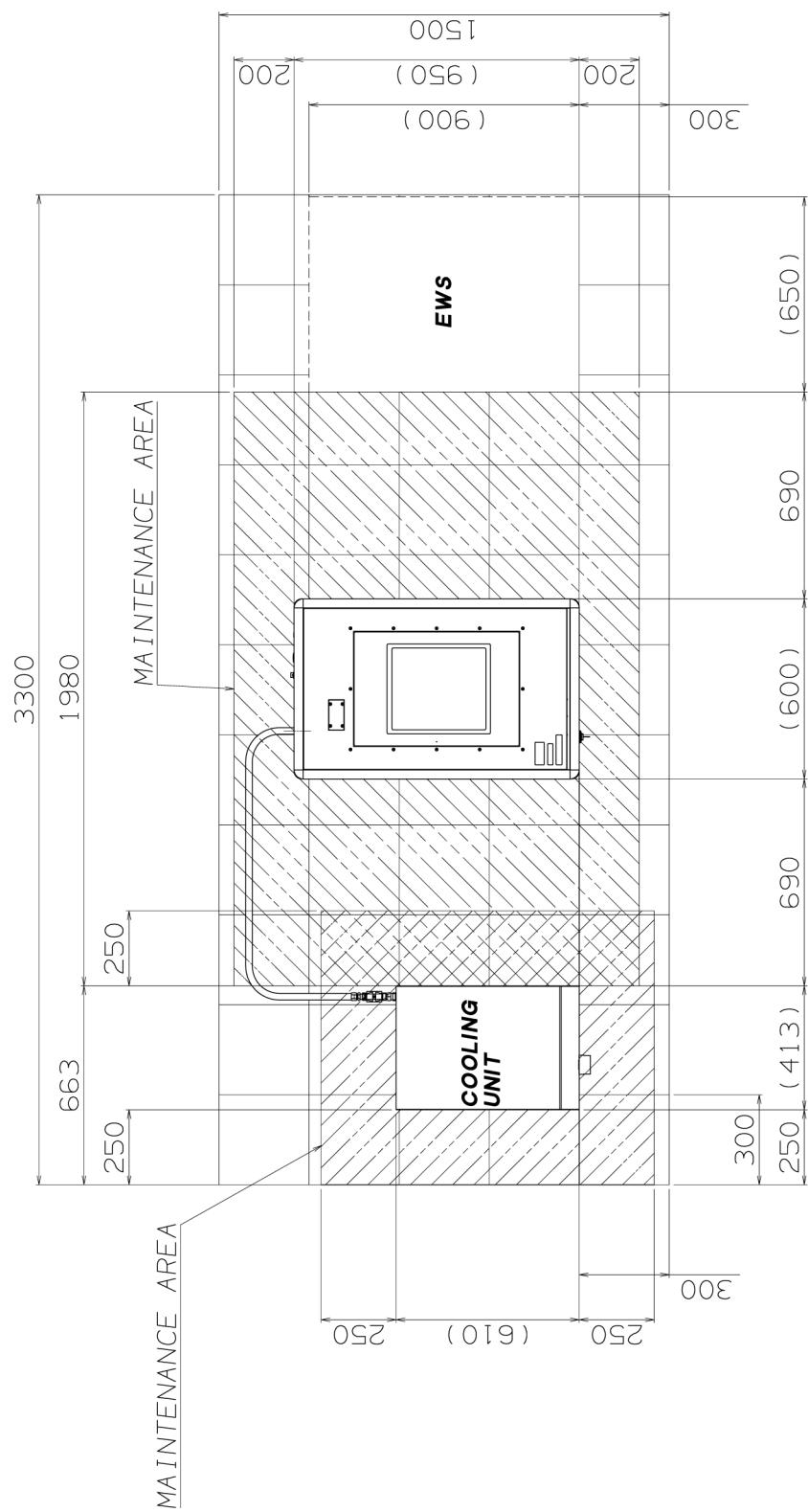


Figure 5-7 T5830PES Floor Plan

5.1.6 System Weight

Table 5-7 T5830P System Weight

Unit Name	Weight
MAIN FRAME	615 kg
TEST HEAD	32 Site + 4 HLVDR
	32 Site + 6 HLVDR
	32 Site + 12 HLVDR
	905 kg

The test head includes cables (entire length) and a mother board.

Table 5-8 T5830PES System Weight

Unit Name	Weight
ES MAIN FRAME	185 kg
COOLING UNIT	85 kg

ES MAIN FRAME includes a mother board.

5.1.7 Tester Name Plate

When operating multiple test systems, it is convenient to assign a name to each test system. This test system has a name tag on the left side of the mainframe that allows a name to be written on it. A maximum of five alphanumeric characters can be written after "T5830P" or "T5830PES."

Example: T5830P AT1
 T5830PES AT1

5.1.8 Carriage Requirements

- Floor strength: 8.7 kPa to 12.9 kPa

CAUTION!

Maximum floor pressure where a wheel of the test head passes: 770 kg per wheel

Average floor pressure: 385 kg per wheel

Take into account the floor strength of the pathway. Use floor guard boards if necessary.

- Width and height of building entrance: Width: 2.0 m or wider Height: 2.5 m or higher
- Width and height of route: Width: 2.3 m or wider Height: 2.5 m or higher
- Width and height of test room entrance: Width: 2.0 m or wider Height: 2.0 m or higher

5.1.9 Earthquake-proof

Advantest provides fixtures to protect test systems and their peripheral devices against earthquake damage (Option). The fixtures must be secured to the floor with anchor bolts. Thus, the location of the test systems must be determined in advance.

For installation of the earthquake kit, refer to [Figure 5-8](#), [Figure 5-9](#), and [Figure 5-10](#).

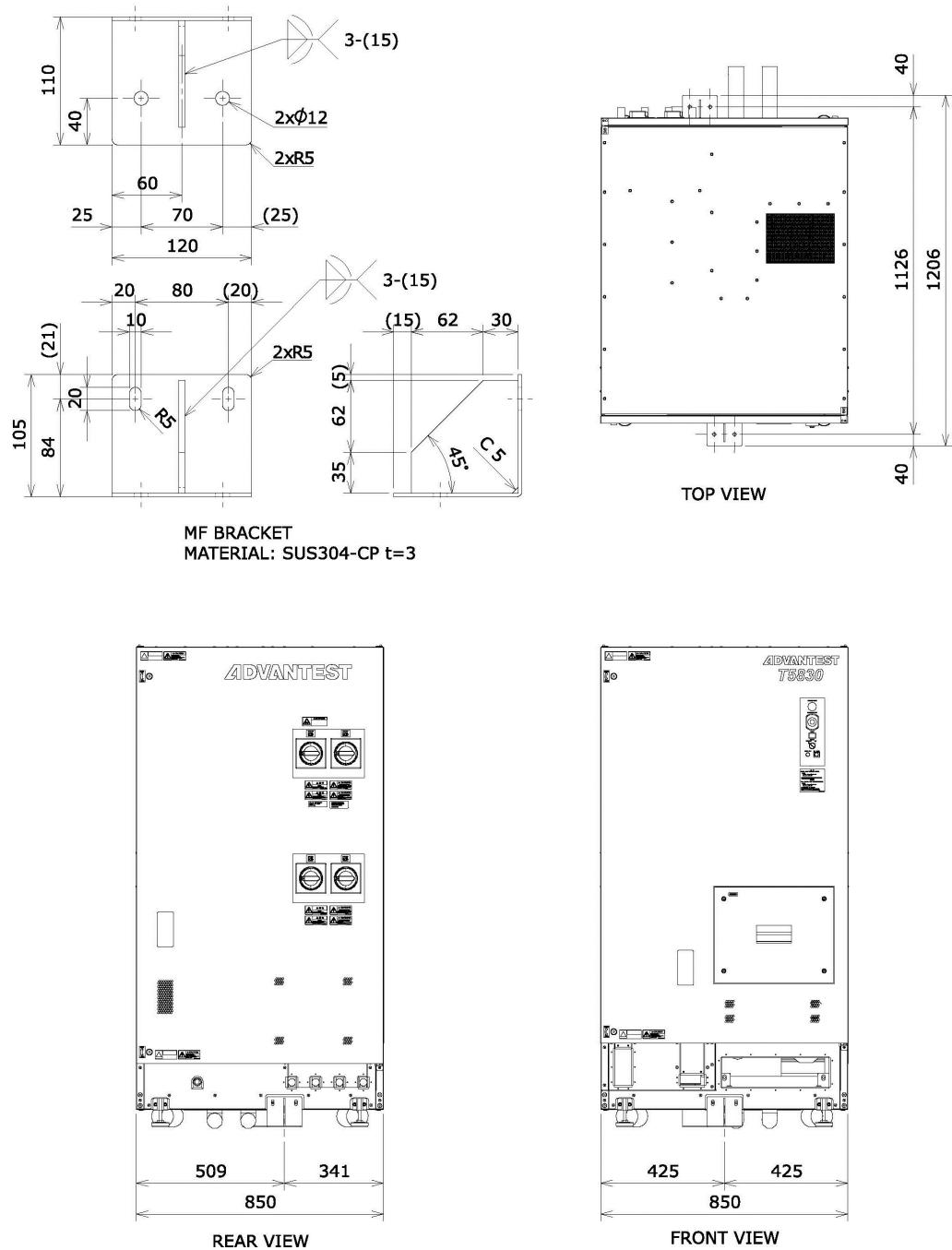


Figure 5-8 Earthquake Kit Installation (T5830P Mainframe)

5.1 Installation Plan

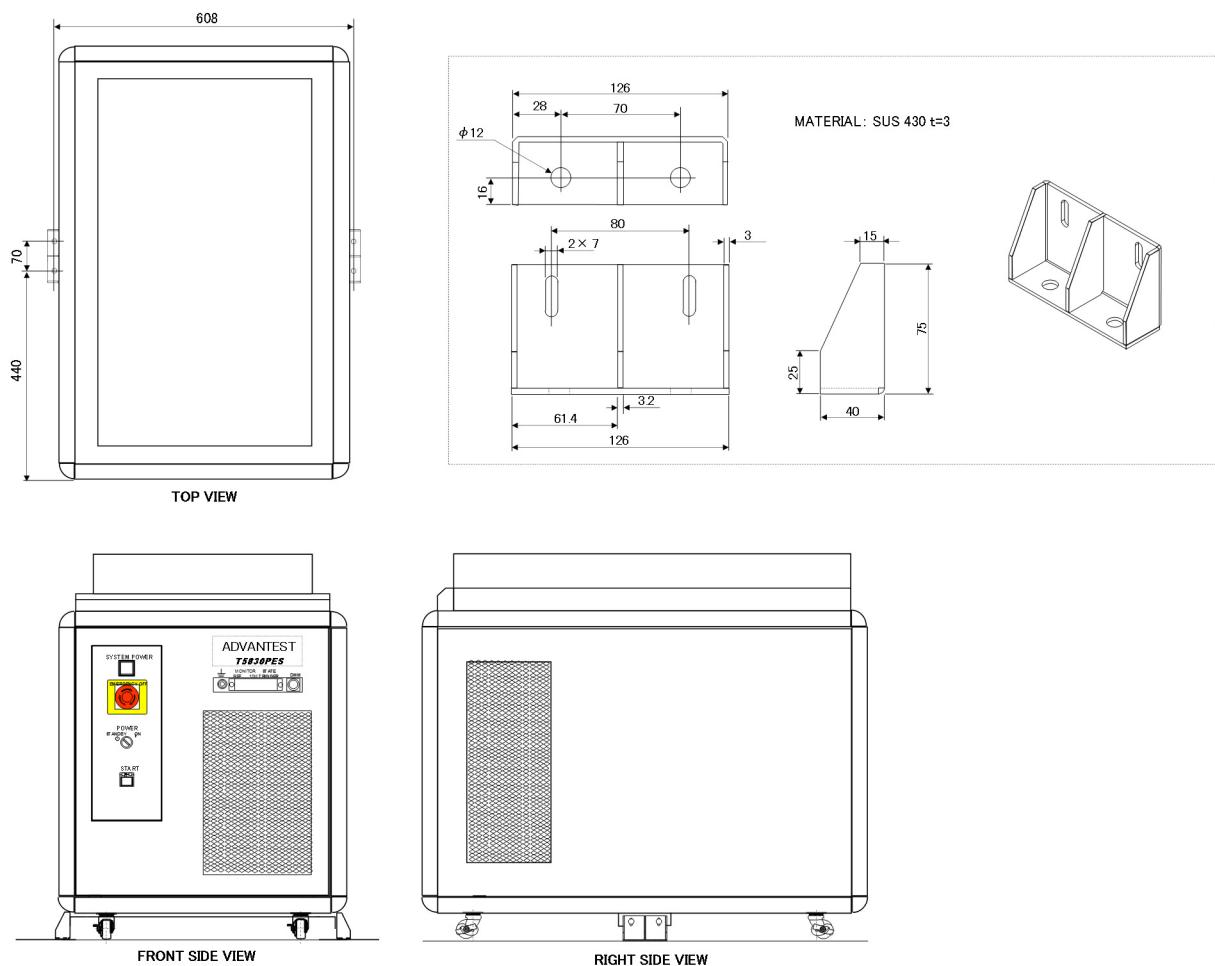


Figure 5-9 Earthquake Kit Installation (T5830PES Mainframe)

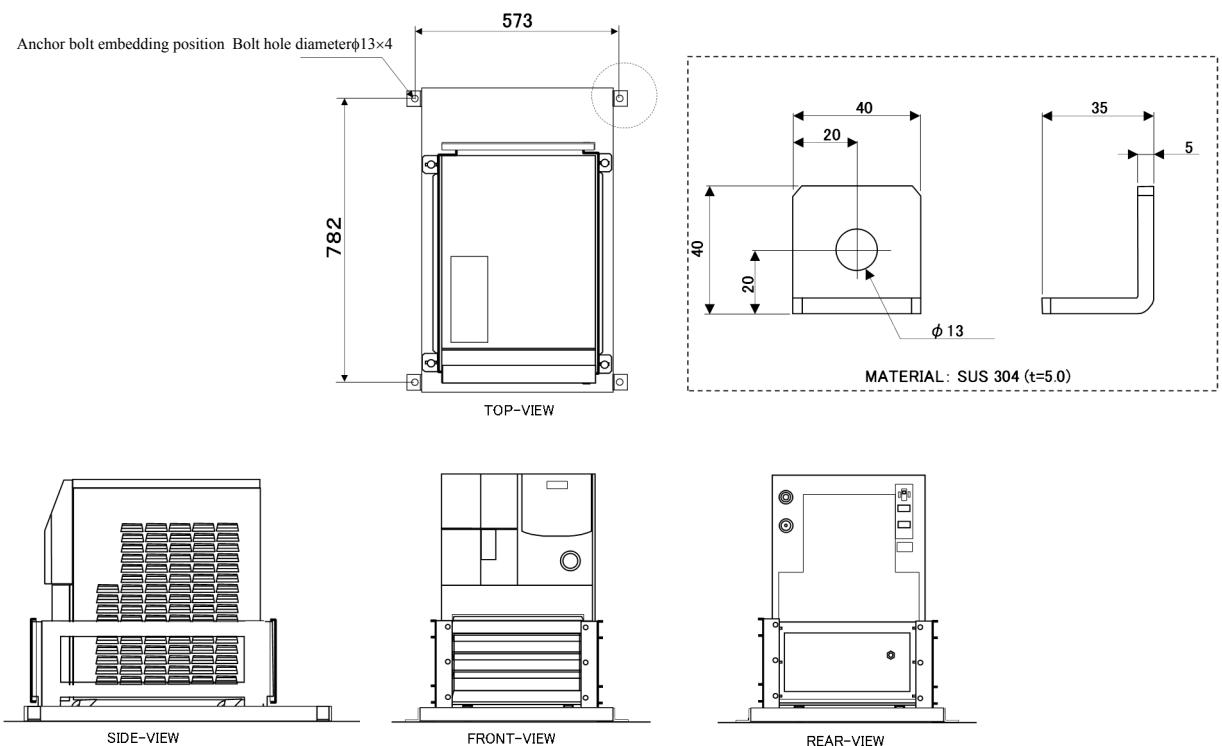


Figure 5-10 Earthquake Kit Installation (T5830PES Cooling Unit)

5.1.10 Cooling Water (T5830P)

The tester cooling unit requires externally supplied cooling water.

(1) Cooling water supply conditions

Cooling water supplied to the test system cooling unit must satisfy the following conditions:

- Temperature range: 7°C to 20°C
- Temperature variation: The amount of temperature change within ten minutes is 1°C or less.
- Flow variation: 5%/min. or less
- Pressure: 0.15 MPa to 0.7 MPa
- Return pressure: 0.35 MPa or less
(However, the difference from the supply pressure must be 0.15 MPa or greater.)

Supply flow rate and pressure loss vary depending on the cooling water temperature ([Figure 5-11](#)).

The numeric values are roughly estimated based on the heat discharge of a full configuration test system.

Heat discharge with the full configuration: 26.0 kW

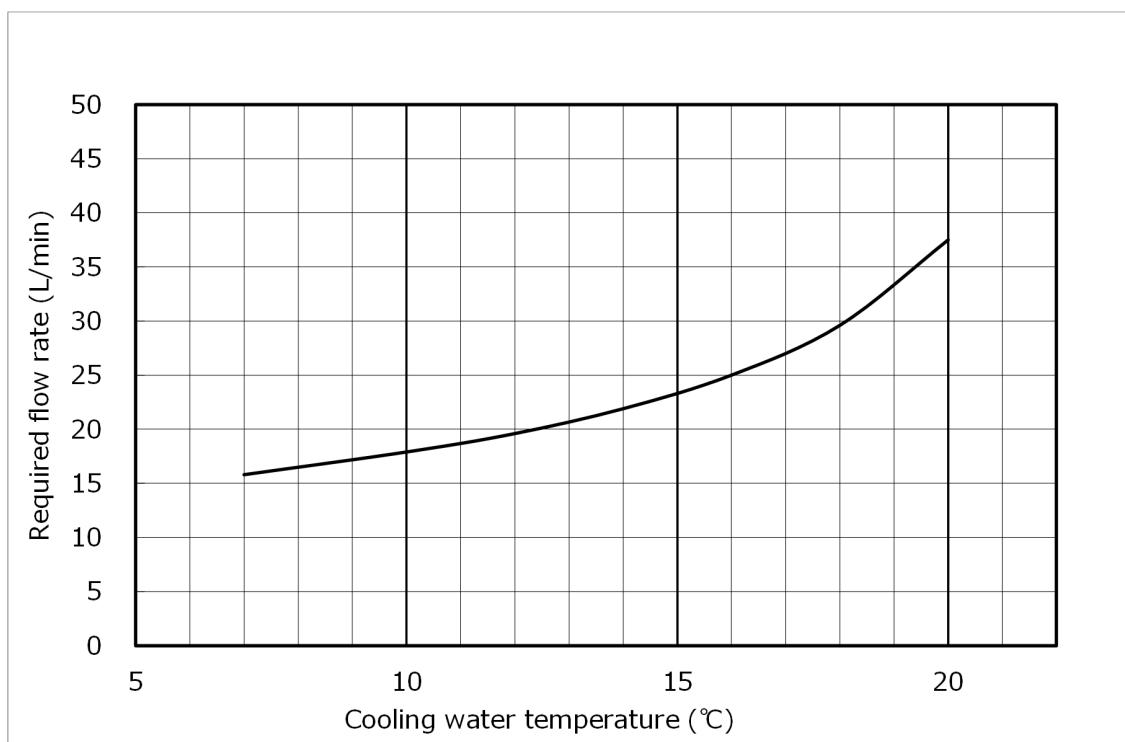


Figure 5-11 Cooling Water Temperature and Required Flow Rate

(2) Water quality conditions

The cooling water must meet the following conditions:

<Standard items>

pH (25°C)		:	6.8 to 8.0
Conductivity (25°C)	(μS/cm)	:	400 or less
Chloride ion	Cl ⁻ (mgCl ⁻ /l)	:	50 or less
Sulfate ion	SO ₄ ²⁻ (mgSO ₄ ²⁻ /l)	:	50 or less
Acid consumption (pH 4.8)	(mgCaCO ₃ /l)	:	50 or less
Total hardness	(mgCaCO ₃ /l)	:	70 or less
Ionized silica	SiO ₂ (mgSiO ₂ /l)	:	30 or less
Calcium hardness	(mgCaCO ₃ /l)	:	50 or less

<Reference items>

Iron	Fe	(mgFe/l)	:	1.0 or less
Sulfide ion	S ²⁻	(mgS ²⁻ /l)	:	Cannot be detection
Ammonium ion	NH ₄ ⁺	(mgNH ₄ ⁺ /l)	:	1.0 or less
Copper	Cu	(mgCu/l)	:	1.0 or less
Residual chlorine		(mgCl/l)	:	0.3 or less
Free carbon dioxide		(mgCO ₂ /l)	:	4.0 or less

The above water quality is based on the water quality standard (JRA-GL-02-1994) by Japan Refrigeration and Air Conditioning Industry Association.

- Pure water, distilled water, and ion exchange water must not be used because these types of water may damage the cooling unit.
However, if use of these water types is unavoidable, comply with the standard related to metal ion and adjust the resistivity to $10^4 \Omega\cdot\text{cm}$ or lower.
- If water-treatment chemicals are used, the water quality described above may change.
For appropriate use of water-treatment chemicals, consult with the relevant dealer.

(3) Others

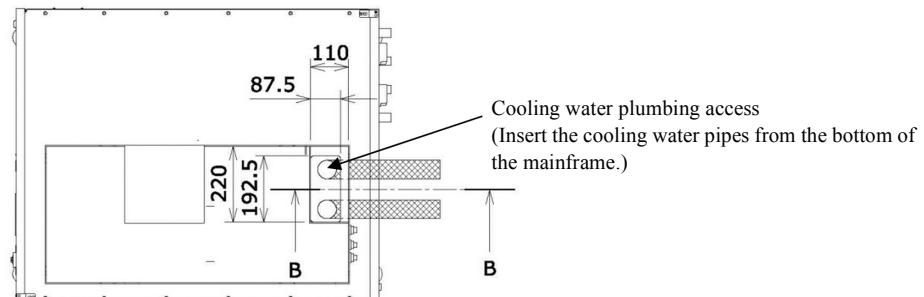
Stainless steel pipes are recommended for the external cooling water plumbing. If galvanized steel pipes or lined steel pipes are used, cooling unit maintenance may have to be performed more often due to factors besides those in Water Quality described above.

5.1.11 Plumbing (T5830P)

(1) Main Frame External cooling water pipe Routing

The connection locations and size of the cooling system plumbing for the test system are as follows:

- ① Cooling water inlet (with a shut-off valve.) × 1
Tapered female coupling Rc1-1/4 (ISO 7/1)
- ② Cooling water outlet (with a shut-off valve.) × 1
Tapered female coupling Rc1-1/4 (ISO 7/1)
- ③ Drain (secured with a plug) × 1
Tapered female coupling Rc1/2 (ISO 7/1)



SECTION A-A

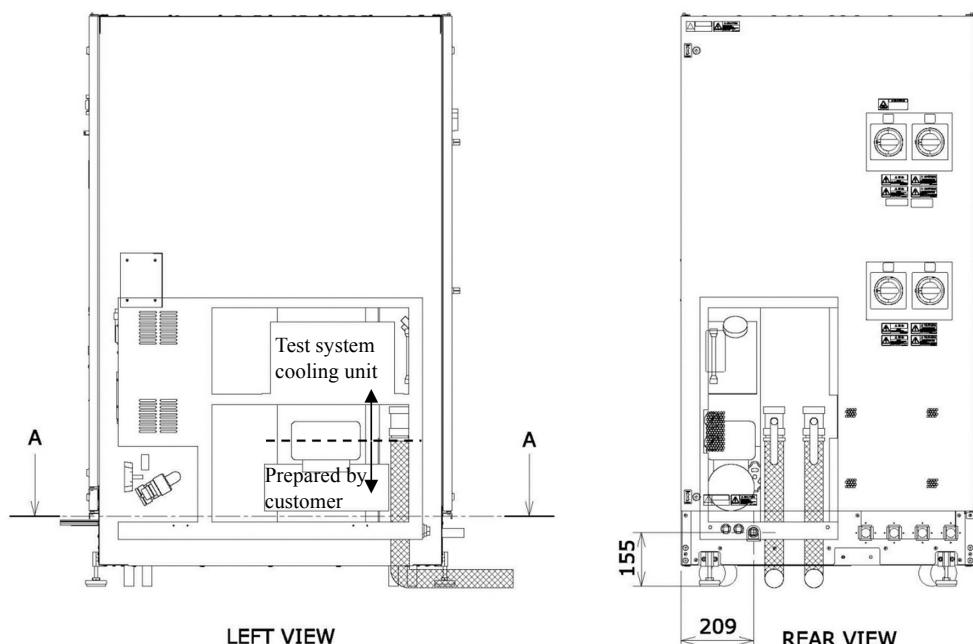


Figure 5-12 Plumbing Connections (1)

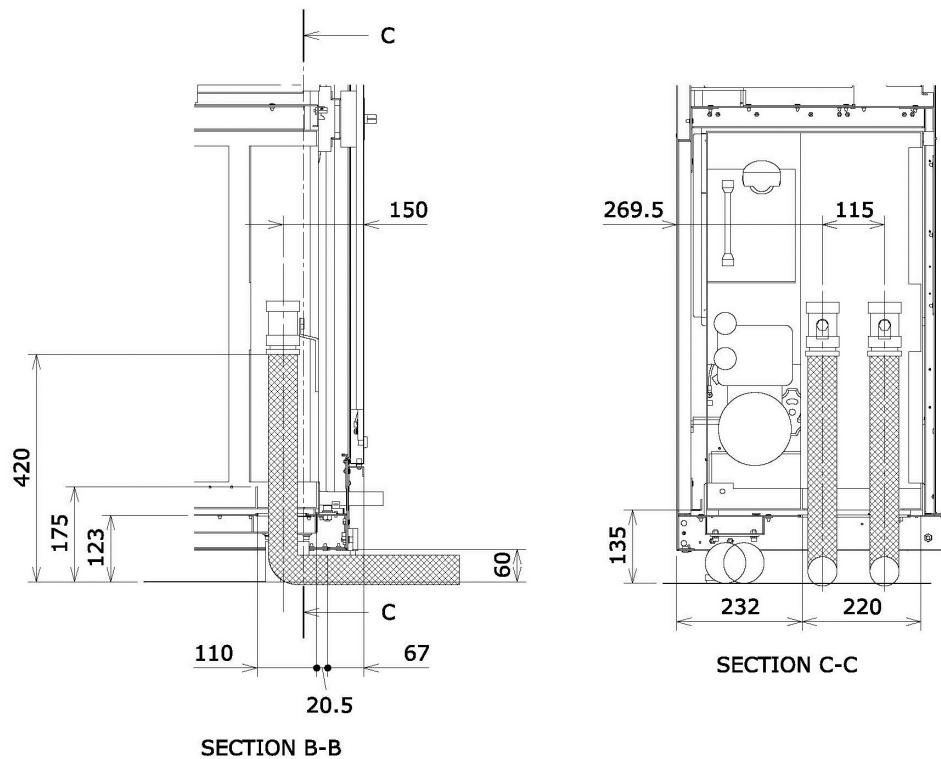


Figure 5-13 Plumbing Connections (2)

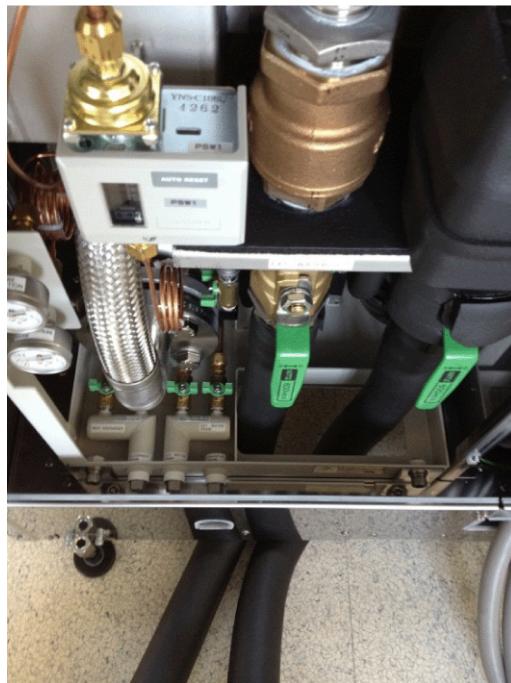


Figure 5-14 Plumbing Connections (3)

(2) Plumbing

- All plumbing work needs to be prepared by the customer.
- Install a mesh strainer (size: 100) on the cooling water inlet to prevent foreign matter from entering.
- The cooling water may cause condensation on the pipe surface, depending on the temperature of the water. Because of this, protect the plumbing from the effects of the surrounding air when necessary.
- If water leaks inside the chiller, drain the water from the chiller.
- Fluorinert may be mixed with the cooling water in the drainpipe. For this reason, install a valve outside the drain outlet so that the Fluorinert/water mixture is not drained directly to the waste water treatment facility.
- Install a thermometer, pressure gage and flow meter so that the status of the cooling water can be monitored. When selecting a flow meter, consider that the flow rate of cooling water changes depending on the configuration and usage condition of the test system.
- When the test system is stopped, the inlet valve shuts the cooling water off so that it cannot flow into the chiller. The cooling water supply equipment has to operate correctly when the valve is closed.

Figure 5-15 shows an example of how the pipes are installed.

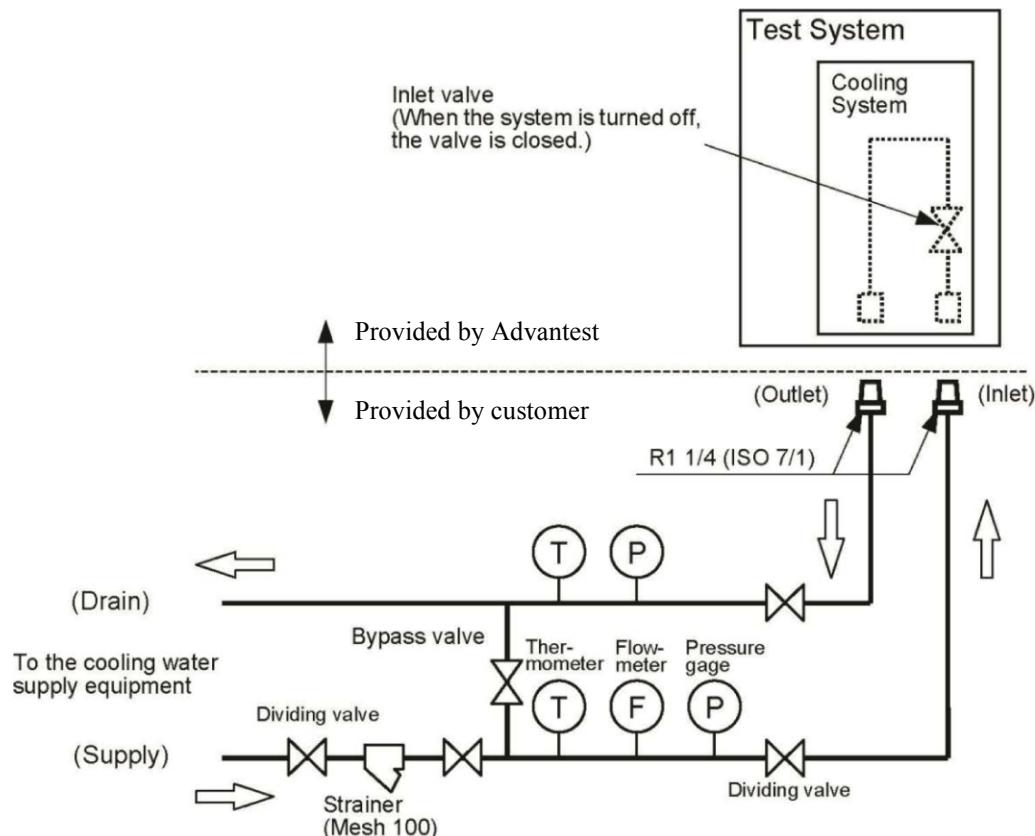


Figure 5-15 Cooling Water Plumbing Example

5.2 Safety

This section describes safety measures for the T5830P/T5830PES memory test system.

5.2.1 Standards Compliance

Compliant with the following standards according to the supported option:

<Safety>

- SEMI S2
- SEMI S8

<EMC>

- FCC Part15
- KC Mark

FCC Part 15 Subpart B Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

KC Class A

A 급 기기(업무용 방송통신기기)

이 기기는 업무용(A 급)으로 전자파적합등록을 한 기기이오니
판매자 또는 사용자는 이 점을 주의하시기 바라며, 가정외의
지역에서 사용하는 것을 목적으로 합니다.

Applicant: ADVANTEST corporation

Registration No.: MSIP-REM-qa2-T5830

Equipment Name: Memory Test System

Basic Model Number: T5830

Series Model Number: T5830P

Manufacturer: ADVANTEST corporation

Country of Origin: Japan

Applicant: ADVANTEST corporation

Registration No.: MSIP-REM-qa2-T5830ES

Equipment Name: Memory Test System

Basic Model Number: T5830ES

Series Model Number: T5830PES

Manufacturer: ADVANTEST corporation

Country of Origin: Japan

5.3 Witness Test and Installation

5.3.1 Witness Inspection Procedure

If the witness inspection is required before shipment of this test system from the factory, the following procedure must be used.

- (1) Verification of system configuration according to acceptance specification
- (2) Verification of system performance according to test certificate
- (3) Test system performance test according to diagnostic programs applied by Advantest
- (4) Verification of carry-in conditions and installation environment

Verification of system configuration mentioned in (1) refers to a check to be conducted according to the individual manufacture specification you approved in advance.

Verification of system performance mentioned in (2) refers to a check to be conducted according to the test certificate stating the system test items and its results.

(3) is performed according to diagnostic program and diagnostic performance board. This diagnostic program is confirmed by the display of the following message.

For the T5830P: T5830P DIAGNOSIS PASS

For the T5830PES: T5830PES DIAGNOSIS PASS

The check according to this diagnostic program is to be conducted for the test system which has been passed 30 minutes or more after its power source is turned on.

Test (4) is to confirm that no problems such as obstacles exist on the system transportation route and to check the installation environment and layout.

Additional requirements other than for witness test items and procedures (1) through (4) prepared by Advantest should be submitted to us prior to the witness test. These requirements will be included in the witness test items when approved by us. Extra charge for the witness test by the additional requirements shall be borne by the Customer.

5.4 Installation and Acceptance

- (1) The installation work includes the following:
 - Delivery to specified site
 - Moving into place, assembly, and adjustment
 - Installation completion verification.
- (2) The connection of power supply and ground lines is the customer's responsibility, it should be ready within one hour after the system has arrived.
- (3) This test system is transported on its attached casters, from shipping to installation site. It is essential to select an appropriate path to ensure safe carriage (be careful about stairs, cracks, width, height, rain, dust, and corrosive gases).
- (4) The carriage path and the installation site must be satisfied with conditions described in Section 5.1, "[Installation Plan](#)."
If any trouble exists, contact us beforehand.
- (5) System installation is made on the basis of the layout depicted in the individual product specification.
- (6) The completion of installation must be checked by following the same procedure of Section 5.3.1, and the Installation Completion Report must be created.
- (7) An installation completion memo verifies that the installation and acceptance are completed.

6. Diagnosis and Maintenance

6.1 System Diagnostic Programs

This test system provides three system diagnostic programs:

- (1) Self-diagnostic program for use during system startup

The self-diagnostic program for use during system startup is used for self-diagnosis of the system processors, and is executed immediately after the system power has been turned on. Unless this diagnostic result is PASS, the system software cannot start.

- (2) System diagnostic program

The system diagnostic program checks all of the various system functions. Its main function is to isolate faulty boards which need to be replaced.

- (3) Peripheral diagnostic programs

The peripheral diagnostic program checks each of the peripheral equipment functions, as well as I/O communication with the peripheral processor.

6.2 Maintenance

6.2.1 System Maintenance

The system maintenance has been designed to locate a faulty board by using the system diagnostic program. The faulty board can be replaced with the spare board.

6.2.2 Test System Cooling Unit Maintenance

6.2.2.1 Test System Cooling Unit Maintenance (T5830P)

To maintain optimum performance of the cooling unit, the unit needs to be checked periodically.

(1) Monthly check

Check the following items once a month.

For more information on how to check the items, refer to the maintenance manual.

Fluorinert flow rate: 71 ± 4 L/min (basic frame configuration)

Fluorinert temperature: $27 \pm 1^\circ\text{C}$

Operating noise or vibration: Ensure that no abnormal operating noise or vibration is generated.

Leakage: Ensure that no leakage is present in the piping system.

Liquid level of the tank: Ensure that the tank liquid level meter indicates a proper liquid level.

(2) Periodical check

To maintain the cooling unit performance and safety, the cooling unit should be inspected once a year and some limited-life parts must be replaced. Advantest recommends that preventative maintenance be implemented through our annual maintenance contract or inspection service.

(3) Preventative maintenance

To prevent cooling unit failure and to maintain it in a good condition, Advantest recommends that parts of the cooling unit be checked, adjusted, and replaced (overhauled) every 4 or 5 years.

However, depending on the environment in which the cooling unit is installed, some parts may need to be adjusted or replaced in shorter periods than specified replacement/adjustment periods.

6.2.2.2 Tester Cooling Unit Maintenance (T5830PES)

To maintain optimum performance of the cooling unit, the unit needs to be checked periodically.

(1) Monthly check

Check the following items once a month.

For more information on how to check the items, refer to the maintenance manual.

Table 6-9 T5830PES Monthly Check

No.	Inspection item	Description	Judgment standard	Necessity of recording
1	Fluorinert temperature	Confirm that the temperature value displayed when the unit is operating is within the specified range.	Within $27 \pm 1^{\circ}\text{C}$	Necessary
2	Pump discharge pressure	Confirm that the pump discharge pressure value displayed when the unit is operating is within the specified range.	Between 380 and 460 kPa	
3	Operation noise or vibration	Confirm that there is no abnormal vibration or noise during operation of the unit.	No abnormal vibration and operating noise	Unnecessary
4	Fluorinert leakage	Confirm that Fluorinert is not leaking from the unit during operation.	No leakage	
5	Fluorinert tank liquid level	Check the liquid level indicated on the tank liquid level meter.	The liquid level must be between NORMAL and LOW. (*1)	
6	Condenser (radiator fins)	Check whether any dust or dirt is on the fins.	Visible dust and dirt must not be on the fins.	

(*1) *If the Fluorinert liquid level is lower than LOW, refer to the maintenance manual to add Fluorinert up to the acceptable level.*

(2) Periodical check

To maintain optimum performance and safety of the tester cooling unit, each part of the cooling unit needs to be checked on a yearly basis and life-limited components need to be replaced. Advantest recommends that preventative maintenance be implemented through our annual maintenance contract or inspection service.

(3) Preventative maintenance

To prevent cooling unit failure and to maintain it in a good condition, Advantest recommends that the pump transducer be replaced every one or two years and other parts of the cooling unit be checked, adjusted, and replaced (overhauled) every 3 or 4 years.

However, depending on the environment in which the cooling unit is installed, some parts may need to be adjusted or replaced in shorter periods than specified replacement/adjustment periods.

7. Replacement of Limited Life Parts

To ensure stable operation of the system, replace the limited life parts by referring to their life expectancy shown in the table below.

However, depending on the environment in which the parts are used, or the frequency of the usage, replacement may be required before the specified time limit.

Table 7-1 Limited Life Parts

Part name	Service life	Remarks
Unit power supply	5 years	Including capacitors
Fan motor	5 years	
LCD backlight	3 years	
Optical drive	5 years	Operating rate: 1%, insertion/removal of media: once/2 days
Hard disk drive	2 years	Operating for 24 H/day 365 days/year
Coaxial LIF connector	1000 cycles	
Lithium battery	5 years	EWS (T5830P/T5830PES) HUB (T5830PES) RCPU (T5830P)
T5830PES Chiller (2KW Chiller)	Pump	1.1 years
	Pump motor	3.5 years
	Fan motor	2 years
	Compressor	5 years
	Solenoid valve	3 years
T5830P CU (40KW CU)	Cooling unit motor	5 years
	Cooling pump	4 years
	Inverter	3 years

8. Warranty and Customer Support

8.1 Warranty

- (1) Unless otherwise specifically agreed by customer and Advantest in writing, Advantest warrants that products (other than consumables and third party products) shall be free from defects in material and workmanship and shall conform to its specifications during the warranty period.
- The warranty period is : twelve (12) months from the date of installation for products (other than consumables, parts, and third party products),
- (2) Advantest warrants that software will not fail to execute its programming instructions due to defects in materials and workmanship when properly installed and used on the hardware designated by Advantest and will substantially conform to its specifications and documentation as they exist on the delivery date for a period of twelve (12) months following (i) for software installed on the system as of such system's delivery date, the installation date of the system, or (ii) for all other software, its delivery date. In addition to any other warranty limitations in these terms, Advantest does not warrant that software will operate in hardware and software combinations selected by customer, or meet requirements specified by customer.
 - (3) This warranty (and all of Advantest's obligations with respect thereto) terminates and is void in the event that, without Advantest's prior written consent, (i) the product is moved from its original installation site or (ii) the product is sold or transferred by the customer to a third party.
 - (4) The warranty provided herein is extended solely to customer and not to any third party.
 - (5) This warranty does not apply to defects or damages to the product or any parts or components thereof resulting from any of the following:
 - (5-1) any improper or inadequate maintenance, any improper or inadequate site preparation, handling, unauthorized modification, carriage or storage of the product by the customer or any third party (other than Advantest or its agents);
 - (5-2) use of the product not in conformance with or under operating conditions or environments different than those specified in the specifications or the operation manual or recommended in writing by Advantest, including, without limitation, (1) instances where the product has been subjected to physical stress or electrical voltage exceeding the permissible range and (2) instances where the corrosion of electrical circuits or other deterioration was accelerated by exposure to corrosive gases or dusty environments;
 - (5-3) use of the product in connection with software, interfaces, products or parts other than software, interfaces, products or parts supplied or recommended in writing by Advantest;
 - (5-4) incorporation in the product of any parts or components (1) provided by customer or (2) provided by a third party at the request or direction of customer or due to specifications or designs supplied by customer (including, without limitation, any degradation in performance of such parts or components);
 - (5-5) Advantest's incorporation or use of any specifications or designs supplied by customer;
 - (5-6) the occurrence of an event of force majeure; or
 - (5-7) any negligent act or omission of the customer or any third party other than Advantest.

- (6) If Advantest receives notice of defects or non-conformance during the warranty period for products other than software, customer's exclusive remedy under this warranty shall be repair or replacement, at Advantest's option, of the affected products. If Advantest determines that it is unable, within a reasonable time, to repair or replace the affected products, Advantest will grant a refund of the purchase price less a reasonable depreciation, upon prompt return of the products to Advantest. Advantest's sole obligation under this warranty with respect to software shall be limited to using commercially reasonable efforts to correct material defects and supply customer with a corrected version of such software as soon as practicable after customer has notified Advantest of such material defects.
- (7) Except as otherwise specifically agreed by Advantest and customer in writing, Advantest warrants consumables purchased by customer shall be free from defects in materials and workmanship upon receipt. Customer's exclusive remedy under this warranty is limited to replacement of the defective consumable(s).
- (8) Advantest does not warrant that the operation of products shall be uninterrupted or error free.
- (9) Advantest reserves the right to use remanufactured, refurbished and/or reconditioned parts, which are equivalent to new in performance, in products and Remarketed products.
- (10) To the extent legally permitted, Advantest does not warrant or support any third party products even if included with other Advantest branded products. Advantest provides all such third party products AS-IS. However, the original manufacturers or suppliers may provide their own warranties as specified in the documentation accompanying such third party products.
- (11) Customer is responsible for removing any items not eligible for warranty service. Failure to remove such items may result in additional charges to customer computed at Advantest's then current standard service rates.
- (12) Customer is responsible for maintaining a procedure external to the products to reconstruct lost or altered customer files, data or programs. Customer shall have a representative present when Advantest provides warranty services at customer's site. Customer shall notify Advantest if products are being used in an environment, which poses a potential health hazard to Advantest employees or subcontractors. Advantest may refuse to provide warranty services in such environment or require customer to maintain such products under Advantest supervision.
- (13) EXCEPT TO THE EXTENT EXPRESSLY PROVIDED HEREIN, ADVANTEST HEREBY EXPRESSLY DISCLAIMS, AND CUSTOMER HEREBY WAIVES, ALL WARRANTIES, WHETHER EXPRESS OR IMPLIED, STATUTORY OR OTHERWISE, INCLUDING, WITHOUT LIMITATION, (1) ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, NON-INFRINGEMENT, COURSE OF DEALING OR USAGE OF TRADE AND (2) ANY WARRANTY OR REPRESENTATION AS TO THE VALIDITY, SCOPE, EFFECTIVENESS OR USEFULNESS OF ANY TECHNOLOGY OR ANY INVENTION. THE REMEDIES SET FORTH HEREIN SHALL BE THE SOLE AND EXCLUSIVE REMEDY OF CUSTOMER FOR BREACH OF WARRANTY WITH RESPECT TO THE PRODUCT(S).
- (14) products are not fault-tolerant and are not designed or intended for any use requiring fail-safe performance in which the failure of a product could lead to death, serious personal injury, or severe physical and environmental damages (collectively, "High Risk Activities"), such as the operation of nuclear facilities, aircraft navigation or communication systems, air traffic control, weapons systems and/or direct life-support machines. ADVANTEST EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS FOR HIGH RISK ACTIVITIES.

8.2 Chargeable Maintenance Service

Advantest provides chargeable maintenance services during and after the warranty period.

For details, please contact Advantest.

8.3 Maintenance Period

Maintenance services are provided for up to 10 years after the end-of life (EOL) declaration for the system. However, customers need to sign off a maintenance agreement after a lapse of 5 years of the EOL.

8.4 Preventive Maintenance

Some of the components and parts of products have a limited operating life. A regular preventive maintenance program is the best method to maintain trouble-free operation.

Advantest has the support resources for the user to execute the necessary preventive maintenance work.

Periodic parts replacement is required for some electronic and mechanical parts such as fan motors and unit power supply in products. The operating life may vary depending on various factors such as operating condition and environment. For more information, contact the nearest Advantest office.

If any trouble occurs owing to a part whose specified life has expired, performance warranty and repair may be unavailable.

8.5 Export Control

Customer who exports, re-exports, transfers or imports products, technology or technical data purchased hereunder, assumes responsibility for complying with applicable U.S. and other laws and regulations, and for obtaining required export and import authorizations. Customer shall comply with U.S. and other laws and regulations prohibiting transfers, exports and re-exports to certain end-users and destinations or for certain end-uses, unless written authorization is obtained from the appropriate government. Advantest may suspend performance if Advantest believes that customer is in violation or threatened violation of applicable laws or regulations. As part of Advantest's export compliance program, customer may be required to provide end use, end user statements as well as trade compliance statements and export policy statements regarding the products purchased by or licensed to customer.

8.6 Intellectual Property Claims

- (1) Advantest shall defend or settle any claim against customer for IP Losses provided that customer promptly notifies Advantest in writing, and cooperates with and provides full control of the defense or settlement to Advantest, to the extent legally permissible. For the purpose of these terms, "IP Losses" means defense costs, settlement amounts and court-awarded damages arising from any claim against customer that products (excluding custom products) delivered under these terms infringe an intellectual property right in the country where the products are used or sold to customer under these terms (an "IP Claim").
- (2) If an IP Claim is asserted or appears likely, Advantest may, at its option, modify the allegedly infringing product, procure any necessary license, or replace the product with a non-infringing substitute or, if Advantest determines that none of these alternatives is reasonably available, repurchase the product at customer's purchase price less depreciation (based on a five-year straight-line depreciation).
- (3) Advantest has no obligation to indemnify customer against IP Losses arising from:
 - (3-1) Advantest's compliance with, or use of, customer's designs, specifications, instructions or technical information;
 - (3-2) Product modifications by customer or a third party;
 - (3-3) Product use prohibited by specifications or related application notes; or
 - (3-4) Use of the product with products not supplied by Advantest.
- (4) These terms state Advantest's entire liability for claims of intellectual property infringement.

8.7 LIMITATION OF LIABILITY AND REMEDIES

- (1) ADVANTEST, ITS AFFILIATES, SUBCONTRACTORS AND SUPPLIERS SHALL NOT HAVE ANY LIABILITY TO CUSTOMER OR ANY THIRD PARTY FOR ANY INDIRECT, INCIDENTAL, SPECIAL, CONSEQUENTIAL OR PUNITIVE DAMAGES, INCLUDING, WITHOUT LIMITATION, DOWNTIME COSTS, LOSS OF DATA, COSTS OF PROCUREMENT OF SUBSTITUTE PRODUCTS BY CUSTOMER, RESTORATION COST, LOSS OF ANTICIPATED PROFITS OR REVENUES, IN ANY AND ALL CIRCUMSTANCES, EVEN IF ADVANTEST HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES AND WHETHER ARISING OUT OF BREACH OF CONTRACT, WARRANTY, TORT (INCLUDING, WITHOUT LIMITATION, NEGLIGENCE), STRICT LIABILITY, INDEMNITY, CONTRIBUTION OR OTHERWISE AND EVEN IF ANY OF THE LIMITED REMEDIES IN THESE TERMS FAIL OF THEIR ESSENTIAL PURPOSE.
- (2) TO THE EXTENT THAT LIMITATION OF LIABILITY IS PERMITTED BY LAW, ADVANTEST'S CUMULATIVE LIABILITY UNDER THESE TERMS FOR ALL CAUSES OF ACTION, WHETHER ASSERTED AS A TORT CLAIM OR CONTRACT CLAIM, SHALL NOT EXCEED THE LESSER OF (I) THE AMOUNT PAID BY CUSTOMER FOR THE PRODUCT(S) OR SERVICE(S) GIVING RISE TO THE LIABILITY, OR (II) US\$3,000,000.00, EXCEPT THAT ADVANTEST'S OBLIGATION TO MAKE WARRANTY REFUNDS IS LIMITED TO THE PRODUCT PURCHASE PRICE. THE LIMITATIONS SET FORTH IN THIS LIMITATION OF LIABILITY AND REMEDIES SECTION SHALL NOT APPLY TO DAMAGES FOR BODILY INJURY OR DEATH.
- (3) THE REMEDIES IN THESE TERMS ARE CUSTOMER'S SOLE AND EXCLUSIVE REMEDIES.

9. Test System Specifications

This chapter describes the system specifications which are valid when the system power supply is turned on and the automatic calibration is executed 30 minutes after startup of system software.

9.1 System Specifications

- (1) Computing system

Table 9-1 System Controller Specifications

Function	Specification
OS	Linux
CPU	Xeon E3-1225v2 3.2 GHz
Memory	4 GB
I/O	Primary Ethernet:10/100/1000Mbps × 1 Secondary Ethernet:10/100/1000Mbps × 1 GPIB × 1
Hard disk drive	1 TB
Optical drive	Compatible format: DVD-R, DVD-RW, DVD-ROM, CD-R, CD-RW, CD-ROM
Graphic monitor	19-inch LCD monitor with 1280 × 1024 pixel resolution
Keyboard	104 English, connector: PS/2
Mouse	Mouse with a scroll wheel, connector: USB

Table 9-2 Satellite Processor Specifications

Function	Specification
OS	Linux
CPU	Atom Z530 1.6 GHz
Memory	1 GB
I/O	Ethernet: 10/100/1000Mbps × 1 Tester control bus: 100 MB/s data rate

Table 9-3 Module Processor Specifications

Function	Specification
OS	Linux
CPU	1.2 GHz dual core
Memory	4 GB
I/O	Ethernet: 10/100/1000base-TX × 1 Tester control bus: 100 MB/s data rate

Table 9-4 Test Function Configuration

Configuration		Quantity	Condition
ALPG	X address	24 bits	
	Y address	24 bits	
	Instruction memory	4 kilowords	
Timing generator	BCLK	1 edge/pin	128 at maximum
	CCLK	1 edge/pin	128 at maximum
	DRECLK	1 edge/pin	Maximum DREL: 128, DRET: 128
	STRB	2 edges/pin	128 at maximum
	Timing set	16	
FM	Total memory capacity	384 Gb	32-site
DC test unit		384 ch	32-site
PPS		PPS : 1152 ch	32-site, for three branches in a module
HVLVDR		HVLVDR : 1728 ch	32-site + 6-HVLVDR configuration with six branches in a module, or 32-site + 12-HVLVDR configuration with three branches in a module
Driver output voltage VIH, VIL		On a pin basis	
Comparator comparison voltage VOH		On a pin basis	
Termination voltage VT		On a pin basis	
Handler and prober GPIB interface		1	

Table 9-5 Test Station Configuration

Test station configuration	Quantity
Test head cabinet	1

Table 9-6 Test Station Channel Configuration (T5830P)

Site Configuration	I/O	DC	PPS	HVLVDR
32 Site + 4 HVLVDR	4608 ch	384 ch	1152 ch	1152 ch
32 Site + 6 HVLVDR	4608 ch	384 ch	1152 ch	1728 ch
32 Site + 12 HVLVDR	4608 ch	384 ch	1152 ch	1728 ch

Table 9-7 Test Station Channel Configuration (T5830PES)

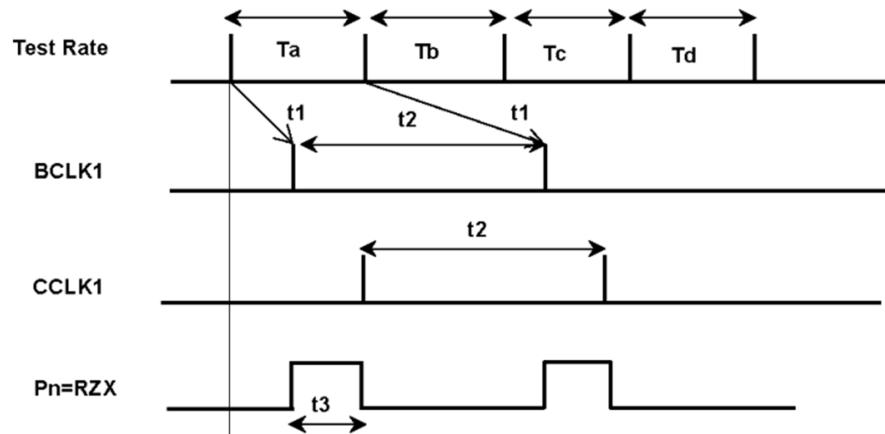
Site Configuration	I/O	DC	PPS	HVLVDR
2 Site + 1 HVLVDR	288 ch	24 ch	48 ch	32 ch

9.2 Timing Generator

9.2.1 Timing Edge

Table 9-8 Timing Edge Specifications

Item		Item
Base test rate (BASE RATE)		6.667 ns/7.5 ns/8 ns/8.889 ns/9.630 ns
Test rate		$10 \mu s \geq T \geq \text{BASE RATE} (1\text{way})$
Test rate resolution		BASE RATE/8
Timing edge	BCLK CCLK DRECLK STRB	$2 \mu s \geq t_1 \geq 0 \text{ ns}$ and $T - \text{BASE RATE}/8 \geq t_1$ $t_2 \geq \text{BASE RATE} (1\text{way})$ $t_3 \geq \text{BASE RATE}/4$
Timing edge setting resolution		BASE RATE/8



Note: Timings cannot be selected on-the-fly between different base test rates.

9.3 Driver Specifications

9.3.1 Normal Driver Specifications

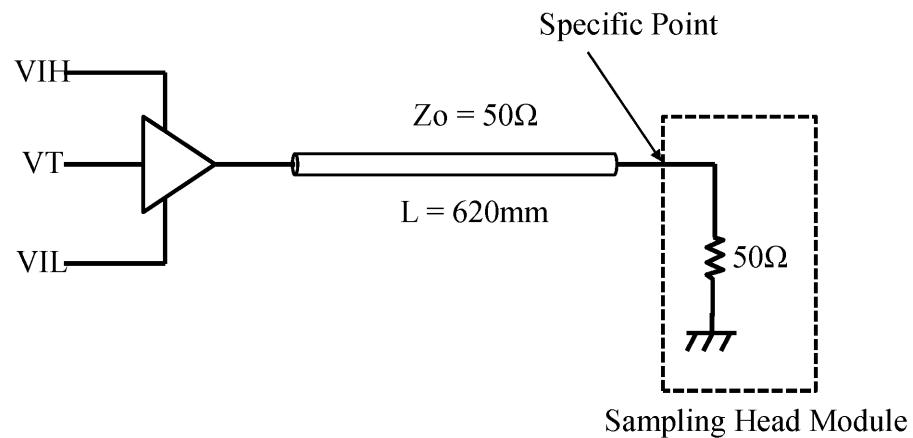
Table 9-9 Normal Driver Specifications

Item	Specification
Output level	VIH: -0.5 V to +6.0 V VIL: -1.0 V to +5.65 V
Output amplitude	0.35 Vp-p to 6.75 Vp-p
Output voltage setting resolution	1 mV
DC accuracy	$\pm(1\% + 20 \text{ mV})$
Rise and fall time	400 ps (20% to 80%) (VIH = 1.0 V, VIL = 0 V)
Minimum pulse width	3.33 ns (VIH = 1.0 V, VIL = 0 V)
Driver skew	360 ps p-p
Output impedance	$50 \pm 5 \Omega$
Maximum output current	$\pm 30 \text{ mA}$
I/O switching accuracy	$\pm 1.2 \text{ ns}$
Minimum ON and OFF time when using I/O	6.2 ns
Minimum Driver to VT pulse width (DRET)	5000 ps $\pm 500 \text{ ps}$
Minimum VT to Driver pulse width (DREL)	3500 ps $\pm 500 \text{ ps}$

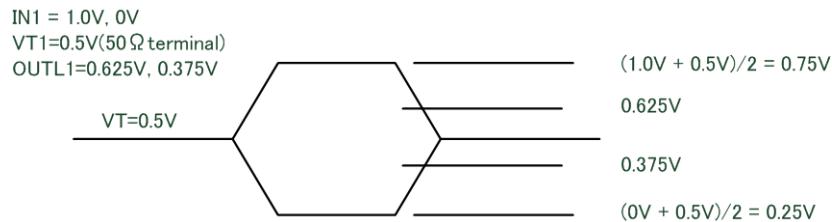
(1) Specified driver AC characteristic conditions

The AC characteristics measurement is specified when a data acquisition mother board and data acquisition socket board are used.

Measurement based on the criteria is formed when a sampling head module with a bandwidth of 6 GHz or more is used.



- (2) I/O switching accuracy and minimum DR on/off time specified conditions



9.3.2 High-Voltage Driver Specifications

Table 9-10 High-Voltage Driver Specifications

Item	Specification
Output level	VHH: 0 V to +13 V
Output amplitude	0 Vp-p to 13 Vp-p
Output voltage setting resolution	2 mV
DC accuracy	$\pm(2.0\% + 50 \text{ mV})$
Rise and fall time	160 ns (20% to 80%)
Output impedance	$\leq 100 \Omega$
Maximum output current	$\pm 2.5 \text{ mA} (\text{VHH} \leq 13 \text{ V})$ $\pm 10 \text{ mA} (\text{VHH} \leq 12 \text{ V})$

9.4 Comparator Specifications

9.4.1 Comparator Specifications

Table 9-11 Comparator Specifications

Item	Specification
Equivalent rise time	$\leq 400 \text{ ps} / 1.0 \text{ V}$ (20% to 80%)
Comparator skew	360 ps p-p
Input voltage range	-1.0 V to 6.00 V
Comparator voltage range	-1.0 V to 6.00 V
Reference voltage accuracy	$\pm(1\% + 25 \text{ mV})$
Comparison voltage setting resolution	1 mV

Note: If the I/O mode is used, output comparison cannot be performed during the trailing edge of the DUT output comparison cycle ($2.5 \text{ ns} + 2 \times T_c$) when a DUT output comparison cycle is switched to a pattern-applied cycle. T_c is the propagation delay time from the PE board edge to the measurement device.

9.4.2 Terminator Specifications

Table 9-12 Terminator Specifications

Item	Specification
Output level	VTT: -0.75 V to 5.75 V
Output voltage setting resolution	1 mV
DC accuracy	$\pm(1\% + 20 \text{ mV})$
Output impedance	$50 \pm 5 \Omega$
Maximum output current	$\pm 30 \text{ mA}$

9.4.3 Passive Load Specifications

Table 9-13 Passive Load Specifications

Item	Specification
Output current level	$\pm 14 \text{ mA}$ (0.5 k Ω) $\pm 7 \text{ mA}$ (1.0 k Ω) $\pm 1 \text{ mA}$ (8.0 k Ω)
Load resistance range	0.5 k Ω / 1.0 k Ω / 8.0 k Ω
Load resistance accuracy	$\pm 75 \Omega$ (0.5 k Ω) $\pm 150 \Omega$ (1.0 k Ω) $\pm 1200 \Omega$ (8.0 k Ω)
Output voltage level	VCOM: -1.0 V to 6.0 V
Output setting resolution	1 mV
DC accuracy	$\pm(1\% + 225 \text{ mV})$

9.5 DC Parametric Test Unit Specifications

9.5.1 Voltage Source Current Measurement (VSIM)

- (1) Programmable voltage (Note)

Table 9-14 Programmable Voltages (VSIM)

Voltage setting range	Output voltage range	Resolution	Program accuracy (10% to 100% of full scale)	Maximum current ^{*1}
20 V	-1.0 V to +13.0 V	2 mV	$\pm(0.2\%+10 \text{ mV}+20 \text{ mV}/10 \text{ mA})$	$\pm20 \text{ mA}$

***1:** The maximum current is limited by the current measurement range and the current limit value.

Note: This is the output value specified on a performance board.

- (2) Current measurement

Table 9-15 Current Measurement (VSIM)

Current measurement range	Setting voltage value	Measurement range	Resolution	Measurement accuracy (10% to 100% of full scale)
8 μ A	$-1 \text{ V} \leq \text{VS} \leq +13 \text{ V}$	-5 μ A to +5 μ A	1 nA	$\pm(0.5\% + 30 \text{ nA} + 2 \text{ nA/V})$
80 μ A		-20 μ A to +20 μ A	4 nA	$\pm(0.5\% + 60 \text{ nA} + 10 \text{ nA/V})$
800 μ A		-200 μ A to +200 μ A	40 nA	$\pm(0.5\% + 400 \text{ nA} + 100 \text{ nA/V})$
8 mA		-2 mA to +2 mA	400 nA	$\pm(0.5\% + 4 \text{ } \mu\text{A} + 1 \text{ } \mu\text{A/V})$
80 mA	-1 V \leq VS $<$ 0 V	-10 mA to +10 mA	20 μ A	$\pm(0.5\% + 120 \text{ } \mu\text{A} + 40 \text{ } \mu\text{A/V})$
	0 V \leq VS \leq +9 V	-20 mA to +20 mA		
	+9 V $<$ VS \leq +12.5 V	-5 mA to +5 mA		
	+12.5 V $<$ VS \leq +13 V	-2.5 mA to +2.5 mA		

(3) Current limitation (for positive and negative values)

Table 9-16 Current Limitation (VSIM)

Current setting range	Setting voltage value	Setting range		Setting resolution	Current limit accuracy	
8 µA	$-1 \text{ V} \leq \text{VS} \leq +13 \text{ V}$	Positive	Fixed at $+5 \mu\text{A}$ ^{*1}	-	Positive	$+(2.4 \mu\text{A} \text{ to } 0 \text{ A})$
		Negative	Fixed at $-5 \mu\text{A}$ ^{*1}		Negative	$-(2.4 \mu\text{A} \text{ to } 0 \text{ A})$
		Positive	Fixed at $+20 \mu\text{A}$ ^{*1}	-	Positive	$+10 \mu\text{A} \text{ to } 0 \text{ A}$
		Negative	Fixed at $-20 \mu\text{A}$ ^{*1}		Negative	$-10 \mu\text{A} \text{ to } 0 \text{ A}$
		Positive	Fixed at $+200 \mu\text{A}$ ^{*1}	-	Positive	$+100 \mu\text{A} \text{ to } 0 \text{ A}$
		Negative	Fixed at $-200 \mu\text{A}$ ^{*1}		Negative	$-100 \mu\text{A} \text{ to } 0 \text{ A}$
		Positive	$+200 \mu\text{A} \text{ to } +2 \text{ mA}$	8 µA	Positive	$+(20\% + 700 \mu\text{A}) \text{ to } 0 \text{ A}$
		Negative	$-200 \mu\text{A} \text{ to } -2 \text{ mA}$		Negative	$-(20\% + 700 \mu\text{A}) \text{ to } 0 \text{ A}$
80 mA	$-1 \text{ V} \leq \text{VS} < 0 \text{ V}$	Positive	$+2.0 \text{ mA} \text{ to } +10 \text{ mA}$	250 µA	Positive	$+(20\% + 5 \text{ mA}) \text{ to } 0 \text{ A}$
		Negative	$-2.0 \text{ mA} \text{ to } -10 \text{ mA}$		Negative	$-(20\% + 5 \text{ mA}) \text{ to } 0 \text{ A}$
	$0 \text{ V} \leq \text{VS} \leq +9 \text{ V}$	Positive	$+2.0 \text{ mA} \text{ to } +20 \text{ mA}$		Positive	$+(20\% + 5 \text{ mA}) \text{ to } 0 \text{ A}$
		Negative	$-2.0 \text{ mA} \text{ to } -20 \text{ mA}$		Negative	$-(20\% + 5 \text{ mA}) \text{ to } 0 \text{ A}$
	$+9 \text{ V} < \text{VS} \leq +12.5 \text{ V}$	Positive	$+2.0 \text{ mA} \text{ to } +5 \text{ mA}$	250 µA	Positive	$+(20\% + 5 \text{ mA}) \text{ to } 0 \text{ A}$
		Negative	$-2.0 \text{ mA} \text{ to } -5 \text{ mA}$		Negative	$-(20\% + 5 \text{ mA}) \text{ to } 0 \text{ A}$
	$+12.5 \text{ V} < \text{VS} \leq +13 \text{ V}$	Positive	$+2.0 \text{ mA} \text{ to } +2.5 \text{ mA}$		Positive	$+(20\% + 5 \text{ mA}) \text{ to } 0 \text{ A}$
		Negative	$-2.0 \text{ mA} \text{ to } -2.5 \text{ mA}$		Negative	$-(20\% + 5 \text{ mA}) \text{ to } 0 \text{ A}$

**1: Program setting unavailable*

(4) Output short-circuit/open characteristics

Table 9-17 Output Short-Circuit/Open Characteristics (VSIM)

Current measurement range	Peak voltage	Recovery time
8 µA to 80 mA	3 V	2 ms or less

Note: The recovery time is the time required to reach the setting value $\pm 10\%$ when short-circuit and open are repeated at 10 ms intervals with no load other than the short-circuit load.

(5) VSIM settling time

Table 9-18 VSIM Settling Time

Current measurement range	Difference between measured and final values		
	1% or less of full scale	0.1% or less of full scale	1% or less of 1/10 of full scale
8 µA	10 ms	15 ms	15 ms
80 µA	3 ms	4 ms	4 ms
800 µA	0.7 ms	0.8 ms	0.8 ms
8 mA	0.5 ms	0.6 ms	0.6 ms
80 mA	0.5 ms	0.6 ms	0.6 ms

Load condition: resistance + capacitance (100 pF)

9.5.2 Current Source Voltage Measurement (ISVM)

(1) Programmable current (Note)

Table 9-19 Programmable Current (ISVM)

Current setting range	Output current range	Resolution	Maximum output voltage *1	Output impedance on reference off
80 μ A	-20 μ A to +20 μ A	2.5 nA	-1.0 V to +13.0 V	191 k Ω ±10%
800 μ A	-200 μ A to +200 μ A	25 nA		
8 mA	-2 mA to +2 mA	250 nA		
80 mA	-10 mA to +10 mA	10 μ A	-1.0 V to +0.0 V	9.5 k Ω ±10%
	-20 mA to +20 mA		0.0 V to +9.0 V	
	-5 mA to +5 mA		+9.0 V to +12.5 V	
	-2.5 mA to +2.5 mA		+12.5 V to +13.0 V	

Current setting range	Program accuracy (10% to 100% of full scale)
80 μ A	±(0.5% + 120 nA + 100 nA/V)
800 μ A	±(0.5% + 1 μ A + 1 μ A/V)
8 mA	±(0.5% + 10 μ A + 10 μ A/V)
80 mA	±(0.5% + 200 μ A + 200 μ A/V)

*1 : The maximum output voltage is limited by the voltage measurement range and voltage limit value.

Note: This is the output value specified on a performance board.

(2) Voltage measurement

Table 9-20 Voltage Measurement (ISVM)

Voltage measurement range	Measurement range	Resolution	Measurement accuracy
+20 V	-0.3 V to +13.0 V	2 mV	±(0.2%+6 mV+20 mV/10 mA)
-20 V	-1.0 V to +0.3 V		

(3) Voltage limitation

Table 9-21 Voltage Limitation (ISVM)

Voltage measurement range	Current measurement range	Current setting value	Setting range		Resolution	Setting accuracy
+20 V	80 µA 800 µA 8 mA	-20 µA ≤ IS ≤ +20 µA	Positive	+0.6 V to +13.2 V	0.2 V	±0.2 V
		-200 µA ≤ IS ≤ +200 µA	Negative	Fixed at -0.6 V		
		-2 mA ≤ IS ≤ +2 mA	Positive	+0.6 V to +9.2 V		
	80 mA	-20 mA ≤ IS < -5 mA	Negative	Fixed at -0.6 V		
		+5 mA < IS ≤ +20 mA	Positive	+0.6 V to +12.8 V		
		-5 mA ≤ IS < -2.5 mA	Negative	Fixed at -0.6 V		
		+2.5 mA < IS ≤ +5 mA	Positive	+0.6 V to +13.2 V		
		-2.5 mA ≤ IS ≤ +2.5 mA	Negative	Fixed at -0.6 V		
-20 V	80 µA 800 µA 8 mA	-20 µA ≤ IS ≤ +20 µA	Positive	Fixed at +0.6 V	0.2 V	±0.2 V
		-200 µA ≤ IS ≤ +200 µA	Negative	-1.2 V to -0.6 V		
		-2 mA ≤ IS ≤ +2 mA	Positive	Fixed at +0.6 V		
	80 mA	-10 mA ≤ IS ≤ +10 mA	Negative	-1.2 V to -0.6 V		

(4) ISVM settling time

Table 9-22 ISVM Settling Time

Source current range	Setting value	Voltage measurement		
		0.8 V	8.0 V	
		1%	1%	0.1%
80 µA	2 µA	15.0 ms	20.0 ms	30.0 ms
	20 µA	2.0 ms	4.0 ms	7.0 ms
800 µA	20 µA	3.0 ms	5.0 ms	10.0 ms
	200 µA	0.5 ms	0.5 ms	1.0 ms
8 mA	0.2 mA	0.5 ms	3.0 ms	5.0 ms
	2 mA	0.5 ms	0.5 ms	0.5 ms
80 mA	2.0 mA	0.5 ms	5.0 ms	8.0 ms
	20 mA	0.5 ms	0.5 ms	0.7 ms

Load condition: resistance + capacitance (100 pF)

Time to reach 0.1% and 1% of the final value

The settling time for 0.1% when the measured voltage is 0.8 V is not described because it is below the measurement voltage resolution.

9.5.3 Maximum Load Capacitance (VSIM and ISVM)

Table 9-23 Maximum Load Capacitance (VSIM and ISVM)

Current range	Maximum load capacitance
8 µA	1000 pF
80 µA	
800 µA	
8 mA	
80 mA	

The maximum load capacitance guarantees 10% of the setting value of overshoot and undershoot (or 0.5 V, whichever is greater) due to reference on or off, when a capacitive load is connected.

9.6 Device Power Supply Specifications

9.6.1 Voltage Source Current Measurement (VS)

(1) Programmable voltage

Table 9-24 Programmable Voltage (VS)

Voltage setting range	Output voltage range	Setting resolution	Program accuracy *1	Maximum output current *2
2 V	0.0 V to +2.2 V	1 mV	$\pm(0.1\% + 6 \text{ mV})$	-200 mA to 1200 mA
3 V	0.0 V to +3.3 V			-200 mA to 1200 mA
4 V	0.0 V to +4.0 V			-200 mA to 1000 mA
16 V	-1.0 V to +13.0 V		$\pm(0.1\% + 16 \text{ mV})$	-200 mA to 400 mA

*1: Applied when the output current is within the measurement range.

*2: Limited by the current range and the current limit value.

Table 9-25 Programmable Voltage (3-Branch)

Voltage setting range	Output voltage range	Setting resolution	Program accuracy	Maximum output current *3
2 V	0.0 V to +2.2 V	1 mV	$\pm(0.1\% + 6 \text{ mV} + 0.5 \text{ mV}/\sum 10 \text{ mA}^{*1}$ $+4 \text{ mV}/\Delta 10 \text{ mA}^{*2})$	-200 mA to 1200 mA
3 V	0.0 V to +3.3 V			-200 mA to 1200 mA
4 V	0.0 V to +4.0 V			-200 mA to 1000 mA
16 V	-1.0 V to +13.0 V		$\pm(0.1\% + 16 \text{ mV} + 0.5 \text{ mV}/\sum 10 \text{ mA}^{*1}$ $+4 \text{ mV}/\Delta 10 \text{ mA}^{*2})$	-200 mA to 400 mA

*1: Error generated in proportion to the sum of branch destination current

*2: Error generated in proportion to the difference of branch destination current

*3: Total current of branch output values. The maximum output current is limited by the current measurement range and the current limit value.

(2) Current limitation (positive and negative current can be independently set)

Table 9-26 Current Limitation (VS)

Current measurement range	Voltage setting range	Setting voltage value	Setting range ^{*1}		Setting resolution	Current limit accuracy	
40 μA	2 V, 3 V, 4 V, 16 V	±FSR	Positive	+(5 μA to 25 μA)	25 nA	+(0 to 20%FS) (-0 to 20%FS)	
			Negative	-(5 μA to 25 μA)			
			Positive	+(50 μA to 250 μA)	0.25 μA		
			Negative	-(50 μA to 250 μA)			
			Positive	+(0.5 mA to 2.5 mA)	2.5 μA		
			Negative	-(0.5 mA to 2.5 mA)			
			Positive	+(5 mA to 25 mA)	25 μA		
			Negative	-(5 mA to 25 mA)			
400 mA	2 V, 3 V, 4 V	±FSR	Positive	+(100 mA to 400 mA)	0.5 mA		
			Negative	-(100 mA to 200 mA)			
	16 V	+8.000 V to +13.000 V	Positive	+(100 mA to 400 mA)	0.5 mA		
			Negative	-(100 mA to 200 mA)			
		+0.000 V to + 7.999 V	Positive	+(100 mA to VS*25 mA+200 mA)			
			Negative	-(100 mA to 200 mA)			
		-1.000 V to 0.000 V	Positive	+(100 mA to 200 mA)			
			Negative	-(100 mA to 200 mA)			
8 A	2 V	+0.700 V to +2.200 V	Positive	+(200 mA to 1200 mA)	1.0 mA	+(0 to 20%FS) (-0 to 20%FS)	
			Negative	Fixed at -200 mA			
		+0.000 V to +0.699 V	Positive	+(200 mA to VS*500 mA+850 mA)			
			Negative	Fixed at -200 mA			
	3 V	+2.000 V to +3.300 V	Positive	+(200 mA to 1200 mA)			
			Negative	Fixed at -200 mA			
		+0.000 V to +1.999 V	Positive	+(200 mA to VS*400 mA+400 mA)			
			Negative	Fixed at -200 mA			
	4 V	+2.600 V to +4.000 V	Positive	+(200 mA ~ 1000 mA)			
			Negative	Fixed at -200 mA			
		+0.000 V to +2.599 V	Positive	+(200 mA to VS*300 mA+220 mA)			
			Negative	Fixed at -200 mA			
	16 V		Unusable				

***1:** In the 8A range, the setting range for current limitation is limited according to the programmable voltage setting value (VS).

(3) Current measurement

Table 9-27 Current Measurement (VS)

Current measurement range	Measurement range	Measurement resolution	Measurement accuracy	Maximum output current
40 μ A	-25 μ A to +25 μ A	12.5 nA	$\pm(0.5\% + 100 \text{ nA} + 10 \text{ nA/V})$	$\pm 25 \mu\text{A}$
400 μ A	-250 μ A to +250 μ A	125 nA	$\pm(0.5\% + 1 \mu\text{A} + 100 \text{ nA/V})$	$\pm 250 \mu\text{A}$
4 mA	-2.5 mA to +2.5 mA	1.25 μ A	$\pm(0.5\% + 10 \mu\text{A} + 1 \mu\text{A/V})$	$\pm 2.5 \text{ mA}$
40 mA	-25 mA to +25 mA	12.5 μ A	$\pm(0.5\% + 100 \mu\text{A} + 10 \mu\text{A/V})$	$\pm 25 \text{ mA}$
400 mA	-200 mA to +400 mA	250 μ A	$\pm(0.5\% + 2.4 \text{ mA} + 100 \mu\text{A/V})$	-200 mA / 400 mA ^{*1}
8 A	-200 mA to +1200 mA	500 μ A	$\pm(0.5\% + 4.8 \text{ mA} + 200 \mu\text{A/V})$	-200 mA / 1200 mA ^{*1}

**1: Limited by the voltage setting range and the current limit value.*

(4) Maximum load capacitance

Table 9-28 Maximum Load Capacitance (VS)

Current measurement range	Compensation capacitor setting				
	C(0) (Not specified)	C(1)	C(2)	C(3)	C(4)
40 μ A	0 to 0.22 μ F	0.22 to 10 μ F		10 μ F to 100 μ F	
400 μ A	0 to 0.22 μ F	0.22 to 10 μ F		10 μ F to 100 μ F	
4 mA	0 to 0.22 μ F	0.22 to 10 μ F		10 μ F to 100 μ F	
40 mA	0 to 0.22 μ F	0.22 to 10 μ F		10 μ F to 100 μ F	
400 mA	0 to 0.22 μ F	0.22 to 10 μ F		10 μ F to 100 μ F	
8 A	0 to 0.22 μ F	0.22 to 10 μ F		10 μ F to 100 μ F	

The maximum load capacitance guarantees 10% of the setting value of overshoot and undershoot (or 0.5 V, whichever is greater) due to reference on or off, when a capacitive load is connected.

Use it with the compensation capacitor setting suitable for the load capacitance.

When branch output is used, the total load capacitance of all branch destinations is used as the maximum load capacitance.

(5) Slew rate

Table 9-29 Slew Rate (VS)

Setting range	Setting resolution	Program accuracy ^{*1}
50 μ s/V ^{*2} to 15000 μ s/V	10 μ s/V	$\pm 20\%$

**1: Affected by the setting current range, current limit setting value, and load capacitance.*

**2: The minimum setting value for an operation to reduce the voltage (reference on for negative voltage or reference off) is limited to 250 μ s/V.*

(6) VSIM settling time

Table 9-30 VSIM Settling Time

Current measurement range	Time for the difference between the measured value and final value to be 1% (or a 20 count, whichever is greater)				Condition	
	Load capacitance (compensation capacitor setting)					
	No load (C0)	0.22 µF (C0)	10 µF (C1)	100 µF (C2)	Voltage setting value	Current limit setting value
40 µA	10 ms	25 ms	-	-	2 V	+/- 25 µA
400 µA	2 ms	4 ms	-	-		+/-250 µA
4 mA	1 ms	2 ms	12 ms	-		+/-2.5 mA
40 mA	1 ms	1 ms	2 ms	12 ms		+/- 25 mA
400 mA	1 ms	1 ms	1 ms	3 ms		+/-100 mA
8 A	1 ms	1 ms	1 ms	2 ms		+/-200 mA

Specified by the time until the measured current value reaches 1% or less of the accuracy after reference on.

The settling time for the voltage source (VS) is included.

9.6.2 Voltage Source Current Measurement (Parallel Connection)

The variable n in each table represents the number of channels in the parallel connection.

Up to four channels can be connected in parallel. Note, however, that there are limits on the combination of channels.

For more information, see [Table 9-38](#).

In addition, parallel connection and branching cannot be specified at the same time for the same channel.

(1) Programmable voltage (parallel connection)

Table 9-31 Programmable Voltage (Parallel Connection)

Voltage setting range	Output voltage range	Setting resolution	Program accuracy	Maximum output current
2 V	0.0 V to +2.2 V	1 mV	±(0.1% + 6 mV)	-n × 200 mA to +n × 1200 mA
3 V	0.0 V to +3.3 V			-n × 200 mA to +n × 1200 mA
4 V	0.0 V to +4.0 V			-n × 200 mA to +n × 1000 mA
16 V	-1.0 V to +13.0 V		±(0.1% +16 mV)	-n × 200 mA to +n × 400 mA

(2) Current limitation (positive and negative current can be set individually) (parallel connection)

Table 9-32 Current Limitation (Parallel Connection)

Current measurement range	Voltage setting range	Setting range	Setting range		Setting resolution	Current limit accuracy
40 µA to 40 mA			Unusable			
400 mA	2 V, 3 V, 4 V	±FSR	Positive	Fixed at +(n × 400 mA)	-	+(0 to 20%FS) -(0 to 20%FS)
			Negative	Fixed at -(n × 200 mA)	-	
	16 V	+8.000 V to +13.000 V	Positive	Fixed at +(n × 400 mA)	-	
			Negative	Fixed at -(n × 200 mA)	-	
		+0.000 V to +7.999 V	Positive	Fixed at +n × (VS*25 mA + 200 mA) ^{*1}	-	
			Negative	Fixed at -(n × 200 mA)	-	
		-1.0000 V to 0.000 V	Positive	Fixed at +(n × 200 mA)	-	
			Negative	Fixed at -(n × 200 mA)	-	
8 A	2 V	+0.700 V to +2.200 V	Positive	Fixed at +(n × 1200 mA)	-	+(0 to 20%FS) -(0 to 20%FS)
			Negative	Fixed at -(n × 200 mA)	-	
		+0.000 V to +0.699 V	Positive	Fixed at +n × (VS*500 mA + 850 mA) ^{*1}	-	
			Negative	Fixed at -(n × 200 mA)	-	
	3 V	+2.000 V to +3.300 V	Positive	Fixed at +(n × 1200 mA)	-	
			Negative	Fixed at -(n × 200 mA)	-	
		+0.000 V to +1.999 V	Positive	Fixed at +n × (VS*400 mA + 400 mA) ^{*1}	-	
			Negative	Fixed at -(n × 200 mA)	-	
	4 V	+2.600 V to +4.000 V	Positive	Fixed at +(n × 1000 mA)	-	
			Negative	Fixed at -(n × 200 mA)	-	
		+0.000 V to +2.599 V	Positive	Fixed at +n × (VS*300 mA + 220 mA) ^{*1}	-	
			Negative	Fixed at -(n × 200 mA)	-	

**1: Determined according to the programmable voltage setting value (VS).*

(3) Current measurement (parallel connection)

Table 9-33 Current Measurement (Parallel Connection)

Current measurement range	Measurement range	Measurement resolution	Measurement accuracy	Maximum output current
40 µA to 40 mA	Unusable			
400 mA	n × (-200 mA to +400 mA)	250 µA	±(0.5% + n × 2.4 mA + n × 100 µA/V)	n × 400 mA
8 A	n × (-200 mA to +1200 mA)	500 µA	±(0.5% + n × 4.8 mA + n × 200 µA/V)	n × 1200 mA

(4) Maximum load capacitance (parallel connection)

Table 9-34 Maximum Load Capacitance (Parallel Connection)

Current measurement range	Compensation capacitor setting				
	C(0) (Not specified)	C(1)	C(2)	C(3)	C(4)
40 uA to 40 mA	Unusable				
400 mA	$n \times (0 \text{ to } 0.22 \mu\text{F})$	$n \times (0.22 \text{ to } 10 \mu\text{F})$		$n \times (10 \mu\text{F} \text{ to } 100 \mu\text{F})$	
8 A	$n \times (0 \text{ to } 0.22 \mu\text{F})$	$n \times (0.22 \text{ to } 10 \mu\text{F})$		$n \times (10 \mu\text{F} \text{ to } 100 \mu\text{F})$	

(5) Slew rate (parallel connection)

Table 9-35 Slew Rate (Parallel Connection)

Setting range	Setting resolution	Program accuracy *1
$50 \mu\text{s/V}^{*2} \text{ to } 15000 \mu\text{s/V}$	$10 \mu\text{s/V}$	$\pm 20\%$

*1: Affected by the setting current range, current limit setting value, and load capacitance.

*2: The minimum setting value for an operation to reduce the voltage (reference on for negative voltage or reference off) is limited to $250 \mu\text{s/V}$.

9.6.3 Average Current Measurement

Sampling rate: 1 ms (fixed)

Maximum number of samples: 2047 times

9.6.4 PCON Capacitance

This product includes an independent PCON for each PPS branch.

Table 9-36 PCON Capacitance

PCON capacitance
$22 \mu\text{F}^{*1}/\text{branch output}$

*1: JIS/EIA Class 2 ceramic capacitor

9.6.5 Limitations when Using Device Power Supply

(1) VS setting limitations

PPS channels having the same No. shown in [Table 9-37](#) cannot be assigned to different voltage setting ranges.

Assign them to the same voltage setting range when using the device power supply.

Table 9-37 List of Channel Groups Having Same Setting (12PPS/Site Configuration)

No	PPS channel No.
1	1-4
2	5-8
3	9-12

(2) Limitations on parallel connection setting

Channels that can be connected in parallel are limited to each combination of up to four parallel connections within a four-consecutive-channel group shown in [Table 9-38](#).

Table 9-38 Combinations of Channels Connectable in Parallel (12PPS/Site Configuration)

Channel	Parallel connections = 2						Parallel connections = 3						Parallel connections = 4			
	Combination 1		Combination 2		Combination 3		Combination 4			Combination 5			Combination 6			
PPS 1-4	1	2	3	4	2	3	1	2	3	2	3	4	1	2	3	4
PPS 5-8	5	6	7	8	6	7	5	6	7	6	7	8	5	6	7	8
PPS 9-12	9	10	11	12	10	11	9	10	11	10	11	12	9	10	11	12

*: Combination 1 and Combination 2 can be specified together.

9.7 HLVDR Specifications

The T5830P HLVDR module (HLVDR) has 48 channels and 6 branches (6 lines) per module.

9.7.1 Voltage Source Current Measurement (VSIM)

- (1) Programmable voltage ^{*1}

Table 9-39 Programmable Voltage (VSIM)

Voltage setting range	Output voltage range ^{*1}	Resolution	Maximum current ^{*2}
8 V	-8 V to +8 V	1 mV	-80 mA to 90 mA
32 V	-10 V to +32 V	2 mV	-80 mA to 90 mA

***1:** This specification is applied for the output value on a performance board.

***2:** The maximum current is limited by the current measurement range and the current limit value. In addition, the maximum current is the sum of current values for branches connecting to a channel.

Table 9-40 Programmable Voltage Accuracy (VSIM)

Voltage setting range	Program accuracy (10% to 100% of full scale) ^{*1}
8 V	$\pm(0.1\%+4 \text{ mV}+7.0 \text{ mV}/10 \text{ mA})$
32 V	$\pm(0.2\%+16 \text{ mV}+7.0 \text{ mV}/10 \text{ mA})$

***1:** This specification is applied when the output current is within the measurement range.

- (2) Current measurement

Table 9-41 Current Measurement (VSIM)

Current measurement range	Measurement range	Resolution	Measurement accuracy (10% to 100% of full scale)
8 μ A	-8 μ A to +8 μ A	0.25 nA	$\pm(0.5\%+56 \text{ nA}+0.5 \text{ nA/V})$
80 μ A	-80 μ A to +80 μ A	2.5 nA	$\pm(0.2\%+90 \text{ nA}+5 \text{ nA/V})$
800 μ A	-800 μ A to +800 μ A	25 nA	$\pm(0.2\%+450 \text{ nA}+50 \text{ nA/V})$
8 mA	-8 mA to +8 mA	0.25 μ A	$\pm(0.2\%+4.05 \text{ } \mu\text{A}+0.5 \text{ } \mu\text{A/V})$
128 mA	-80 mA to +90 mA	5 μ A	$\pm(0.5\%+120 \text{ } \mu\text{A}+10 \text{ } \mu\text{A/V})$

(3) Current limit (for positive and negative values)

Table 9-42 Current Limit (VSIM)

Current measurement range	Voltage setting range	Setting range		Resolution	Current limit accuracy	
8 μ A	-10 V to +32 V	Positive	Fixed at +1 mA ^{*1}	-	Positive	+2 mA to 0 A
		Negative	Fixed at -1 mA ^{*1}		Negative	-2 mA to 0 A
80 μ A	-10 V to +32 V	Positive	Fixed at +1 mA ^{*1}	-	Positive	+2 mA to 0 A
		Negative	Fixed at -1 mA ^{*1}		Negative	-2 mA to 0 A
800 μ A	-10 V to +32 V	Positive	Fixed at +1 mA ^{*1}	-	Positive	+2 mA to 0 A
		Negative	Fixed at -1 mA ^{*1}		Negative	-2 mA to 0 A
8 mA	-10 V to +32 V	Positive	+1 mA to +8 mA	1 mA	Positive	+/(20%+2 mA) to 0 A
		Negative	-1 mA to -8 mA		Negative	-(20%+2 mA) to 0 A
128 mA	-10 V to +32 V	Positive	+1 mA to +90 mA	1 mA	Positive	+/(20%+20 mA) to 0 A
		Negative	-1 mA to -80 mA		Negative	-(20%+20 mA) to 0 A

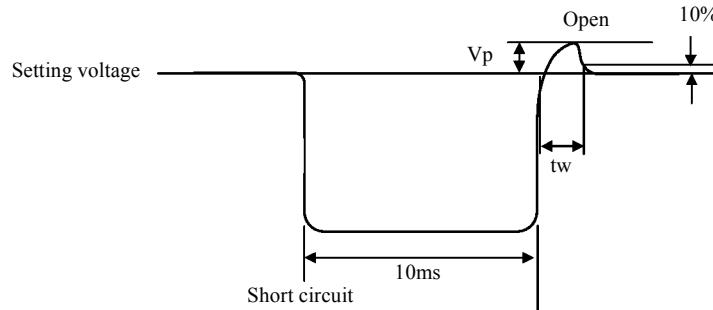
***1:** The maximum current is limited by the current measurement range and the current limit value.
In addition, the maximum current is the sum of current values for branches connecting to a channel.

(4) Output short-circuit and open characteristics (VSIM)

Table 9-43 Output Short-Circuit and Open Characteristics (VSIM)

Current measurement range	Peak voltage (Vp)	Recovery time (tw) ^{*1}
8 μ A to 128 mA	3 V	2 ms or less

***1:** The recovery time is the time required to reach the setting value $\pm 10\%$ when short-circuit and open are repeated at 10 ms intervals with no load other than the short-circuit load.

**Figure 9-1 Output Short-Circuit and Open Characteristics when VSIM Is Set**

(5) VSIM settling time

Table 9-44 VSIM Settling Time

Voltage setting range	Current measurement range	Difference between measured and final values		
		1% or less of full scale	0.1% or less of full scale	1% or less of 1/10 full scale
$\pm 8 \text{ V}/\pm 32 \text{ V}$	8 μA	5.0 ms	10.0 ms	10.0 ms
	80 μA	0.4 ms	0.5 ms	0.5 ms
	800 μA	0.2 ms	0.3 ms	0.3 ms
	8 mA	0.2 ms	0.3 ms	0.3 ms
	128 mA	0.4 ms	0.4 ms	0.5 ms

Load condition: resistance + capacitance (100 pF)

9.7.2 Maximum Load Capacitance (VSIM)**Table 9-45 Maximum Load Capacitance (VSIM)**

Current range	Maximum load capacitance
8 μA	100 pF
80 μA	1000 pF
800 μA	1000 pF
8 mA	0.01 μF
128 mA	0.1 μF

The maximum load capacitance is the sum of load values for branches connecting to a channel.

The maximum capacitance load ensures whichever is the greater 10% of the setting value or 0.5 V of overshoot/undershoot due to reference on/off when a load capacitance is connected.

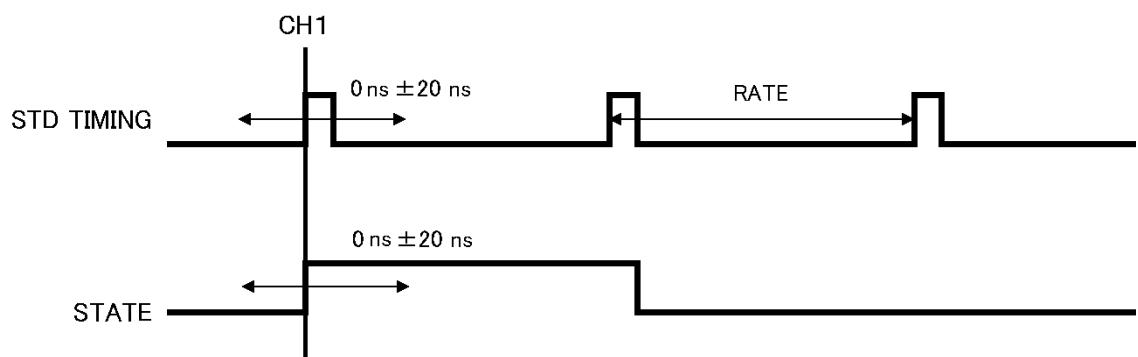
9.7.3 Voltage Measurement (MVM)**Table 9-46 Voltage Measurement (MVM)**

Voltage measurement range	Measurement range	Resolution	Measurement accuracy	Input impedance
+8 V	-0.3 V to +8 V	1 mV	$\pm(0.1\%+4 \text{ mV})$	10 M Ω or greater
-8 V	-8 V to +0.3 V	1 mV	$\pm(0.1\%+4 \text{ mV})$	10 M Ω or greater
+32 V	-0.3 V to +32 V	4 mV	$\pm(0.2\%+16 \text{ mV})$	10 M Ω or greater
-32 V	-10 V to +0.3 V	4 mV	$\pm(0.2\%+16 \text{ mV})$	10 M Ω or greater

9.8 Trigger Box Output Timing

Table 9-47 Trigger Box Output Timing

Output connector	Timing	Condition
STD TIMING	0 ns ± 20 ns	CH1 reference-on PB
STATE TRIGGER	0 ns ± 20 ns	



9.9 Utility Power Supply

Table 9-48 Utility Power Supply when Standard WMB is Installed (T5830P)

Power supply	Output voltage accuracy	Allowable output current	Overcurrent detection	Power resources
P5VPBRL1	+5 V ± 5%	7.5 A	7.5 A - 10 A	2 lines
P5VPB1	+5 V ± 5%	7.5 A	7.5 A - 10 A	2 lines
P5VPB2	+5 V ± 5%	7.5 A	7.5 A - 10 A	2 lines
P3R3VPB	+3.3 V ± 5%	2 A	2.2 A - 3.6 A	2 lines

Table 9-49 Utility Power Supply when Standard ESMB is Installed (T5830PES)

Power supply	Output voltage accuracy	Allowable output current	Overcurrent detection	Power resources
P5VPBRL2HS1	+5 V ± 5%	0.5 A	0.5 A - 1.3 A	1 line
P5VPB1HS1	+5 V ± 5%	0.5 A	0.5 A - 1.3 A	1 line
P3R3VPB	+3.3 V ± 5%	2 A	2.2 A - 3.6 A	1 line

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