

PENN STATE ELECTRICAL ENGINEERING  
EE 441 – SPRING 2019

# EE 441 –Final Lab report

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**Group 4A**

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## **Objective:**

This course has taught us the fundamentals of semiconductor device and the knowledge of integrated circuit technology. In this lab report, we will emphasize on the advanced silicon ICs fabrication. We will develop a p-type (100) wafer with 100 mm diameters into NMOS transistors. The process will take 8 lab sessions. In the following, there is a brief summary of each lab.

## **Introduction:**

### **Lab1: Wafer Characterization and Field Oxide Growth**

In this lab, we need to determine our wafer size and its resistivity by using a 4-point probe method. The four-point probe method is typically used to measure the bulk resistivity of wafers. When a current is passed through the two-outer probes, the voltage would be induced and detected by the inner voltage probes. Therefore, we used the equation (1) to calculate the resistivity of our wafer.

$$\rho = \frac{\pi}{\ln 2} \times \frac{V}{I} \times t \times k^* \quad R_{sh} = \frac{\rho}{t} \quad (1)$$

The current was set at 0.4532 mA, and the voltage was read at 1.85 V when the wafer has not been cleaned. The sheet resistance we got was 18500 by using equation (1), which was not reliable. Therefore, we had to clean out the surface contaminants and measured the wafer again. After cleaning, we had 8.724 mV, so we plugged into the equation (1) to get the sheet resistance and resistivity. The value of sheet resistance was 87. The resistivity value was between 4.36 Ω-cm and 4.79 Ω-cm. We used the value 4.79 Ω-cm in the end. Then, we would need to clean the contaminants on our wafer by using DHF, SC1, and SC2 at the wet bench. The majority of cleaning operations in semiconductor manufacturing are liquid-phase chemistries and ultra-pure water rinsing. The first step was using nanostrip to remove all the organics and metal because metal contaminants could affect the interface trap density and carrier lifetime and organic contaminants would influence the gate oxide integrity. Then, we needed to rinse the wafer in water to clear out the chemical. Later, we had a DHF solution to remove native oxide and then rinse with water again. Next, we repeated the process but used SC1 and SC2 respectively to replace the nanostrip solution. SC1 was used to remove particle and organic contaminants, and SC2 was used to remove metal contaminants. It was important to rinse with water after each operation in order to ensure that there were no other solutions left. Moreover, it was necessary to use dedicated baths for each chemical because of several reasons such as safety, automation, or recirculation (overflow). After cleaning the wafer, we would need to use the four-point probe to measure our wafer again to ensure it met our requirement. Next, we will send the wafer into the thermal oxidation furnace system to have the thermal oxidation process.

## ***Thermal Oxidation:***

One of the major reasons for using silicon in ICs is silicon has an excellent oxide  $\text{SiO}_2$ . It is widely used as an insulator and in the region of the active devices. Although silicon will oxidize in air at room temperature, it is not sufficiently mobile to diffuse through the native oxide, and not get much thicker than 25 Å. Hence, we would heat the wafer in the presence of an oxidizing ambient in order to have enough oxide. We want our temperature at 1050 °C, so we looked up the figure

to find A and B coefficient, which were 0.18 and 0.4 respectively. Then, we needed to plugged in the number to get out the t value. Also, we knew the tox value was 0.7  $\mu\text{m}$  and toxi was 0.

$$t = \frac{0.18}{0.4} * 0.7 \mu\text{m} + \frac{0.7^2}{0.4} = 1.54 \text{ hr} = 1\text{hr } 40 \text{ mins.}$$

So, we operated the system 1 hour and 40 minutes for oxidizing the surface, and waited for the next process in lab 2.

### **Lab2: Source & Drain (S/D) Open**

In the lab 2, we would observe the thickness of our wafer to make sure our target was at 700 nm. If our wafer was too thick or too thin, we would need to adjust the spin speed for the photoresist application. The color we observed from our wafer was pink-green, so we guessed that our wafer thickness was around 4600~5200 Å from the color chart. After measuring from the Nano spec, the value was displayed in Table 1.

Average	6347 Å
Minimum	6147 Å
Maximum	6530 Å
Range	383 Å
Std Dev	117.673 Å

Table 1. The result of oxide characterization.

The average thickness was 6347 Å, which was pretty closed to 7000 Å with only 9.33 % difference. However, we would need to adjust the spin speed for coating photoresists. Next, we would have SPR3012 ready and bake it on the wafer. In this procedure, we would put our wafer on the spin machine with two different materials HDMS and SPR3012 in order to coat the photoresist. Still, we need to check our wafer was clean or not. In the process, we noticed that there were some particles on the wafer surface, so we tried to use a high-pressure air to clean out the particles. Then, we baked the wafer at 99 °C for one minute, and we centered our wafer by vacuuming on the HMDS and rotated at 2500 rpm for the first time. Next, we baked the wafer again for another one minute, and placed SPR3012 on the surface and rotated at 2500 rpm as well. The amount of SPR3012 was determined by the inch of the wafer. One inch the wafer would have one microliter SPR3012. Afterward, we put the wafer into a photolithography stepper to give us the patterns on the mask. We found our best exposure time was found at 0.3, and then we started the fusion by DUV light in order to improve the resist stabilization. The reason why we need to hard bake the wafer was to make the resist structures more stable by subsequent physical or chemical processes in the resist. In the end, we would determine the etch rate for the etching progress by measuring the thickness of the wafer. Therefore, we could determine the approximate etch rate by using the value provided above. The equation we used was showed below.

$$\text{Etch Rate (ER)} = \frac{\Delta d}{\text{time}} = \frac{(d_0 - d_1)}{\text{time}}$$

$$\text{Etch Rate (ER)} = \frac{\Delta d}{\text{time}} = \frac{6347 - 1303.8 \text{ \AA}}{10 \text{ min}} = 504.3 \text{ \AA/min}$$

$$\text{time should etch} = \frac{1303.8}{504.3} * (1 + 10\%) = 2.84 \text{ min}$$

From the calculation showed above, we needed to etch for 2.84 minutes to get our wafer thickness as 0 Å. The reason why we wanted to add 10% to our time was the safety reason which prevented the wafer process. After etching, we got our thickness was 41 Å and 0 Å at two points, which made our expectation. In addition, we could calculate the etch non-uniformity by using the formula below.

$$NU (\%) = \frac{E_{max} - E_{min}}{2E_{ave}} = \frac{6530 - 6147}{2 * 6347} = 3\%$$

The value was pretty good for our wafer, which showed our wafer was pretty much uniform.

### Lab3: Dopant Diffusion

In this lab, the background doping level of Boron was  $1.5e16 \sim 2.17e15$  atoms/cm<sup>3</sup>. We were using a 2 steps diffusion process, which were pre-deposition and drive-in dopant. In pre-deposition, we placed the wafer into a container with liquid Phosphorous. The temperature of the bath was at 975 °C and the time process was 45 minutes. We knew the Phosphorous diffusivity in silicon was 4.5 cm<sup>2</sup>/sec, and solid solubility of Phosphorous was  $7e20$  atoms/cm<sup>3</sup>. Therefore, we could use equation (2) to calculate the diffusivity ( $D_1$ ), which was  $6.19e-15$  cm<sup>2</sup>/sec. Also, we calculated  $D_1 t_1$  in order to get the dose (Q) by using the equation (3). The dose we got was  $3.23e15$  atoms/cm<sup>2</sup>.

$$D_1 = D_0 e^{(-\frac{E_A}{kT})} \quad (2)$$

$$D_1 = 4.5 e^{(-\frac{3.68 \text{ eV}}{8.617 \times 10^{-5} \times 1248})} = 6.19 \times 10^{-15} \text{ cm}^2/\text{sec}$$

$$D_1 t_1 = 6.19 \times 10^{-15} \times 45 \times 60 = 1.67 \times 10^{-11} \text{ cm}^2$$

$$Q = \frac{2N}{\sqrt{\pi}} \sqrt{Dt} = \frac{2 \times 7 \times 10^{20}}{\sqrt{\pi}} \times \sqrt{1.67 \times 10^{-11}} = 3.23 \times 10^{15} \frac{\text{atoms}}{\text{cm}^2} \quad (3)$$

We then put the wafer in a 10:1 BOE for sixty seconds in order to remove the phosphosilicate glass. Our goal was made the surface concentration larger than  $1e20$ , and junction depth larger than 0.5 μm, so we need to calculate the new diffusivity for the drive-in diffusion, which was  $4.31e-14$  cm<sup>2</sup>/sec, and  $D_2 t_2$  was  $7.75e-11$  cm<sup>2</sup>. Hence, the parameters we provided above can give us an initial concentration  $2.07e20$  cm<sup>-3</sup> and junction depth 0.544 μm. In the end, we would get an NMOS silicon wafer.

### Lab4: Gate Open

In the previous lab, we have created the source and drain regions for our p-type substrates. So, we will need to use HF to etch away the thermal SiO<sub>2</sub> in the gate region. Therefore, we have to be properly aligned to the S/D regions which we made in the diffusion process. The first step was to apply photoresist. All of the baking steps in this process lasted 60 second at 95 °C. This was

followed by spinning on HMDS at 2500 RPM for 15 second (we saw a color change on wafer). HMDS could help photoresist adhesion by creating a hydrophobic surface. After the HMDS was baked on, we would start to bake the photoresist. The resist we used was SPR3012 and it was spinning for 6000 rpm for 45 second. Then, the SPR3012 was backed. Later, we put our wafer into GCA8000, Photolithography Stepper to do the second lithography. It was necessary to align the mask so that only the gate region is exposed. We used the global alignment marker to help us adjust the alignment. The global alignment marker was located in the corner of each patterns, and it was showed in Figure 1.

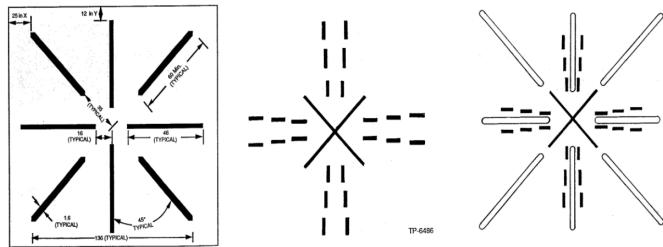


Figure 1. Global alignment marker.

We used the joy stick to switch between right and left in order to adjust x-align at right side, and adjust y-align at left side. The calibration would be completed until the maker was matched. After we finished the global alignment progress, the system will begin to calibrate the local alignment. As we knew that the two-points alignment method yields an accuracy of +/- 250 nm, so the software will use a dark field microscopy system and collect light from the edge of a feature, resulting in a sharper signal. This process could reduce the error to +/- 150 nm. The developer we used in this lab was a base called CD-26, which was 2.4% Tetramethylammonium hydroxide. An automatic developer was used. The developer first rinses the wafer with DI water, then develops the wafer for 80 seconds using CD-26, and then finishes by rinsing the wafer in DI water again. Finally, the wafer was dried and ready for deposition.

### **Lab5: Gate Dielectric Deposition**

After we opened the gate, we will do the ALD process, and deposit on 10 nm Al<sub>2</sub>O<sub>3</sub> gate dielectric.

#### ***Atomic Layer Deposition (ALD):***

The overall process was showed in Figure 2.

Steps	Gas	Purpose
1	H <sub>2</sub> O Pulse	Hydrolyze Surface
2	Wait (w/ N <sub>2</sub> Purge)	Remove excess water vapor with Inert gas
3	Metal Organic Precursor	Metal organic reacts with hydrolyzed surface. No further reaction possible
4	Wait (w/ N <sub>2</sub> Purge)	Remove excess metal organic with Inert gas
5	Repeat steps 1-4	Increase thickness

Figure 2. ALD overall progress.

Before the ALD process, the wafers were cleaned using the standard RCA clean in order to ensure a better interface between the aluminum oxide and silicon. The process is the deposition of Al<sub>2</sub>O<sub>3</sub> from Trimethyl Aluminum (TMA) and H<sub>2</sub>O. It has been assumed that the exposure of the surface to water vapor leads to the formation of a monolayer of surface hydroxyl groups and that these groups react with the aluminum source molecules, which lose one of the methyl groups and in the process form a bond to the substrate. So, at certain temperature, this aluminum reacts with the weak O-H bonds and replaces the hydrogen. TMA does not react with itself, limiting the reaction to one layer. This occurs across the entire layer, and then another nitrogen purge clears the precursor out. Another H<sub>2</sub>O pulse enters, and the water vapor reacts with the dangling methyl groups, replacing them with oxygen and another dangling hydrogen. This process is repeated until the desired thickness is reached. At the deposition temperature of 300 C, the growth rate is 0.84 Å/cycle, so 119 cycles were needed to reach 10 nm. The thickness of 10 nm was chosen because it provides a significant enough capacitance to prevent charge flow through the oxide layer for aluminum oxide.

### **Lab6: Source and Drain (S/D) Contact Open**

The objective of this lab is to open and isolate the source and drain regions of the transistor. This will be achieved by patterning the windows with photolithography and dry etching the Al<sub>2</sub>O<sub>3</sub> & SiO<sub>2</sub> layer. We used a different photoresist, SPR 955 this time. It was better for plasma dry etching. We put HDMS first on the wafer and spun it at 3000 rpm for 60 second. Then, we baked the wafer and put SPR 955 on the wafer. We spun it at 3000 rpm for 45 second in order to have thicker photoresist (~1.8um) for dry etching. After etching, we put the wafer into the stepper and do the exposure dose at 0.35. Then, we put the wafer 120 seconds in CD-26 to develop the resist. The wafer was hard baked using the Fusion DUV hard bake equipment for 5 minutes at 100°C. Later, we did the plasma dry etching on the wafer. We followed the parameter which shows in Figure 3 to calculate the etching rate for Al<sub>2</sub>O<sub>3</sub> and SiO<sub>2</sub>.

**Al<sub>2</sub>O<sub>3</sub> Dry Etch**

Pressure: 5 mT  
 RF Coil Power: 1000 W  
 Substrate Power: 75 W  
 Cl<sub>2</sub>: 6 SCCM  
 BC<sub>l</sub>3: 30 SCCM  
 Al<sub>2</sub>O<sub>3</sub> ER: 6 Å /s  
 SPR955 ER: 45.4 Å /s  
 Avg. Thickness: 100 Å  
 or 140 Å  
 Time: 20 s

**SiO<sub>2</sub> Dry Etch**

Pressure: 10 mT  
 RF Coil Power: 500 W  
 Substrate Power: 200 W  
 CF<sub>4</sub>: 40 SCCM  
 SiO<sub>2</sub> ER: 55 Å /s  
 SPR955 ER: 68.1 Å /s  
 Avg. Thickness: 1103 Å  
 Time: 24 sec

Figure 3. Dry etch parameter.

During the process, BC<sub>l</sub> radicals reactive with O in Al<sub>2</sub>O<sub>3</sub> forming volatile BC<sub>l</sub>xO, and Cl reacts with Al to form the volatile compound AlCl<sub>3</sub>. Then, CF radicals react with SiO<sub>2</sub> to form SiF<sub>4</sub> and CO. CF won't affect Al<sub>2</sub>O<sub>3</sub>, so we don't need to worry about over etch in Al<sub>2</sub>O<sub>3</sub>. In the end, we had to strip the remaining photoresist from the rest of the wafer. Nanostrip could not be used in this process because it would also strip away at the metal gate oxide layer as well.

### Lab 7: Metallization

This lab, we will focus on the metal evaporation by using the e-beam evaporation to deposit a metal layer which will be patterned to form the contact pads and interconnects and we will measure witness sample to determine thickness of deposited Platinum, which is important for the metal etch in next lab.

#### *E-beam evaporation*

Normally, a simple low flux electron beam system, which showed in Figure 4, consists of a loop heated tungsten wire surrounding a thin rod of material held at a high bias with respect to the wire. Electrons boiling off the wire impact the rod, raising the temperature at the end of the rod and creating an atomic beam.

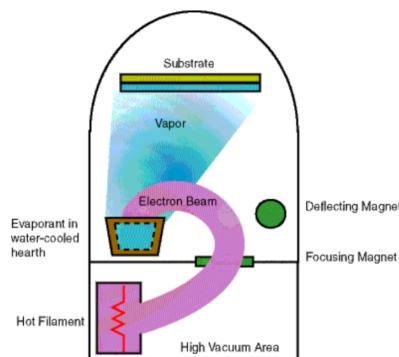


Figure 4. E-beam system imagination.

The chamber of the system is often vacuum in order to move particles from point A to point B without a collision and also reach long mean free path. Electron beam heating forms much purer films than filament or crucible heating. The generated electron beam is accelerated to a high kinetic energy and directed towards the evaporation material. Upon striking the evaporation material, the electrons will lose their energy very rapidly. The kinetic energy of the electrons is converted into other forms of energy through interactions with the evaporation material. The thermal energy that is produced heats up the evaporation material causing it to melt or sublime. Once temperature and vacuum level are sufficiently high, vapor will result from the melt or solid. The resulting vapor can then be used to coat surfaces.

Our target thickness is 1000 Å. The reason why we chose to use e-beam evaporation instead of thermal evaporation is that the system can give us more flexibility. It is much easier to control at higher melting points. It is imperative to calculate the mean free path (MFP) of platinum in order to control the thickness. At room temperature, we can simplify the calculation for the mean free path to just  $\lambda=3.7 \cdot 3/P$ . The pressure in the chamber is a key component of the process. The vacuum creates a low-pressure environment that prevents particle collisions. Once the chamber pressure is high enough, the e-beam evaporation can occur in the special chamber. Electrons are directed into a crucible filled with platinum. Then resulting metal vapor sublimes onto substrate. The recipe of the e-beam system is P1500A. The rate is 2 Å per second, and the cool down time is 300 seconds. After finishing the evaporation, we measured the height difference between two points that is between the unexposed area and the exposed glass wafer surface. The thickness could help us determine the profilometry. The measurements are shown in Table 2.

Table 2. Profilometry measurement.

Top measurement	604.7 Å
Middle measurement	583.8 Å
Bottom measurement	Bad data
Left measurement	597.3 Å
Right measurement	573.9 Å

### **Lab8: Contact Patterning**

The primary goal of this lab was to etch away Platinum metal in connecting areas of the source, gate, and drain regions allowing the physical isolation of the described areas to provide the correct device operation. The process is shown in Figure 5&6. We will need to have the fourth lithography for the contact pads and interconnects in this metal layer.



Figure 5. Metal contact deposition.

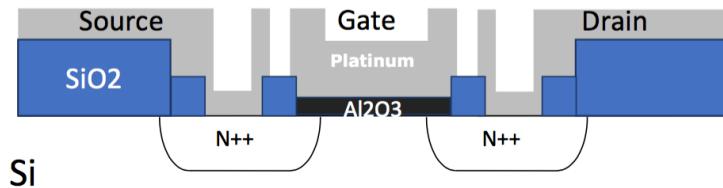


Figure 6. Metal etching.

The resist we used is SPR 3012 because it has more forgiving during development compare to SPR955. Once SPR 955 is removed from developer it can't be put back in and developed further. Also, Pt layer is thin and will etch through before the resist is consumed. The recipe we used is D09\_40\_45. The spin speed is 4000 rpm. It will start at 900 rpm to get SPR balance on the surface and then speed up to 4000 rpm. The hot plate temperature is 100 °C for 1 minute. After finishing the lithography, we will have to check the alignment offsets before we do the dry etching. Then, we will do the dry etching to remove the platinum on the surface. The recipe name is EE441 MC. The etch parameters is shown in Figure 7. The little oxygen is for the photoresist in order to prevent the platinum metal to get back to the substrate.

- Pressure: 3.5 mT
- RF Coil Power: 900 W
- Substrate Power: 225 W
- Cl<sub>2</sub>: 30 SCCM
- Ar: 40 SCCM
- O<sub>2</sub>: 4 SCCM
- Pt Etch Rate: 14 Å /s
- Time: 45 s

Figure 7. Etching parameter.

At the final step, we will have our wafer on the hard bake to do the resist strip. The temperature is 100°C for 5 minutes in order to prevent the wafer not to stick on the etch chamber. In the end, our NMOS wafer has been made, and we will provide our testing results in the following section.

## Testing results

In the last two labs, we are going to test the device characterization. We are going to measure the step coverage chain, capacitance, and resistance. Moreover, we will plot the I-V graph of the diode and Id-Vd diagram of the MOSFET. The equipment is called electrical probe station, which is shown in Figure 8.

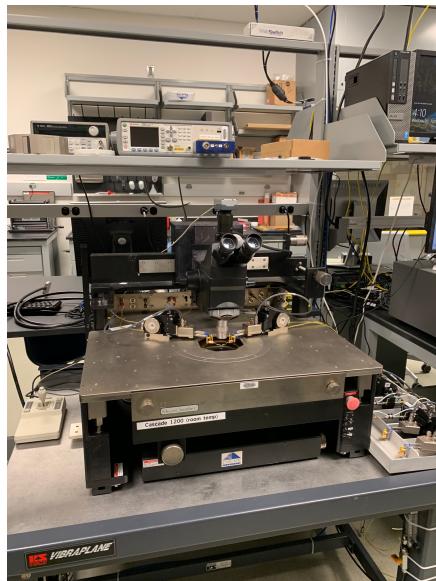


Figure 8. Electrical Probe Station.

We will measure the contact chain in order to determine whether the chain is completely coverage or not. The schematic of continuity between the probes can be seen in Figure 9.



Figure 9. Chain continuity.

We will put our probes on the pattern which displayed in Figure 10. We expect to get a larger value of resistance for the measurement.

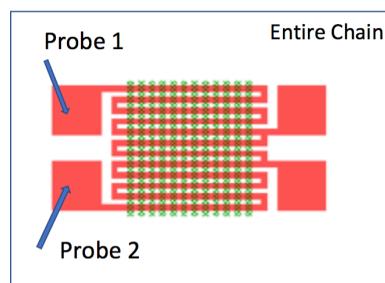


Figure 10. Location of the probes.

We measured the wafer ID is 1B and the results is provided in Table 3.

Table 3. The measurement of the entire chain.

Location	Entire Chain
Top	751 Ω
Center	792 Ω
Bottom	753 Ω
Left	8.5*10 <sup>5</sup> Ω
Right	960 Ω

We noticed that the resistance of the wafer on the left side has larger difference value than others. We believed that there is an error which caused by the resist on the wafer. The resist did not clean well and the probe we measured also scratch the pattern. Then, we need to measure the resistor on the wafer and compare to the 4-point probe value measured earlier in the semester. We can calculate the theory resistance by using the equation below. Sheet Resistance (Rs) units is ohms per square (Ω / sq). The value of sheet resistance we used is 87.

$$R = R_s \times (\# \text{ of Squares})$$

For example, the square is 30 μ x 30 μ, and the resistor size is 30 μ x 100 μ, so the number of squares is 10/3. Therefore, when we do the calculation, the resistivity value should get larger from R1 to R4. In the following table, it was the results we have measured.

Resistor	Bottom	Right	Theory
R1	391 kΩ	320 kΩ	290 kΩ
R2	693 kΩ	226 kΩ	580 kΩ
R3	239 kΩ	198 kΩ	870 kΩ
R4	549 kΩ	147 kΩ	1160 kΩ

In this case, we can notice that this wafer has bad measurement data, so the resistor on this wafer cannot work precisely. Besides, comparing the data between the location Bottom and Right, there are still lots of difference, which need to be improved in the next fabrication. Later, we measure the capacitor by putting the probe on the gate oxide (ALD Alumina). We will compare our results with the theoretical value by using the formula below and find out the dissimilarity. The measurement is measure at 1 MHz frequency. The software will start from -1V to 1V with 0.1 for each step.

$$C = \frac{k \varepsilon_0 A}{d}, \quad \text{ALD parameter } k \text{ is } 9.1 \quad \varepsilon_0 = 8.854 \times 10^{-12}$$

Capacitor	Top	Bottom	Center	Left	Right	Theory
Small	47.5 fF	81 fF	95 fF	66 fF	70.5 fF	$9.1 \times 10^{-2}$ nF
Medium	192 fF	149 fF	184 fF	50 fF	81 fF	1.81 nF
Large	218 fF	250 fF	260 fF	125 fF	274 fF	3.22 nF

The distance between plates is 10 nm, and the area are  $10^{-8}$ ,  $2.25 \times 10^{-8}$ ,  $4 \times 10^{-8}$  m<sup>2</sup>. Therefore, we can see our result has huge error percentage. Hence, we can conclude that our capacitor is not precisely as well. In addition, we can see the left and right side has worse data than other three locations. Also, the medium capacitors have many errors. We concern the reason is that alignment is not accuracy during the lithography, so the patterns are overlapped. Next, we can create a P-N junction diode by using just source or drain regions in the MOSFET on p substrate. The diode's ideal I-V characteristics can be described by the equation  $I_d = I_s (e^{(eV/nkT)} - 1)$  when diode is in forward biased mode. We did the I-V measurement when lights are off in order to have lower carrier generation, which gave us a lower current compared to the lights are on. We will put the probe on the pattern which shows in Figure 13 and the screen in Figure 14 displayed how the software works.

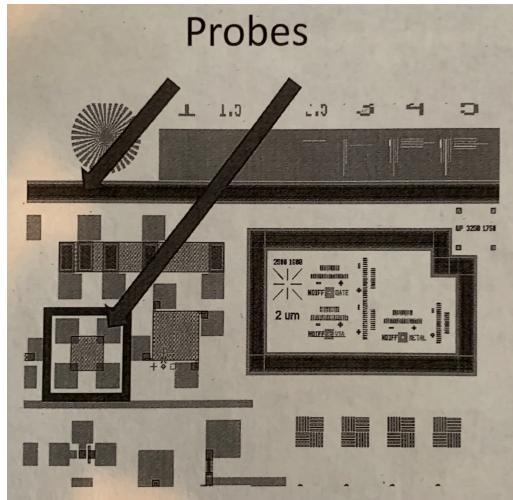


Figure 12. P-n junction diode.

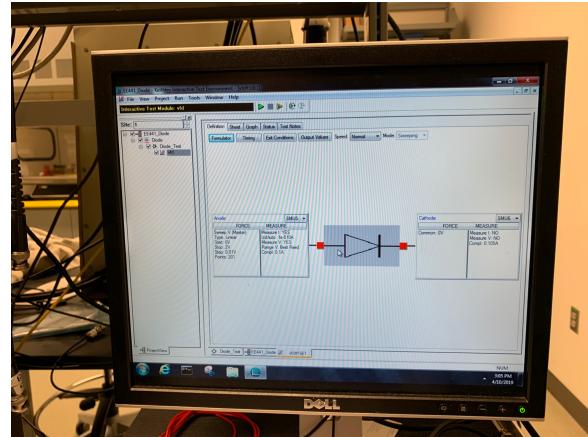


Figure 13. Screen of testing diode I-V sweep.

We start the program from 0V to 2V with 0.01 V per step. We have measured five locations as previous measurements and each location we have three different sweeps on different area of the junction. We decided to analyze the results at the center, top, and bottom location because we conclude there are many errors at right and left side from the previous testing. So, I used OriginPro to replot our measurement diagrams, which are shown in below. I calculate the average of each location and plot them together in the same diagram.

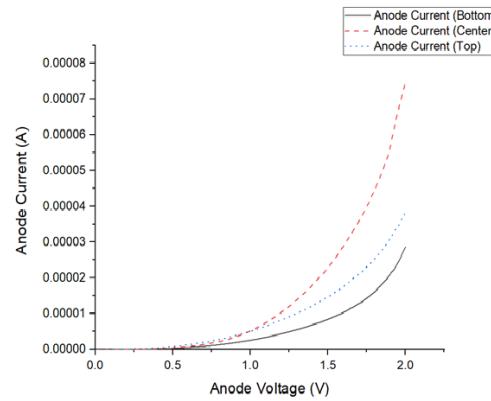


Figure 14. I-V diagram

We can determine the ideality factor by analyzing the linear region of the I-V curve. By taking the log of the current and plotting it against the voltage, we can determine the slope of the line, which shows in Figure 16.

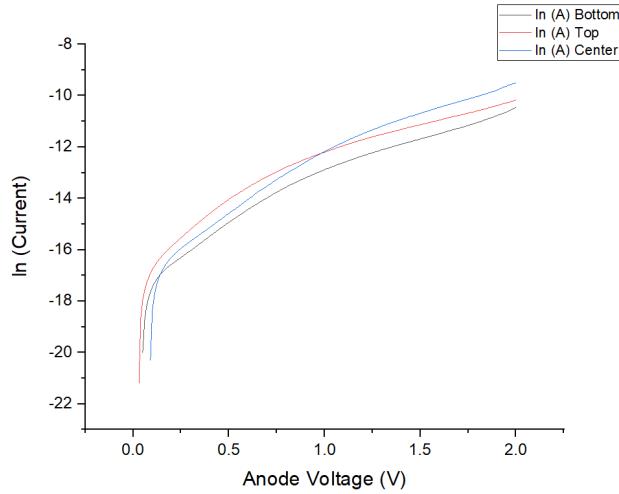


Figure 15.  $\ln(I)$  - V diagram.

We can find the identify factor  $n$  from the slope, which can calculate by  $n = 1 / (\text{slope} * 0.0259)$ . Therefore, our  $n$  value from the measurement is 11.3. The number is quite made sense. If  $n$  value is larger than 1, it can indicate that the linear region is over a longer voltage period before the diode reached saturation. Last, we will determine the MOSFET characteristics by measuring W/L value at 2 and 10. We plotted the  $I_{ds}$  vs  $V_{ds}$  at several different gate biases, which shows in Figure 17 & 18.

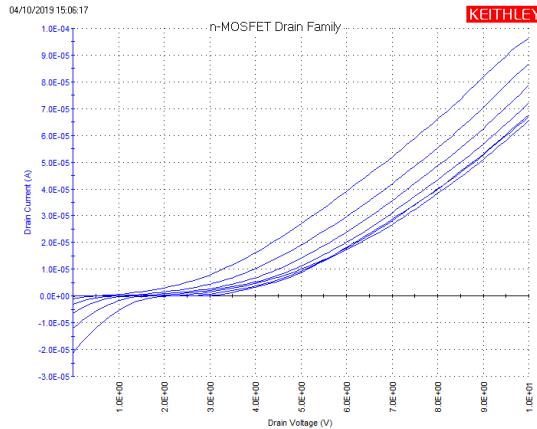


Figure 16.  $I_d$ - $V_{ds}$  with top location of  $W/L$  at 10.

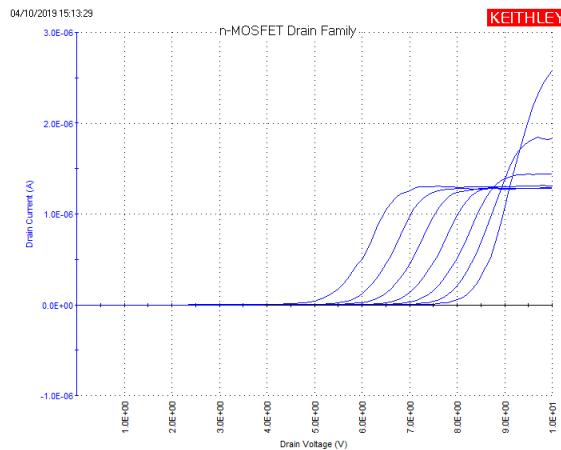


Figure 17. Id-Vds with top location of W/L at 2.

From the diagram, we noticed that our current is really low. This is reason why our device performed poorly since our device required a larger turn-on voltage and remained in the linear region for longer than is expected. All in all, our testing of the wafer is successful, but the measurement does not match our expectation. We should focus more on cleaning and align the masks in order to improve the accuracy.