AKD4678-C

Evaluation board Rev.0 for AK4678

GENERAL DESCRIPTION

The AKD4678-C is an evaluation board for AK4678, 24bit stereo CODEC with Microphone/ Receiver/ Headphone/ Speaker/ Line amplifier. The AKD4678-C has the Digital Audio I/F and can achieve the interface with digital audio systems via optical connector.

■ Ordering Guide

AKD4678-C --- AK4678 Evaluation Board
(A cable for connecting with USB port of PC and a control software are packed with this.)

FUNCTION

- **DIR/DIT with optical input/output**
- **10pin Header for Digital Audio I/F and PCM I/F (Baseband, Bluetooth)**
- **10pin Header for I²C control mode**

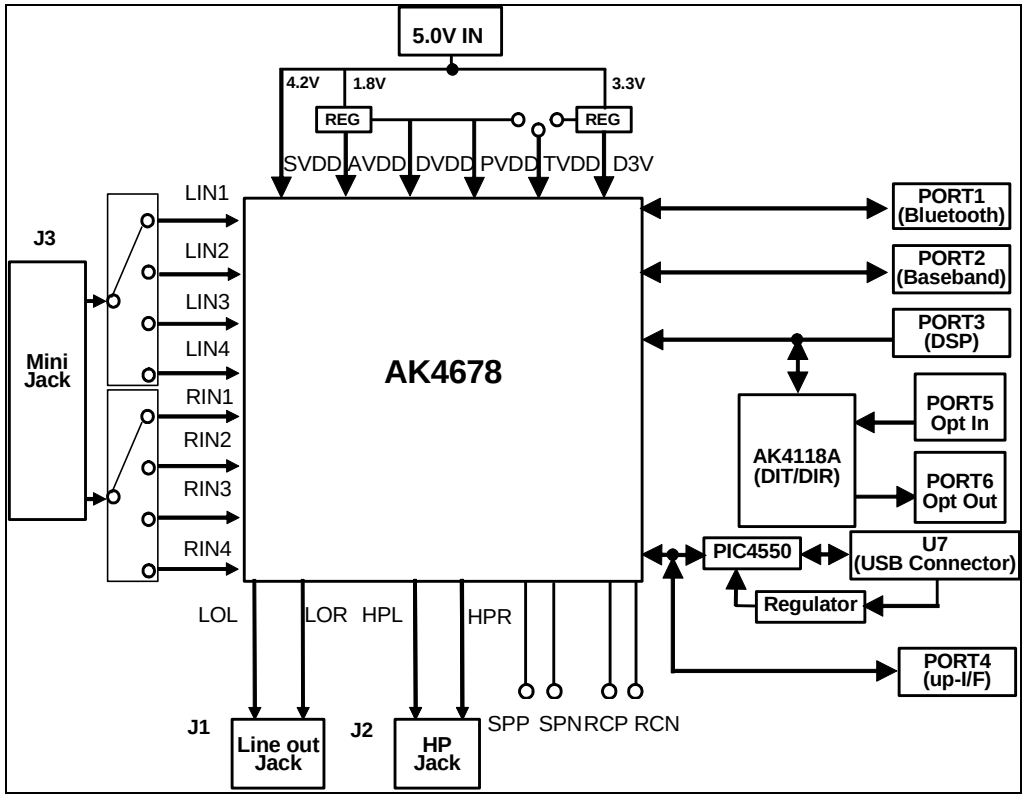

Figure 1. AKD4678-C Block Diagram

*Circuit diagram and PCB layout are attached at the end of this manual.

■ Component layout

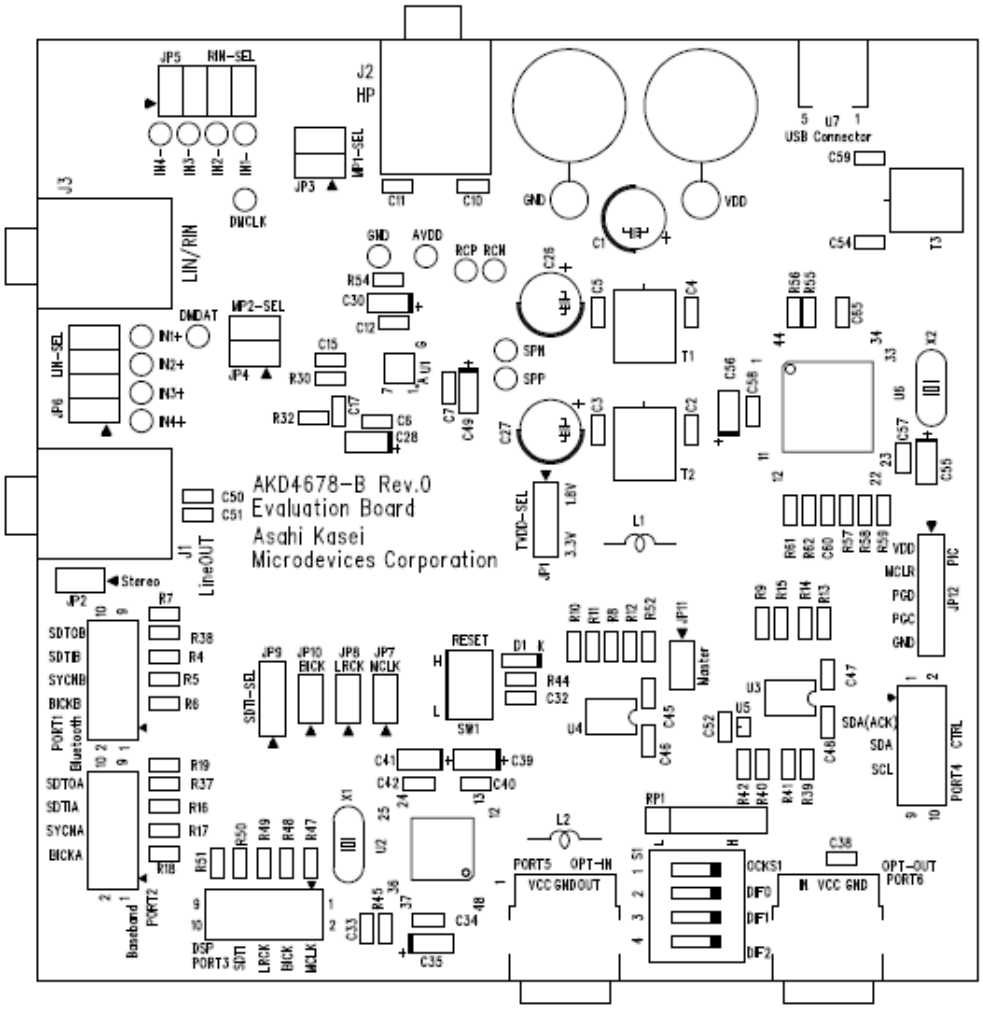

Figure 2. AKD4678-C Component layout

■ Component explanation

1. J1,2 (Mini Jacks)
   Output terminal of analog signal

2. J3 (Mini Jacks)
   Input terminal of analog signal

3. +4.2V, GND (Power Supply Connector)
   Please connect to Power Supply. Each supply line should be distributed from the power supply unit.

4. PORT1, PORT2, PORT3 (10pin Header)
   PORT1 (Bluetooth port) : MCLKB, BICKB, LRCKB, SDTOB, SDTIB can output and input from PORT1.
   PORT2 (Baseband port) : MCLKA, BICKA, LRCKA, SDTOA, SDTIA can output and input from PORT2.
   PORT3 (DSP port) : MCLK, BICK, LRCK, SDTI, SDTO can output and input from PORT3.

5. PORT5, PORT6 (Optical Connectors)
   PORT6 (Output) : PORT6 outputs Optical Digital Signal from AK4118A.
   PORT5 (Input) : PORT5 inputs Optical Digital Signal from AK4118A.

EVALUATION BORAD

■ Operation Sequence

[1] Power Supply

1) Set up the Power Supply Lines

Name	Color	Power	Function	Other
+4.2V	RED	+4.2V	Regulator	Please be sure to connect.
GND	BLACK	0V	GND	Please be sure to connect.

Table 1 . Set up the Power Supply Line

2) Set up the evaluation mode and jumper pins

See the followings

3) Power on

The AK4678 should be reset once bringing SW1 (PDN) “L” upon power-up.

[2] Evaluation Mode

1). External Slave Mode

(a) Evaluation of A/D using DIT of AK4118A
(b) Evaluation of D/A using DIR of AK4118A <default>
(c) Evaluation of Loop-back using AK4118A
(d) All interface signals including master clock are fed externally

2). External Master Mode

(a) Evaluation of A/D using DIT of AK4118A
(b) Evaluation of D/A using DIR of AK4118A
(c) Evaluation of Loop-back using AK4118A
(d) All interface signals including master clock are fed externally

3). PLL Slave Mode

(a) All interface signals including master clock are fed externally

4). PLL Master Mode

(a) All interface signals including master clock are fed externally

5). PCM I/F A&B

(a) All interface signals including master clock are fed externally

[3] Jumper Pin and SW Setting

[2] Evaluation Mode

(2-1). External Slave Mode

In case of AK4678 evaluation using AK4118A, it is necessary to correspond to audio interface format for AK4678 and AK4118A. Audio Interface Format of AK4678 refer to datasheet and Audio Interface Format of AK4118A refer to Table 3, respectively.
In the case evaluation mode sets to Ext Slave Mode, AK4118A set to Master Mode and register setup for AK4678 set to Ext Slave Mode.
Please refer to the data sheet about a register setup of AK4678.

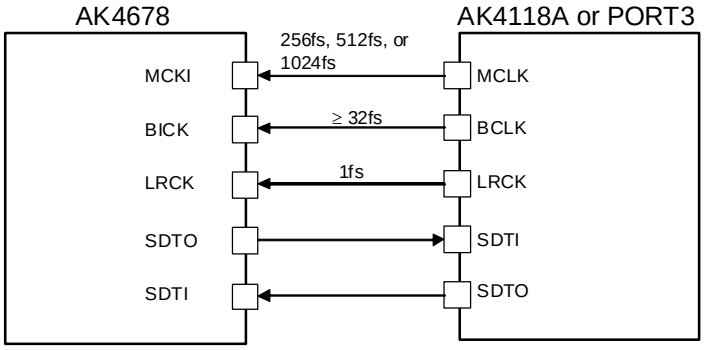

Figure 3. EXT Slave Mode

(a) Evaluation of A/D using DIT of AK4118A
X1(X'TAL) and PORT6 (DIT) are used. Nothing should be connected to PORT5 (DIR) and PORT3 (DSP).
MCLK, BICK and LRCK are supplied from AK4118A, AK4678 supplies SDTO to AK4118A.

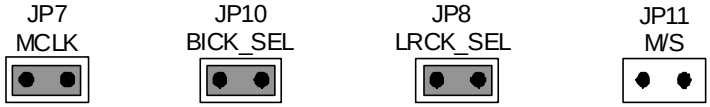

Figure 4. JP Setting - 1

(b) Evaluation of D/A using DIR of AK4118A <default>
PORT5 (DIR) is used. Nothing should be connected to PORT3 (DSP) and PORT6 (DIT).
MCLK, BICK, LRCK, SDTI are supplied from AK4118A.

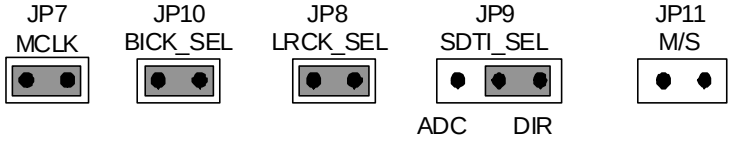

Figure 5. JP Setting - 2

(c) Evaluation of Loop-back using AK4118A
X1(X'TAL) is used. Nothing should be connected to PORT5 (DIR), PORT3 (DSP) and PORT6 (DIT).
MCLK, BICK and LRCK are supplied from AK4118A, SDTO is loopback to SDTI.

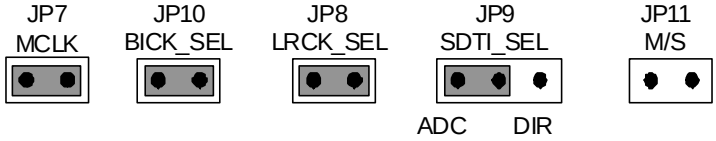

Figure 6. JP Setting – 3

※AK4118A accepts more than fs=32kHz. When evaluate AK4678 less than fs=32kHz, Please use the other mode.

(d) All interface signals including master clock are fed externally
PORT3 (DSP) is used. Nothing should be connected to PORT5 (DIR) and PORT6 (DIT).
MCLK, BICK and LRCK are supplied from PORT3, AK4678 supplies SDTO to PORT3.

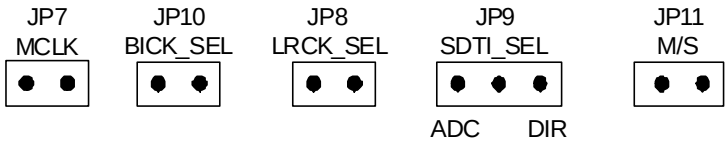

Figure 7. JP Setting – 4

(2-2). External Master Mode

In case of AK4678 evaluation using AK4118A, it is necessary to correspond to audio interface format for AK4678 and AK4118A. Audio Interface Format of AK4678 refer to datasheet and Audio Interface Format of AK4118A refer to Table 3, respectively.
In the case evaluation mode sets to Ext Master Mode, AK4118A set to Slave Mode and register setup for AK4678 set to Ext Master Mode.
Please refer to the data sheet about a register setup of AK4678.

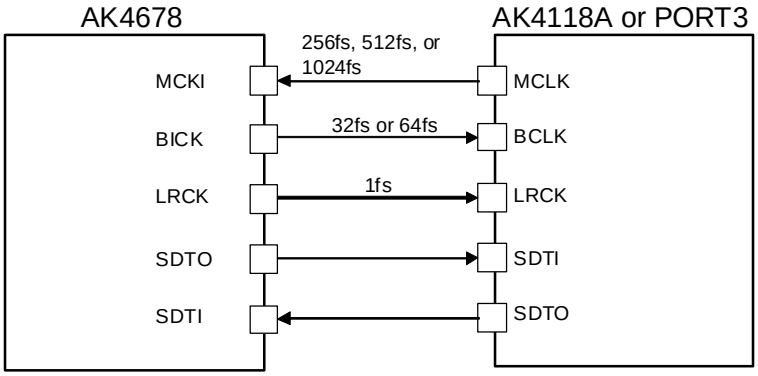

Figure 8. EXT Master Mode

(a) Evaluation of A/D using DIT of AK4118A
X1(X'TAL) and PORT6 (DIT) are used. Nothing should be connected to PORT5 (DIR) and PORT3 (DSP).
MCLK is supplied from AK4118A, AK4678 supplies BICK, LRCK and SDTO to AK4118A.

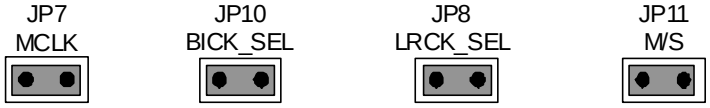

Figure 9. JP Setting – 5

(b) Evaluation of D/A using DIR of AK4118A
PORT5 (DIR) is used. Nothing should be connected to PORT3 (DSP) and PORT6 (DIT).
MCLK and SDTI are supplied from AK4118A, AK4678 supplies BICK and LRCK to AK4118A.

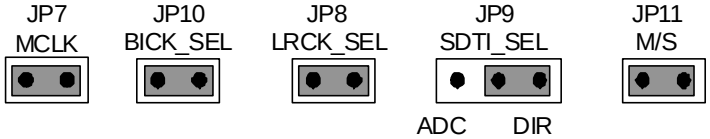

Figure 10. JP Setting – 6

(c) Evaluation of Loop-back using AK4118A
X1(X'TAL) is used. Nothing should be connected to PORT5 (DIR), PORT3 (DSP) and PORT6 (DIT).
MCLK is supplied from AK4118A, AK4678 supplies BICK and LRCK to AK4118A.
SDTO is loopback to SDTI.

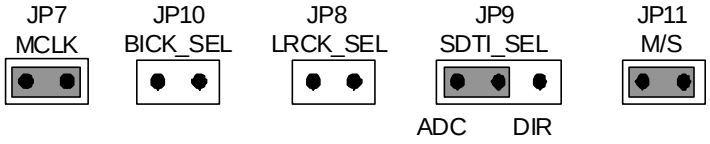

Figure 11. JP Setting – 7

(d) All interface signals including master clock are fed externally
PORT3 (DSP) is used. Nothing should be connected to PORT1 (DIR) and PORT6 (DIT).
MCLK and SDTI are supplied from PORT3, AK4678 supplies BICK, LRCK and SDTO to PORT3.

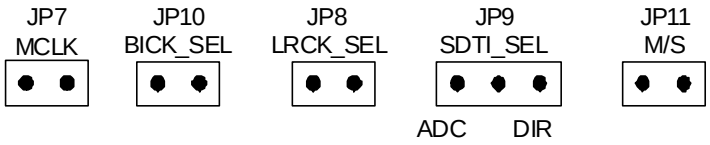

Figure 12. JP Setting – 8

(2-3). PLL Slave Mode

A reference clock of PLL is selected among the input clocks to BICK pin. The required clock to the AK4678 is generated by an internal PLL circuit.

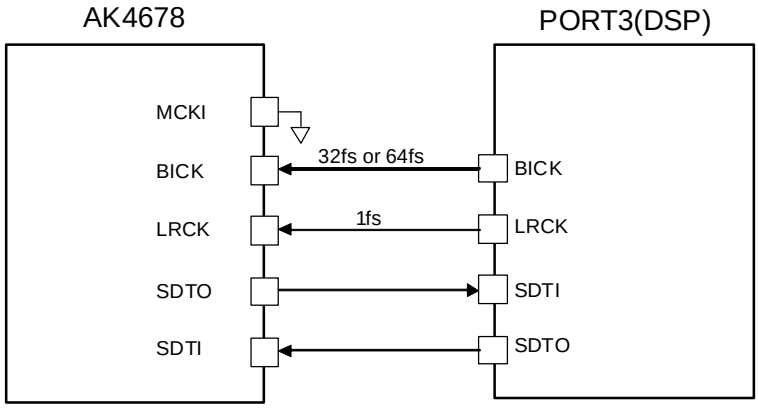

Figure 13. PLL Slave Mode (PLL Reference Clock: BICK pin)

(a) All interface signals including master clock are fed externally
PORT3 (DSP) is used. Nothing should be connected to PORT5 (DIR) and PORT6 (DIT).
BICK, LRCK and SDTI are supplied from PORT3, AK4678 supplies SDTO to PORT3.
This evaluation mode can use various fs by using the internal PLL circuit.

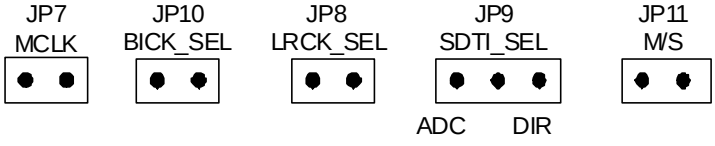

Figure 14. JP Setting – 9

(2-4). PLL Master Mode

A reference clock of PLL is selected among the input clocks to MCLK pin. The required clock to the AK4678 is generated by an internal PLL circuit.

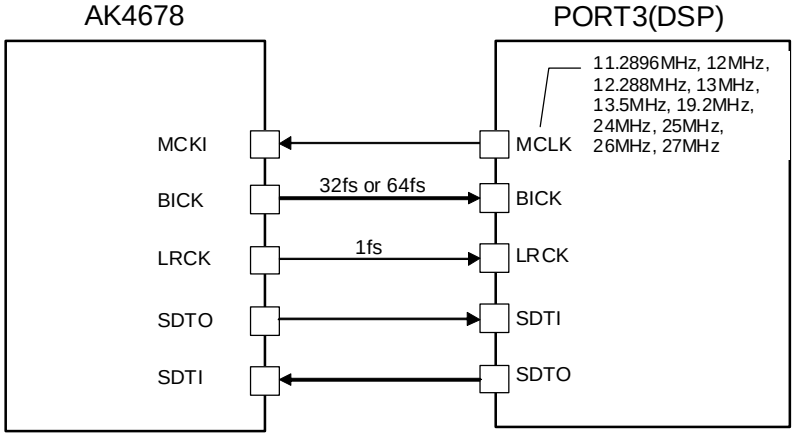

Figure 15. PLL Master Mode

(a) All interface signals including master clock are fed externally
PORT3 (DSP) is used. Nothing should be connected to PORT5 (DIR) and PORT6 (DIT).
MCLK and SDTI are supplied from PORT3, AK4678 supplies BICK, LRCK and SDTO to PORT3.
This evaluation mode can use various fs by using the internal PLL circuit.

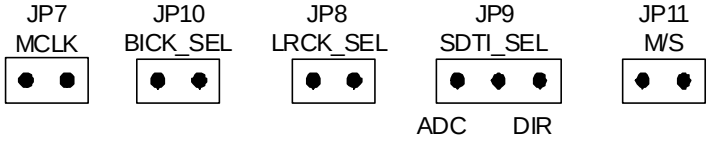

Figure 16. JP Setting - 10

(2-5). PCM I/F A&B

The AK4678 has two PCM I/F ports. PCM I/F A, PCM I/F B and Audio I/F can be operated by asynchronous clock because the AK4678 has four SRCs.

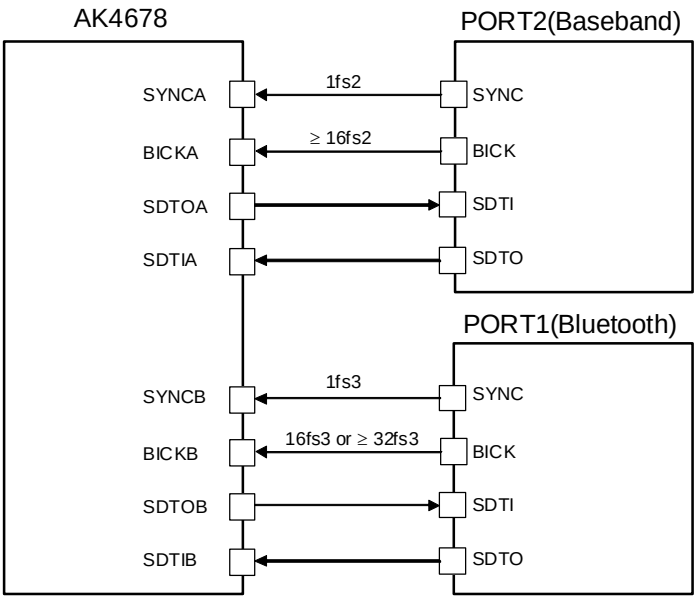

Figure 17. PCM I/F A and B

(a) All interface signals including master clock are fed externally
When supplying a clock to PCM I/F A, PORT2(Baseband) is used. And PORT1(Bluetooth) is used, When supplying a clock to PCM I/F B.
Nothing should be connected to PORT3(DSP), PORT5(DIR) and PORT6(DIT).

SYNCA, BICKA and SDTIA are supplied from PORT2, SDTOA outputs from PORT2.
SYNCB, BICKB and SDTIB are supplied from PORT1, SDTOB outputs from PORT1.

[3] Jumper Pin and SW Setting

1). Other Jumper pins Setup

[JP1 (TVDD_SEL)] : The selection of TVDD.
3.3V : TVDD is supplied 3.3V.
1.8V : TVDD is supplied 1.8V.

[JP2 (Stereo_SEL)] : The selection of output signal to J1(Mini Jack) connector.
Short : Differential Output
Open : Stereo Output

[JP3 (MPWR1 SEL)]: The selection of Mic-power1.
SHORT : MIC-power1 is supplied.
OPEN : MIC-power1 is not supplied. (Default)

[JP4 (MPWR2 SEL)]: The selection of Mic-power2.
SHORT : MIC-power2 is supplied.
OPEN : MIC-power2 is not supplied. (Default)

[JP5 (RIN_SEL)]: The selection of input signal from J3(Mini Jack) connector to AK4678 (RIN ch).
RIN1 : Connect to RIN1/IN1- pin. (Default)
RIN2 : Connect to RIN2/IN2- pin.
RIN3 : Connect to RIN3/IN3- pin.
RIN4 : Connect to RIN4/IN4- pin.

[JP6 (LIN_SEL)]: The selection of input signal from J3(Mini Jack) connector to AK4678 (LIN ch).
LIN1 : Connect to LIN1/IN1+ pin. (Default)
LIN2 : Connect to LIN2/IN2+ pin.
LIN3 : Connect to LIN3/IN3+ pin.
LIN4 : Connect to LIN4/IN4+ pin.

2). SW Setting

Upper-side is “ON(H)” and lower-side is “OFF(L)”.

[S1] (SW DIP-4): AK4118A setting

No.	Name	ON (“H”)	OFF (“L”)	Default
1	DIF2	AK4118A Audio Format Setting See Table 3		ON
2	DIF1			OFF
3	DIF0			OFF
4	OCKS1	AK4118A Master Clock Setting : See Table 4		OFF

Table 2. Mode Setting for AK4678 and AK4118A

DIF2	DIF1	DIF0	DAUX	SDTO	LRCK		BICK		
L	L	L	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
L	L	H	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
L	H	L	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
L	H	H	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
H	L	L	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	Default
H	L	H	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	
H	H	L	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I	
H	H	H	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I	

Table 3. Setting for AK4118A Audio Interface Format

OCKS1	MCKO1	X’tal	
L	256fs	256fs	Default
H	512fs	512fs	

Table 4. Setting for AK4118A Master Clock

■ Board Control

It is possible to control AKD4678-C via general USB port. Connect cable with the U7 (USB Connector) on board and PC.
Control software is packed with this board. The software operation sequence is included in the evaluation board manual.
And it is possible to control AKD4678-C via the printer port (parallel port) of IBM-AT compatible PC.
PORT4(CTRL) with PC by 10 wire flat cable packed with the AKD4678-C.

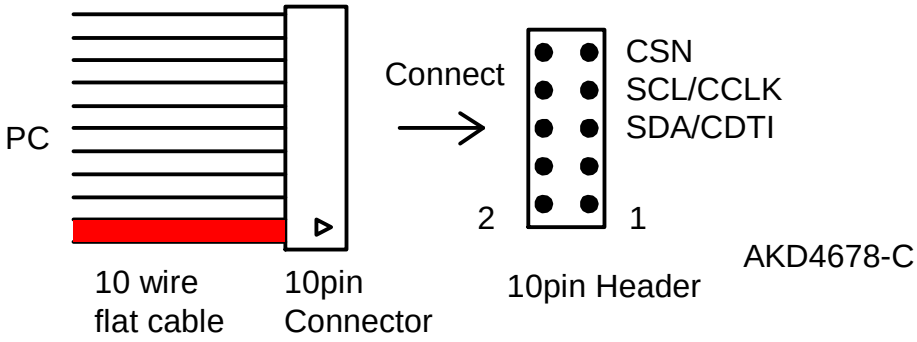

Figure 18. Connection of 10 wire flat cable

■ Analog Input/Output Circuits

(1) Input circuit

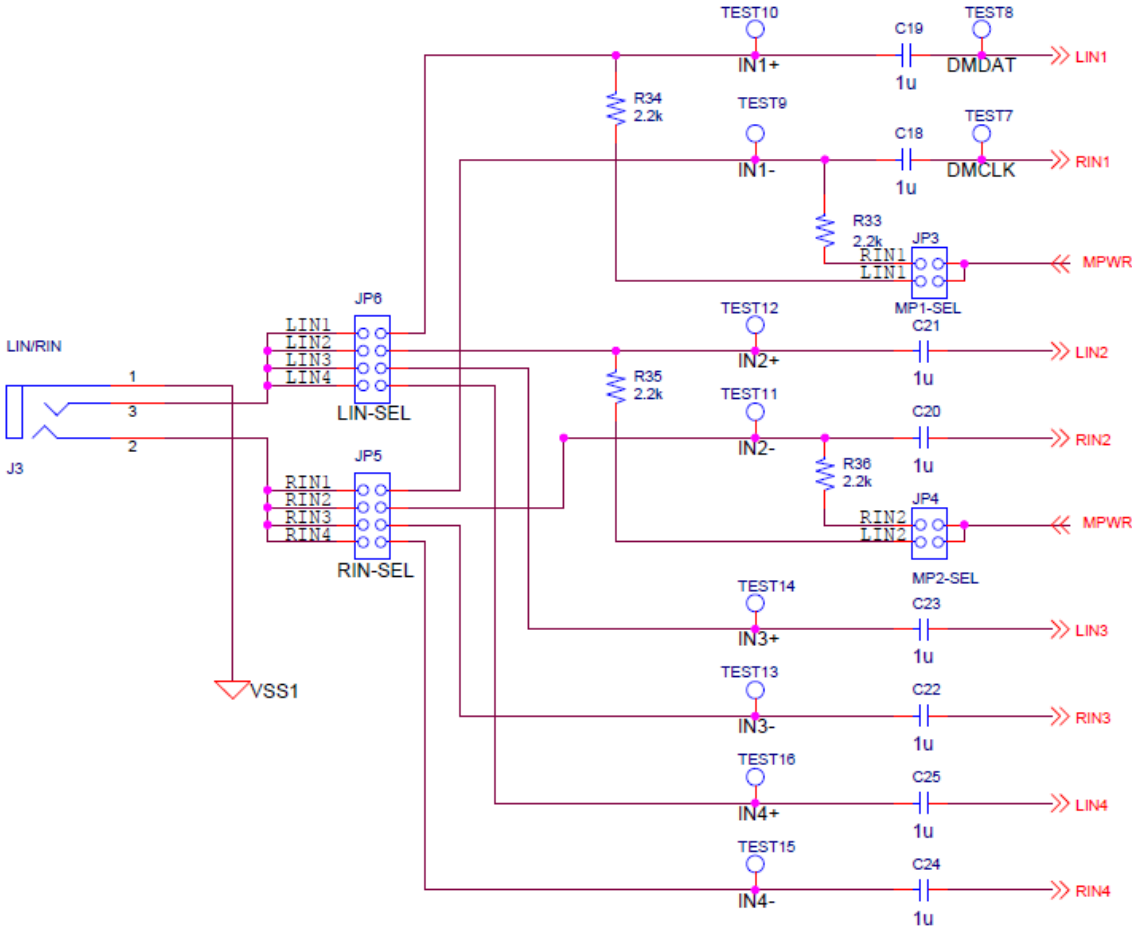

Figure 19. Input Circuit

(2) Output circuit

1. HP Output Circuit

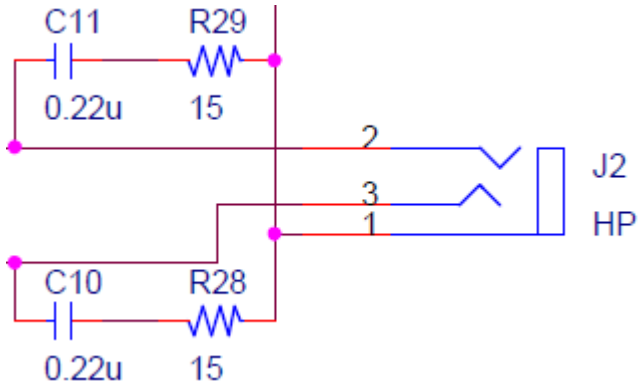

Figure 20 . HP Output Circuit

2. Line Output Circuit

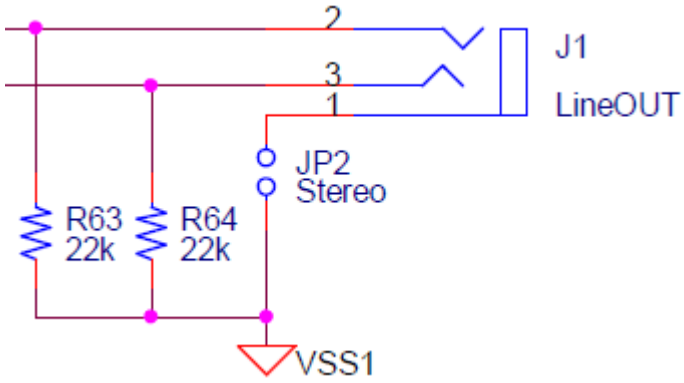

Figure 21 .Line Output Circuit

3. Speaker Output Circuit

Figure 22 . Speaker Output Circuit

4. Receiver Output Circuit

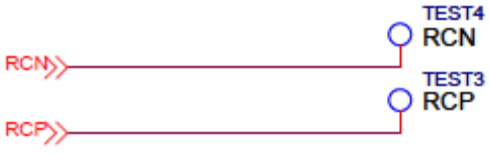

Figure 23. Receiver Output Circuit

Control Soft Manual

■ Evaluation Board and Control Soft Settings

1.Set an evaluation board properly.

2. Connect Evaluation board to PC with USB cable.
USB control is recognized as HID (Human Interface Device) on the PC.
When it can not be recognized correctly please Connect Evaluation board to PC with USB cable.

3. Proceed evaluation by following the process below.

4. Start up the control program following the process above.

Note 1. After the evaluation board's power is supplied, the AK4678 must be reset once bring SW1 (PDN) "L" to "H", and Click [Dummy Command] button.

5. The operation screen is shown below.

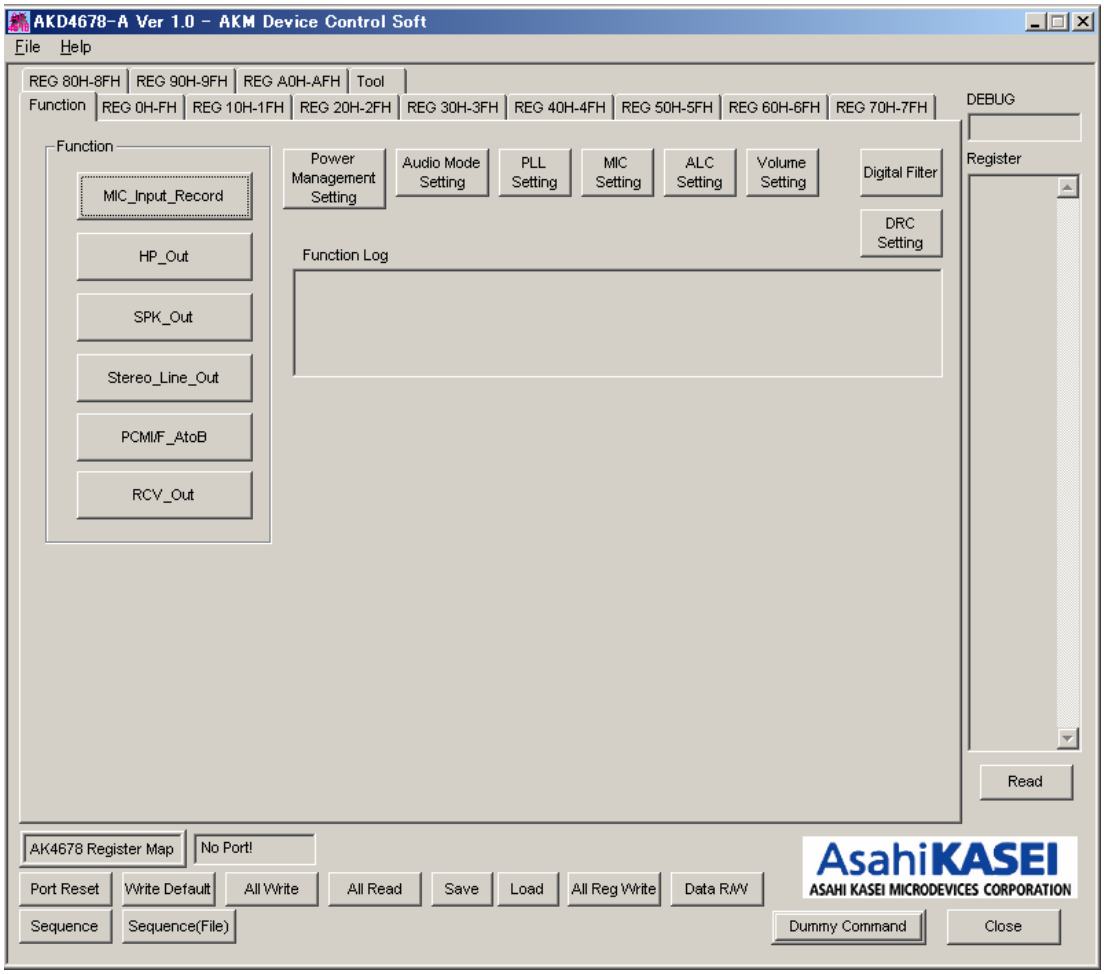

Figure 24. Window of Control Soft

■ Function Button

[MIC_Input_Record]

When [MIC_Input_Record] button is clicked,
[LIN2/RIN2 → MICL/R → ADCL/R → ALC → Audio I/F → SDTO] sequence is set up.
Set up the evaluation board is referred to (2-1) External Slave Mode (a) Evaluation of A/D using DIT of AK4118A. or (d) All interface signals including master clock are fed externally.

[HP_Out]

When [HP_Out] button is clicked,
[SDTI → Audio I/F → 5-band EQ → DATT-A → DACL/R → HPL/HPR] sequence is set up.
Set up the evaluation board is referred to (2-1) External Slave Mode (b) Evaluation of D/A using DIR of AK4118A. or (d) All interface signals including master clock are fed externally.

[SPK_Out]

When [SPK_Out] button is clicked,
[SDTI → Audio I/F → 5-band EQ → DATT-A → DACL/R → SPP/SPN] sequence is set up.
Set up the evaluation board is referred to (2-1) External Slave Mode (b) Evaluation of D/A using DIR of AK4118A. or (d) All interface signals including master clock are fed externally.

[Stereo_Line_Out]

When [Stereo_Line_Out] button is clicked,
[SDTI → Audio I/F → 5-band EQ → DATT-A → DACL/R → LOUT/ROUT] sequence is set up.
Set up the evaluation board is referred to (2-1) External Slave Mode (b) Evaluation of D/A using DIR of AK4118A. or (d) All interface signals including master clock are fed externally.

[PCMIF_AtoB]

When [PCMIF_AtoB] button is clicked,
[SDTIA→PCM I/F A→SRCAI→DATT-C→MIX3→PCM I/F B→SDTOB &
SDTIB→PCM I/F B→BIVOL→MIX2A→MIX2C→SRCAO→PCM I/F A→SDTOA] sequence is set up.
Set up the evaluation board is referred to
(2-5) PCM I/F A&B (a) All interface signals including master clock are fed externally.

[RCV_Out]

When [RCV_Out] button is clicked,
[SDTIA→PCM I/F A→SRCAI→DATT-B→MIX1R→5-Band EQ→DATT-A→DACR→RCP/RCN]
sequence is set up.
Set up the evaluation board is referred to
(2-5) PCM I/F A&B (a) All interface signals including master clock are fed externally.

■Operation Overview

CODEC Function

Function, register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the Dialog Boxes for details of each dialog box setting.

1. [Port Reset]: For when connecting to USB Cable.
   Click this button after the control soft starts up when connecting USB I/F.

2. [Write Default]: Register Initializing
   When the device is reset by a hardware reset, use this button to initialize the registers.

3. [All Write]: Executing write commands for all registers displayed.

4. [All Read]: Executing read commands for all registers displayed.

5. [Save]: Saving current register settings to a file.

6. [Load]: Executing data write from a saved file.

7. [All Reg Write]: “All Reg Write” dialog box is popped up.

8. [Data R/W]: “Data R/W” dialog box is popped up.

9. [Sequence]: “Sequence” dialog box is popped up.

10. [Sequence(File)]: “Sequence(File)” dialog box is popped up.

11. [Read]: Reading current register settings and display on to the Register area on the right of the main window.
    This is different from [All Read] button, it does not reflect to a register map, only displaying hexadecimal.

12. [Dummy Command]: Write a dummy command
    After the evaluation board power is supplied, the AK4678 must be reset once bring SW1 (PDN) “L” to “H”, and then the [Dummy Command] button should be clicked once to reset the register setting of the AK4678.

1. [Function]: Function control

This tab is for function control.
Each operation is executed by the function buttons on the left side of the screen.

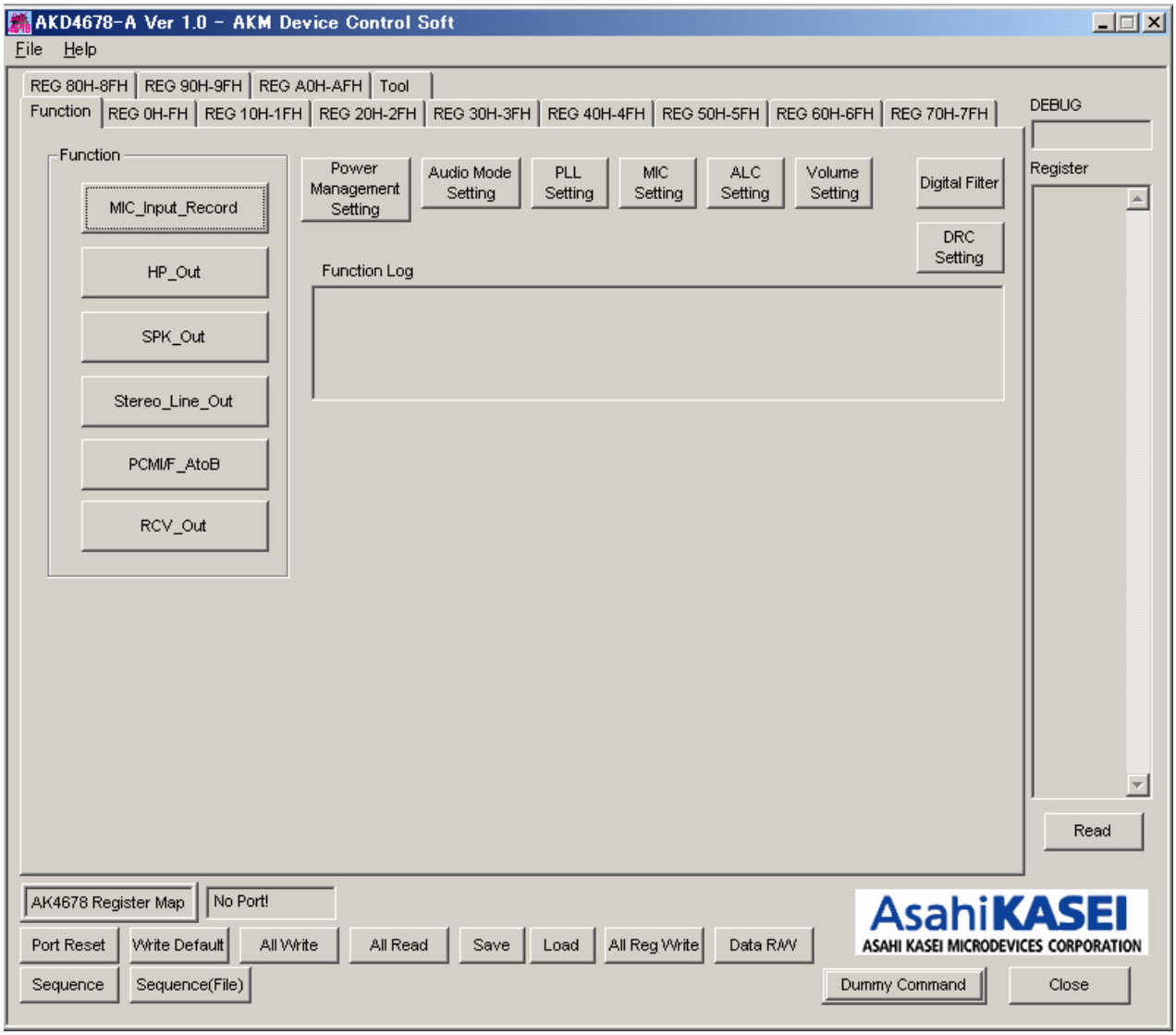

Figure 25. Window of [Function]

1-1. Power Management Setting

When [Power Management Setting] button is clicked, the window as shown in Figure 26 opens.
This window is for Power Management Setting.
Refer to the datasheet for register settings of the AK4678.

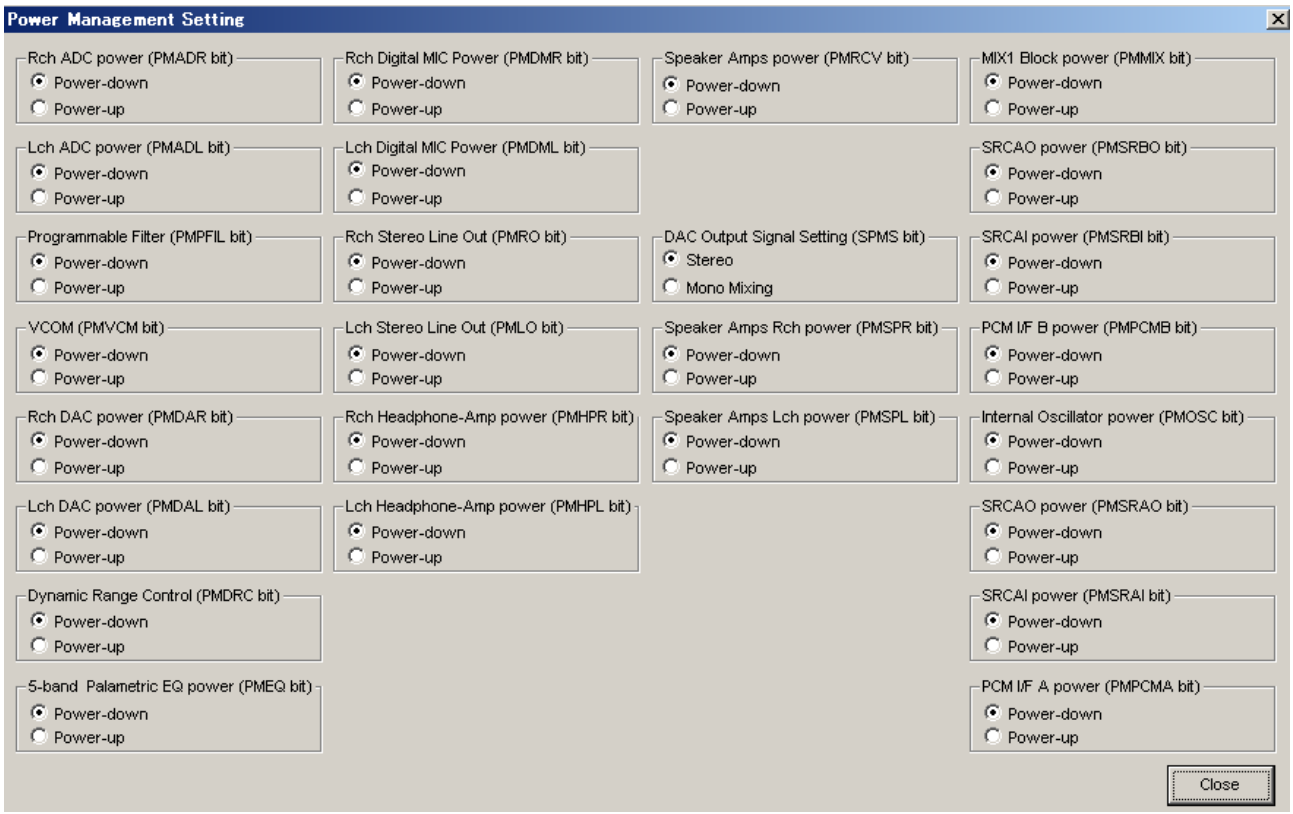

Figure 26. Window of [Power Management Setting]

1-2. Audio Mode Setting

When [Audio Mode] button is clicked, the window as shown in Figure 27 opens.
This window is for Audio Mode Setting.
Refer to the datasheet for register settings of the AK4678.

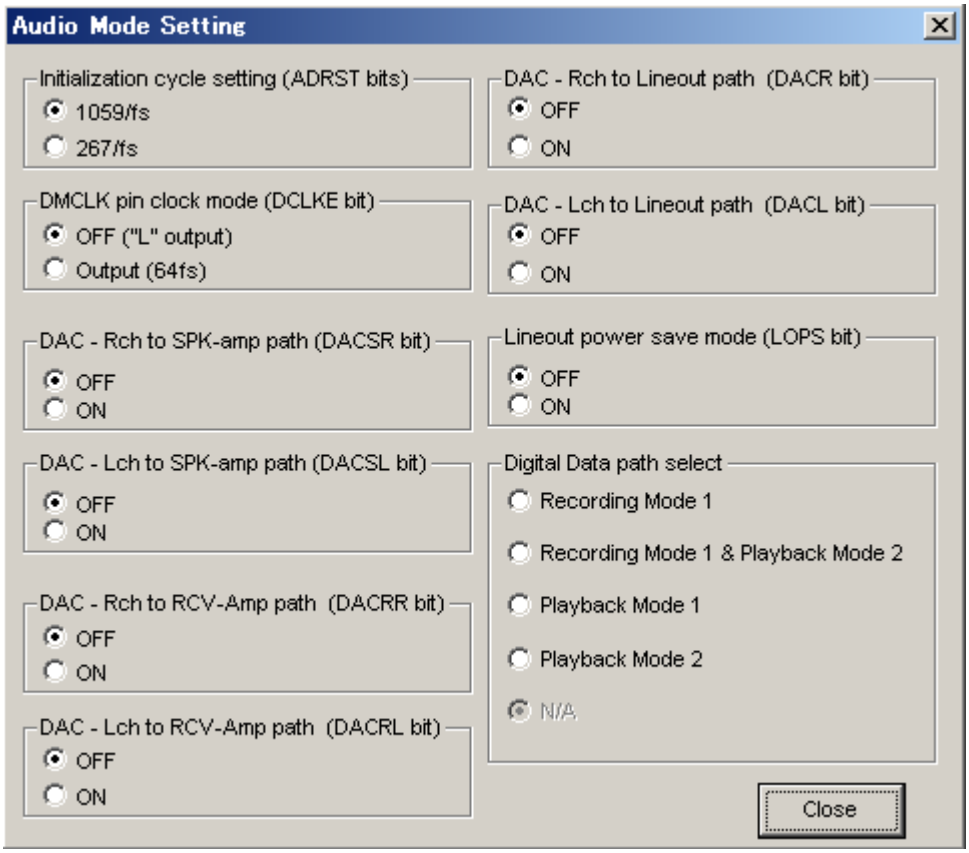

Figure 27. Window of [Audio Mode Setting]

1-3. System Clock, Audio I/F Setting

When [PLL Setting] button is clicked, the window as shown in Figure 28 opens.
This window is for System Clock and Audio I/F Setting
Refer to the datasheet for register settings of the AK4678.

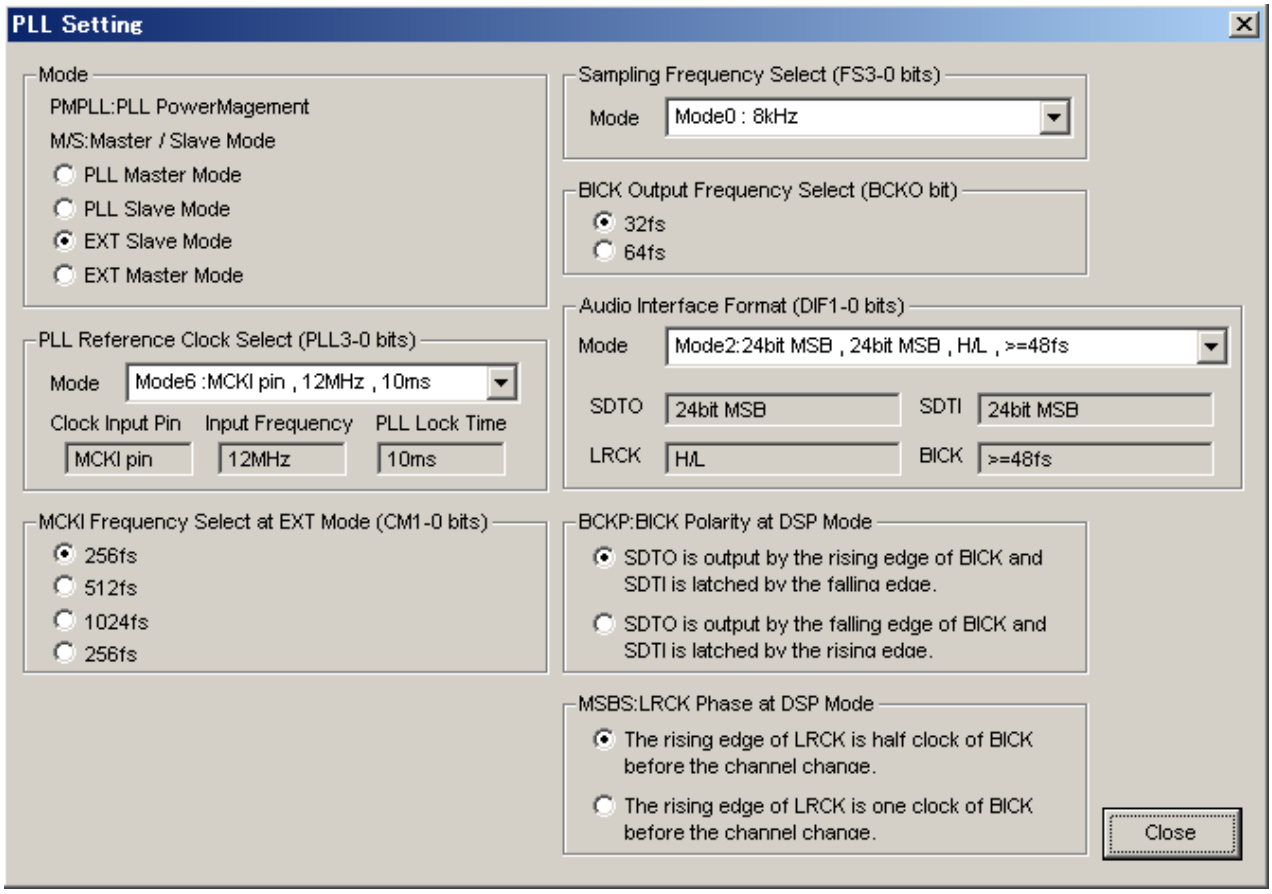

Figure 28. Window of [PLL Setting]

1-4. MIC Setting

When [MIC Setting] button is clicked, the window as shown in Figure 29 opens.
This window is for MIC Setting.
Refer to the datasheet for register settings of the AK4678.

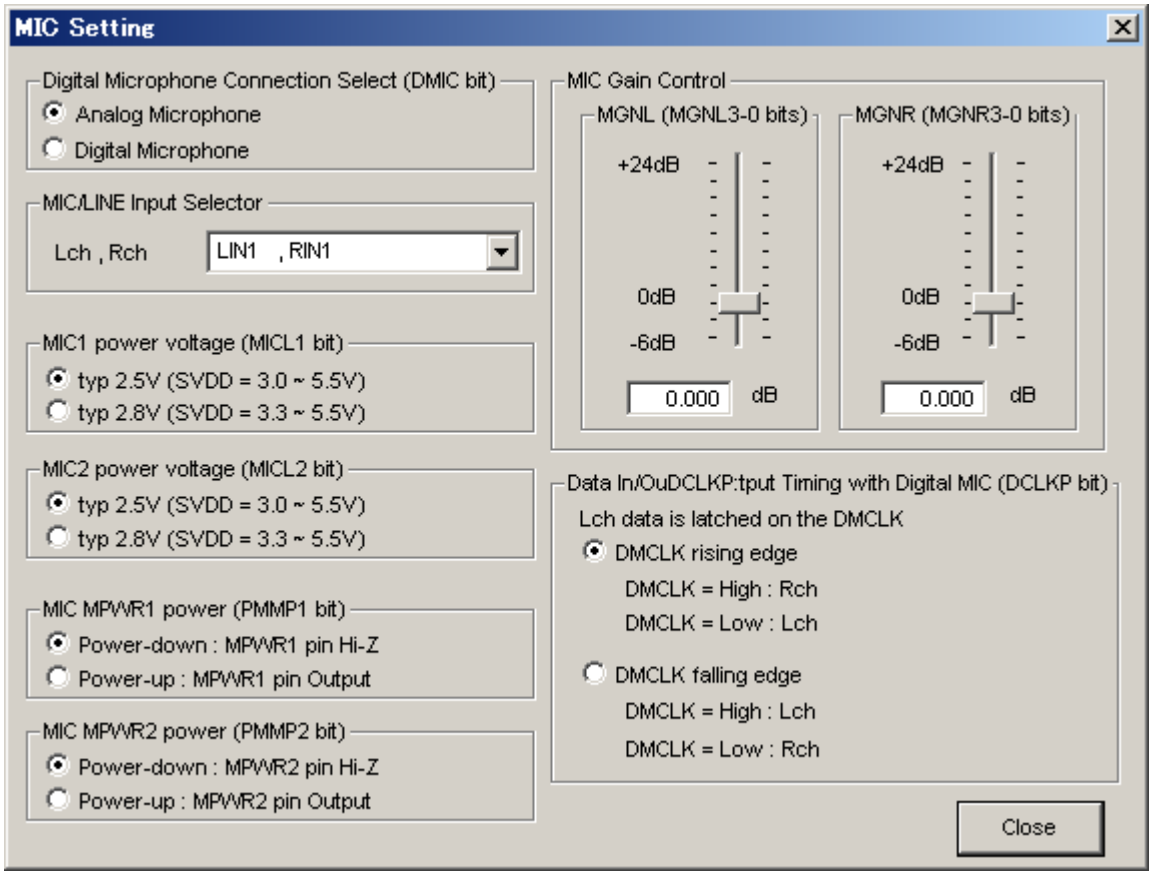

Figure 29. Window of [MIC Setting]

1-5. ALC Setting

When [ALC Setting] button is clicked, the window as shown in Figure 30 opens.
This window is for ALC setting.
Refer to the datasheet for register settings of the AK4678.

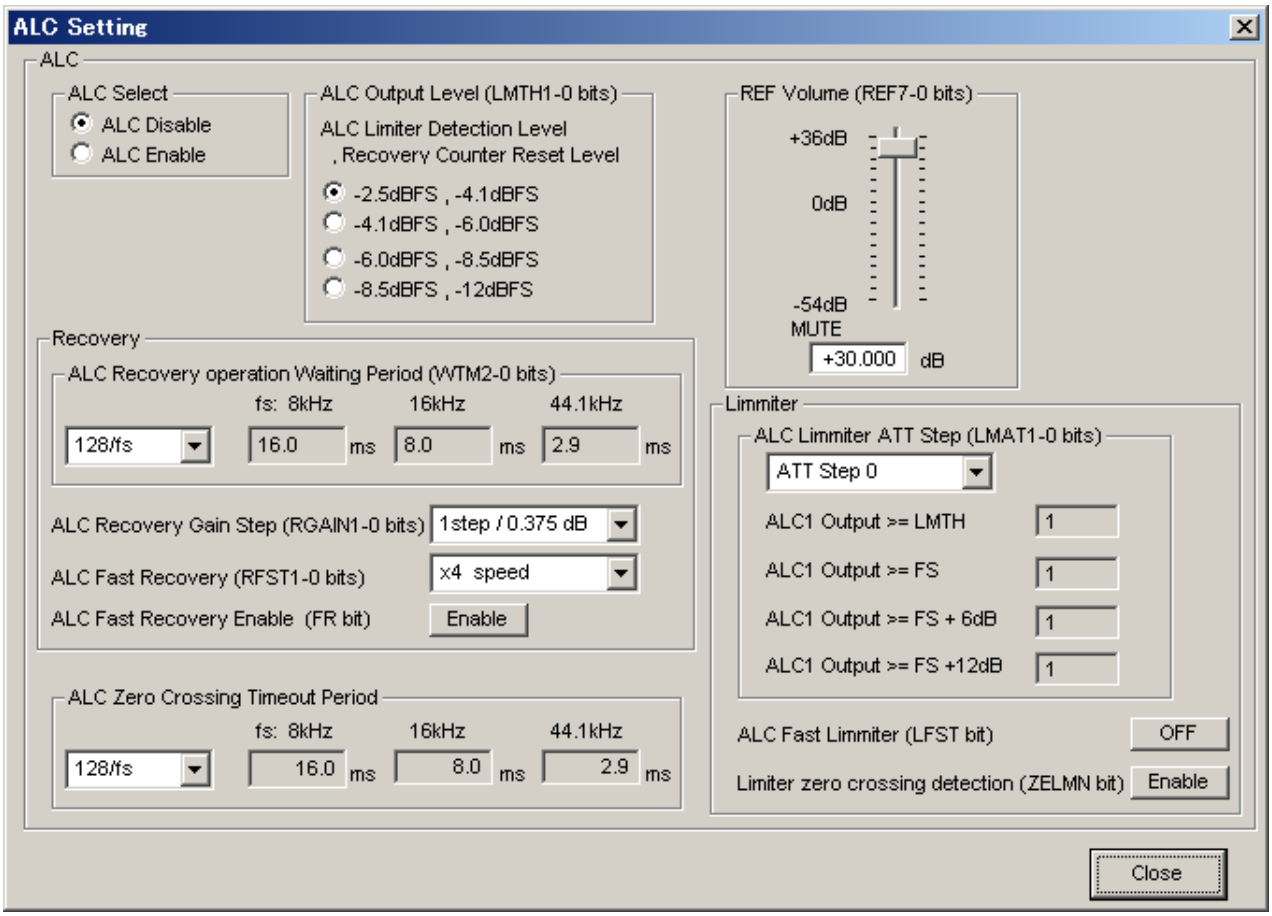

Figure 30. Window of [ALC Setting]

1-6. Volume Setting

When [Volume Setting] button is clicked, the window as shown in Figure 31 opens.
This window is for Volume setting.
Refer to the datasheet for register settings of the AK4678.

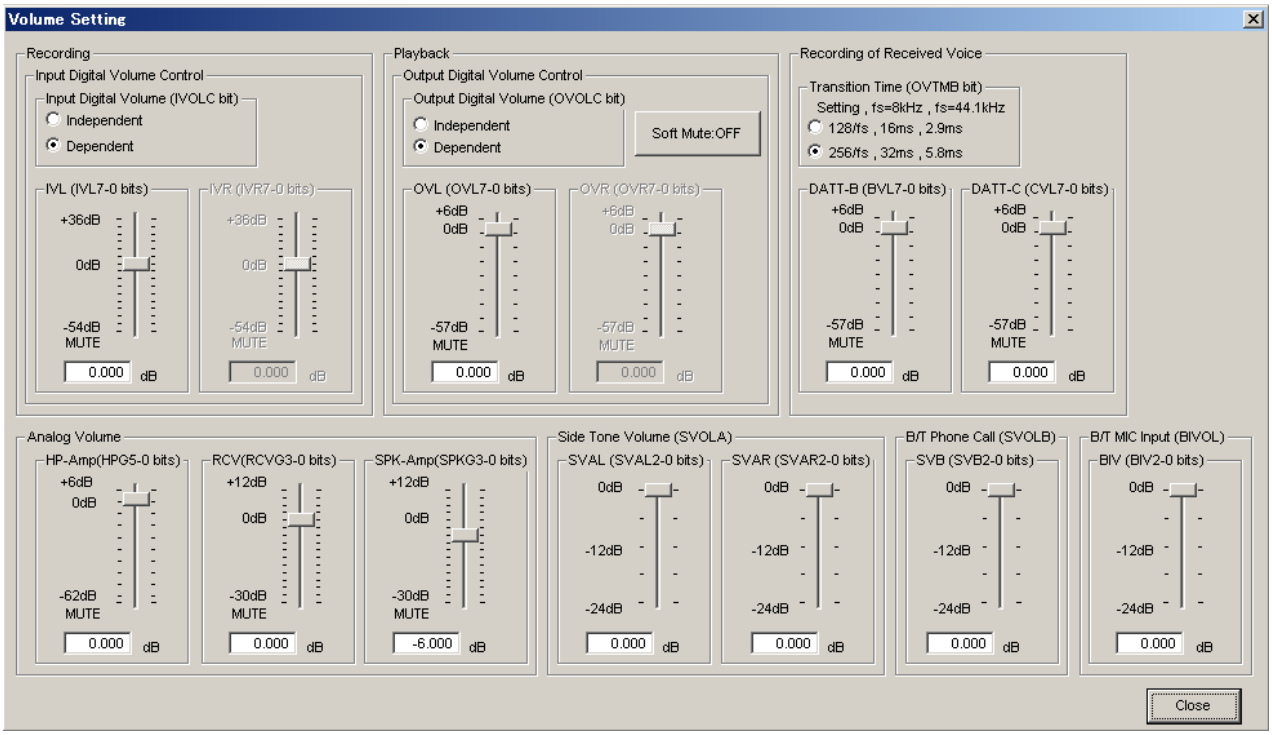

Figure 31. Window of [Volume Setting]

Register map

10H	RCVG3	RCVG2	RCVG1	RCVG0	SPKG3	SPKG2	SPKG1	SPKG0
11H	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
12H	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0

Volume Control by Pull-down Menu

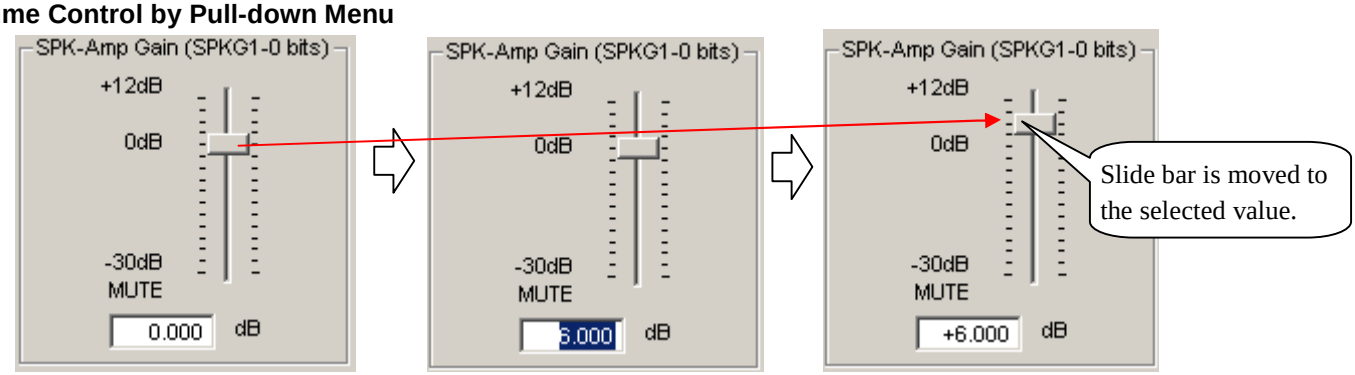

Figure 32. Volume Control by Pull

The volume can be controlled by slide bars.
Register writing is made on every slide bar move.

After the volume slide is moved, it is reflected on to the register map and data writing dialog box.

The volume can also be changed by writing a value in a dialog box. The slide bar is moved to the value that written in the dialog box. Use the mouse or arrow keys on the keyboard for small adjustments.

1-7. Digital Filter Setting

When [Digital Filter Setting] button is clicked, the window as shown in Figure 33 opens.
Refer to the datasheet for register settings of the AK4679A.
A calculation of a coefficient of Digital Programmable Filters such as HPF / LPF and EQ filters, a register writing and a frequency response checking of HPF / LPF and EQ filter can be made.

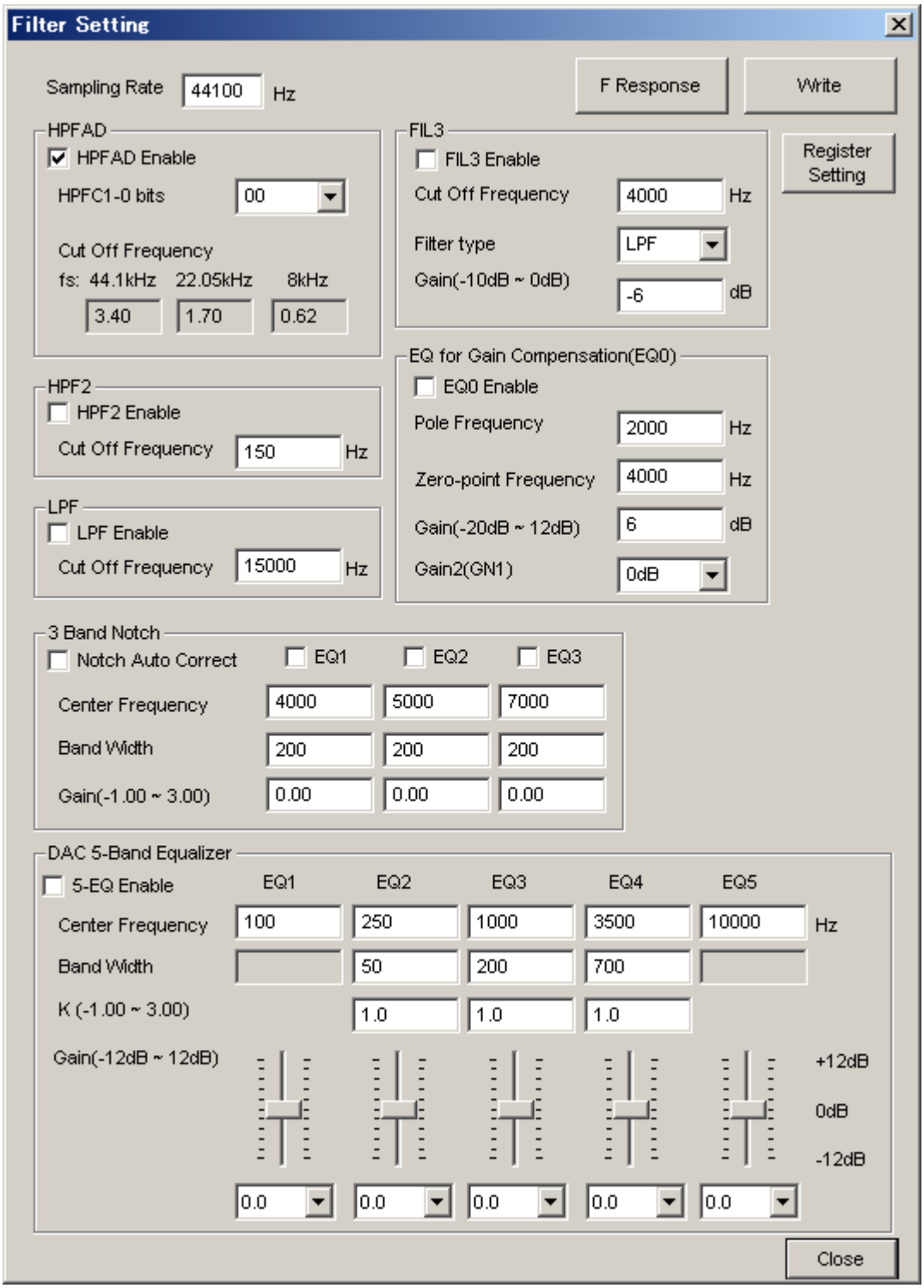

Figure 33. Window of [Digital Filter Setting]

1-7-1. Parameter Setting

(1) Please set a parameter of each Filter.

Parameter	Function	Setting Range
Sampling Rate	Sampling frequency (fs)	7350Hz ≤ fs ≤ 48000Hz
HPF		
Cut Off Frequency	High pass filter cut off frequency	fs/1000 ≤ Cut Off Frequency ≤ (0.497 * fs)
HPF2		
Cut Off Frequency	Low pass filter cut off frequency	fs/1000 ≤ Cut Off Frequency ≤ (0.497 * fs)
FIL3		
Cut Off Frequency	FIL3 cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Gain	Gain	-10≤ Gain < 0
EQ for Gain Compensation(EQ0)		
Pole Frequency	EQ0 Pole Frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Zero-point Frequency	EQ0 Zero-point Frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Gain	Gain	-20≤ Gain < 12
3 Band Equalizer		
EQ1-3 Center Frequency	EQ1-3 Center Frequency	0Hz ≤ Center Frequency < (0.497 * fs)
EQ1-3 Band Width	EQ1-3 Band Width (Note 2)	1Hz ≤ Band Width < (0.497 * fs)
EQ1-3 Gain	EQ1-3 Gain (Note 3)	-1≤ Gain < 3
DAC 5-Band Equalizer		
Center Frequency	LPF1 EQ1-5 HPF1 Center Frequency	fs/1000 ≤ Cut Off Frequency < (0.497 * fs)
Band Width	EQ2-4 Band Width	1Hz ≤ Band Width < (0.497 * fs)
Gain	LPF1 EQ1-5 HPF1 Gain	-12 ≤ Gain ≤ 12

Note 2. Gain difference is a bandwidth of 3dB from center frequency.
Note 3. When the gain is smaller than 0, EQ becomes a notch filter.

(2) “HPFAD Enable”, “HPF Enable” , “LPF Enable” “FIL3 Enable”, “EQ0 Enable”, “EQ1”, “EQ2”, “EQ3”.
Please set ON/OFF of Filter with a check button. When checked it, Filter becomes ON. When “Notch Filter Auto Correction” is checked, perform automatic correction of the center frequency of the notch filter is executed.

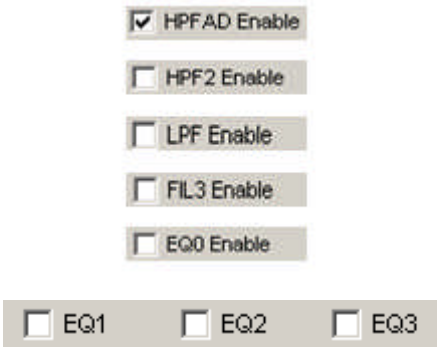

Figure 34. Filter ON/OFF setting button

1-7-2. Calculation of Register

Register set value is displayed when push a [Register Setting] button. When a value out of a setting range is set, error message is displayed, and a calculation of register setting is not carried out.

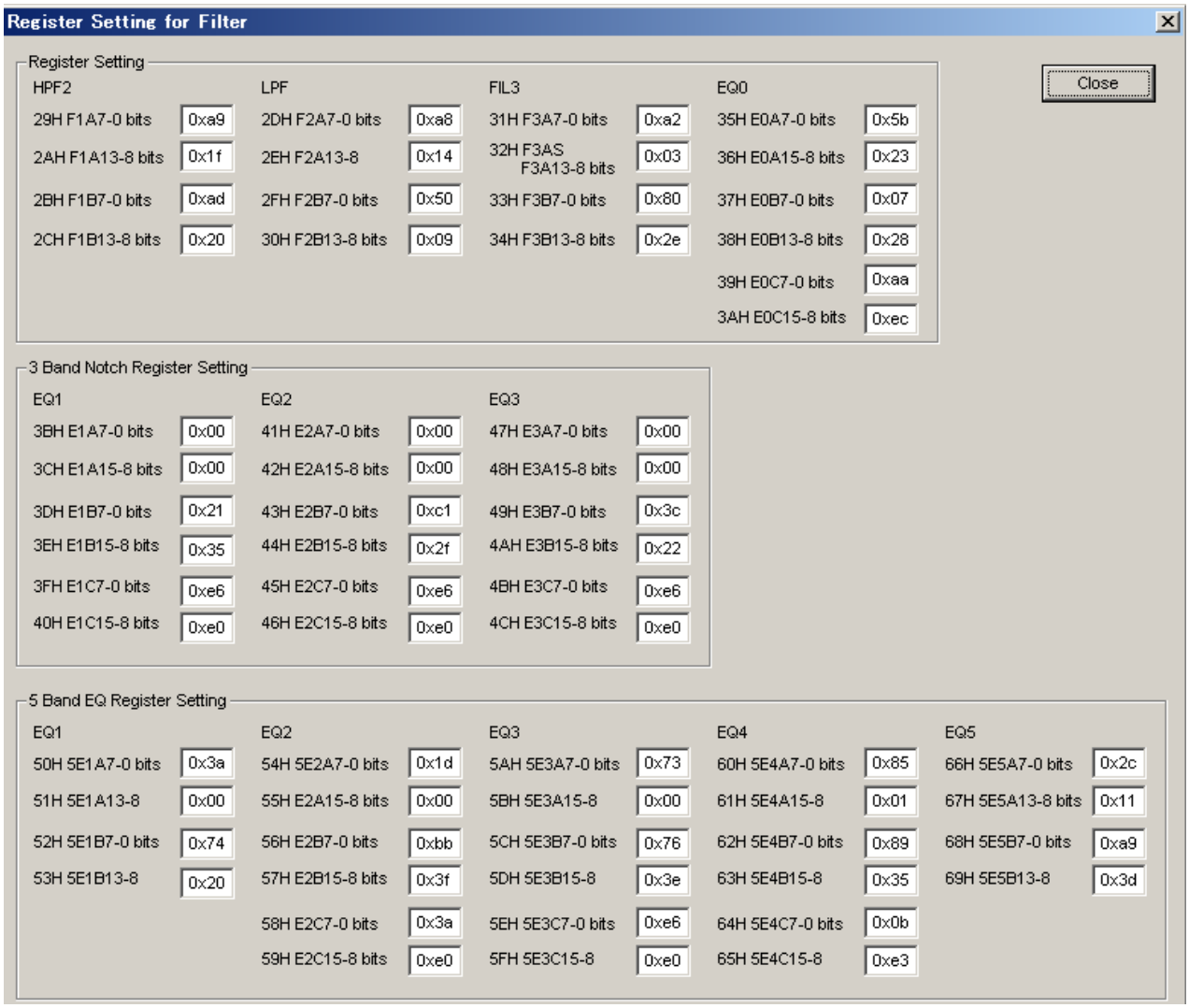

Figure 35. Register setting calculation result

Followings are the cases when a register set value is updated.
(1) When [Register Setting] button was pushed.
(2) When [Frequency Response] button was pushed.
(3) When [UpDate] button was pushed on a frequency characteristic indication window.
(4) When set ON/OFF of a check button “Notch Filter Auto Correction”

1-7-3. Indication of Frequency Characteristic

Frequency characteristic is displayed when push a [F Response] button. Then, a register set point is also updated.
Change “Frequency Range”, and indication of a frequency characteristic is updated when push a [UpDate] button.

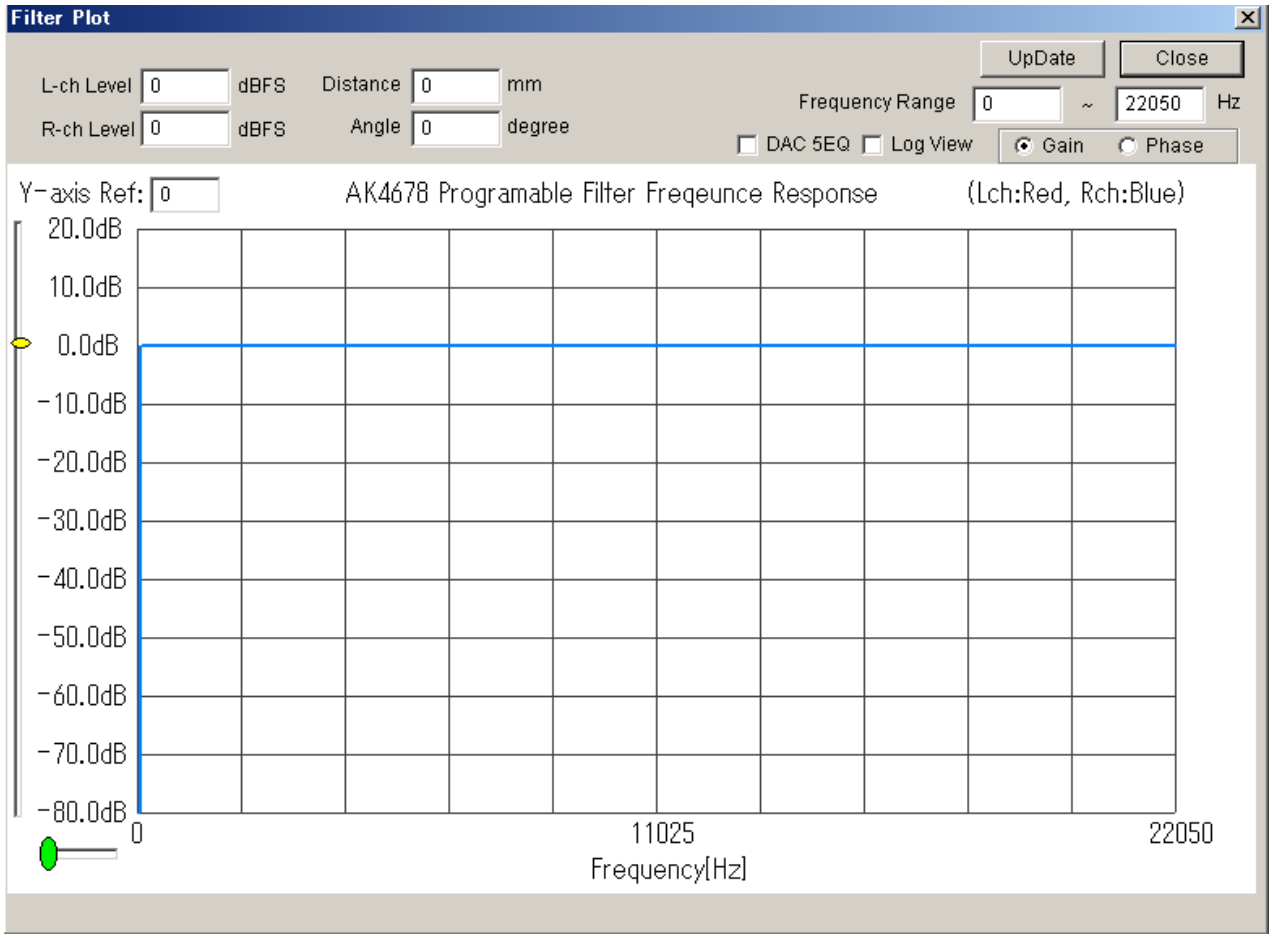

Figure 36. Frequency Characteristic Indication Result

1-7-4. Filter Setting

(a) 3-band Equalizer, DAC 5-band Equalizer

The filter setting can be executed by dragging the number to each equalizers in the mouse.
Band Width can be adjusted in the operation of Center Frequency, K and Gain right-clicking in the operation of the left-click.

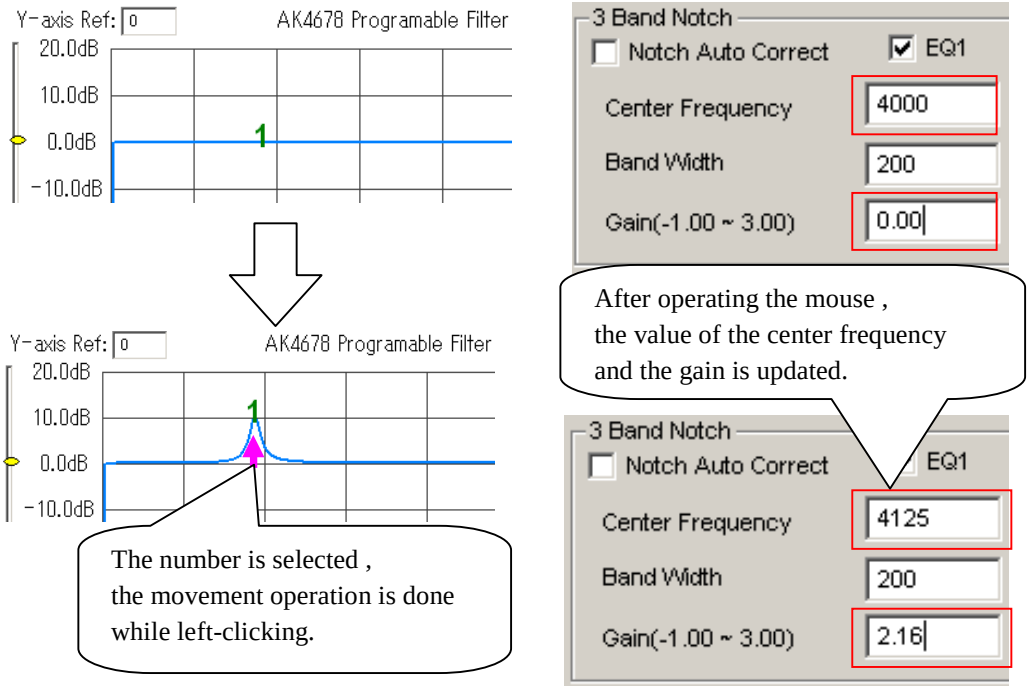

Figure 37. Filter Setting (Right-clicking operation)

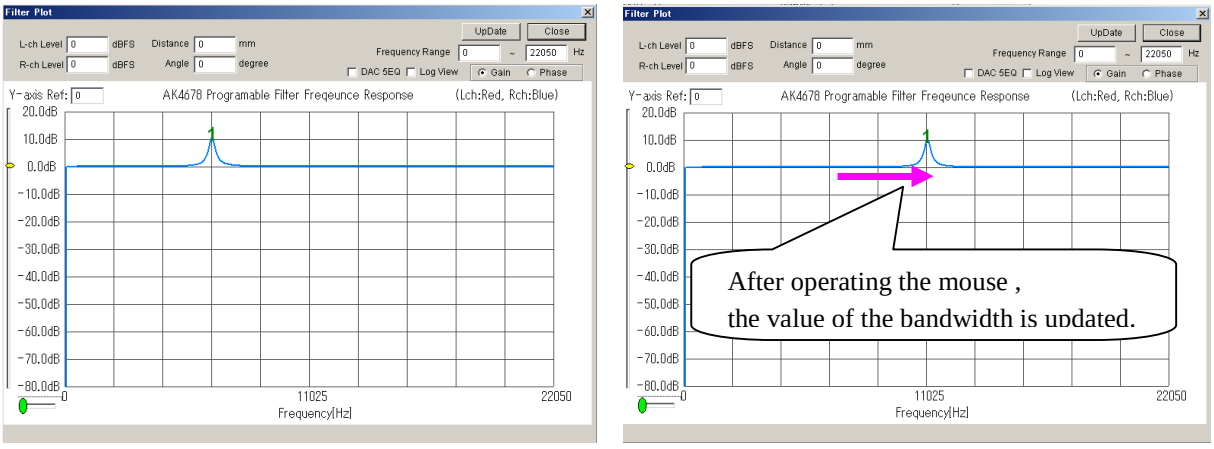

Figure 38. Filter Setting (Left-clicking operation)

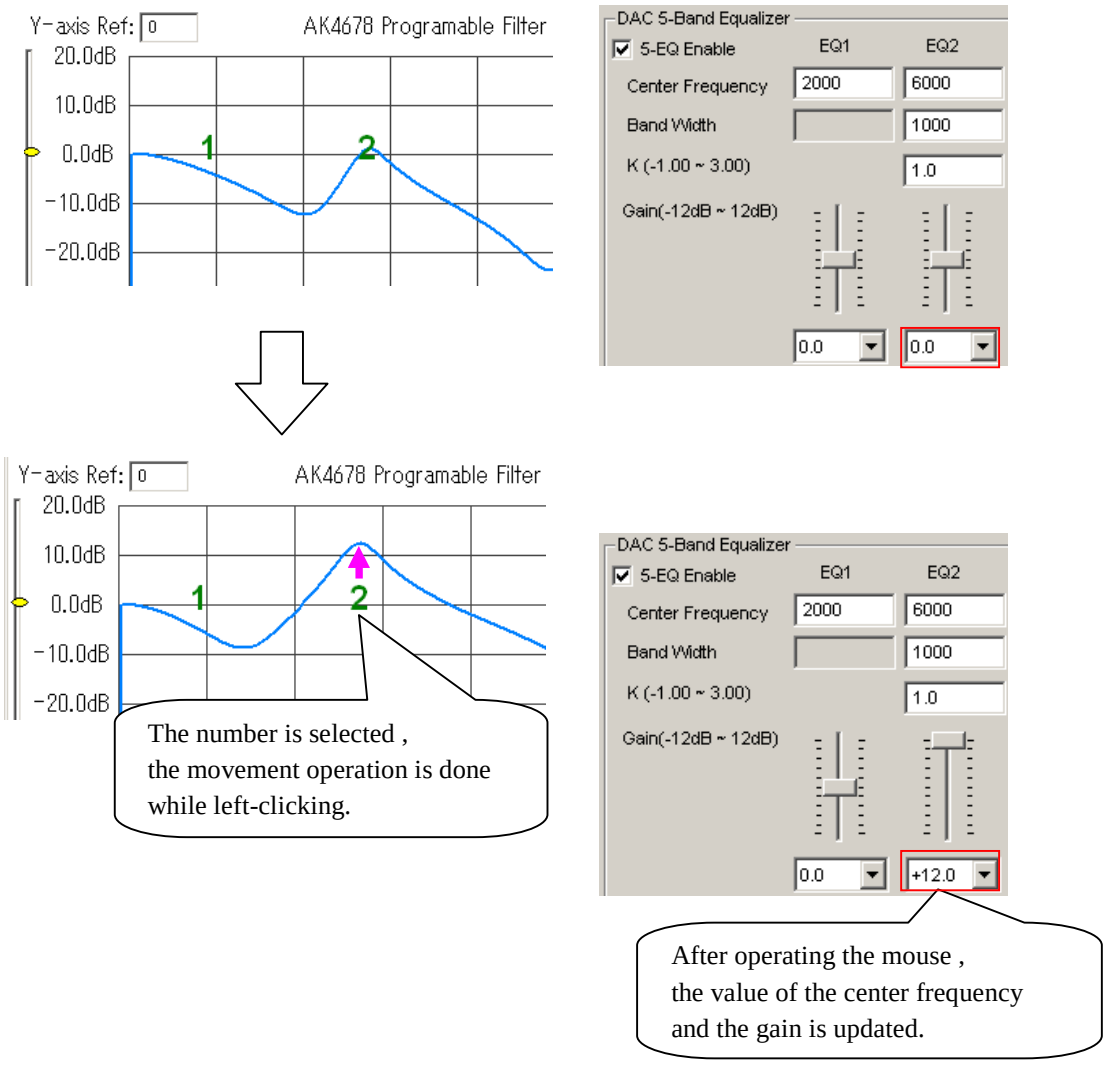

Figure 39. Filter Setting (Gain-Control operation)

1-8. DRC Setting

When [DRC Setting] button is clicked, the window as shown in opens.
This window is for DRC setting.
Refer to the datasheet for register settings of the AK4678.

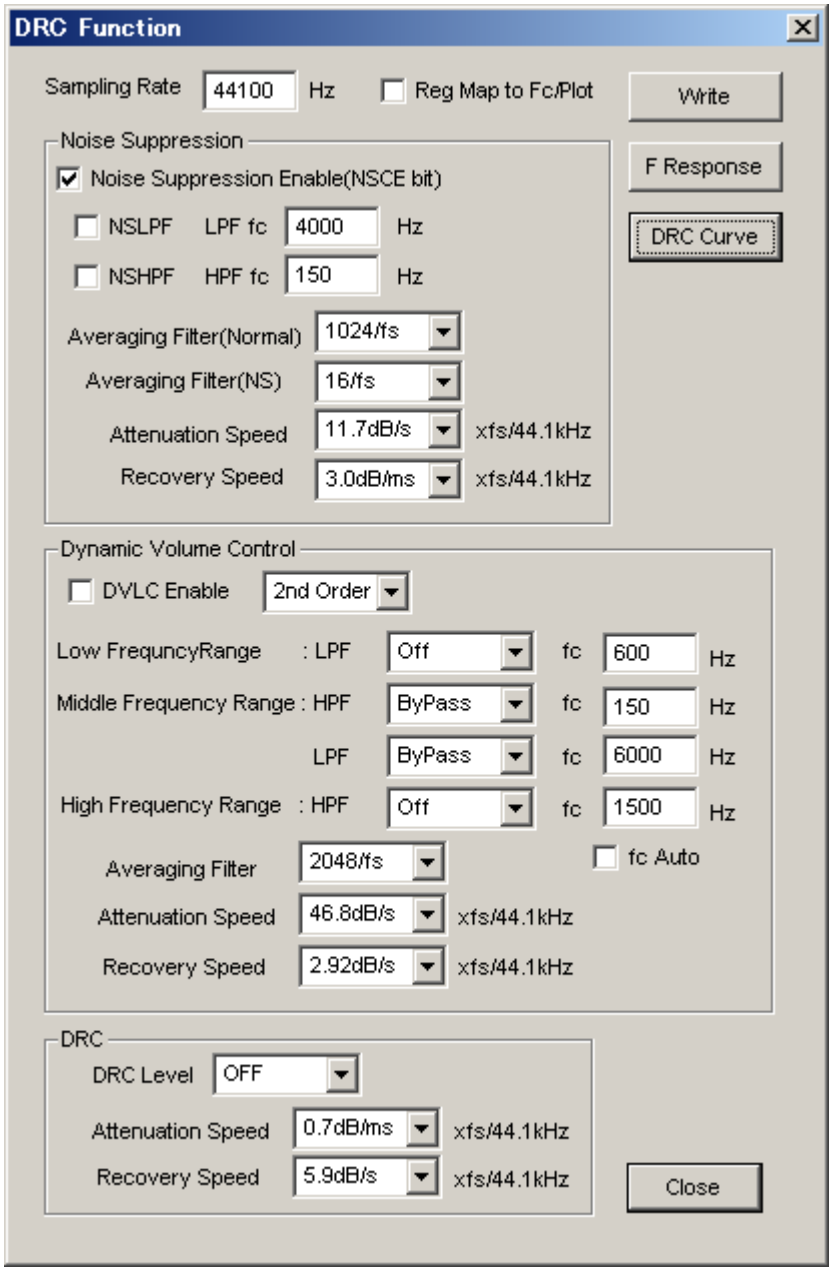

Figure 40. Window of [DRC Setting]

1-8-1. Parameter Setting

(1) Please set a parameter of each Filter and Gain.

Parameter	Function	Setting Range
Sampling Rate	Sampling frequency (fs)	7350Hz ≤ fs ≤ 48000Hz
Noise Suppression		
LPF	Low pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
HPF	High pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Gain	Reference Value Setting	-9 ≤ Gain < -54 (Note 4)
Threshold Level	Noise Suppression Threshold Low/High Level	-82.5≤ Threshold Level < -36.0 (Note 5)
Dynamic Volume Control		
Low Frequency Range		
LPF	Low pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Volume Control	Volume point setting	-70.5≤ Gain < 0 (Note 6)
Middle Frequency Range	Low Frequency Range	
LPF	Low pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
HPF	High pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Volume Control	Volume point setting	-70.5≤ Gain < 0
High Frequency Range		
HPF	High pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Volume Control	Volume point setting	-70.5≤ Gain < 0

Note 4. Gain step of “Reference Value of Noise Suppression” is 3dB.
Note 5. Gain step of “Threshold level Value of Noise Suppression” is 3dB.
Note 6. Gain step of “Volume point Value of Dynamic Volume Control” is 3dB.

(2) When “NSLPF” button is checked, the filter is enabled. When “NSHPF” button is checked, the filter is enabled. When “DVLC Enable” button is checked, the filters of Low/Middle/High Range are enabled according to setting of pull-down menu. When “fc Auto” button is checked, the frequency response of low frequency and high frequency ranges becomes flat automatically.

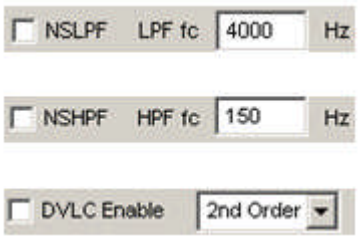

Figure 41. Filter ON/OFF setting button

1-8-2. Frequency Response

Frequency characteristic is displayed when pushing a [F Response] button. Then, a register set point is also updated. When changing “Frequency Range”, frequency characteristic indication window is updated after [UpDate] button is pushed.

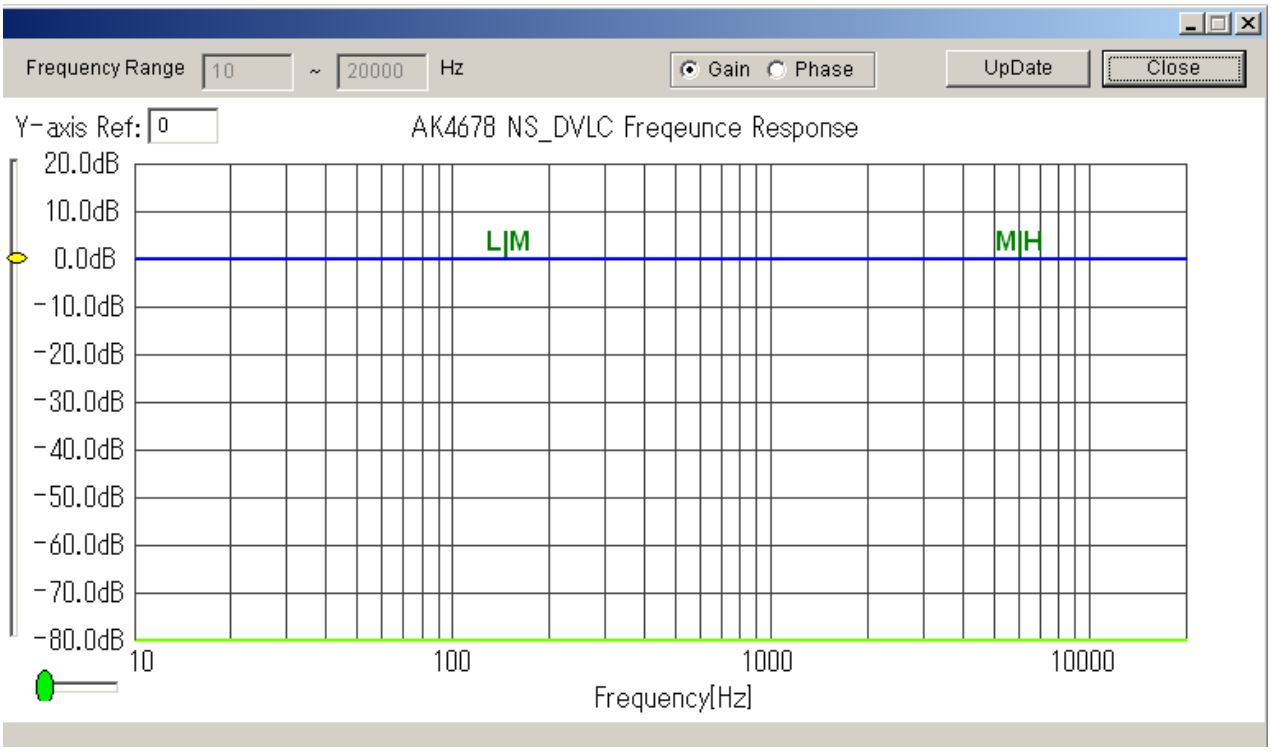

Figure 42. A frequency characteristic indication result

Followings are the cases when a register set value is updated.

(1). When [Register Setting] button was pushed.
(2). When [Frequency Response] button was pushed.
(3). When [UpDate] button was pushed on a frequency characteristic indication window.
(4). When set ON/OFF of a check button “fc Auto”

1-8-3. Filter Setting

The filter setting can be executed by checking the “NSLPF”, “NSHPF” or “DVLC Enable” button.
Band width can be adjusted in the operation of Center Frequency in the operation of the left-click and Filter selecting in the [DRC Setting] window.

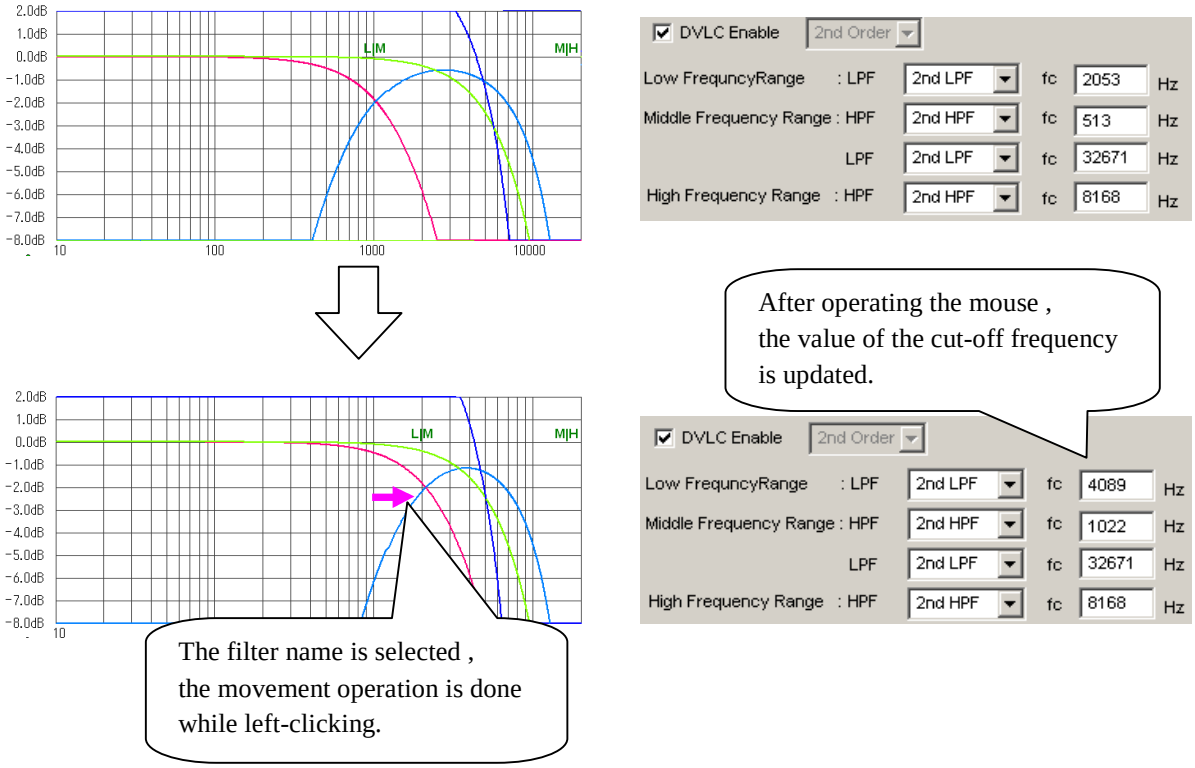

Figure 43. Filter Setting (Left-clicking operation)

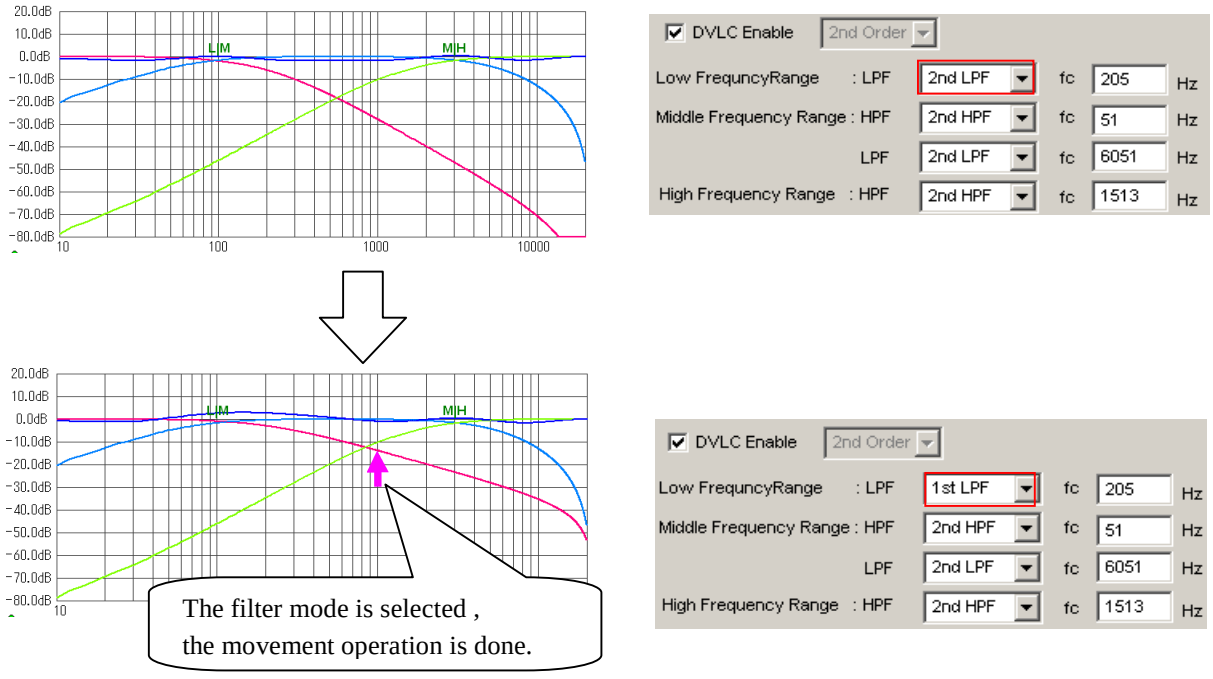

Figure 44. Filter Setting (Filter Selecting)

1-8-4. Noise Suppression

Noise Suppression Control is displayed when “NS” button is checked after [DRV Curve] button is pushed. Then, a register set point is also updated.

Noise Suppression Threshold Low Level and Reference Value can be adjusted by the left-click.

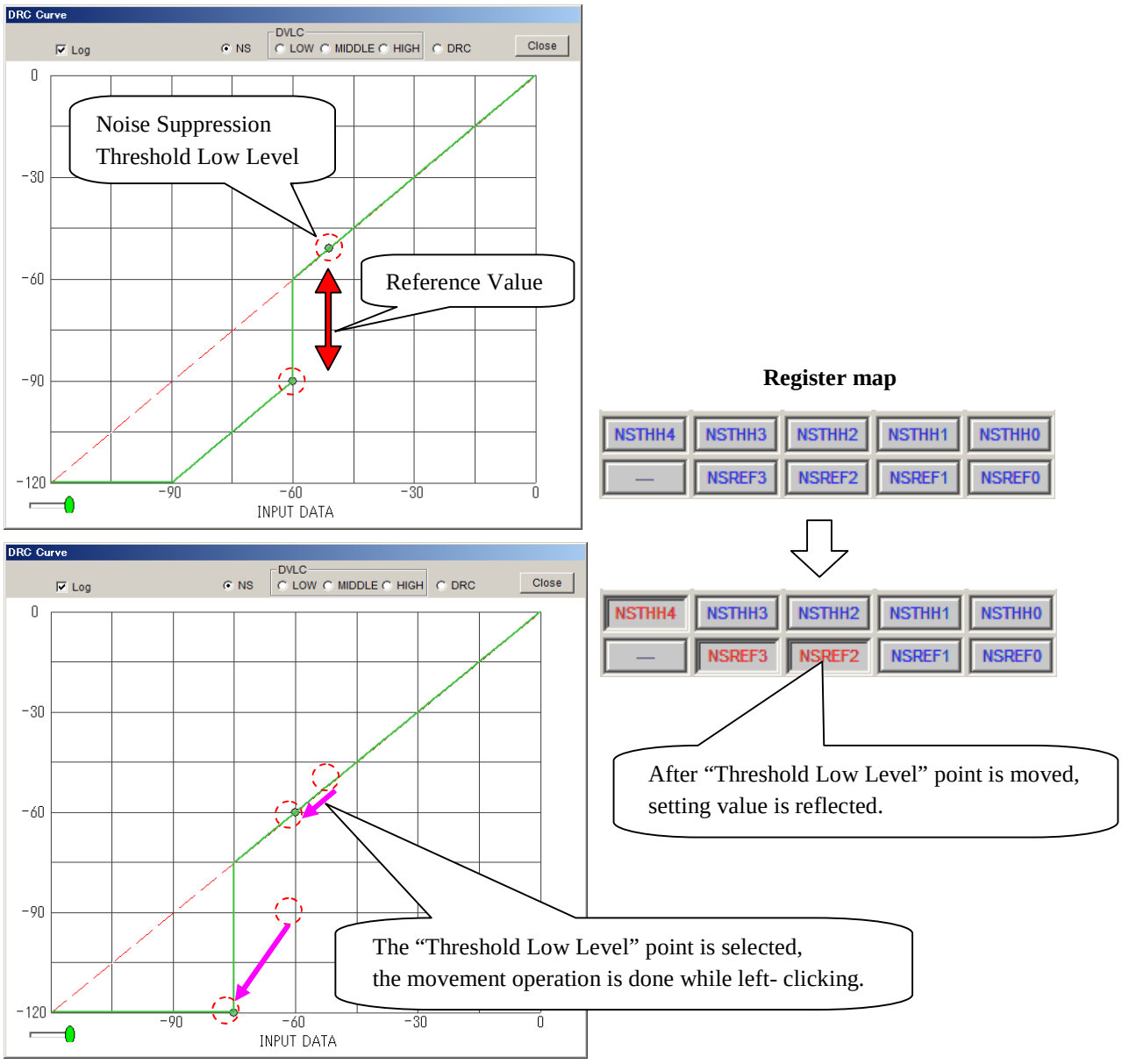

Figure 45. Noise Suppression Setting

1-8-5. Dynamic Volume Control

Dynamic Volume is displayed when “LOW”, ”MIDDLE” or “HIGH” buttons in “DVLC” is checked after [DRV Curve] button is pushed.
Then, a register set point is also updated.

Dynamic Volume Control Points can be adjusted by the left-click.

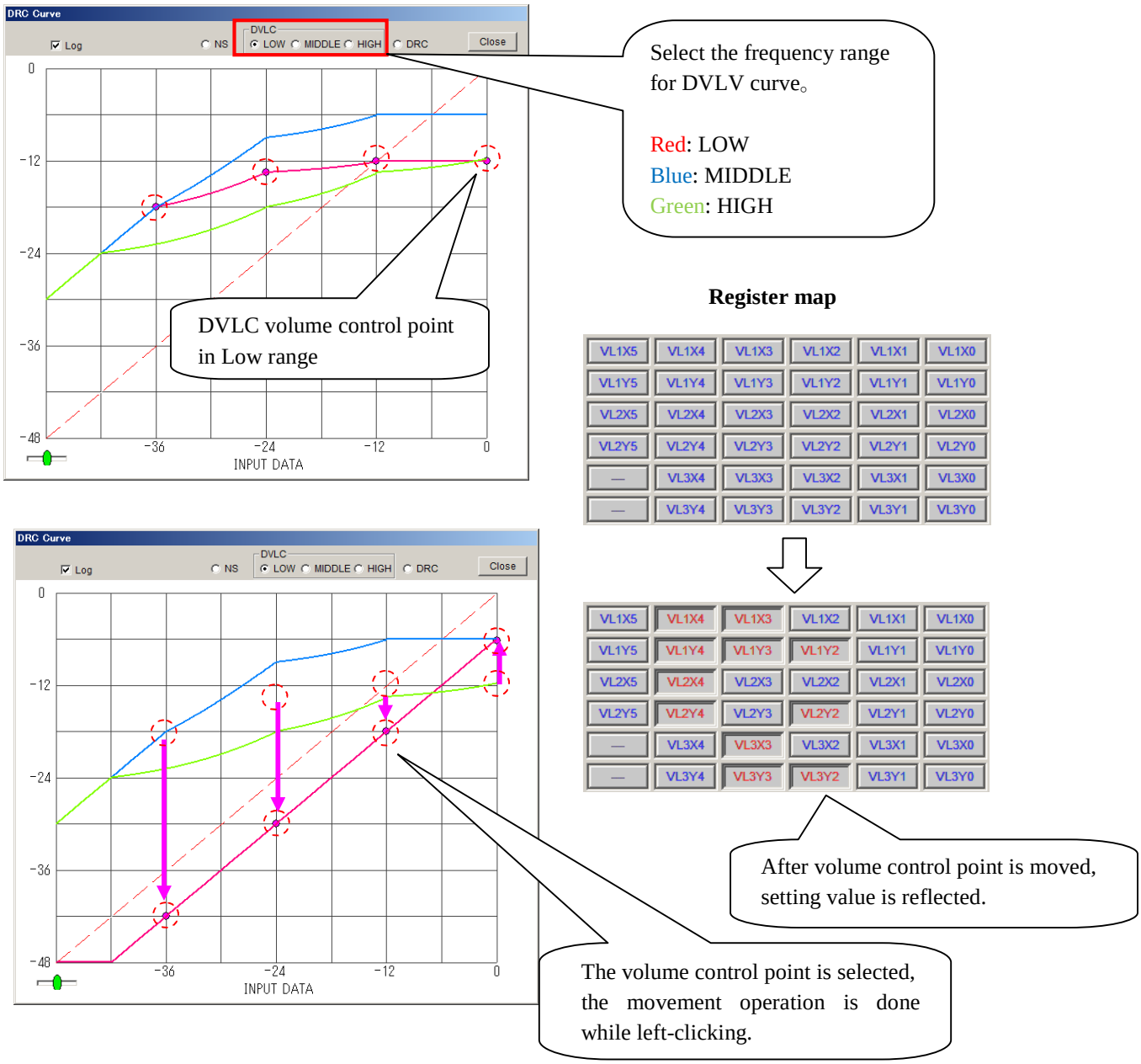

Figure 46. DVLC Curve Setting

1-8-6. Dynamic Range Control

Dynamic Range Control is displayed when “DRC” button is checked after [DRV Curve] button is pushed. Then, a register set point is also updated.

Dynamic Range Compression Level can be adjusted by the left-click.

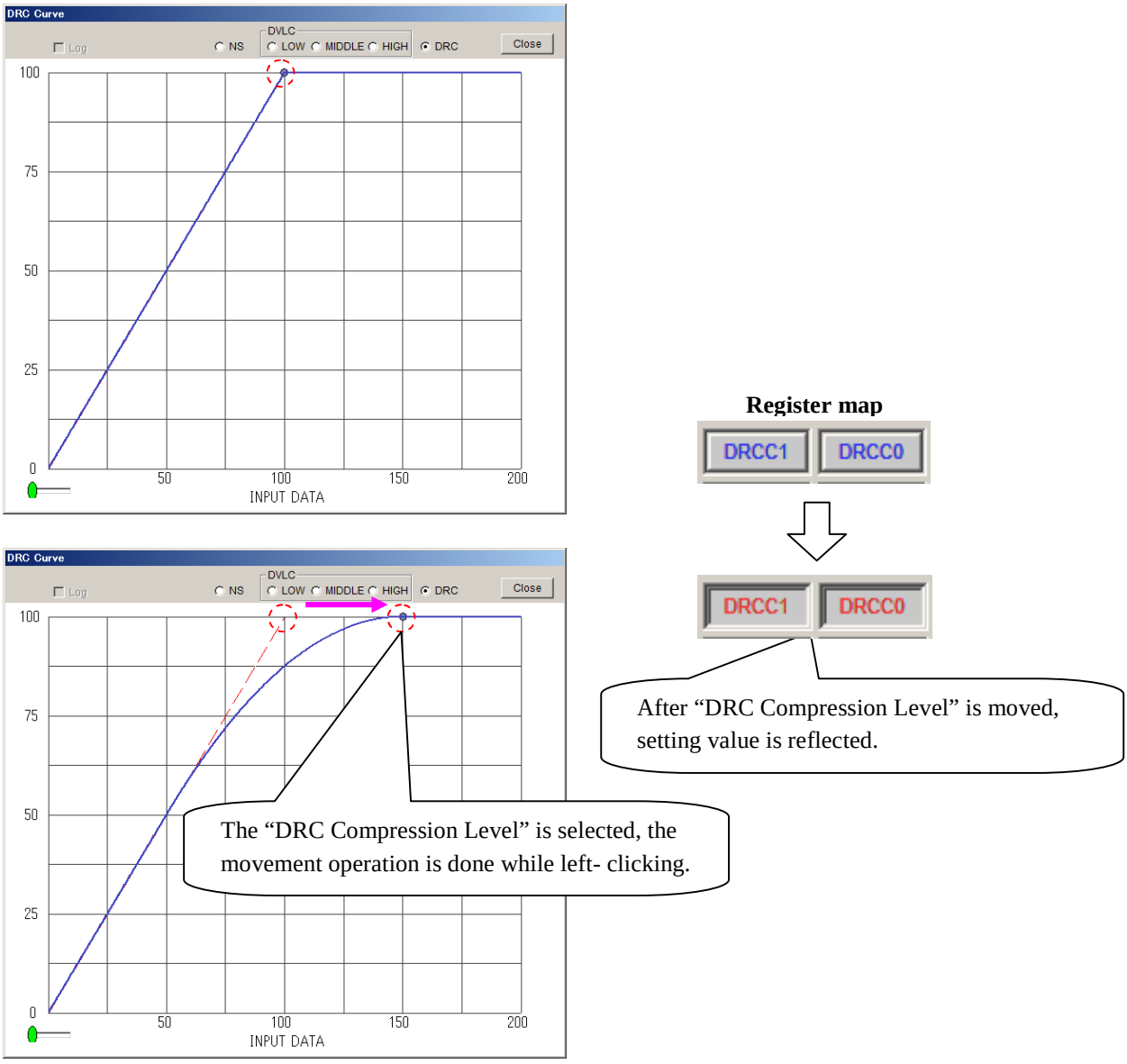

Figure 47. Dynamic Range Control Setting

2. [REG]: Register Map

This tab is for a register writing and reading.

Each bit on the register map is a push-button switch.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Gray out registers are Read Only registers. They can not be controlled.

The registers which is not defined in the datasheet are indicated as “---”.

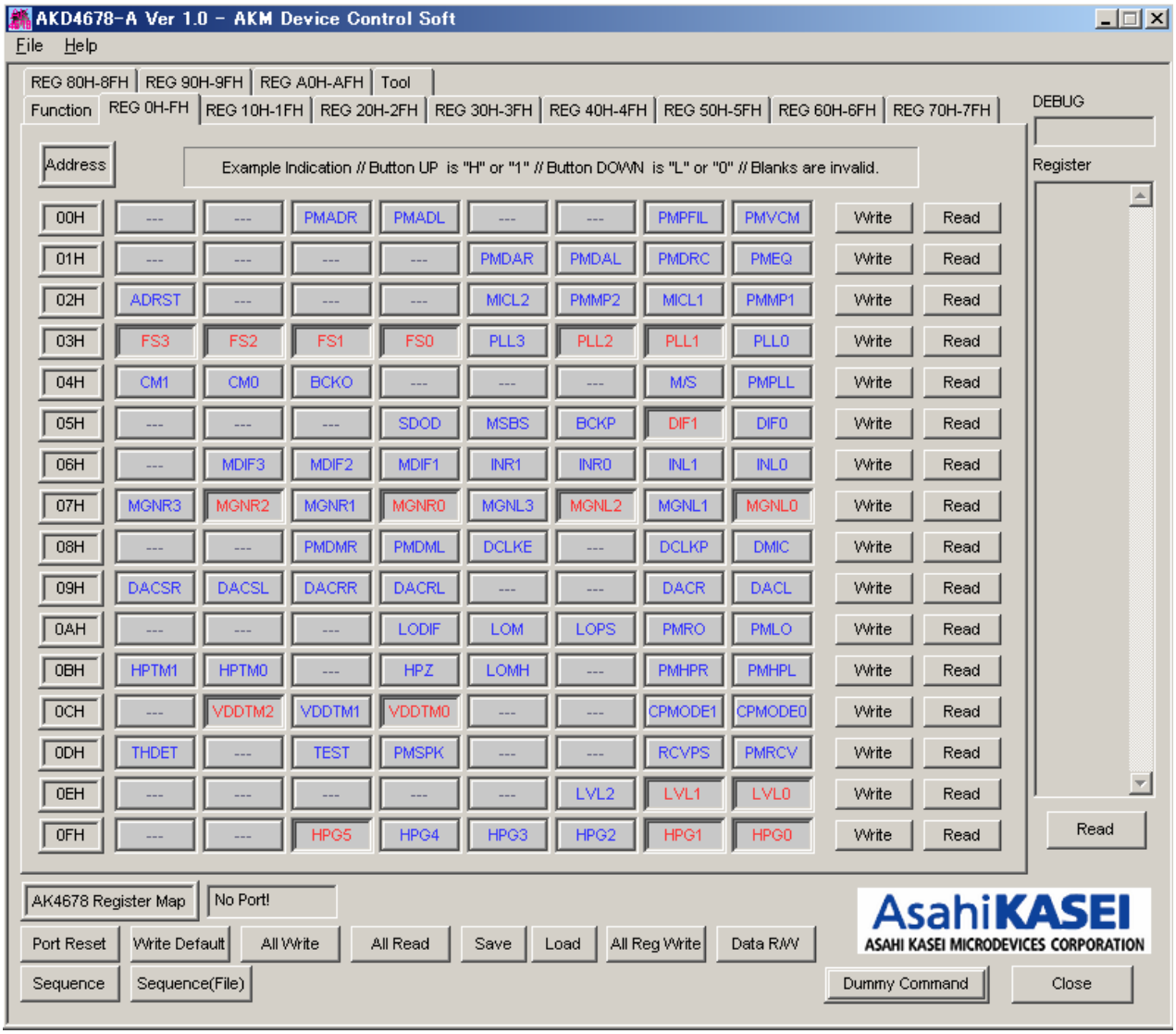

Figure 48. Window of [REG]

[Write]: Data Writing Dialog

It is for when changing two or more bits on the same address at the same time.

Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.

When checking the checkbox, the register will be “H” or “1”, when not checking the register will be “L” or ”0”.
Click [OK] to write setting value to the registers, or click [Cancel] to cancel this setting.

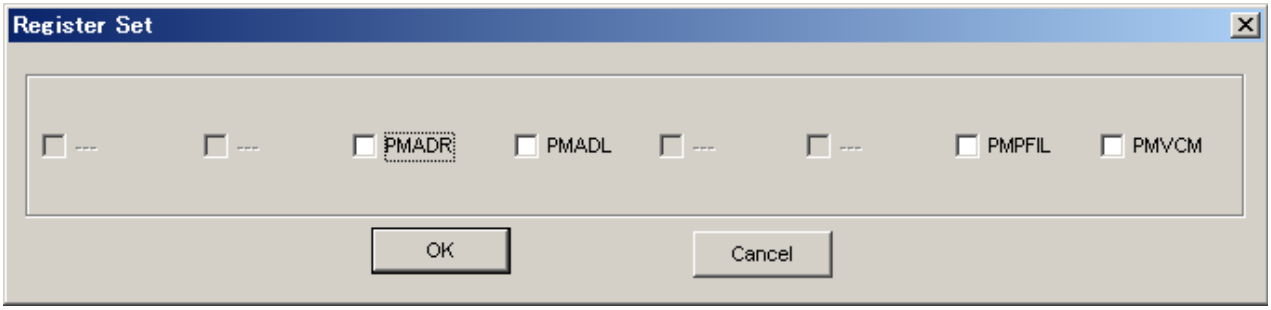

Figure 49. Window of [Register Set]

[Read]: Data Read

Click [Read] button located on the right of the each corresponded address to execute register reading.

After register reading, the display will be updated regarding to the register status.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Please be aware that button statuses will be changed by Read command.

3. [Tool]: Test tool

This tab screen is for evaluation testing tool.
Click buttons for each testing tool.

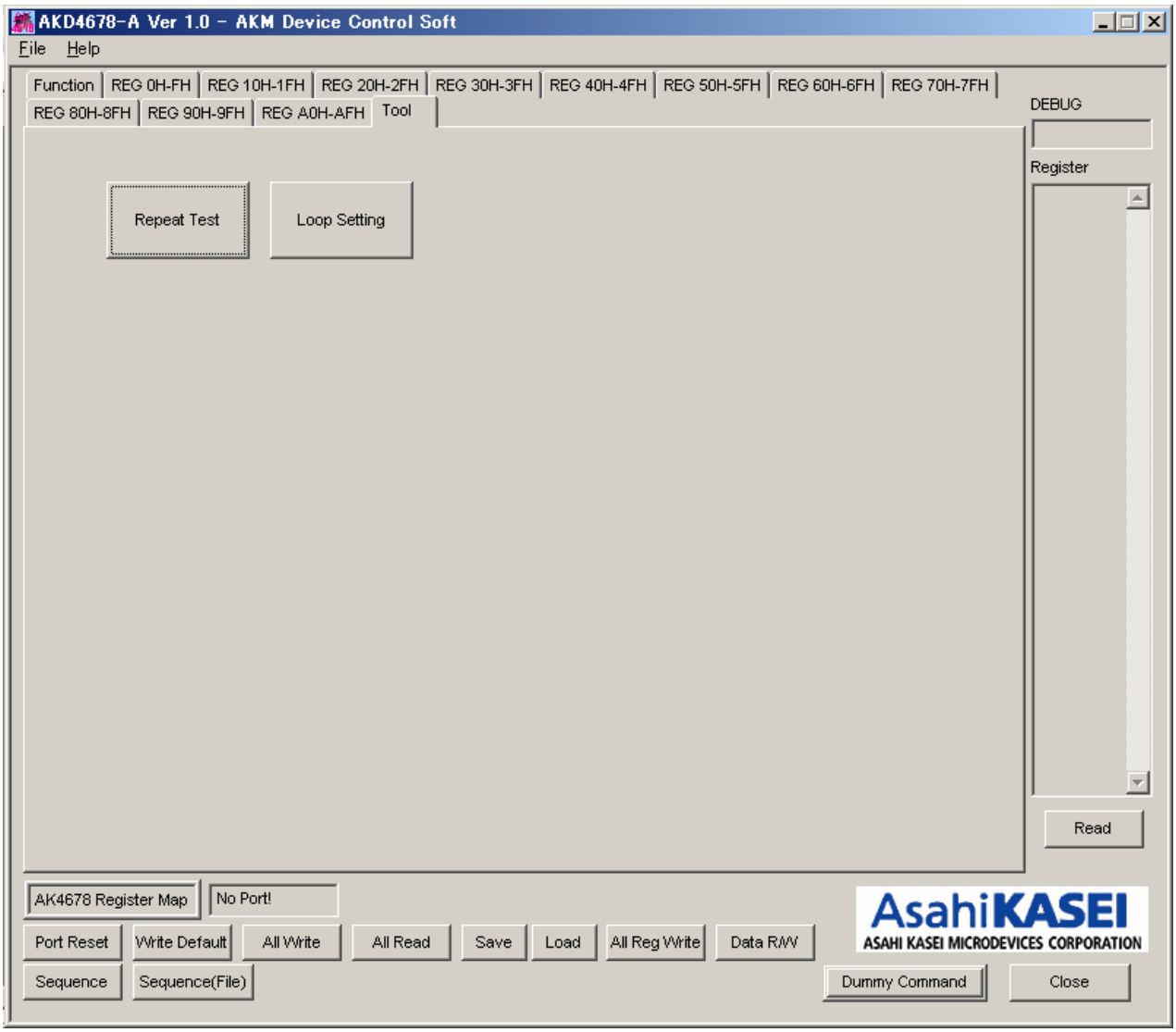

Figure 50. Window of [Tool]

[Repeat Test]: Repeat Test Dialog

Click [Repeat Test] button to open repeat test setting dialog box.
A repetition write test of the setting register files can be applied.

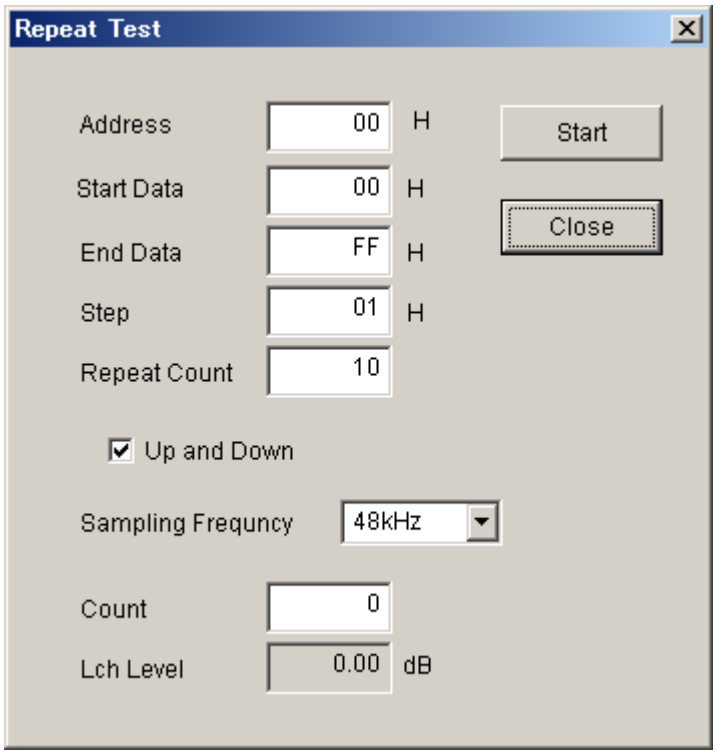

Figure 51. Window of [Repeat Test]

[Start] : When [Start] button is clicked,
The dialog of saving test data settings as a file is shown.
Please set the file name.
After setting save file, repeat test is started.

[Close] : Close this dialog and finish the process.
[Address] : Input data address in hexadecimal numbers for data writing.
[Start Data] : Input start data address in hexadecimal numbers for data writing.
[End Data] : Input finish data address in hexadecimal numbers for data writing.
[Step] : Rewrite data at intervals of step.
[Repeat Count] : Set the count of repetition write test.
[Up and Down] : Set the data flow at 1 count.

Click [OK] to write setting value to the registers, or click [Cancel] to cancel this setting.

・Click [OK] : After rewrite the intervals of step from Start Data to End Data,
Rewrite the intervals of step from End Data to Start Data.
[Execution example] Start Data = 00, End Data = 05, Step = 1, [ ]…Test Flow of 1 count.
Data Flow : [00→01→02→03→04→05→05→04→03→02→01→00]×Repeat Count

・Click [Cancel] : Rewrite the intervals of step from Start Data to End Data.
[Execution example] Start Data = 00, End Data = 05, Step = 1, [ ]…Test Flow of 1 count
Data Flow : [00→01→02→03→04→05]×Repeat Count

[Sampling Frequency] : Select the samplimg frequency 44.1kHz or 48kHz.
[Count] : Show the count under test execution.
[Lch Level] : Show the Lch Level under test execution.

[Loop Setting] : [Loop] Dialog

Click [Loop Setting] button to open loop setting dialog box.
Write test of the setting register files can be applied.

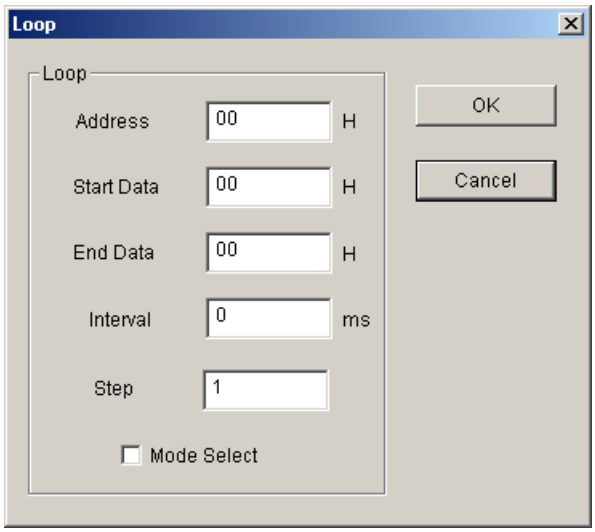

Figure 52. Window of [Loop]

■ Dialog Boxes

[All Reg Write]

Click [All Reg Write] button in the main window to open register setting files.
Register setting files saved by [SAVE] button can be applied.

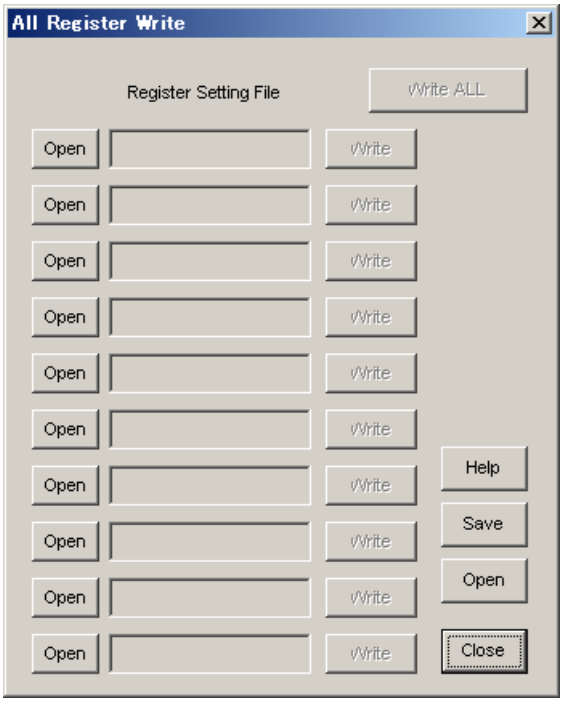

Figure 53. Window of [All Register Write]

[Open (left)]	: Selecting a register setting file (*.akr).
[Write]	: Executing register writing.
[Write All]	: Executing all register writings. Writings are executed in descending order.
[Help]	: Help window is popped up.
[Save]	: Saving the register setting file assignment. The file name is “*.mar”.
[Open (right)]	: Opening a saved register setting file assignment “*. mar”.
[Close]	: Closing the dialog box and finish the process.

*Operating Suggestions

(1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mar” should be stored in the same folder.
(2) When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

[Data R/W]

Click the [Data R/W] button in the main window for data read/write dialog box.
Data write is available to specified address.

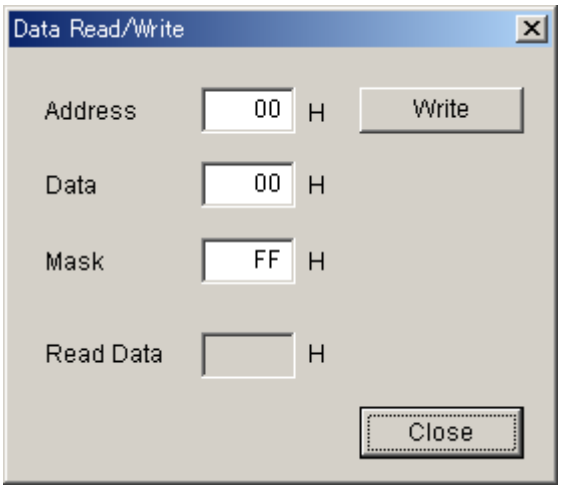

Figure 54. Window of [Data Read/Write]

Address Box	: Input data address in hexadecimal numbers for data writing.
Data Box	: Input data in hexadecimal numbers.
Mask Box	: Input mask data in hexadecimal numbers. This is “AND” processed input data.
[Write]	: Writing to the address specified by “Address” box.
[Close]	: Closing the dialog box and finish the process. Data writing can be cancelled by this button instead of [Write] button.

*The register map will be updated after executing [Write] or [Read] commands.

[Sequence]

Click [Sequence] button to open register sequence setting dialog box.
Register sequence can be set in this dialog box.

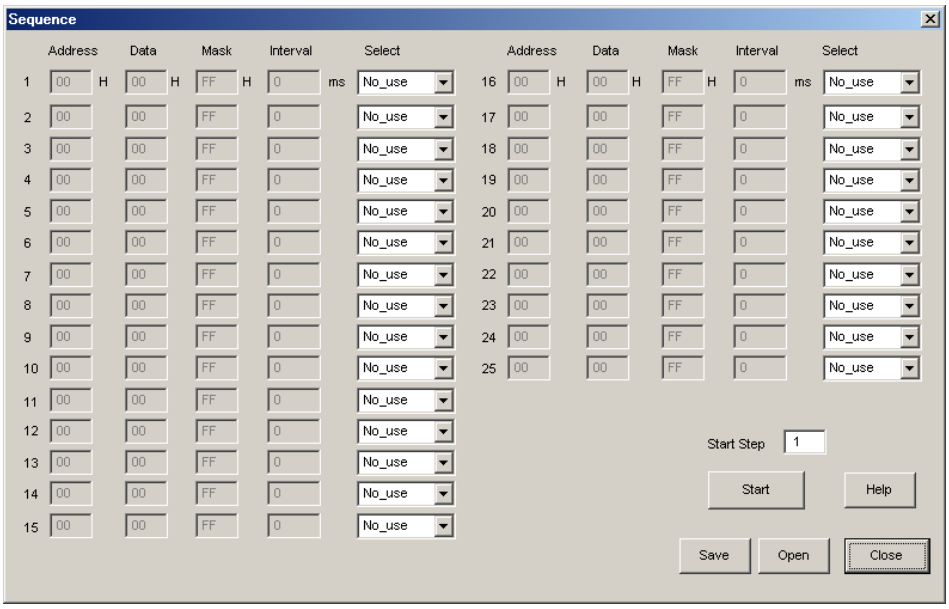

Figure 55. Window of [Sequence]

Sequence Setting

Set register sequence by following process bellow.
(1)Select a command
Use [Select] pull-down box to choose commands.
Corresponding boxes will be valid.
< Select Pull-down menu >
· No_use : Not using this address
· Register : Register writing
· Reg(Mask) : Register writing (Masked)
· Interval : Taking an interval
· Stop : Pausing the sequence
· End : Finishing the sequence

(2)Input sequence
[Address] : Data address
[Data] : Writing data
[Mask] : Mask
[Data] box data is ANDed with [Mask] box data. This is the actual writing data.
When Mask = 0x00, current setting is hold.
When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.
When Mask =0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.
[Interval] : Interval time

Valid boxes for each process command are shown bellow.

· No_use	: None
· Register	: [Address], [Data], [Interval]
· Reg(Mask)	: [Address], [Data], [Mask], [Interval]
· Interval	: [Interval]
· Stop	: None
· End	: None

Control Buttons

The function of Control Button is shown bellow.

[Start]	: Executing the sequence
[Help]	: Opening a help window
[Save]	: Saving sequence settings as a file. The file name is "*.aks".
[Open]	: Opening a sequence setting file "*.aks".
[Close]	: Closing the dialog box and finish the process.

Stop of the Sequence

When "Stop" is selected in the sequence, processing is paused and it starts again when [Start] button is clicked. Restarting step number is shown in the "Start Step" box. When finishing the process until the end of sequence, "Start Step" will return to "1".

The sequence can be started from any step by writing the step number to the "Start Step" box.
Write "1" to the "Start Step" box and click [Start] button, when restarting the process from the beginning.

[Sequence(File)]

Click [Sequence(File)] button to open sequence setting file dialog box.
Those files saved in the “Sequence setting dialog” can be applied in this dialog.

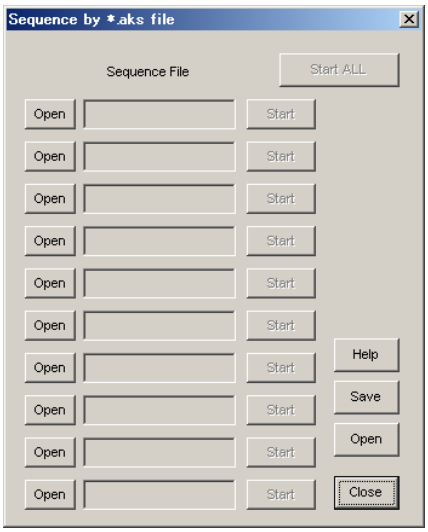

Figure 56. Window of [Sequence(File)]

[Open (left)]	: Opening a sequence setting file (*.aks).
[Start]	: Executing the sequence setting.
[Start All]	: Executing all sequence settings. Sequences are executed in descending order.
[Help]	: Pop up the help window.
[Save]	: Saving sequence setting file assignment. The file name is “*.mas”.
[Open(right)]	: Opening a saved sequence setting file assignment “*. mas”.
[Close]	: Closing the dialog box and finish the process.

*Operating Suggestions

(1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog “*.mas” should be stored in the same folder.
(2) When “Stop” is selected in the sequence the process will be paused and a pop-up message will appear. Click “OK” to continue the process.

Figure 57. Window of [Sequence Pause]

Measurement Result

[Measurement condition]

- Measurement Unit : Audio Precession System Two Cascade
- MCLK : 11.2896MHz
- BICK : 64fs
- fs : 44.1kHz
- Power Supply : AVDD=DVDD=PVDD=TVDD=1.8V, SVDD=4.2V
- Band Width : 22Hz ~ 20kHz
- Measurement Mode : External Slave Mode
- Temperature : Room Temperature

[Measurement Result]

1. ADC

a). LIN1, RIN1 pins, MGNL=MGNR=+18dB

Parameter	Result Lch / Rch	Unit
S/(N+D) (-1dBFS Input)	79.4 / 79.7	dB
D-Range (-60dBFS Input, A-weighted)	87.2 / 87.2	dB
S/N (A-weighted)	87.5 / 87.6	dB
Interchannel Isolation	106.8 / 104.8	dB

b). LIN2, RIN2 pins, MGNL=MGNR=0dB

Parameter	Result Lch / Rch	Unit
S/(N+D) (-1dBFS Input)	81.0 / 81.4	dB
D-Range (-60dBFS Input, A-weighted)	92.3 / 92.4	dB
S/N (A-weighted)	93.4 / 93.4	dB
Interchannel Isolation	110.7 / 103.5	dB

2. DAC

a) Line out (LOUT/ROUT pins, LVL=0dB, R_L=20kΩ)

Parameter	Result Lch / Rch	Unit
S/(N+D) (0dBFS Input)	81.6 / 81.0	dB
S/N (A-weighted)	92.3 / 92.3	dB
Interchannel Isolation	91.8 / 92.3	dB

b) Mono Line Out (LOP/LON pins, LVL=0dB, R_L=20kΩ)

Parameter	Result	Unit
S/(N+D) (0dBFS Input)	73.5	dB
S/N (A-weighted)	95.8	dB

c) Mono Receiver Out (RCP/RCN pins, RCVG=-6dB, R_L=32Ω)

Parameter	Result	Unit
S/(N+D) (0dBFS Input)	58.8	dB
S/(N+D) (0dBFS Input, RCVG=0dB)	37.7	dB
S/N (A-weighted)	95.1	dB
Output Noise Level (RCVG=-9dB)	-100.8	dBV

d) HP Out (HPL/HPR pins, HPG=0dB, R_L=32Ω)

Parameter		Result Lch / Rch	Unit
Output Power (R_L=32Ω)	HPG=-4dB	9.3 / 9.6	mW
	HPG=0dB	23.4 / 24.2	
Output Power (R_L=16Ω)	HPG=-4dB	17.6 / 18.9	mW
	HPG=0dB	38.1 / 41.3	
S/(N+D) (R_L=32Ω)	HPG=-4dB	70.1 / 69.5	dB
	HPG=0dB	42.5 / 46.5	
S/(N+D) (R_L=16Ω)	HPG=-4dB	64.7 / 64.0	dB
	HPG=0dB	20.2 / 20.1	
S/N (A-weighted)		95.0 / 94.7	dB
Output Noise Level (A-weighted, HPG=-14dB)		-107.1 / -107.1	dBV
Interchannel Isolation		99.6 / 103.0	dB

e) SPK Out (SPP/SPN pins, SPKG=-6dB, R_L=8Ω+10uH)

Parameter		Result	Unit
Output Power	SVDD=5.0V THD+N=10% SPKG=-3dBFS	1.53	W
	SVDD=4.2V THD+N=10% SPKG=-3dBFS	1.07	
	SVDD=4.2V THD+N=1% SPKG=0dBFS	0.87	
	SVDD=3.7V THD+N=1% SPKG=-6dBFS	0.67	
Output Voltage (-3dBFS Input)		5.48	Vpp
S/(N+D) (SVDD=3.7V, Po=0.35W)		58.3	dB
Output Noise Level (A-Weighted)		-82.3	dBV

REVISION HISTORY

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Page	Contents
13/03/19	KM114000	0	First Edition		

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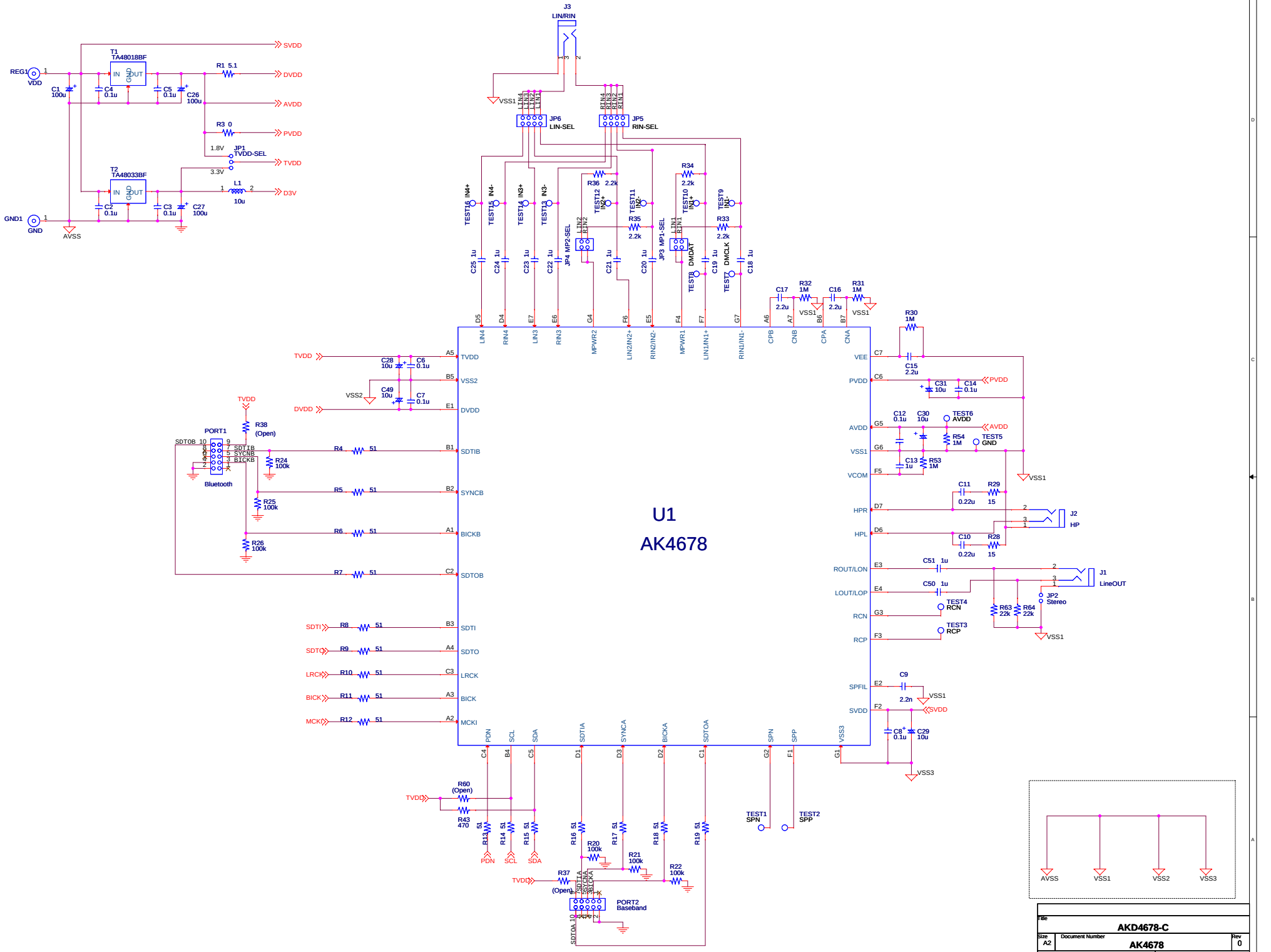

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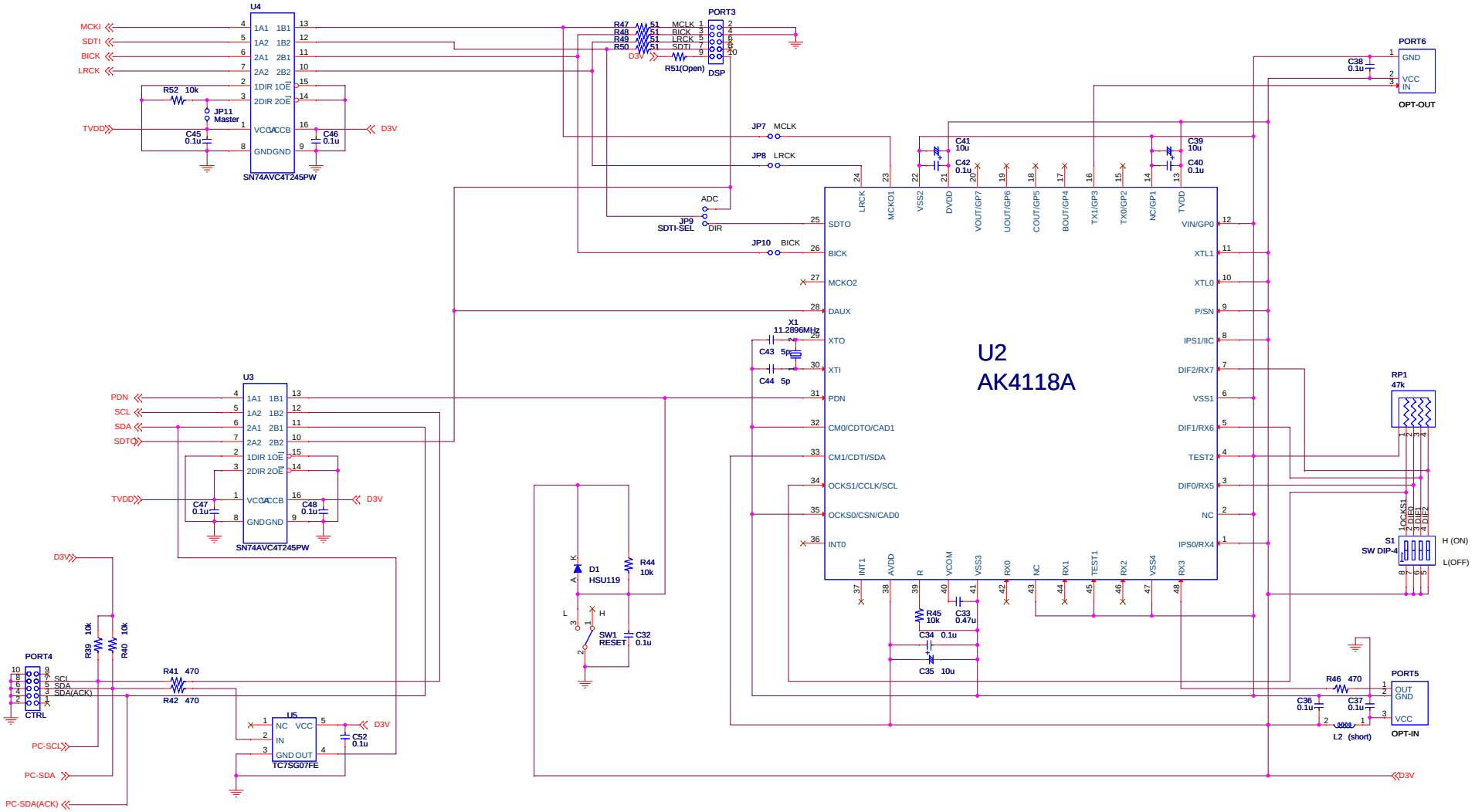
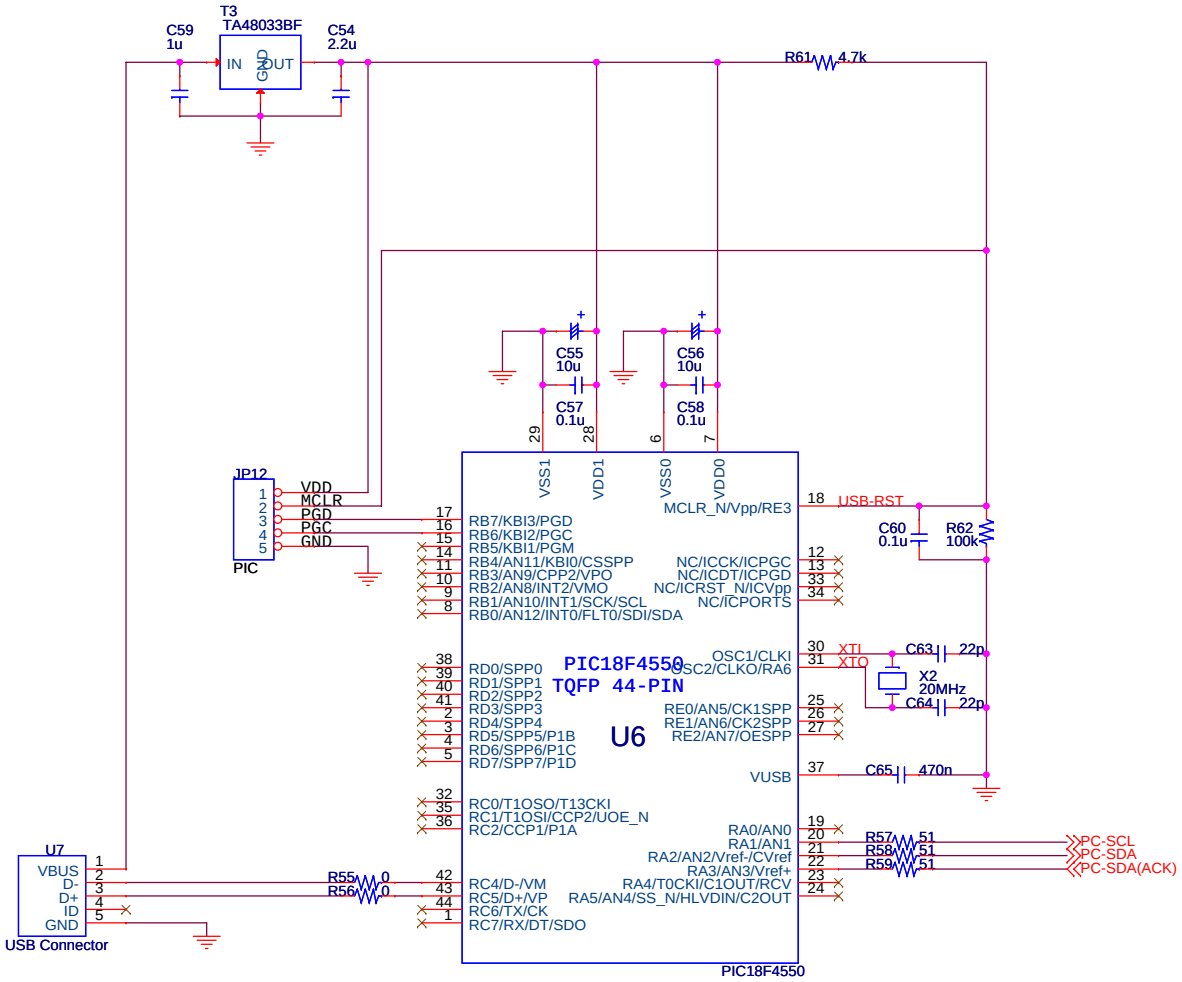
Date: Tuesday, April 09, 2013	Sheet 1 of 3	



Title	AKD4678-C		
Size A2	Document Number DIR/DIT		Rev 0
Date: Tuesday, April 09, 2013	Sheet 2 of 3		



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