单通道 5Ω SP3T 模拟开关
5V/3.3V 3:1 多路复用器/多路信号分离器

1 特性

- 指定的先断后合开关
- 低导通状态电阻
- 高带宽
- 控制输入可承受 5.5V 电压
- 低电荷注入
- 出色的通态电阻匹配
- 低总谐波失真 (THD)
- 1.65V 至 5.5V 单电源运行
- 锁断性能超过 100mA（符合 JESD 78，II 类规范的要求）
- 静电放电 (ESD) 性能测试符合 JESD 22 规范
  - 2000V 人体放电模式（A114-B，II 类）
  - 1000V 充电器件模型 (C101)

2 应用

- 手机
- 掌上电脑 (PDA)
- 便携式仪表

3 说明

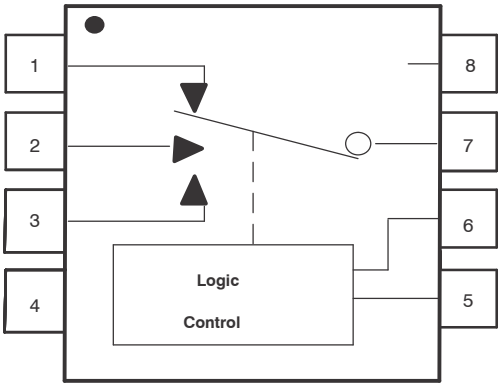
TS5A3357 是一款高性能单通道 3:1 模拟开关，可在 1.65V 至 5.5V 电压范围内运行。该器件可提供低导通状态电阻和低输入/输出电容，因此具有低信号失真。先断后合功能允许在信号失真极低的情况下将信号从一个端口传输到另一个端口。该器件还可提供低电荷注入，因此适用于高性能音频和数据收集系统。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS5A3357	VSSOP (8)	2.3mm x 2mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

逻辑图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (December 2007) to Revision B **Page**

- 增加了*器件信息* 表、*ESD 额定值* 表、*建议运行条件* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1

5 Device Comparison Table

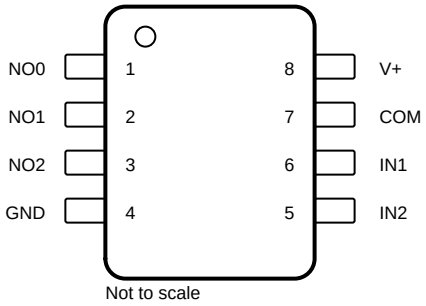
Table 1. Summary of Characteristics(1)

Configuration	Triple 3:1 Multiplexer/ Demultiplexer (1 × SP3T)
Number of channels	1
ON-state resistance (r_{on})	5 Ω
ON-state resistance match (Δr_{on})	0.1 Ω
ON-state resistance flatness ($r_{on(flat)}$)	6.5 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	6.5 ns/3.7 ns
Break-before-make time (t_{BBM})	0.5 ns
Charge injection (Q_C)	3.4 pC
Bandwidth (BW)	334 MHz
OFF isolation (O_{ISO})	–82 dB at 10 MHz
Crosstalk (X_{TALK})	–62 dB at 10 MHz
Total harmonic distortion (THD)	0.05%
Leakage current ($I_{COM(OFF)}$)	±1 μA

(1) V_+ = 5 V, T_A = 25°C

6 Pin Configuration and Functions

DCU Package
VSSOP 8 Pin
Top View



Not to scale

Pin Functions

PIN		DESCRIPTION
NAME	NO.	
NO0	1	Normally open
NO1	2	Normally open
NO2	3	Normally open
GND	4	Digital ground
IN2	5	Digital control to connect COM to NO
IN1	6	Digital control to connect COM to NO
COM	7	Common
V+	8	Power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_+	Supply voltage range(2)		–0.5	6.5	V
V_{NO} V_{COM}	Analog voltage range(2) (3) (4)		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NO}, V_{COM} < 0 or V_{NO}, V_{COM} > V_+	–50	50	mA
I_{NO} I_{COM}	On-state switch current	V_{NO}, V_{COM} = 0 to V_+	–100	100	mA
V_I	Digital input voltage range(2) (3)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100	100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_+	Supply voltage range	1.65	5.5	V
V_{NO} V_{COM}	Analog voltage range	0	V_+	
V_I	Digital input voltage range	0	5.5	

7.4 Thermal Information

THERMAL METRIC(1)		TS5A3357 DCU (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	84.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics for 5-V Supply(1)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Peak ON resistance	r_{peak}	$0 \le V_{NO} \le V_+$, I_{COM} = –30 mA,	Switch ON, See Figure 13	Full	4.5 V			15	Ω
ON-state resistance	r_{on}	V_{NO} = 0, I_{COM} = 30 mA	Switch ON, See Figure 13	25°C	4.5 V		5	7	Ω
				Full				7	
		V_{NO} = 2.4 V, I_{COM} = –30 mA		25°C			6	12	
				Full				12	
		V_{NO} = 4.5 V, I_{COM} = –30 mA		25°C			7	15	
				Full				15	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 3.15 V, I_{COM} = –30 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.1		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO} \le V_+$, I_{COM} = –30 mA,	Switch ON, See Figure 13	25°C	5 V		6.5		Ω
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0	Switch OFF, See Figure 14	25°C	5.5 V	–0.1		0.1	µA
				Full		–1		1	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0 to V_+, V_{NO} = V_+ to 0,	Switch OFF, See Figure 14	25°C	0	–0.1		0.1	µA
				Full		–1		1	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0 to V_+, V_{COM} = Open,	Switch ON, See Figure 14	25°C	5.5 V	–0.1		0.1	µA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 14	25°C	5.5 V	–0.1		0.1	µA
				Full		–1		1	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		V_+ × 0.7		5.5	V
Input logic low	V_{IL}			Full		0		V_+ × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	5.5 V			0.1	µA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 5-V Supply(1) (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	5 V	1.5		6.5	ns
				Full	4.5 V to 5.5 V	1.5		7	
Turn-off time	t_{OFF}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	5 V	0.8		3.7	ns
				Full	4.5 V to 5.5 V	0.8		7	
Break-before-make time	t_{BBM}	V_{NO} = V_+, R_L = 50 Ω,	C_L = 50 pF, See Figure 17	25°C	5 V	0.5			ns
				Full	4.5 V to 5.5 V	0.5			
Charge injection	Q_C	V_{GEN} = 0, C_L = 0.1 nF,	See Figure 21	25°C	5 V		3.4		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	5 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	5 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 15	25°C	5 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 15	25°C	5 V		17		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 15	25°C	5 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	4.5 V to 5.5 V		334		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	4.5 V to 5.5 V		–82		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	4.5 V to 5.5 V		–62		dB
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V			1	μA
				Full				10	

7.6 Electrical Characteristics for 3.3-V Supply(1)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Peak ON resistance	r_{peak}	$0 \le V_{NO} \le V_+$, I_{COM} = –24 mA,	Switch ON, See Figure 13	Full	3 V			25	Ω
ON-state resistance	r_{on}	V_{NO} = 0 V, I_{COM} = 24 mA	Switch ON, See Figure 13	25°C	3 V		6.5	9	Ω
				Full				9	
		V_{NO} = 3 V, I_{COM} = –24 mA		25°C			9	20	
				Full				20	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 2.1 V, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	3 V		0.1		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO} \le V_+$, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	3.3 V		13.5		Ω
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0	Switch OFF, See Figure 14	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0 to V_+, V_{NO} = V_+ to 0,	Switch OFF, See Figure 14	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0,	Switch ON, See Figure 14	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 14	25°C	3.6 V	–0.1		0.1	µA
				Full		–1		1	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		$V_+ \times 0.7$		5.5	V
Input logic low	V_{IL}			Full		0		$V_+ \times 0.3$	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	–1		0.1	µA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 3.3-V Supply[1] (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	3.3 V	2		9.5	ns
				Full	3 V to 3.6 V	2		11	
Turn-off time	t_{OFF}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	3.3 V	1.3		5.1	ns
				Full	3 V to 3.6 V	1.5		5.5	
Break-before-make time	t_{BBM}	V_{NO} = V_+, R_L = 50 Ω,	C_L = 50 pF, See Figure 17	25°C	3.3 V	0.5			ns
				Full	3 V to 3.6 V	0.5			
Charge injection	Q_C	V_{GEN} = 0, C_L = 0.1 nF,	See Figure 21	25°C	3.3 V		1.75		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	3.3 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	3.3 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 15	25°C	3.3 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 15	25°C	3.3 V		17		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 15	25°C	3.3 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	3 V to 3.6 V		327		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	3 V to 3.6 V		–82		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	3 V to 3.6 V		–62		dB
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V			1	µA
				Full				10	

7.7 Electrical Characteristics for 2.5-V Supply(1)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_+	V
Peak ON resistance	r_{peak}	0 ≤ V_{NO} ≤ V_+, I_{COM} = –8 mA,	Switch ON, See Figure 13	Full	2.3 V			50	Ω
ON-state resistance	r_{on}	V_{NO} = 0 V, I_{COM} = 8 mA	Switch ON, See Figure 13	25°C	2.3 V		8	12	Ω
				Full				12	
		V_{NO} = 2.3 V, I_{COM} = –8 mA		25°C			11	30	
				Full				30	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.3		Ω
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} ≤ V_+, I_{COM} = –8 mA,	Switch ON, See Figure 13	25°C	2.5 V		39		Ω
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0	Switch OFF, See Figure 14	25°C	2.7 V	–0.1		0.1	µA
				Full		–1		1	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0 to V_+, V_{NO} = V_+ to 0,	Switch OFF, See Figure 14	25°C	2.7 V	–0.1		0.1	µA
				Full		–1		1	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0,	Switch ON, See Figure 14	25°C	2.7 V	–0.1		0.1	µA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 14	25°C	2.7 V	–0.1		0.1	µA
				Full		–1		1	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		V_+ × 0.75		5.5	V
Input logic low	V_{IL}			Full		0		V_+ × 0.25	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V			0.1	µA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 2.5-V Supply(1) (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	2.5 V	3		15	ns
				Full	2.3 V to 2.7 V	3		16.5	
Turn-off time	t_{OFF}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	2.5 V	2		7.2	ns
				Full	2.3 V to 2.7 V	2		7.8	
Break-before-make time	t_{BBM}	V_{NO} = V_+, R_L = 50 Ω,	C_L = 50 pF, See Figure 17	25°C	2.5 V	0.5			ns
				Full	2.3 V to 2.7 V	0.5			
Charge injection	Q_C	V_{GEN} = 0, C_L = 0.1 nF,	See Figure 21	25°C	2.5 V		1.15		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	2.5 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	2.5 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 15	25°C	2.5 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 15	25°C	2.5 V		17		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 15	25°C	2.5 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	2.3 V to 2.7 V		320		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	2.3 V to 2.7 V		–81		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	2.3 V to 2.7 V		–61		dB
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V			1	μA
				Full				10	

7.8 Electrical Characteristics for 1.8-V Supply(1)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_+	V
Peak ON resistance	r_{peak}	0 ≤ V_{NO} ≤ V_+, I_{COM} = –4 mA,	Switch ON, See Figure 13	Full	1.65 V			150	Ω
ON-state resistance	r_{on}	V_{NO} = 0 V, I_{COM} = 4 mA	Switch ON, See Figure 13	25°C	1.65 V		10	20	Ω
				Full				20	
		V_{NO} = 1.8 V, I_{COM} = –4 mA		25°C			17	50	
				Full				50	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.15 V, I_{COM} = –4 mA,	Switch ON, See Figure 13	25°C	1.65 V		0.3		Ω
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} ≤ V_+, I_{COM} = –4 mA,	Switch ON, See Figure 13	25°C	1.8 V		140		Ω
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0	Switch OFF, See Figure 14	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0 to V_+, V_{NO} = V_+ to 0,	Switch OFF, See Figure 14	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0 to V_+, V_{COM} = V_+ to 0,	Switch ON, See Figure 14	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0 to V_+,	Switch ON, See Figure 14	25°C	1.95 V	–0.1		0.1	µA
				Full		–1		1	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		V_+ × 0.75		5.5	V
Input logic low	V_{IL}			Full		0		V_+ × 0.25	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	1.95 V			0.1	µA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 1.8-V Supply(1) (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	1.8 V	5		32	ns
				Full	1.65 V to 1.95 V	5		34	
Turn-off time	t_{OFF}	V_{NO} = V_+ or GND, R_L = 500 Ω,	C_L = 50 pF, See Figure 16	25°C	1.8 V	3		14	ns
				Full	1.65 V to 1.95 V	3		14.5	
Break-before-make time	t_{BBM}	V_{NO} = V_+, R_L = 50 Ω,	C_L = 50 pF, See Figure 17	25°C	1.8 V	0.5			ns
				Full	1.65 V to 1.95 V	0.5			
Charge injection	Q_C	V_{GEN} = 0, C_L = 0.1 nF,	See Figure 21	25°C	1.8 V		0.3		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	1.8 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 15	25°C	1.8 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 15	25°C	1.8 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 15	25°C	1.8 V		17		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 15	25°C	1.8 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	1.65 V to 1.95 V		341		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	1.65 V to 1.95 V		–81		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	1.65 V to 1.95 V		–61		dB
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	1.95 V			1	μA
				Full				10	

7.9 Typical Characteristics

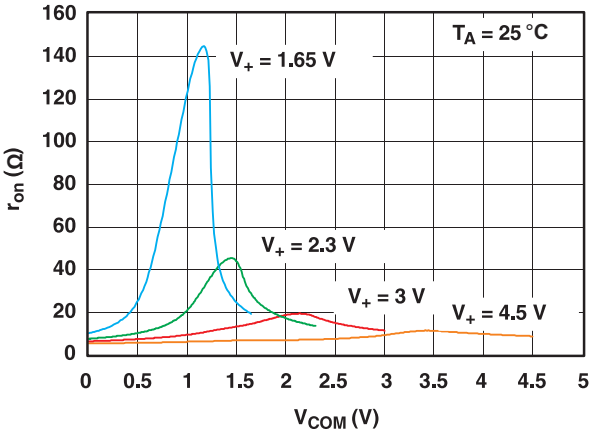


Figure 1. r_{on} vs V_{COM}

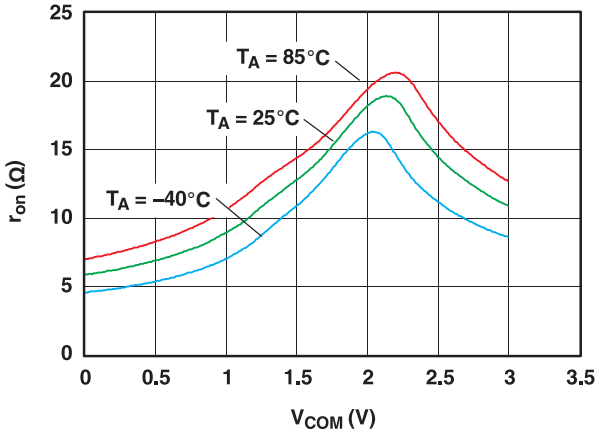


Figure 2. r_{on} vs V_{COM} (V_+ = 3 V)

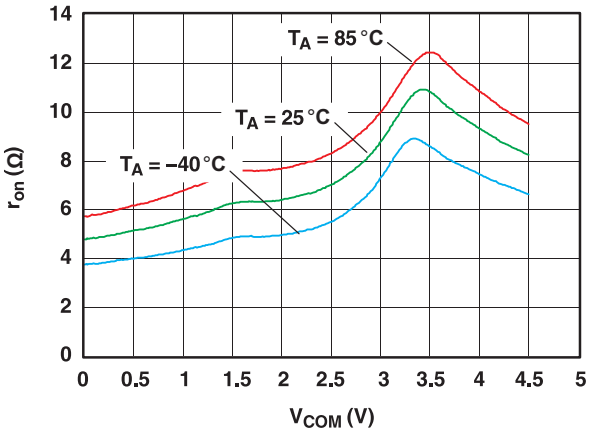


Figure 3. r_{on} vs V_{COM} (V_+ = 4.5 V)

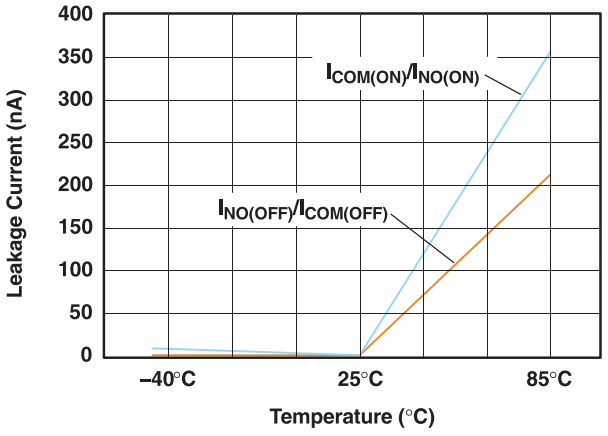


Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)

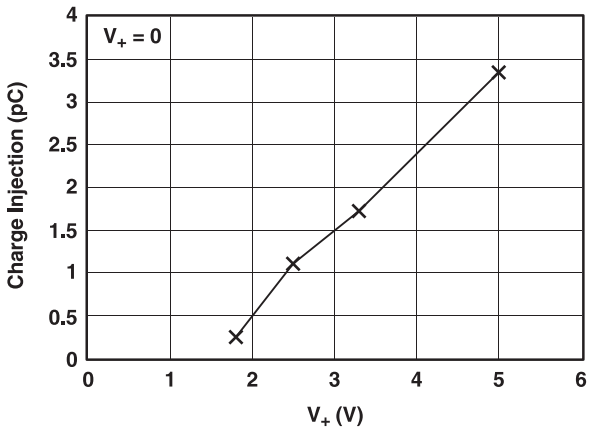


Figure 5. Charge Injection (Q_C) vs V_{COM}

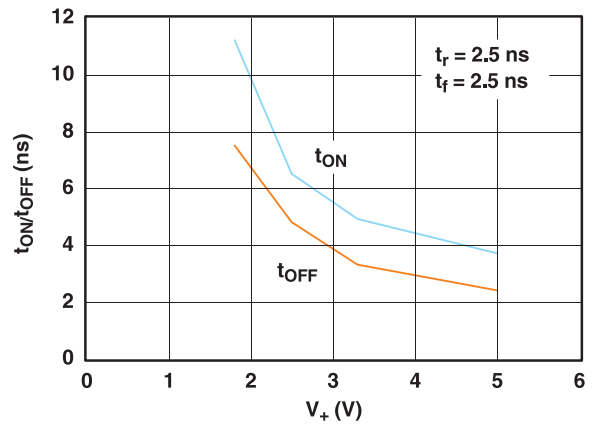


Figure 6. t_{ON} and t_{OFF} vs V_+

Typical Characteristics (continued)

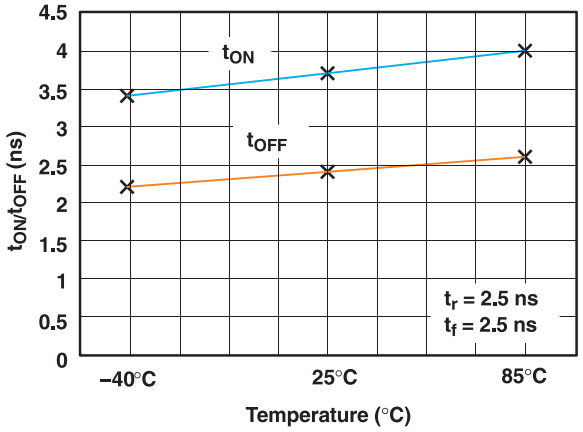


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

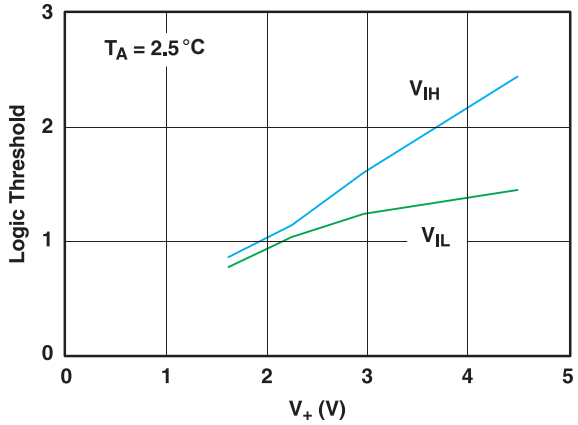


Figure 8. Logic-Level Threshold vs V_+

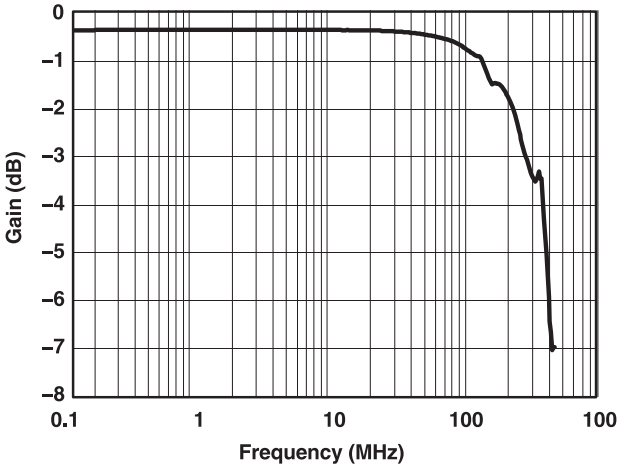


Figure 9. Frequency Response (V_+ = 3 V)

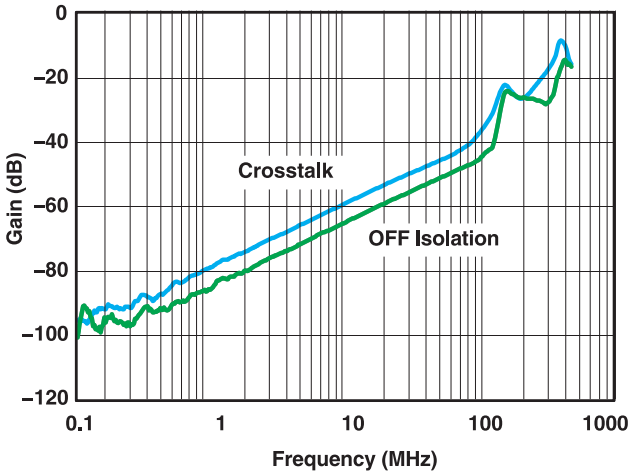


Figure 10. OFF Isolation and Crosstalk vs Frequency (V_+ = 3 V)

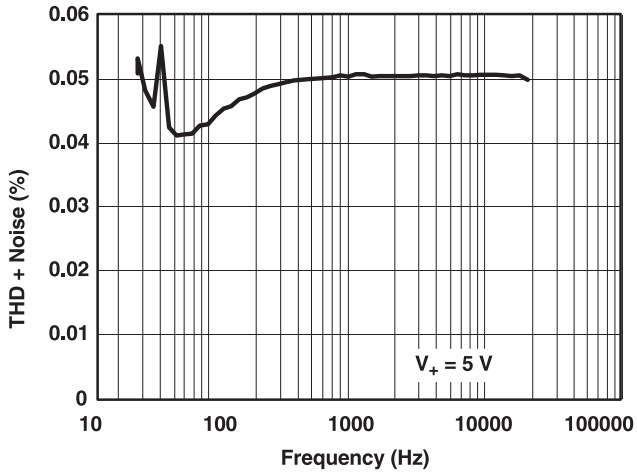


Figure 11. Total Harmonic Distortion vs Frequency (V_+ = 5 V)

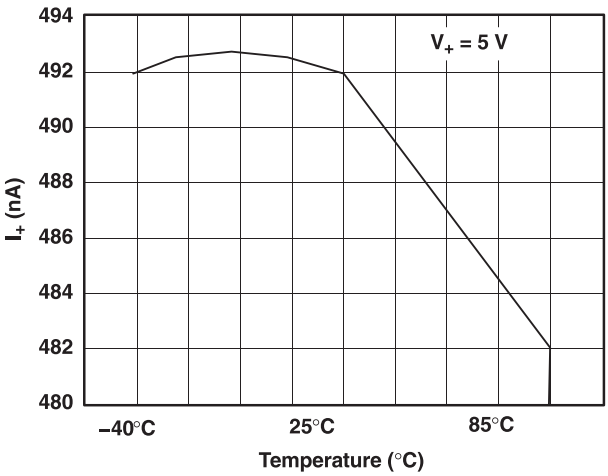


Figure 12. Power-Supply Current vs Temperature (V_+ = 5 V)

8 Parameter Measurement Information

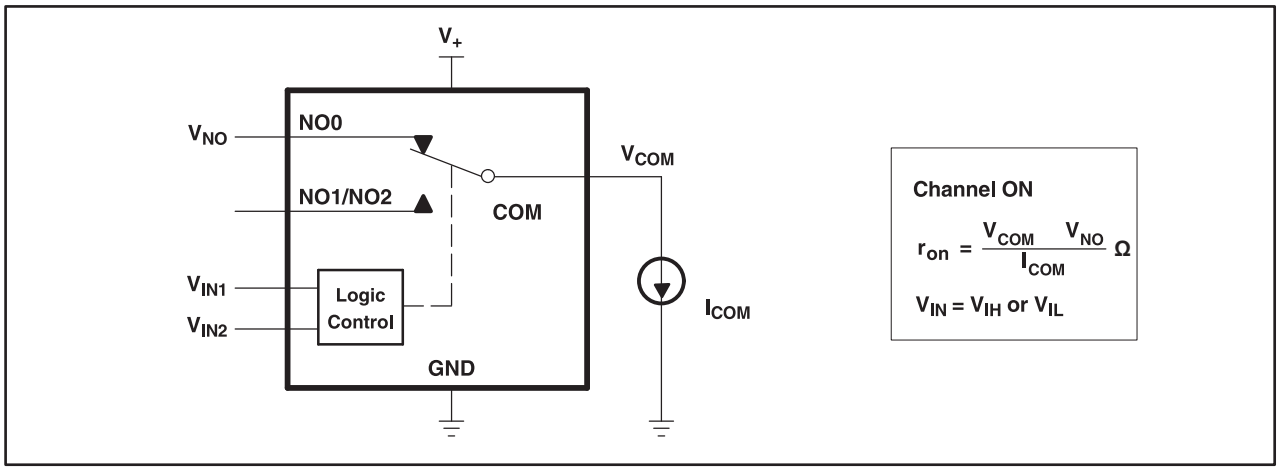


Figure 13. ON-State Resistance (r_{on})

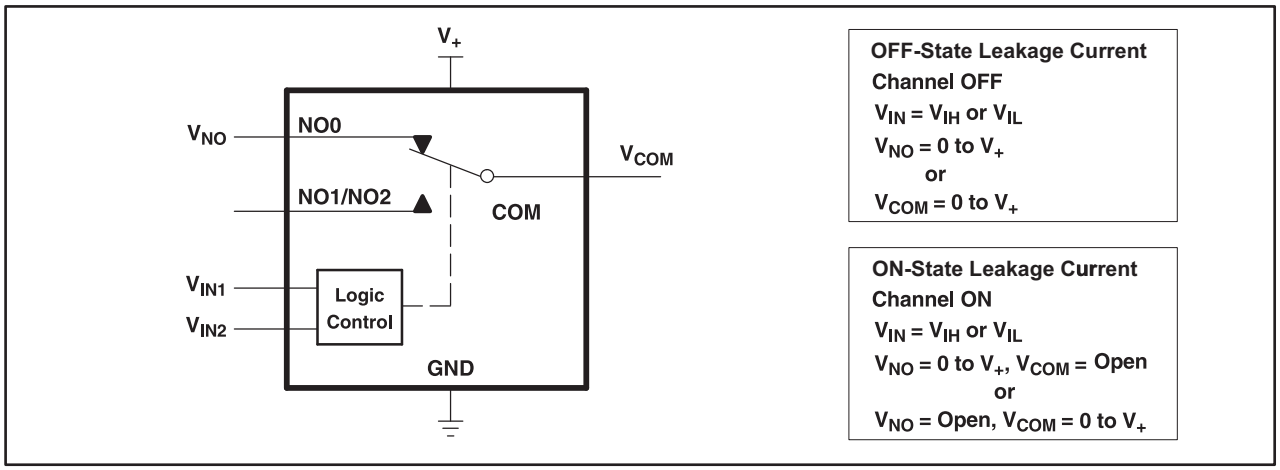


Figure 14. ON- and OFF-State Leakage Current ($I_{COM(ON)}$, $I_{COM(OFF)}$, $I_{NO(ON)}$, $I_{NO(OFF)}$)

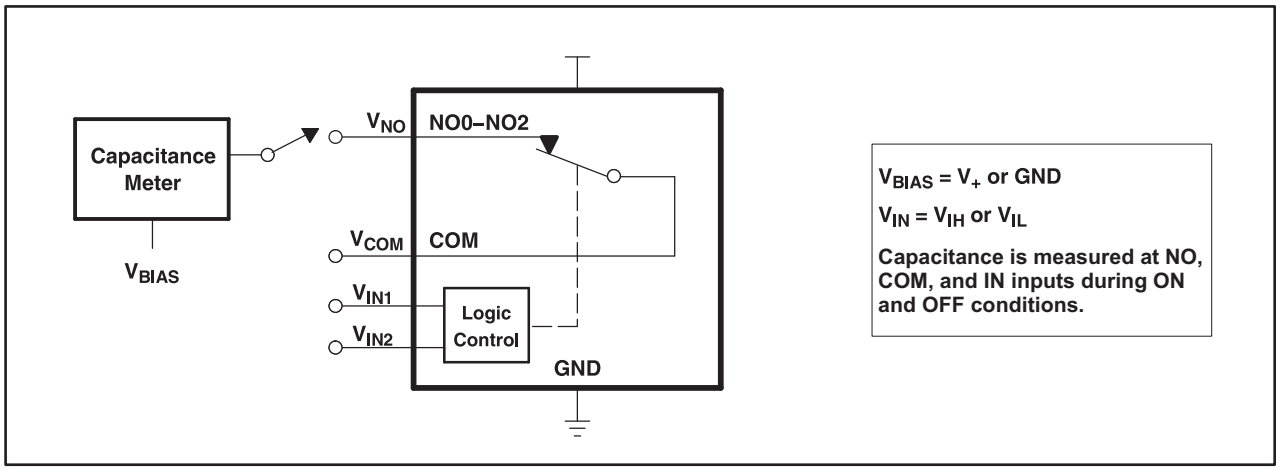
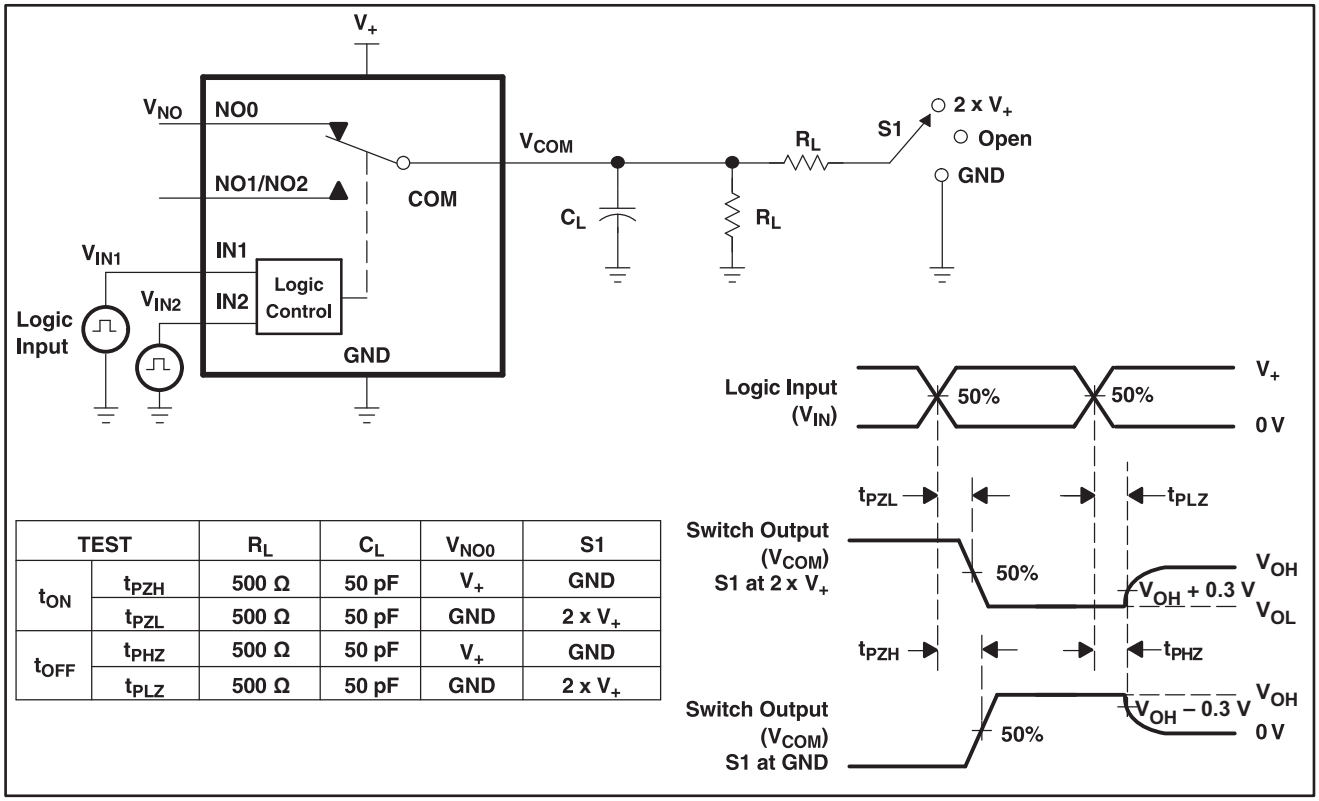


Figure 15. Capacitance (C_I, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{COM(OFF)}$, $C_{NO(ON)}$)

Parameter Measurement Information (continued)

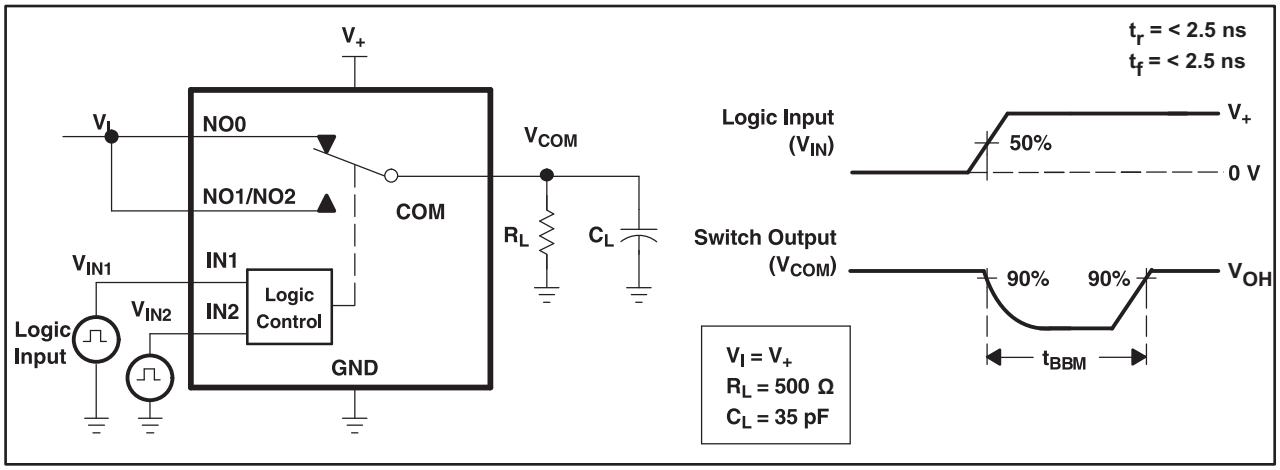


TEST		R_L	C_L	V_{NO0}	S1
t_{ON}	t_{PZH}	500 Ω	50 pF	V_+	GND
	t_{PZL}	500 Ω	50 pF	GND	2 x V_+
t_{OFF}	t_{PHZ}	500 Ω	50 pF	V_+	GND
	t_{PLZ}	500 Ω	50 pF	GND	2 x V_+

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 16. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 17. Break-Before-Make Time (t_{BBM})

Parameter Measurement Information (continued)

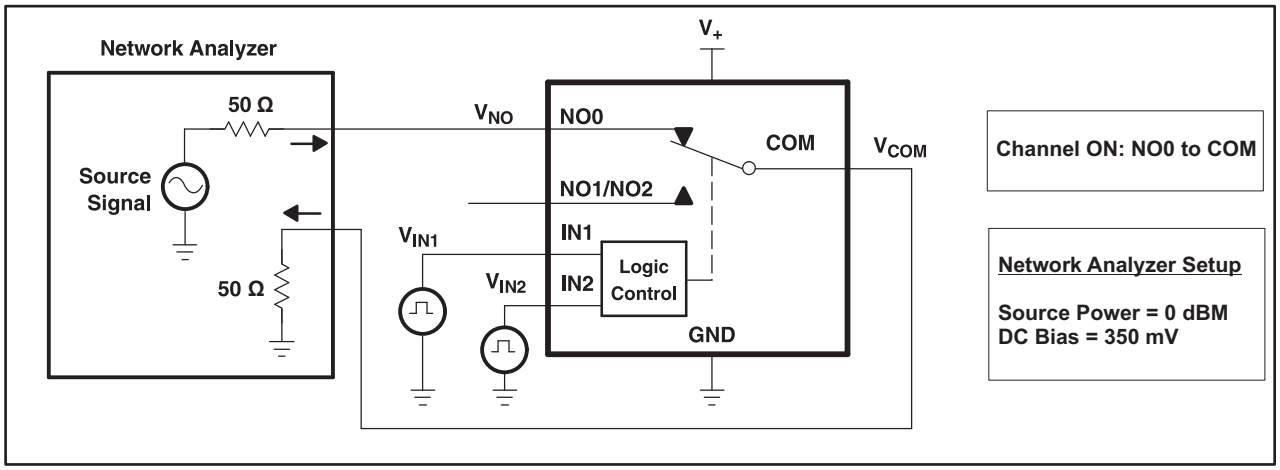


Figure 18. Bandwidth (BW)

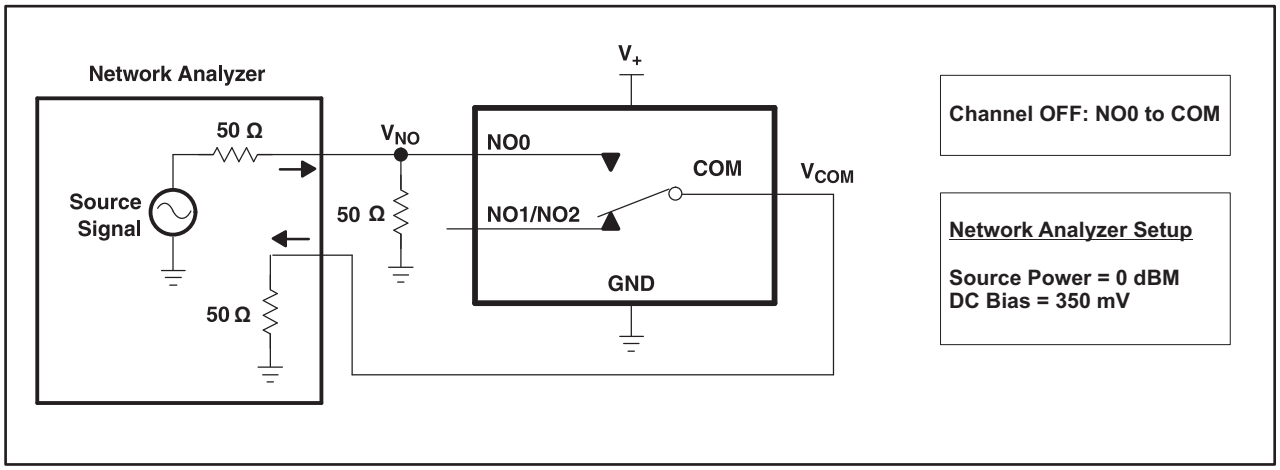


Figure 19. OFF Isolation (O_{ISO})

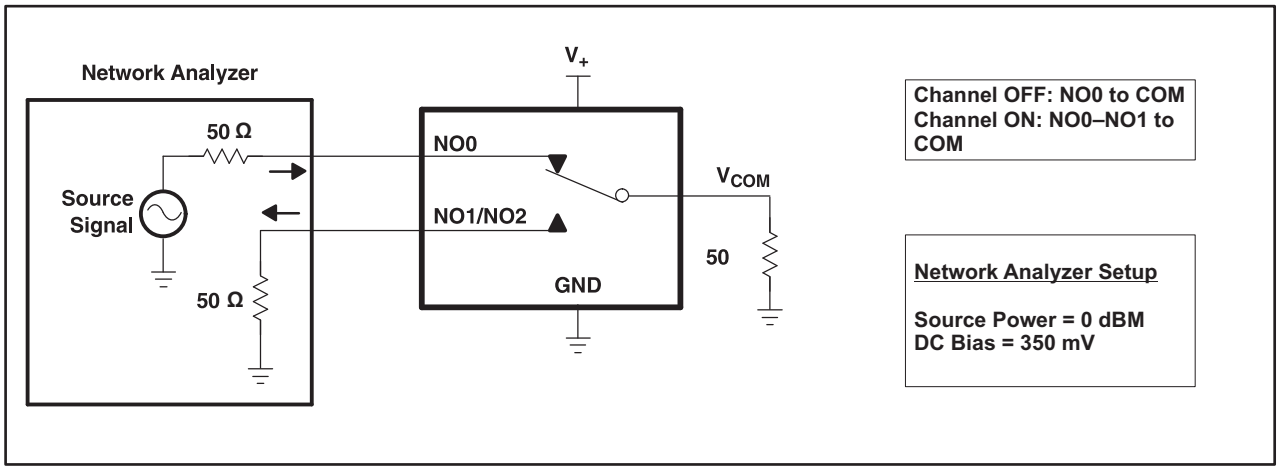
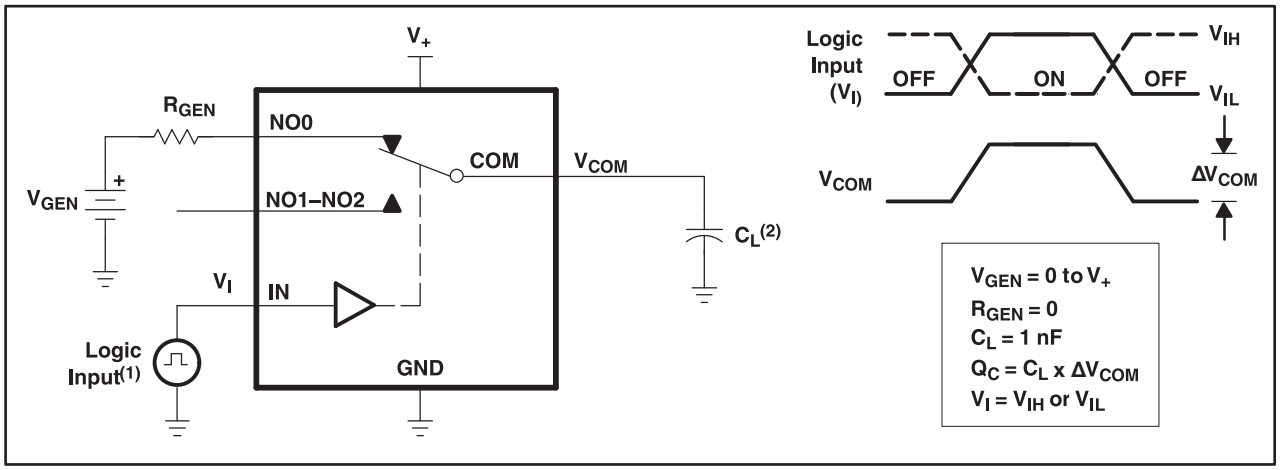


Figure 20. Crosstalk (X_{TALK})

Parameter Measurement Information (continued)



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

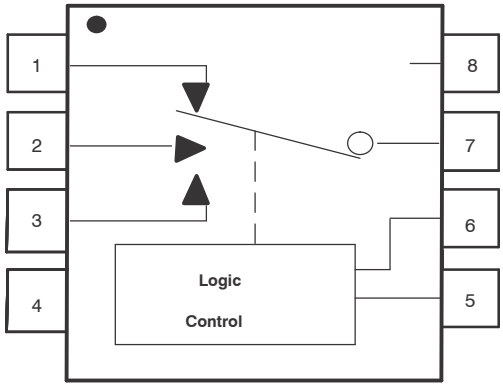
Figure 21. Charge Injection (Q_C)

9 Detailed Description

9.1 Overview

The TS5A3357 is a bidirectional, single-channel, 3:1 analog switch that is designed to operate from 1.65 V to 5.5 V. This device provides a signal switching solution while maintaining excellent signal integrity, which makes the TS5A3357 suitable for a wide range of applications in various markets including personal electronics, portable instrumentation, and test and measurement equipment. The device maintains the signal integrity by its low ON-state resistance, excellent ON-state resistance matching, and total harmonic distortion (THD) performance. To prevent signal distortion during the transferring of a signal from one channel to another, the TS5A3357 device also has a specified break-before-make feature.

9.2 Functional Block Diagram



9.3 Feature Description

Break-before-make

Break-before-make is a safety feature that prevents two inputs from connecting when the TS5A3357 is switching. The TS5A3357 COM pin first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the break and the make is known as a break-before-make delay t_{BBM}.

9.4 Device Functional Modes

The digital control pins IN1 and IN2 determine the state of the connection between the COM and NO pins based on the truth table below.

Table 2. Function Table

IN1	IN2	COM TO NO0	COM TO NO1	COM TO NO2
L	L	OFF	OFF	OFF
H	L	ON	OFF	OFF
L	H	OFF	ON	OFF
H	H	OFF	OFF	ON

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.2 Typical Application

The TS5A3357 switch is bidirectional, so the NO and COM pins can be used as either inputs or outputs. This switch is typically used when there is only one signal path that needs to be able to communicate to 3 different signal paths.

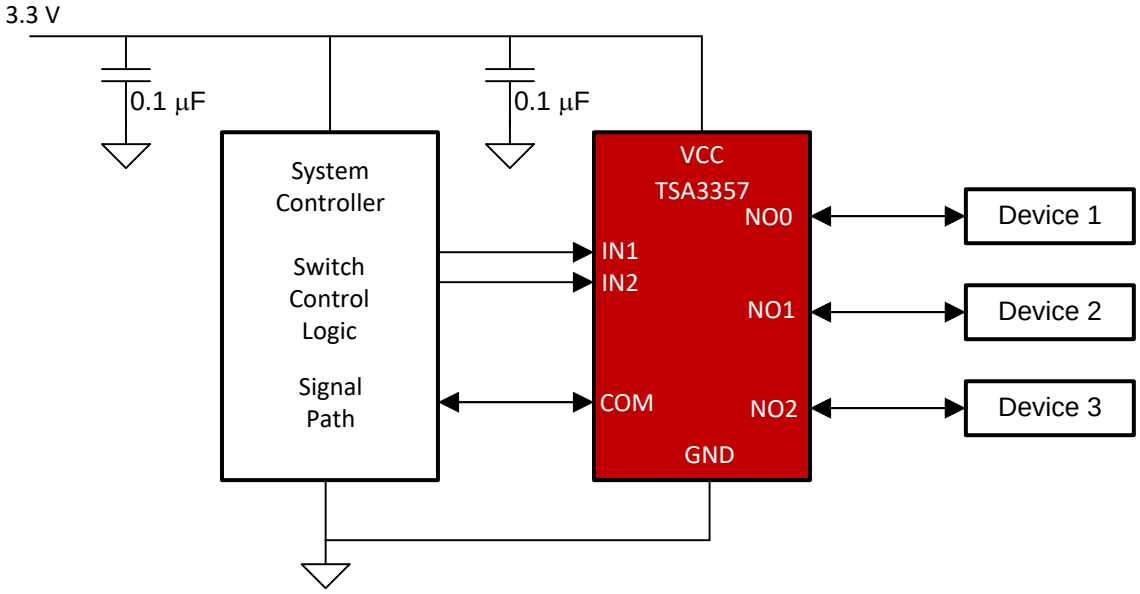


Figure 22. Typical Application Schematic

10.2.1 Design Requirements

The TS5A3357 device can be properly operated without any external components. However, TI recommends connecting unused pins to ground through a 50-Ω resistor to prevent signal reflections back into the device. TI also recommends pulling up the digital control pins (IN1 and IN2) to VCC or pulling down to GND to avoid undesired switch positions that could result from the floating pin.

10.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A3357 input and output signal swing through NO and COM are dependent on the supply voltage V_+. For example, if the desired signal level to pass through the switch is 5 V, VCC must be greater than or equal to 5 V. V_+ = 3.3 V would not be valid for passing a 5-V signal since the Analog signal voltage cannot exceed the supply.

Typical Application (continued)

10.2.3 Application Curves

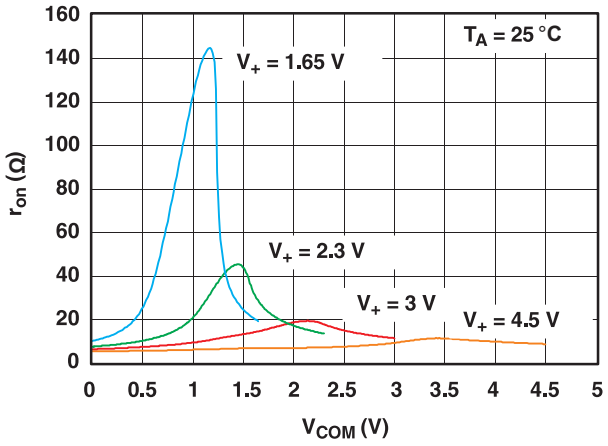


Figure 23. r_{on} vs V_{COM}

11 Power Supply Recommendations

TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence V_+ on first, followed by NO or COM. Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_+ supply to other components. A 0.1-μF capacitor, connected from VCC to GND, is adequate for most applications.

12 Layout

12.1 Layout Guidelines

TI recommends following common printed-circuit board layout guidelines to ensure reliability of the device. Bypass capacitors should be used on power supplies. Short trace lengths should be used to avoid excessive loading.

12.2 Layout Example

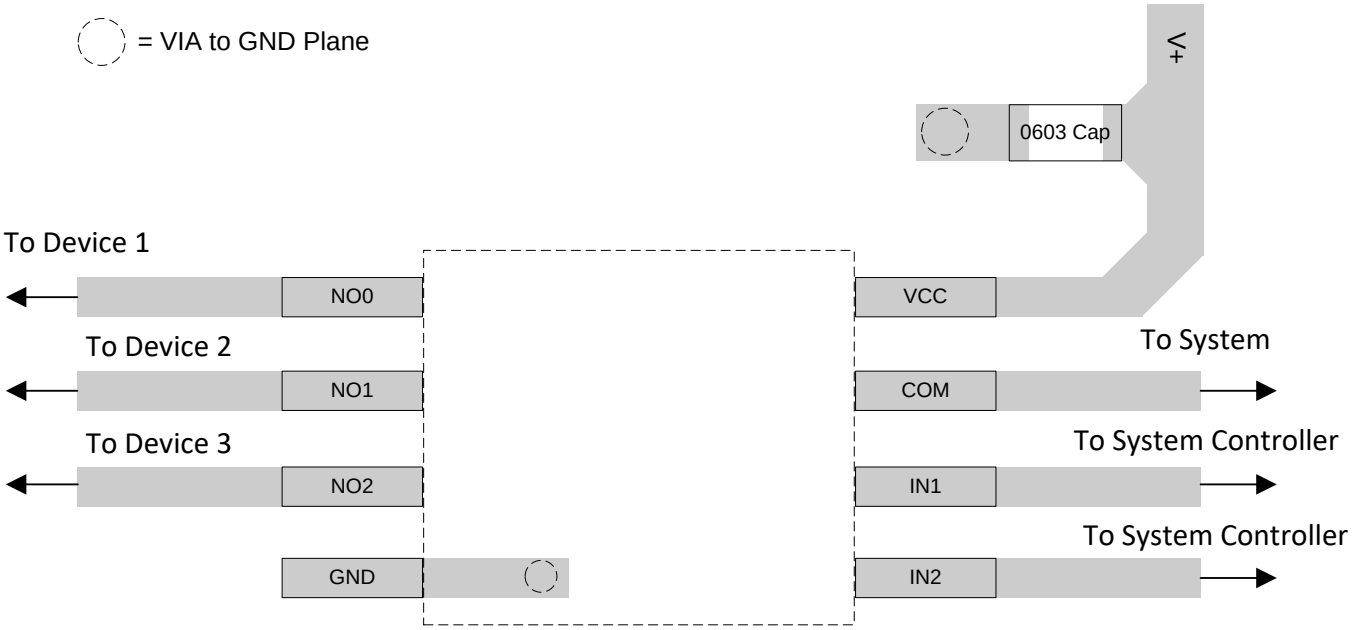


Figure 24. Example Layout

13 器件和文档支持

13.1 器件支持

13.2 文档支持

13.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

13.5 商标

E2E is a trademark of Texas Instruments.

13.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3357DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(JA9Q, JA9R)	Samples
TS5A3357DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JA9R	Samples
TS5A3357DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(JA9Q, JA9R)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

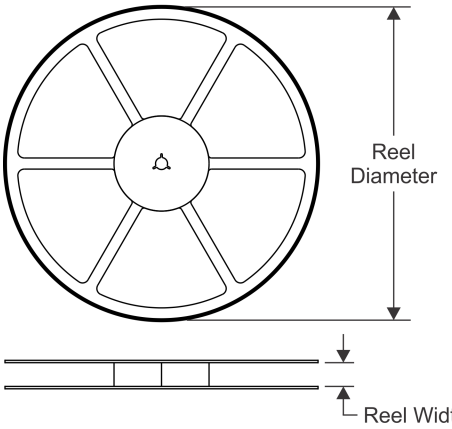
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

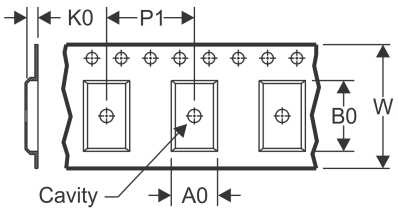
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

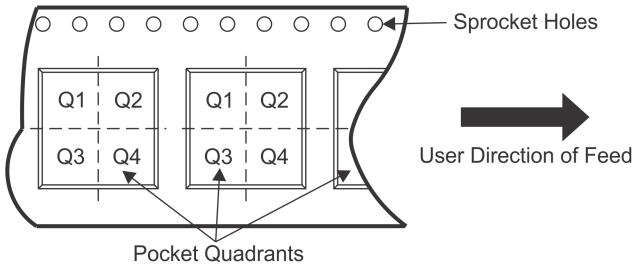


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

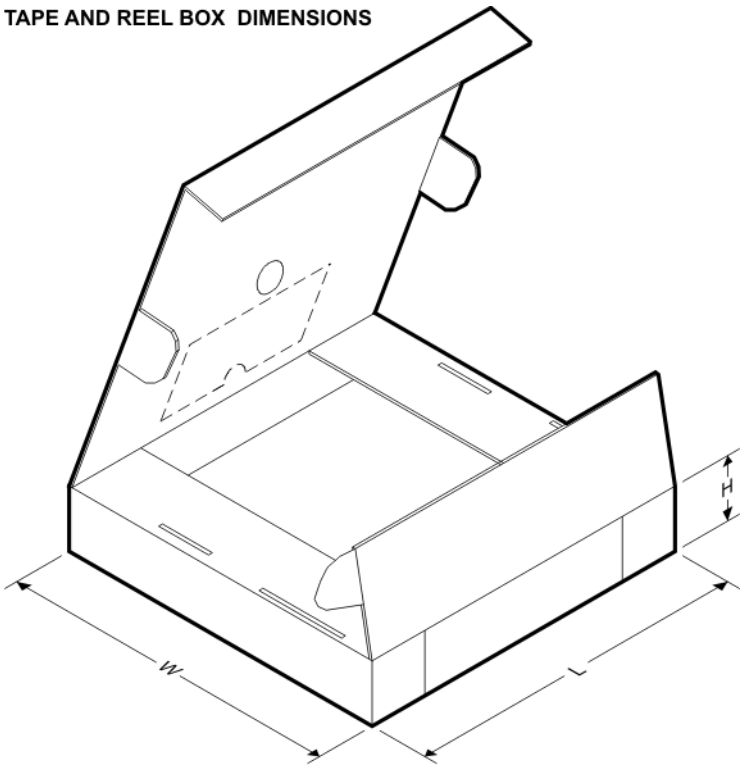
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3357DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A3357DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

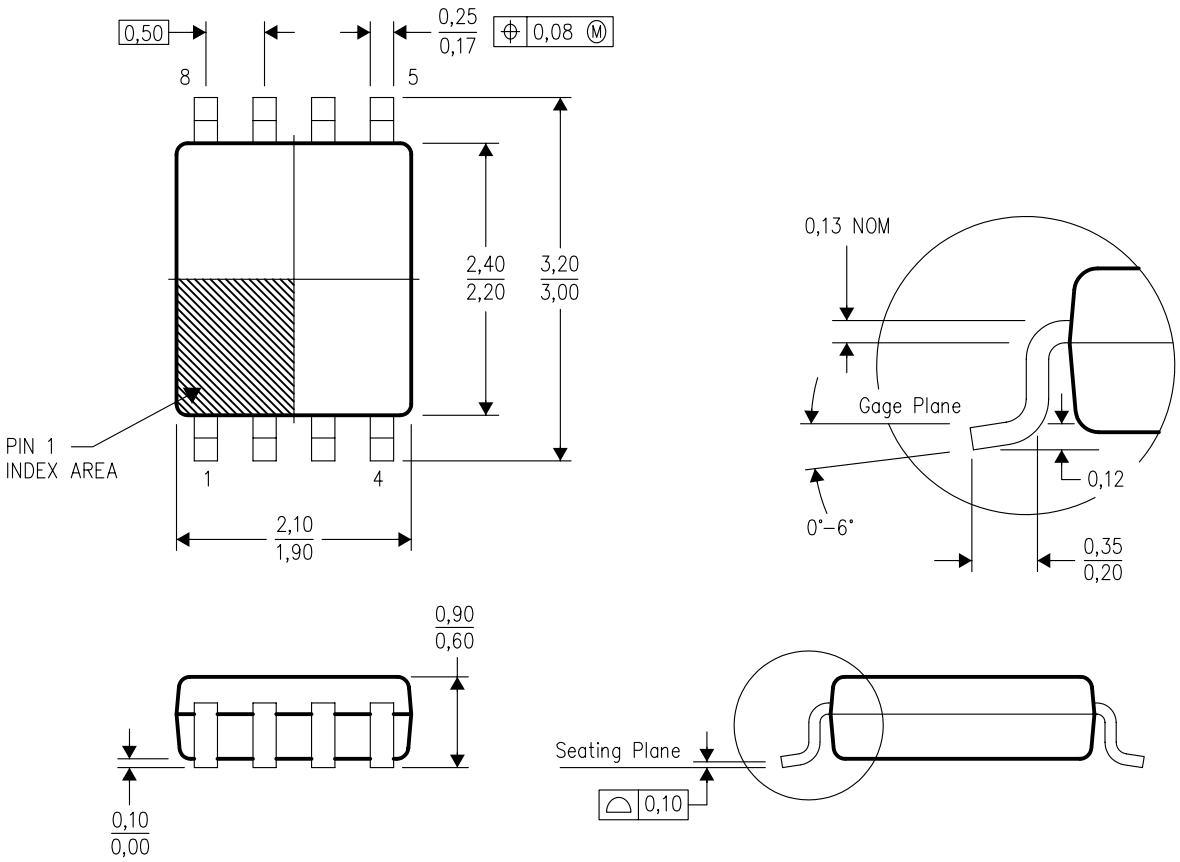
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3357DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A3357DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0

DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



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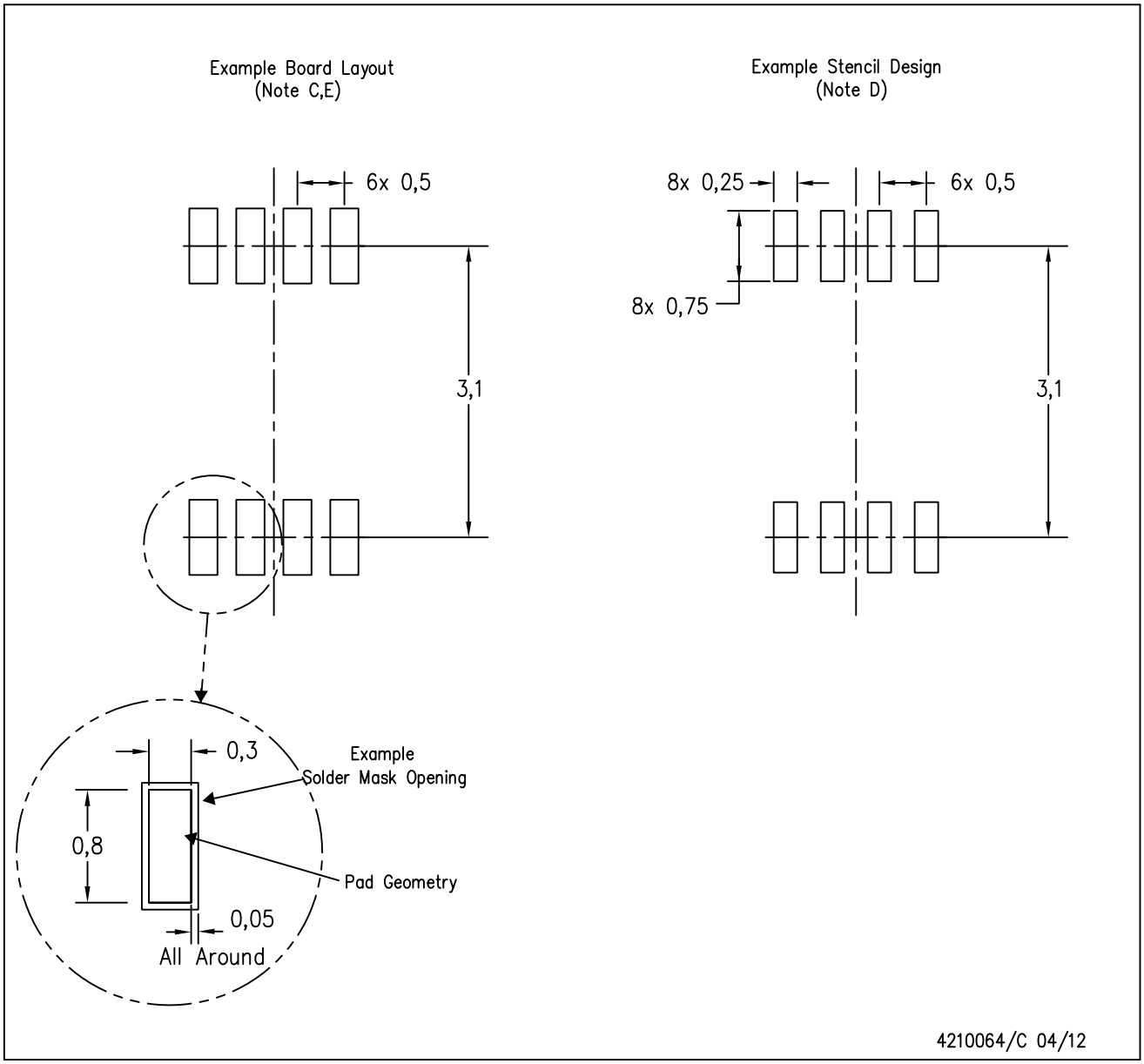
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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