TPS22976 5.7V、6A、14mΩ 导通电阻双通道负载开关

1 特性

- 集成双通道负载开关
- 输入电压范围：0.6V 至 V_{BIAS}
- V_{BIAS} 电压范围：2.5V 至 5.7V
- 导通电阻
  - R_{ON} = 14mΩ（V_{IN} = 0.6V 至 5V，V_{BIAS} = 5V 时的典型值）
  - R_{ON} = 18mΩ（V_{IN} = 0.6V 至 2.5V，V_{BIAS} = 2.5V 时的典型值）
- 每通道最大 6A 持续开关电流
- 静态电流
  - 37µA（V_{IN} = V_{BIAS} = 5V 时双通道的典型值）
  - 35µA（V_{IN} = V_{BIAS} = 5V 时单通道的典型值）
- 控制输入阈值，支持使用 1.2V、1.8V、2.5V 和 3.3V 逻辑器件
- 可配置的上升时间
- 热关断
- 快速输出放电 (QOD)（可选）
- 带有散热焊盘的 14 引脚小外形尺寸无引线 (SON) 封装
- 根据 JESD 22 测试得出的静电放电 (ESD) 性能
  - 2kV 人体放电模式 (HBM) 和 1kV 器件充电模型 (CDM)

2 应用

- Ultrabook™
- 笔记本电脑和上网本
- 平板电脑
- 机顶盒和家庭网关
- 电信系统
- 固态硬盘 (SSD)

3 说明

TPS22976 产品系列包括 2 款器件：TPS22976 和 TPS22976N。每款器件都是一个接通受控的双通道负载开关。此器件包含两个可在 0.6V 至 5.7V 输入电压范围内运行的 N 沟道 MOSFET，并且每通道可支持最大 6A 的持续电流。每个开关可由一个导通/关断输入（ON1 和 ON2）独立控制，此输入可与低压控制信号直接连接。TPS22976 能够在结温超出阈值时热关断，以此关断开关。开关会在结温稳定在安全范围内时再次导通。此外，TPS22976 还包含一个可选 230Ω 片上负载电阻，用于在此开关被关断时进行快速输出放电。

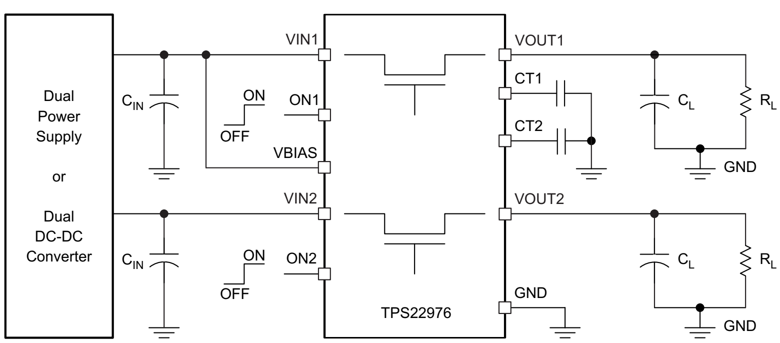
TPS22976 采用小型、节省空间的3mm × 2mm 14-SON (DPU) 封装，此类封装集成有散热焊盘，支持较高功耗。器件在自然通风环境下的额定运行温度范围为 –40°C 至 105℃。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS22976 TPS22976N	WSON (14)	3.00mm x 2.00mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

应用电路



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4 修订历史记录

Changes from Revision A (March 2017) to Revision B	Page
• Updated V_{IH} in *Recommended Operating Conditions*	4

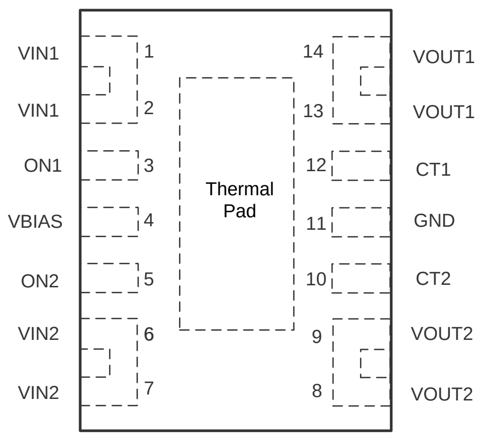
Changes from Original (February 2016) to Revision A	Page
• Updated statement for Equation 4 in *Adjustable Rise Time* section from "CT = 0 pF" to "CT < 100 pF"	22

5 Device Comparison Table

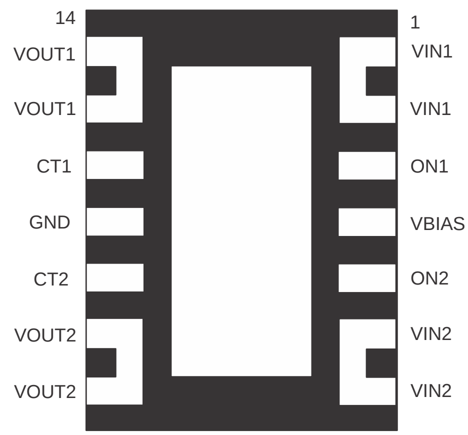
DEVICE	R_{ON} AT V_{IN} = V_{BIAS} = 5 V (TYPICAL)	QUICK OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22976	14 mΩ	Yes	6 A	Active high
TPS22976N	14 mΩ	No	6 A	Active high

6 Pin Configuration and Functions

DPU Package
14-Pin WSON with Exposed Thermal Pad
Top View



DPU Package
14-Pin WSON with Exposed Thermal Pad
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1, 2	VIN1	I	Switch 1 input. Recommended voltage range for these pins for optimal R_{ON} performance is 0.6 V to V_{BIAS}. Place an optional decoupling capacitor between these pins and GND to reduce V_{IN1} dip during turnon of the channel. See the *Application Information* section for more information
3	ON1	I	Active-high switch 1 control input. Do not leave floating
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.7 V. See the *Application Information* section
5	ON2	I	Active-high switch 2 control input. Do not leave floating
6, 7	VIN2	I	Switch 2 input. Recommended voltage range for these pins for optimal R_{ON} performance is 0.6 V to V_{BIAS}. Place an optional decoupling capacitor between these pins and GND to reduce V_{IN2} dip during turnon of the channel. See the *Application Information* section for more information
8, 9	VOUT2	O	Switch 2 output
10	CT2	O	Switch 2 slew rate control. Can be left floating. Capacitor used on this pin must be rated for a minimum of 25 V for desired rise time performance
11	GND	—	Ground
12	CT1	O	Switch 1 slew rate control. Can be left floating. Capacitor used on this pin must be rated for a minimum of 25 V for desired rise time performance
13, 14	VOUT1	O	Switch 1 output
—	Thermal pad	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See the *Layout* section for layout guidelines

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT[2]
$V_{IN1,2}$	Input voltage	–0.3	6	V
$V_{OUT1,2}$	Output voltage	–0.3	6	V
$V_{ON1,2}$	ON-pin voltage	–0.3	6	V
V_{BIAS}	Bias voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current per channel		6	A
I_{PLS}	Maximum pulsed switch current per channel, pulse < 300 µs, 3% duty cycle		8	A
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{IN1,2}$	Input voltage		0.6	V_{BIAS}	V
V_{BIAS}	Bias voltage		2.5	5.7	V
$V_{ON1,2}$	ON voltage		0	5.7	V
$V_{OUT1,2}$	Output voltage			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{BIAS} = 2.5 V to 5 V, T_A< 85°C	1.05	5.7	V
		V_{BIAS} = 2.5 V to 5.7 V, T_A< 105°C	1.2	5.7	
V_{IL}	Low-level input voltage, ON	V_{BIAS} = 2.5 V to 5.7 V	0	0.5	V
$C_{IN1,2}$	Input capacitor		1[1]		µF
T_A	Operating free-air temperature [2]		–40	105	°C

(1) See the *Input Capacitor (Optional)* section.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $TA_{(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$

7.4 Thermal Information

THERMAL METRIC[1]		TPS22976 DPU (WSON) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Thermal Information (continued)

THERMAL METRIC(1)		TPS22976 DPU (WSON) 14 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	18.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.5	°C/W

7.5 Electrical Characteristics—V_{BIAS} = 5 V

Unless otherwise noted, the specifications in the following table applies where V_{BIAS} = 5 V. Typical values are for T_A = 25°C

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q,VBIAS}$	V_{BIAS} quiescent current (both channels)	I_{OUT1} = I_{OUT2} = 0 mA, $V_{IN1,2}$ = $V_{ON1,2}$ = 5 V		–40°C to +85°C		37	48	µA
				–40°C to +105°C			49	
	V_{BIAS} quiescent current (single channel)	I_{OUT1} = I_{OUT2} = 0 mA, V_{ON2} = 0 V $V_{IN1,2}$ = V_{ON1} = 5 V		–40°C to +85°C		35	43	µA
				–40°C to +105°C			44	
$I_{SD,VBIAS}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{VOUT1,2}$ = 0 V		–40°C to +105°C		1.37	2.3	µA
$I_{SD,VIN}$	V_{IN} shutdown current (per channel)	V_{ON} = 0 V, V_{OUT} = 0 V	V_{IN} = 5 V	–40°C to +85°C		.005	5.5	µA
				–40°C to +105°C			11.3	
			V_{IN} = 3.3 V	–40°C to +85°C		.002	1.4	
				–40°C to +105°C			3.4	
			V_{IN} = 1.8 V	–40°C to +85°C		.002	0.5	
				–40°C to +105°C			1.4	
			V_{IN} = 0.6 V	–40°C to +85°C		.001	0.3	
				–40°C to +105°C			0.8	
I_{ON}	ON-pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	On-state resistance (per channel)	I_{OUT} = –200 mA	V_{IN} = 5 V	25°C		14	18	mΩ
				–40°C to +85°C			22	
				–40°C to +105°C			23	
			V_{IN} = 3.3 V	25°C		14	18	
				–40°C to +85°C			22	
				–40°C to +105°C			23	
			V_{IN} = 1.8 V	25°C		14	18	
				–40°C to +85°C			22	
				–40°C to +105°C			23	
			V_{IN} = 1.2 V	25°C		14	18	
				–40°C to +85°C			22	
				–40°C to +105°C			23	
			V_{IN} = 1.05 V	25°C		14	18	
				–40°C to +85°C			22	
				–40°C to +105°C			23	
			V_{IN} = 0.6 V	25°C		14	18	
				–40°C to +85°C			22	
				–40°C to +105°C			23	
$V_{ON,HYS}$	ON-pin hysteresis	V_{IN} = 5 V		25°C		90		mV
R_{PD}(1)	Output pulldown resistance	V_{IN} = V_{OUT} = 5 V, V_{ON} = 0 V		–40°C to +105°C		230	280	Ω
T_{SD}	Thermal shutdown	Junction temperature rising		—		160		ºC
$T_{SD,HYS}$	Thermal-shutdown hysteresis	Junction temperature falling		—		20		ºC

(1) Not present in TPS22976N

7.6 Electrical Characteristics—V_{BIAS} = 2.5 V

Unless otherwise noted, the specifications in the following table applies where V_{VBIAS} = 2.5 V. Typical values are for T_A = 25°C

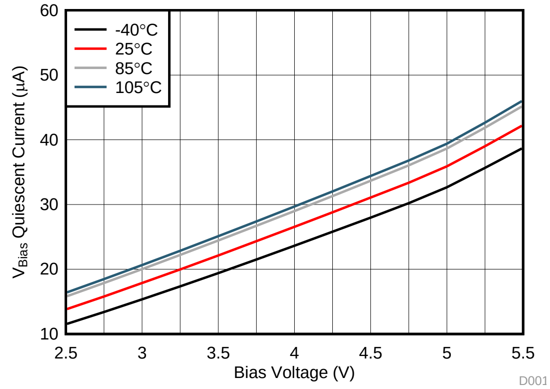
PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q,VBIAS}$	V_{BIAS} quiescent current (both channels)	I_{OUT1} = I_{OUT2} = 0 mA, $V_{IN1,2}$ = $V_{ON1,2}$ = 2.5 V		–40°C to +85°C		15	20	µA
				–40°C to +105°C			20	
	V_{BIAS} quiescent current (single channel)	I_{OUT1} = I_{OUT2} = 0 mA, V_{ON2} = 0 V $V_{IN1,2}$ = V_{ON1} = 2.5 V		–40°C to +85°C		14	19	µA
				–40°C to +105°C			19	
$I_{SD,VBIAS}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{VOUT1,2}$ = 0 V		–40°C to +105°C		.58	1.1	µA
$I_{SD,VIN}$	V_{IN} shutdown current (per channel)	V_{ON} = 0 V, V_{OUT} = 0 V	V_{IN} = 2.5 V	–40°C to +85°C		.005	0.8	µA
				–40°C to +105°C			2.1	
			V_{IN} = 1.8 V	–40°C to +85°C		.002	0.5	
				–40°C to +105°C			1.4	
			V_{IN} = 1.05 V	–40°C to +85°C		.002	0.3	
				–40°C to +105°C			1	
			V_{IN} = 0.6 V	–40°C to +85°C		.001	0.3	
				–40°C to +105°C			0.8	
I_{ON}	ON-pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	On-state resistance (per channel)	I_{OUT} = –200 mA	V_{IN} = 2.5 V	25°C		18	23	mΩ
				–40°C to +85°C			28	
				–40°C to +105°C			30	
			V_{IN} = 1.8 V	25°C		16	23	
				–40°C to +85°C			28	
				–40°C to +105°C			29	
			V_{IN} = 1.5 V	25°C		16	22	
				–40°C to +85°C			27	
				–40°C to +105°C			28	
			V_{IN} = 1.2 V	25°C		16	21	
				–40°C to +85°C			26	
				–40°C to +105°C			28	
			V_{IN} = 1.05 V	25°C		16	21	
				–40°C to +85°C			25	
				–40°C to +105°C			27	
			V_{IN} = 0.6 V	25°C		15	20	
				–40°C to +85°C			25	
				–40°C to +105°C			26	
$V_{ON,HYS}$	ON-pin hysteresis	V_{IN} = 2.5 V		25°C		70		mV
R_{PD} (1)	Output pulldown resistance	V_{IN} = V_{OUT} = 2.5 V, V_{ON} = 0 V		–40°C to +105°C		250	330	Ω
T_{SD}	Thermal shutdown	Junction temperature rising		—		160		ºC
$T_{SD,HYS}$	Thermal-shutdown hysteresis	Junction temperature falling		—		20		ºC

(1) Not present in TPS22976N

7.7 Switching Characteristics

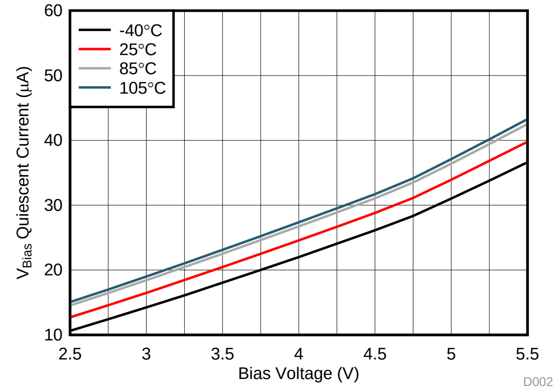
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1490		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		3		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1770		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		620		µs
V_{IN} = 0.6 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		620		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		3		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		285		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		460		µs
V_{IN} = 2.5 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2350		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		4		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2275		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1210		µs
V_{IN} = 0.6 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1410		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		5		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		700		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1030		µs

7.8 Typical DC Characteristics



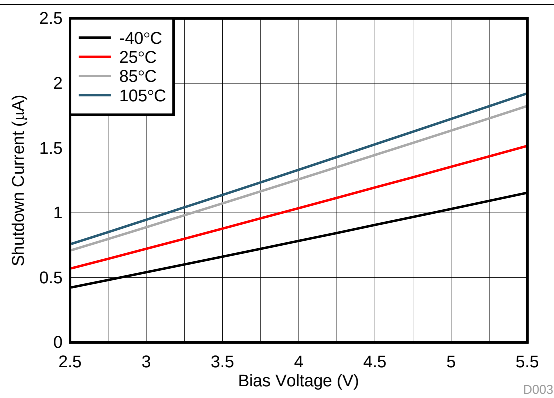
$V_{IN1} = V_{IN2} = V_{BIAS}$ $V_{ON1} = V_{ON2} = 5$ V V_{OUT} = Open

Figure 1. V_{BIAS} Quiescent Current vs Bias Voltage Both Channels



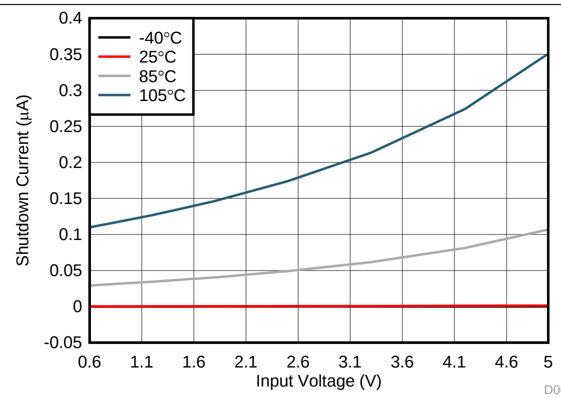
$V_{IN1} = V_{BIAS}$ $V_{ON1} = 5$ V V_{OUT} = Open

Figure 2. V_{BIAS} Quiescent Current vs Bias Voltage Single Channel



$V_{IN1} = V_{IN2} = V_{BIAS}$ $V_{ON1} = V_{ON2} = 0$ V $V_{OUT} = 0$ V

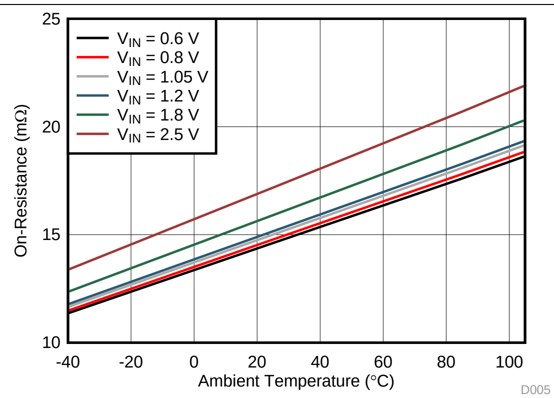
Figure 3. V_{BIAS} Shutdown Current vs Bias Voltage Both Channels



$V_{BIAS} = 5$ V $V_{ON} = 0$ V $V_{OUT} = 0$ V

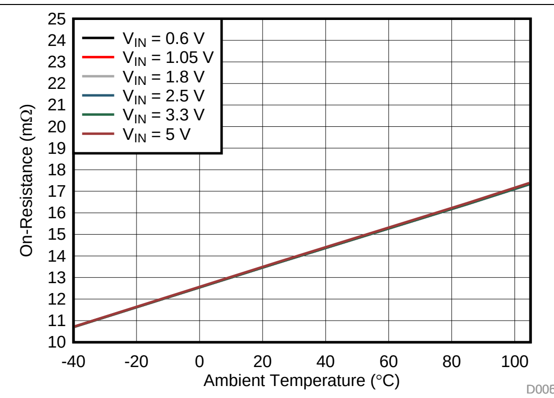
Note: –40°C and 25°C curves have similar values, therefore only one line is visible.

Figure 4. Off-State V_{IN} Current vs Input Voltage Single Channel



$V_{BIAS} = 2.5$ V $I_{OUT} = -200$ mA $V_{ON} = 5$ V

Figure 5. On-Resistance vs Ambient Temperature Single Channel

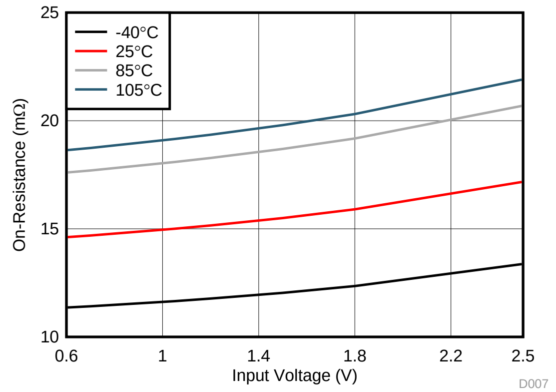


$V_{BIAS} = 5$ V $I_{OUT} = -200$ mA $V_{ON} = 5$ V

Note: All R_{ON} curves have similar values, therefore only one line is visible.

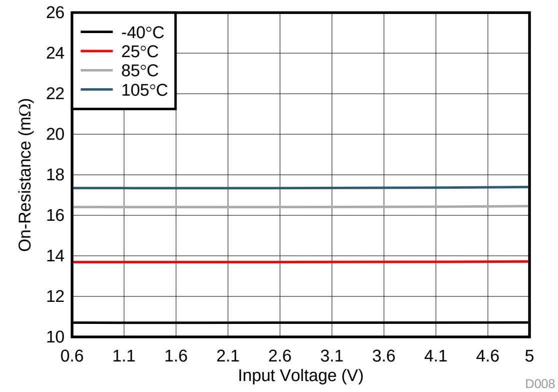
Figure 6. On-Resistance vs Ambient Temperature Single Channel

Typical DC Characteristics (continued)



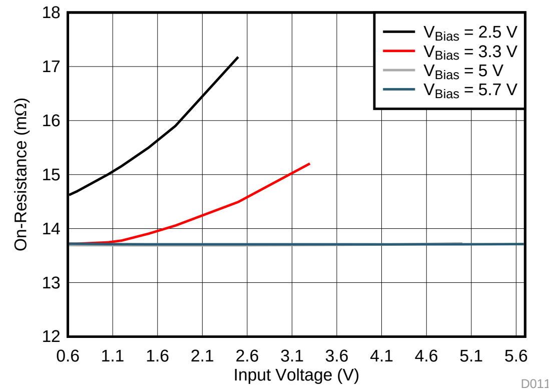
V_{BIAS} = 2.5 V I_{OUT} = –200 mA V_{ON} = 5 V

Figure 7. On-Resistance vs Input Voltage Single Channel - Across Ambient Temperatures



V_{BIAS} = 5 V I_{OUT} = –200 mA V_{ON} = 5 V

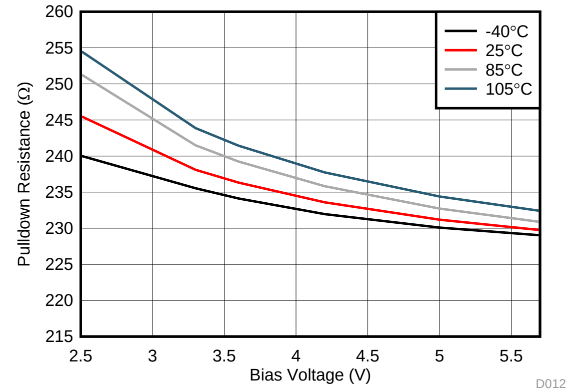
Figure 8. On-Resistance vs Input Voltage Single Channel - Across Ambient Temperatures



T_A = 25°C

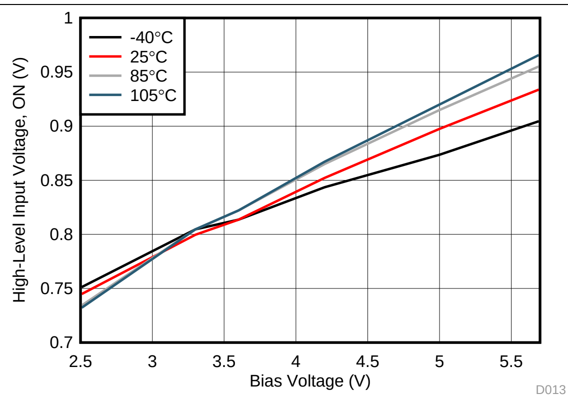
Note: V_{BIAS} = 5 V and 5.7 V curves have similar values, therefore only one line is visible.

Figure 9. On-Resistance vs Input Voltage Single Channel - Across V_{BIAS}



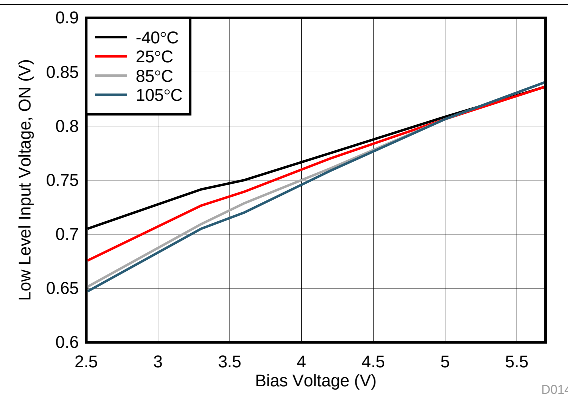
V_{IN} = 2.5 V V_{ON} = 0 V

Figure 10. Pulldown Resistance vs Bias Voltage Single Channel



V_{IN} = V_{BIAS}

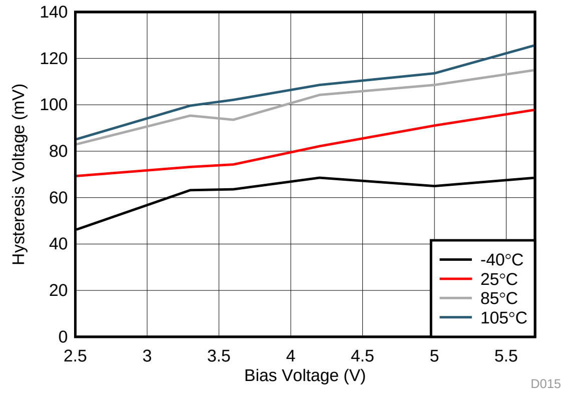
Figure 11. High-Level Input Voltage vs Bias Voltage



V_{IN} = V_{BIAS}

Figure 12. Low-Level Input Voltage vs Bias Voltage

Typical DC Characteristics (continued)

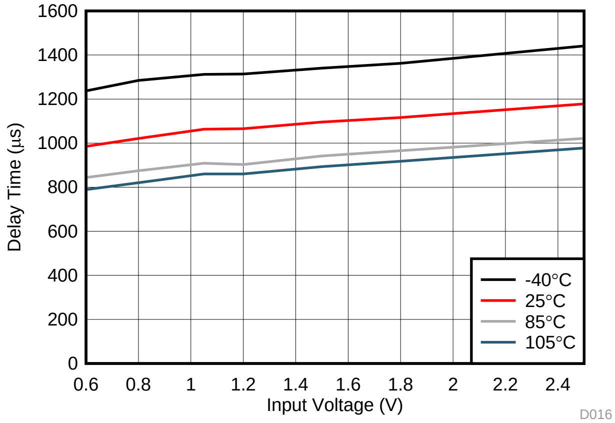


$V_{IN} = V_{BIAS}$

Figure 13. Voltage Input Hysteresis vs Bias Voltage

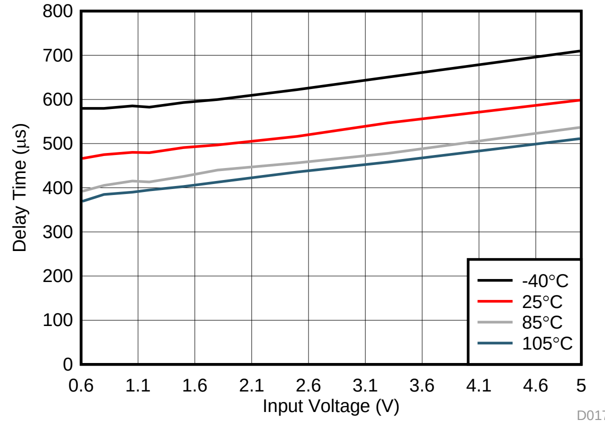
7.9 Typical AC Characteristics

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{ON} = 5 V



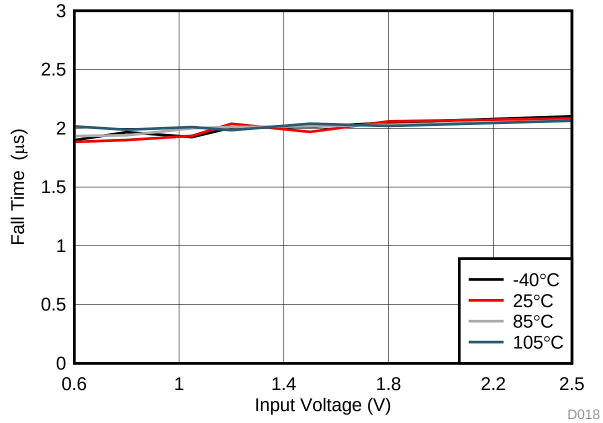
V_{BIAS} = 2.5 V

Figure 14. Delay Time vs Input Voltage



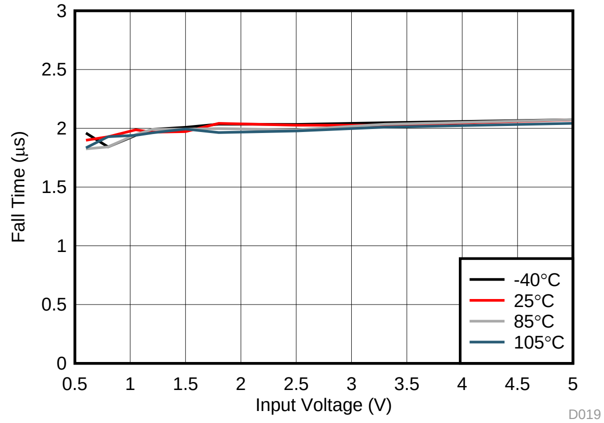
V_{BIAS} = 5 V

Figure 15. Delay Time vs Input Voltage



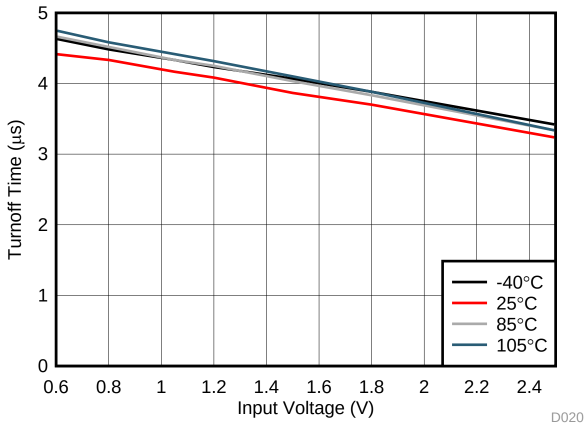
V_{BIAS} = 2.5 V

Figure 16. Fall Time vs Input Voltage



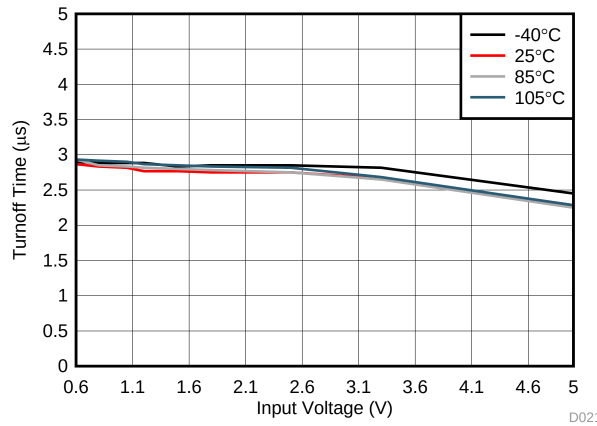
V_{BIAS} = 5 V

Figure 17. Fall Time vs Input Voltage



V_{BIAS} = 2.5 V

Figure 18. Turnoff Time vs Input Voltage

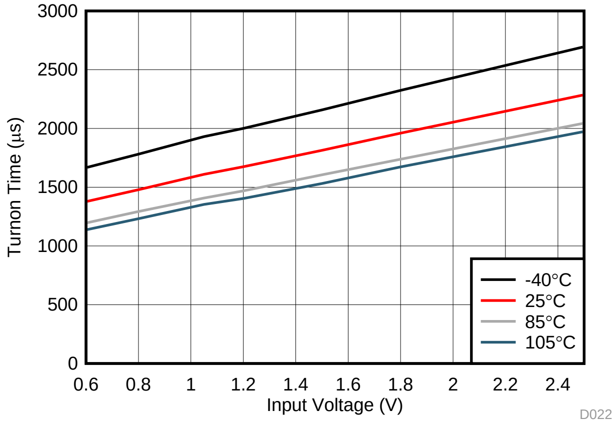


V_{BIAS} = 5 V

Figure 19. Turnoff Time vs Input Voltage

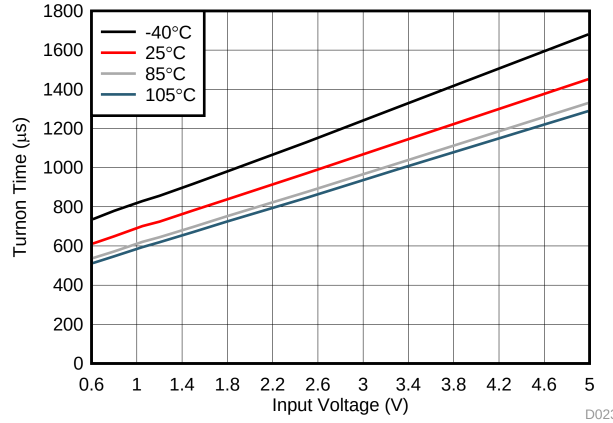
Typical AC Characteristics (continued)

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{ON} = 5 V



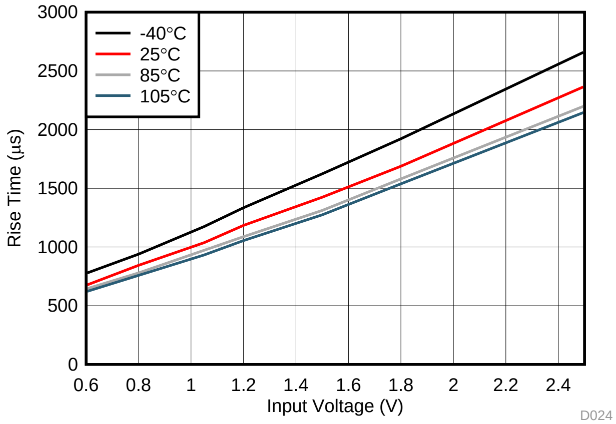
V_{BIAS} = 2.5 V

Figure 20. Turnon Time vs Input Voltage



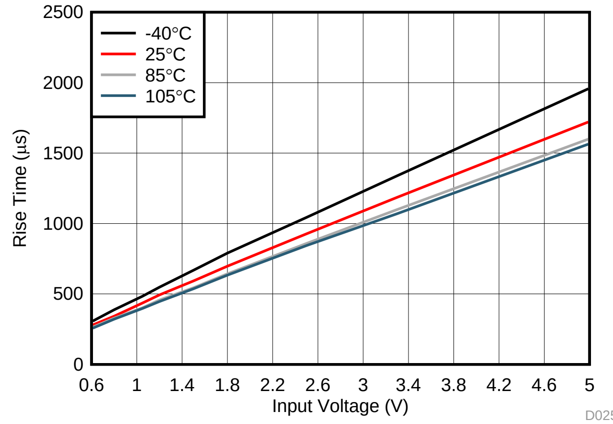
V_{BIAS} = 5 V

Figure 21. Turnon Time vs Input Voltage



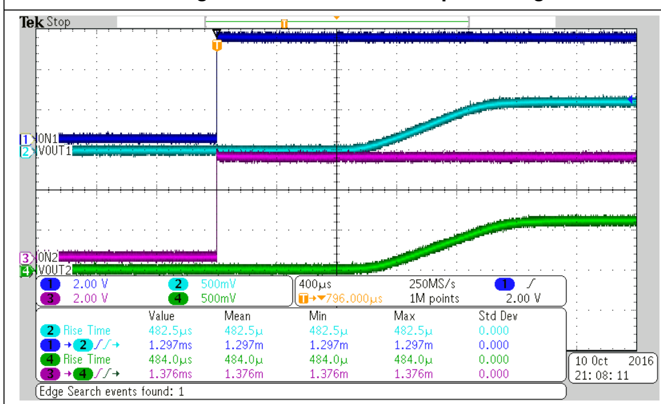
V_{BIAS} = 2.5 V

Figure 22. Rise Time vs Input Voltage



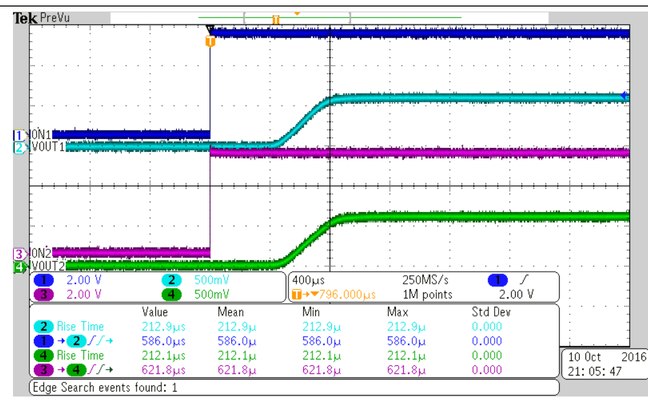
V_{BIAS} = 5 V

Figure 23. Rise Time vs Input Voltage



V_{IN} = 0.6 V V_{BIAS} = 2.5 V

Figure 24. Turnon Response Time

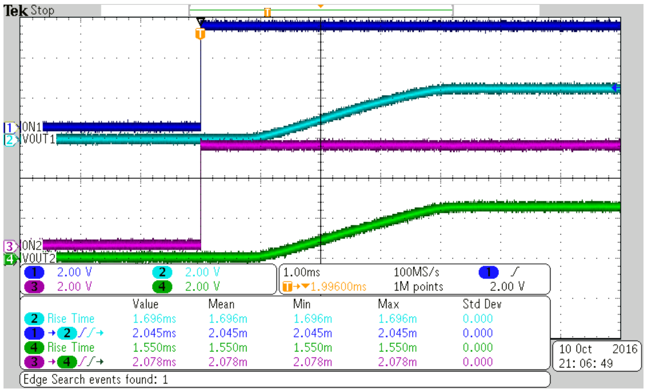


V_{IN} = 0.6 V V_{BIAS} = 5 V

Figure 25. Turnon Response Time

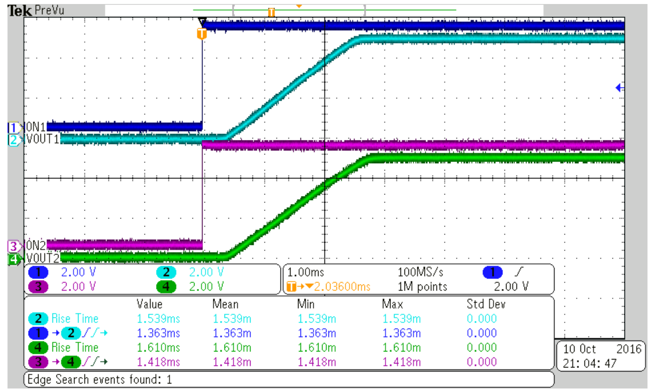
Typical AC Characteristics (continued)

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{ON} = 5 V



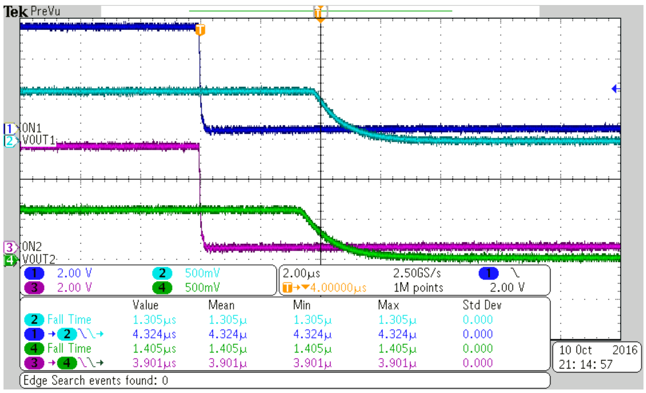
V_{IN} = 2.5 V V_{BIAS} = 2.5 V

Figure 26. Turnon Response Time



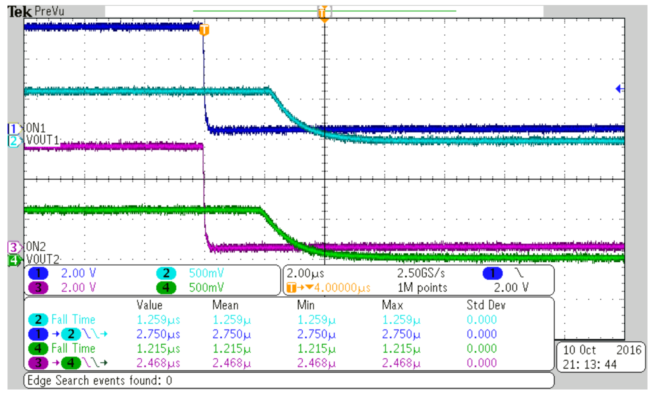
V_{IN} = 5 V V_{BIAS} = 5 V

Figure 27. Turnon Response Time



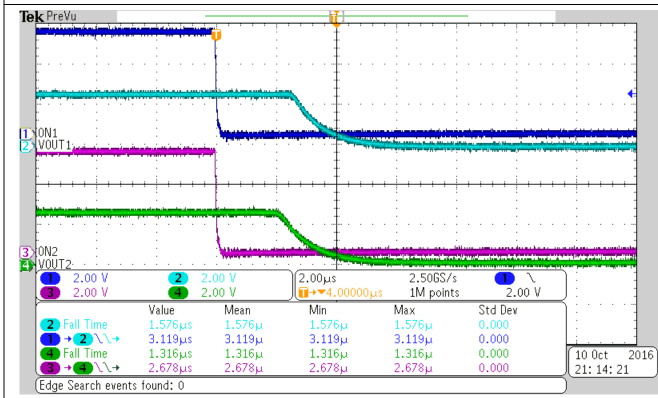
V_{IN} = 0.6 V V_{BIAS} = 2.5 V

Figure 28. Turnoff Response Time



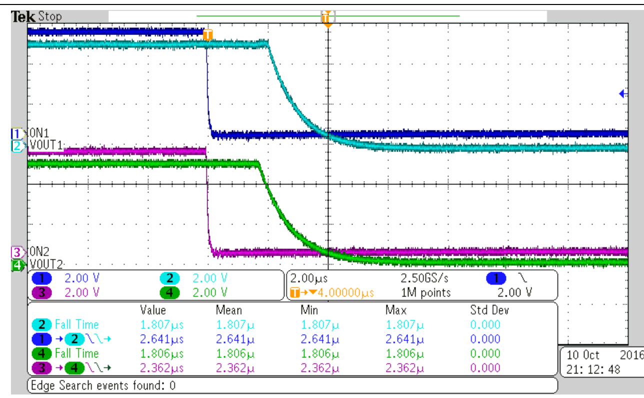
V_{IN} = 0.6 V V_{BIAS} = 5 V

Figure 29. Turnoff Response Time



V_{IN} = 2.5 V V_{BIAS} = 2.5 V

Figure 30. Turnoff Response Time



V_{IN} = 5 V V_{BIAS} = 5 V

Figure 31. Turnoff Response Time

8 Parameter Measurement Information

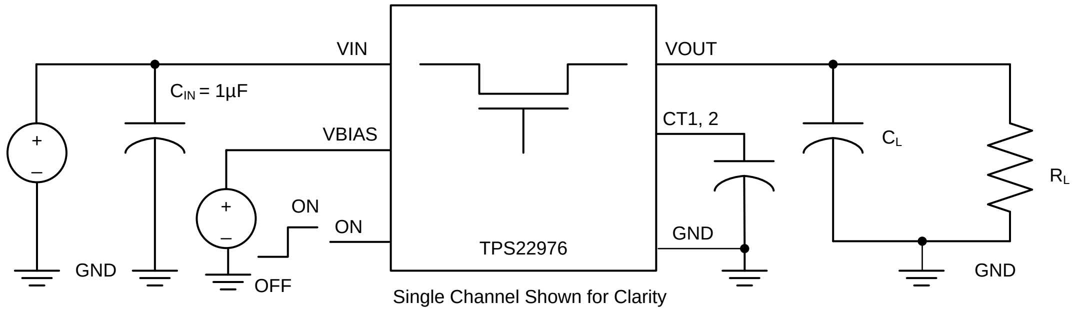


Figure 32. Test Circuit

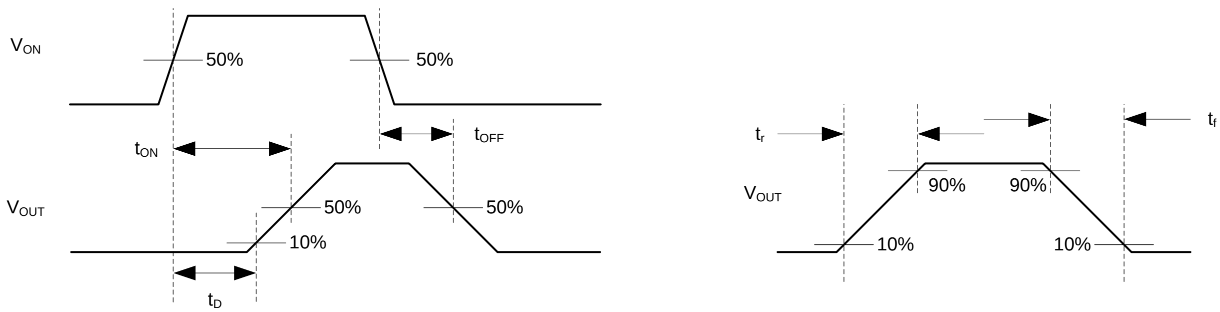


Figure 33. t_{ON} and t_{OFF} Waveforms

9 Detailed Description

9.1 Overview

The TPS22976 is a 5.7-V, dual-channel, 14-mΩ (typical) R_{ON} load switch in a 14-pin WSON package. Each channel can support a maximum continuous current of 6 A and is controlled by an on and off GPIO-compatible input. To reduce the voltage drop in high current rails, the device implements N-channel MOSFETs. Note that the ON pins must be connected and cannot be left floating. The device has a configurable slew rate for applications that require specific rise-time, which controls the inrush current. By controlling the inrush current, power supply sag can be reduced during turnon. Furthermore, the slew rate is proportional to the capacitor on the CT pin. See the *Adjustable Rise Time* section to determine the correct CT value for a desired rise time.

The internal circuitry is powered by the V_{BIAS} pin, which supports voltages from 2.5 V to 5.7 V. This circuitry includes the charge pump, QOD (optional), and control logic. When a voltage is applied to V_{BIAS}, and the $ON_{1,2}$ pins transition to a low state, the QOD functionality is activated. This connects V_{OUT1} and V_{OUT2} to ground through the on-chip resistor. The typical pulldown resistance (R_{PD}) is 230 Ω.

During the off state, the device prevents downstream circuits from pulling high standby current from the supply. The integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, reducing solution size and bill of materials (BOM) count.

9.2 Functional Block Diagram

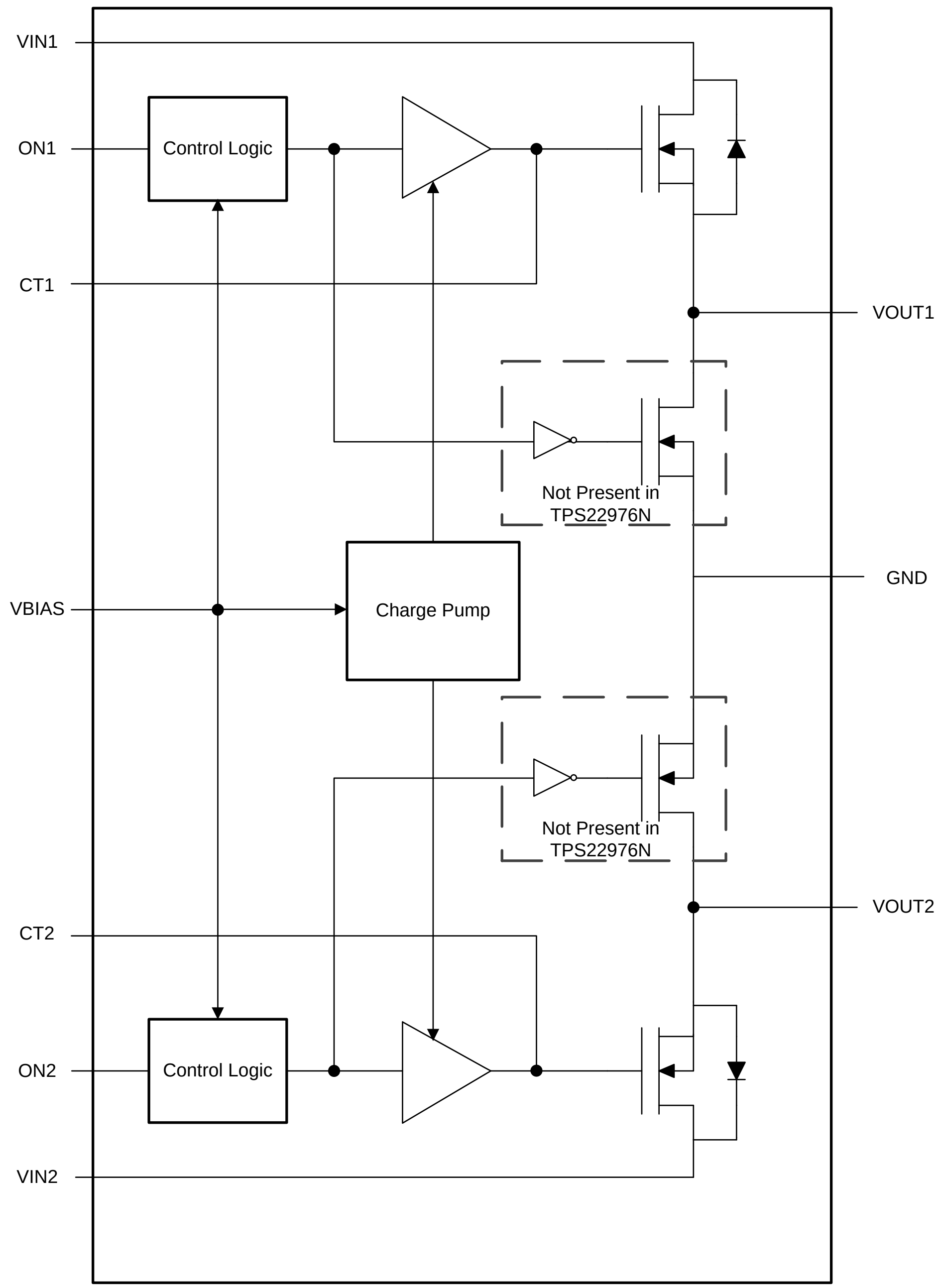


Figure 34. TPS22976 Functional Block Diagram

9.3 Feature Description

9.3.1 ON and OFF Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high with a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

Feature Description (continued)

9.3.2 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

9.3.3 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turnon due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time. (See the *Adjustable Rise Time* section).

9.3.4 Quick Output Discharge (QOD) (Not Present in TPS22976N)

The TPS22976 includes a QOD feature. When the switch is disabled, an internal discharge resistance is connected between VOUT and GND to remove the remaining charge from the output. This resistance prevents the output from floating while the switch is disabled. For best results, it is recommended that the device gets disabled before V_{BIAS} falls below the minimum recommended voltage.

9.3.5 Thermal Shutdown

Thermal Shutdown protects the part from internally or externally generated excessive temperatures. When the device temperature exceeds T_{SD} (typical 160°C), the switch is turned off. The switch automatically turns on again if the temperature of the die drops 20 degrees below the T_{SD} threshold.

9.4 Device Functional Modes

Table 1 lists the TPS22976 functions.

Table 1. TPS22976 Functions Table

ON	VIN to VOUT	VOUT
L	Off	GND
H	On	VIN

Table 2 lists the TPS22976N functions.

Table 2. TPS22976N Functions Table

ON	VIN to VOUT	VOUT
L	Off	Floating
H	On	VIN

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section highlights some of the design considerations for implementing the device in various applications. A PSPICE model for this device is also available on the product page for additional information.

10.1.1 Parallel Configuration

To increase current capabilities and to lower R_{ON}, both channels can be placed in parallel as seen in Figure 35. With this configuration, the CT1 and CT2 pins can be tied together to use one capacitor, CT.

See the *TPS22966 Dual-Channel Load Switch in Parallel Configuration* application report and *Parallel Load Switches for Higher Output Current & Reduced ON-Resistance Design Guide* for more information.

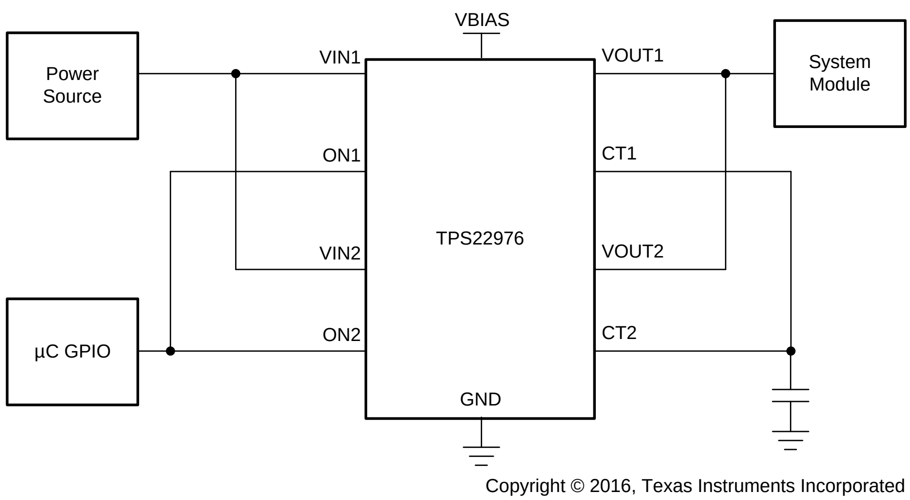


Figure 35. Parallel Configuration

10.1.2 Standby Power Reduction

Battery powered end equipments often have strict power budgets, in which there is a need to reduce current consumption. The TPS22976 significantly reduces system current consumption by disabling the supply voltage to subsystems in standby states. Alternatively, the TPS22976 reduces the leakage current overhead of the modules in standby mode as achieved in Figure 36. Note that standby power reduction can be achieved on either channel, as well as dual-channel operation.

Application Information (continued)

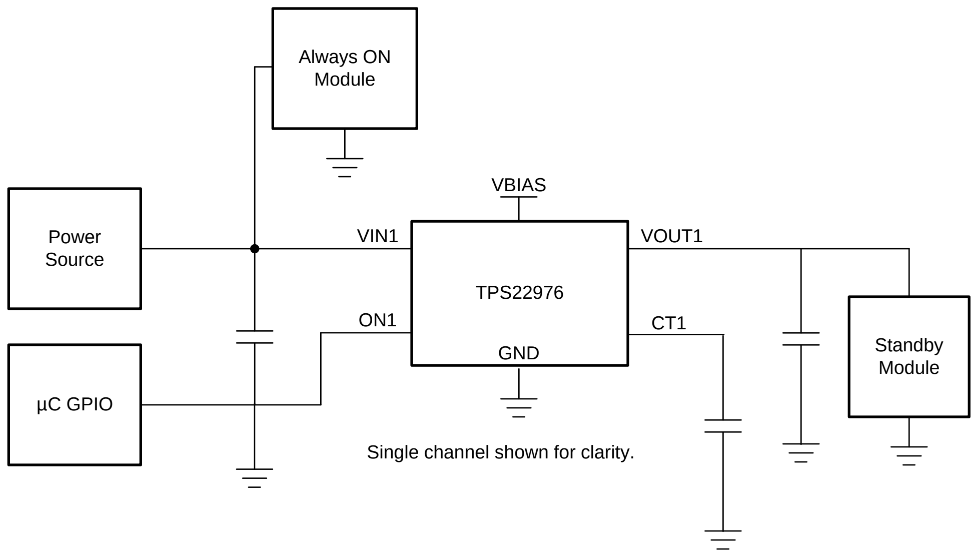


Figure 36. Standby Power Reduction

10.1.3 Power Supply Sequencing without GPIO Input

Sequential startup of several subsystems is often burdensome and adds complexity for several end equipments. The TPS22976 provides a power sequencing solution that reduces the overall system complexity, as seen in Figure 37.

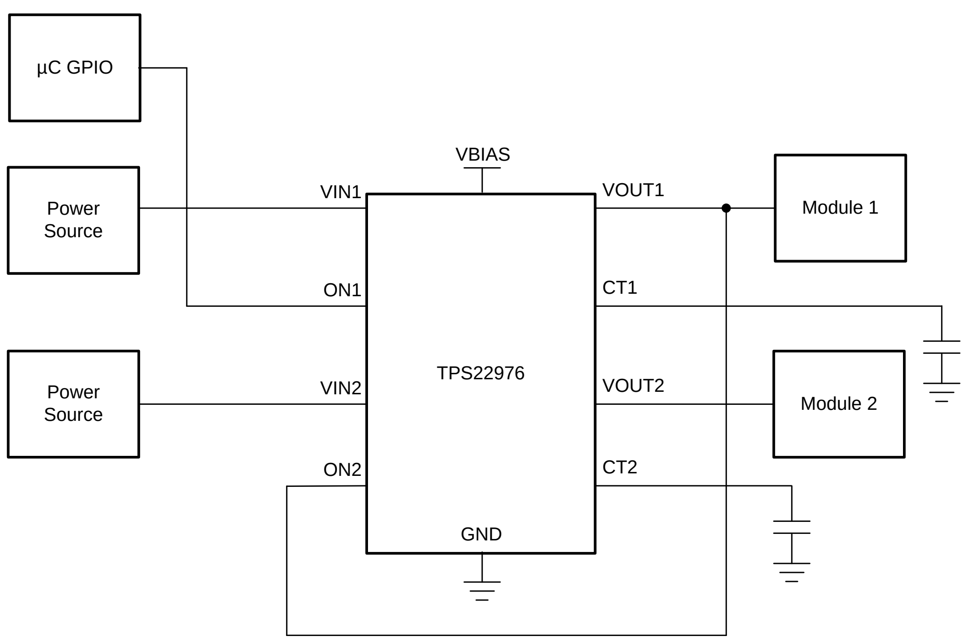


Figure 37. Power Sequencing without a GPIO Input

Application Information (continued)

10.1.4 Reverse Current Blocking

Reverse current blocking is often desired in specific applications, as it prevents current from flowing from the output to the input of the load switch when the device is disabled. With the configuration illustrated in Figure 38, the TPS22976 can be converted into a single-channel switch with reverse current blocking. VIN1 or VIN2 can be used as the input and VIN2 or VIN1 as the output.

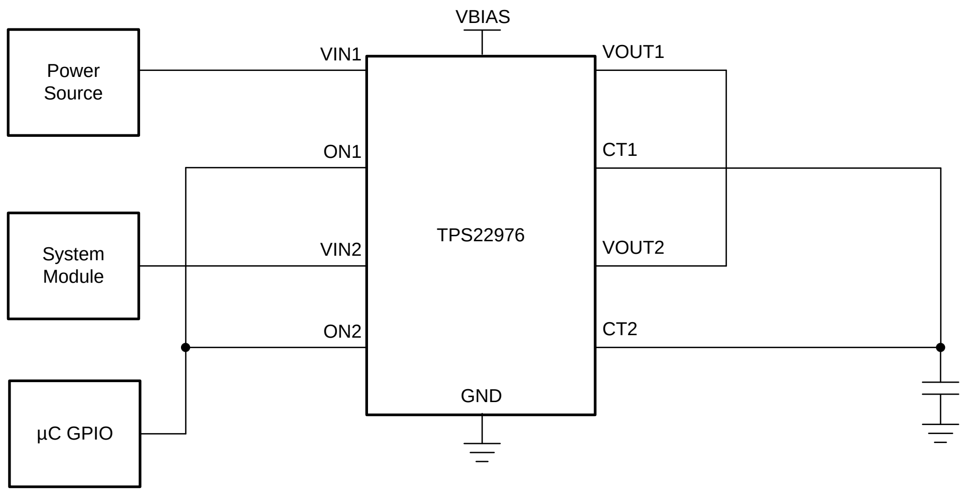


Figure 38. Reverse Current Blocking

10.2 Typical Application

This application demonstrates how the TPS22976 can be used to limit the inrush current when powering on downstream modules.

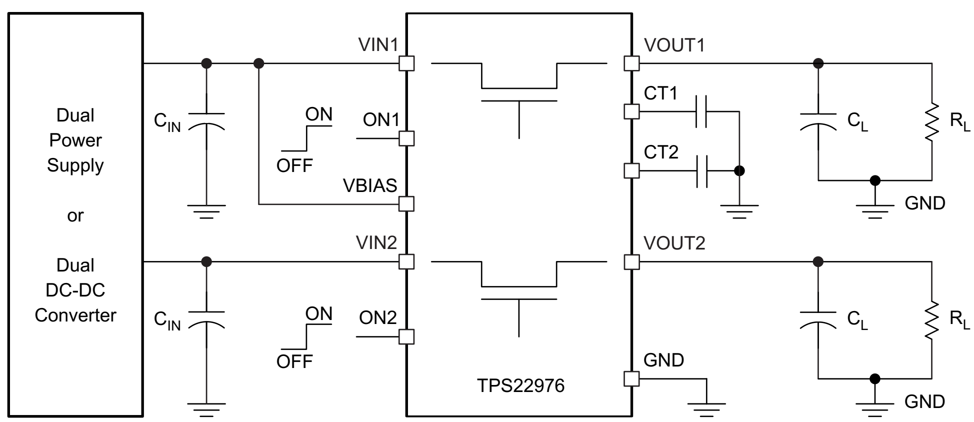


Figure 39. Typical Application Circuit

Typical Application (continued)

10.2.1 Design Requirements

Table 3 shows the TPS22976 design parameters.

Table 3. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage	3.3 V
Bias voltage	5 V
Load capacitance (C_L)	22 µF
Maximum acceptable inrush current	400 mA

10.2.2 Detailed Design Procedure

10.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (3.3 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using Equation 1.

Inrush Current = C × dV/dt

where

- C is the output capacitance
- dV is the output voltage
- dt is the rise time (1)

The TPS22976 offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turnon. The appropriate rise time can be calculated using Table 3 and the inrush current equation. See Equation 2 and Equation 3.

400 mA = 22 µF × 3.3 V/dt (2)

dt = 181.5 µs (3)

To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 181.5 µs. See the oscilloscope captures in the *Application Curves* section for an example of how the CT capacitor can be used to reduce inrush current.

10.2.2.2 Adjustable Rise Time

A capacitor to GND on the CT pins sets the slew rate for each channel. To ensure desired performance, a capacitor with a minimum voltage rating of 25 V must be used on either CT pins. An approximate formula for the relationship between CT and slew rate is shown in Equation 4.

Equation 4 accounts for 10% to 90% measurement on V_{OUT} and does not apply for CT < 100 pF. Use Table 4 to determine rise times for when CT = 0 pF):

$$SR = 0.42 \times CT + 66 \tag{4}$$

where

- SR is the slew rate (in µs/V)
- CT is the capacitance value on the CT pin (in pF)
- The units for the constant 66 is in µs/V.

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 4 shows rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition, and the ON pin is asserted high.

Table 4. Rise Time Values

CT (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω(1)						
	5 V	3.3 V	1.8 V	1.5 V	1.2 V	1.05 V	0.6 V
0	149	112	77	70	60	56	42
220	548	388	236	206	173	154	103
470	968	673	401	342	289	256	169
1000	1768	1220	711	608	505	445	286
2200	3916	2678	1554	1332	1097	949	627
4700	8040	5477	3179	2691	2240	1964	1249
10000	16520	11150	6410	5401	4430	3933	2526

(1) TYPICAL VALUES at 25°C, V_{BIAS} = 5 V, 25 V X7R 10% CERAMIC CAP

10.2.3 Application Curves

V_{BIAS} = 5 V ; V_{IN} = 3.3 V ; C_L = 22 µF

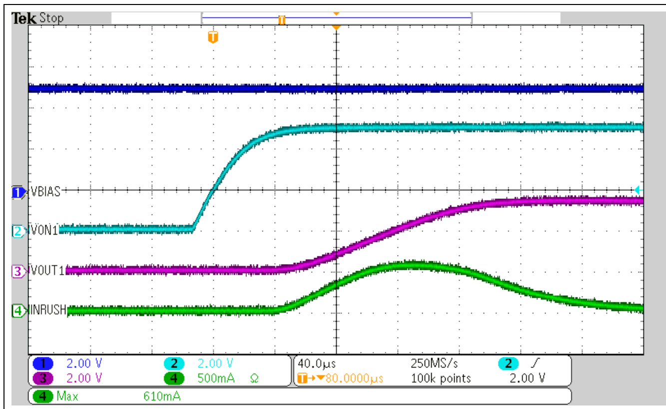


Figure 40. Inrush Current With CT = 0 pF

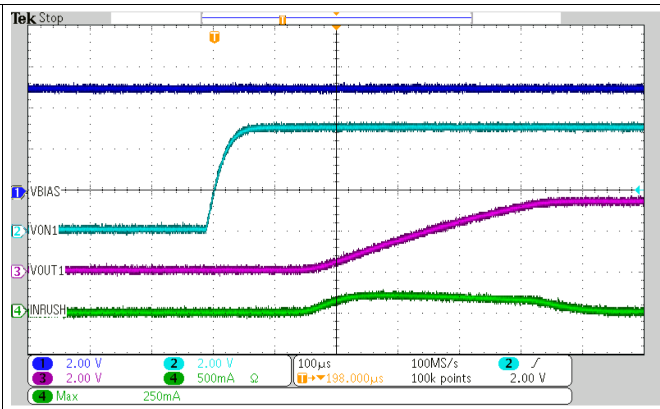


Figure 41. Inrush Current With CT = 220 pF

11 Power Supply Recommendations

The device is designed to operate from a V_{BIAS} range of 2.5 V to 5.7 V and a V_{IN} range of 0.6 V to V_{BIAS}.

12 Layout

12.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

12.2 Layout Example

Notice the thermal vias located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

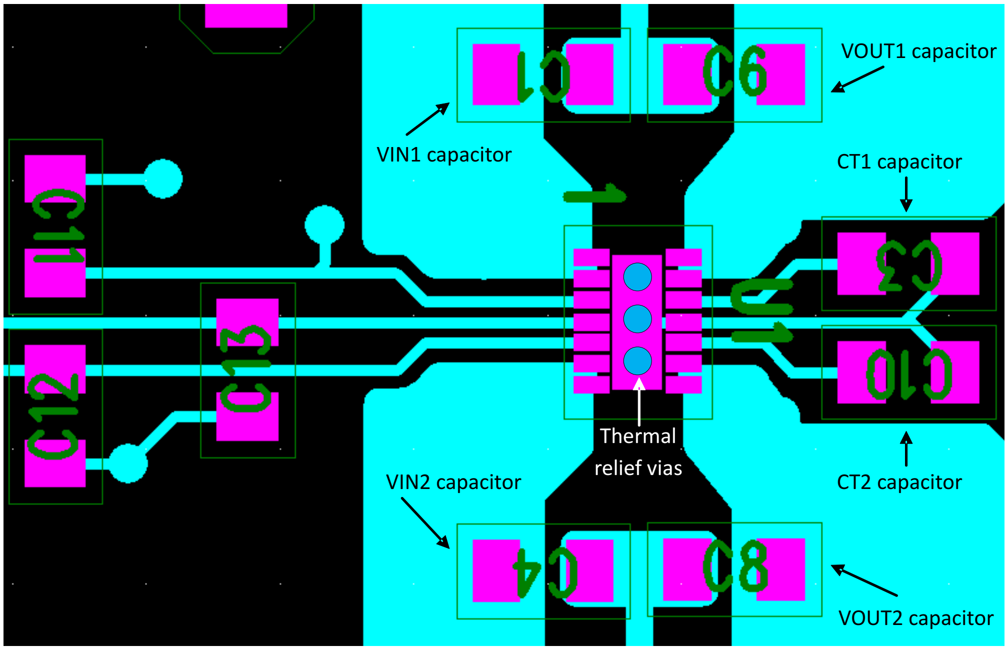


Figure 42. PCB Layout Example

12.3 Power Dissipation

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable power dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 5.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \tag{5}$$

where

- $P_{D(max)}$ is the maximum allowable power dissipation
- $T_{J(max)}$ is the maximum allowable junction temperature (125°C for the TPS22976)
- T_A is the ambient temperature of the device
- θ_{JA} is the junction to air thermal impedance. See the *Thermal Information* section. This parameter is highly dependent upon board layout.

13 器件和文档支持

13.1 器件支持

13.1.1 开发支持

有关 TPS22976N PSpice 瞬态模型的更多信息，请参阅 SLVMBV5。

有关 TPS22976 PSpice 瞬态模型的更多信息，请参阅 SLVMBV6。

13.2 文档支持

13.2.1 相关文档

如需相关文档，请参阅：

用户指南《TPS22976 评估模块》

13.3 接收文档更新通知

如需接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的*提醒我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。本数据随时可能发生变更并且不对本文档进行修订，恕不另行通知。要获取数据表的浏览器版本，请查看左侧的导航面板。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22976ADPUR	ACTIVE	WSON	DPU	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	22976A	Samples
TPS22976DPUR	ACTIVE	WSON	DPU	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	22976	Samples
TPS22976DPUT	ACTIVE	WSON	DPU	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	22976	Samples
TPS22976NDPUR	ACTIVE	WSON	DPU	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	22976N	Samples
TPS22976NDPUT	ACTIVE	WSON	DPU	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	22976N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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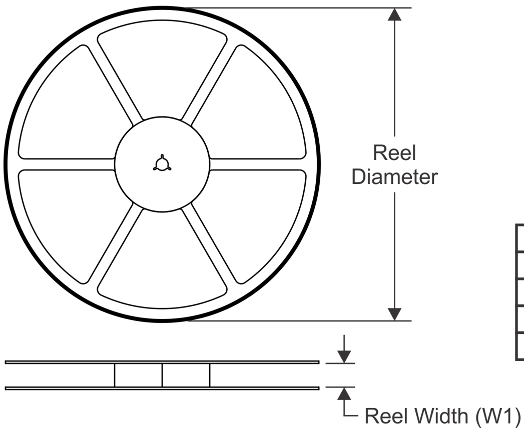
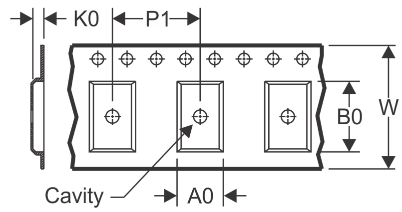
TAPE AND REEL INFORMATION

REEL DIMENSIONS

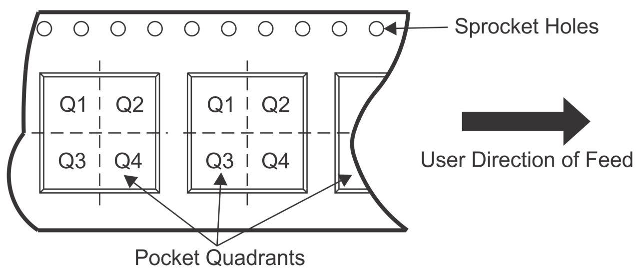


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

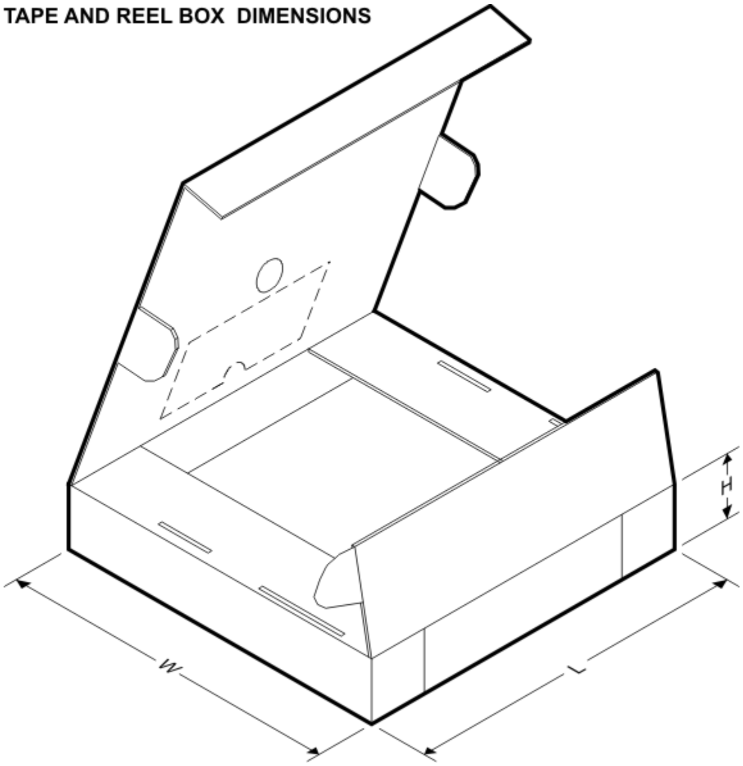
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22976ADPUR	WSON	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22976DPUR	WSON	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22976DPUT	WSON	DPU	14	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22976NDPUR	WSON	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22976NDPUT	WSON	DPU	14	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22976NDPUT	WSON	DPU	14	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

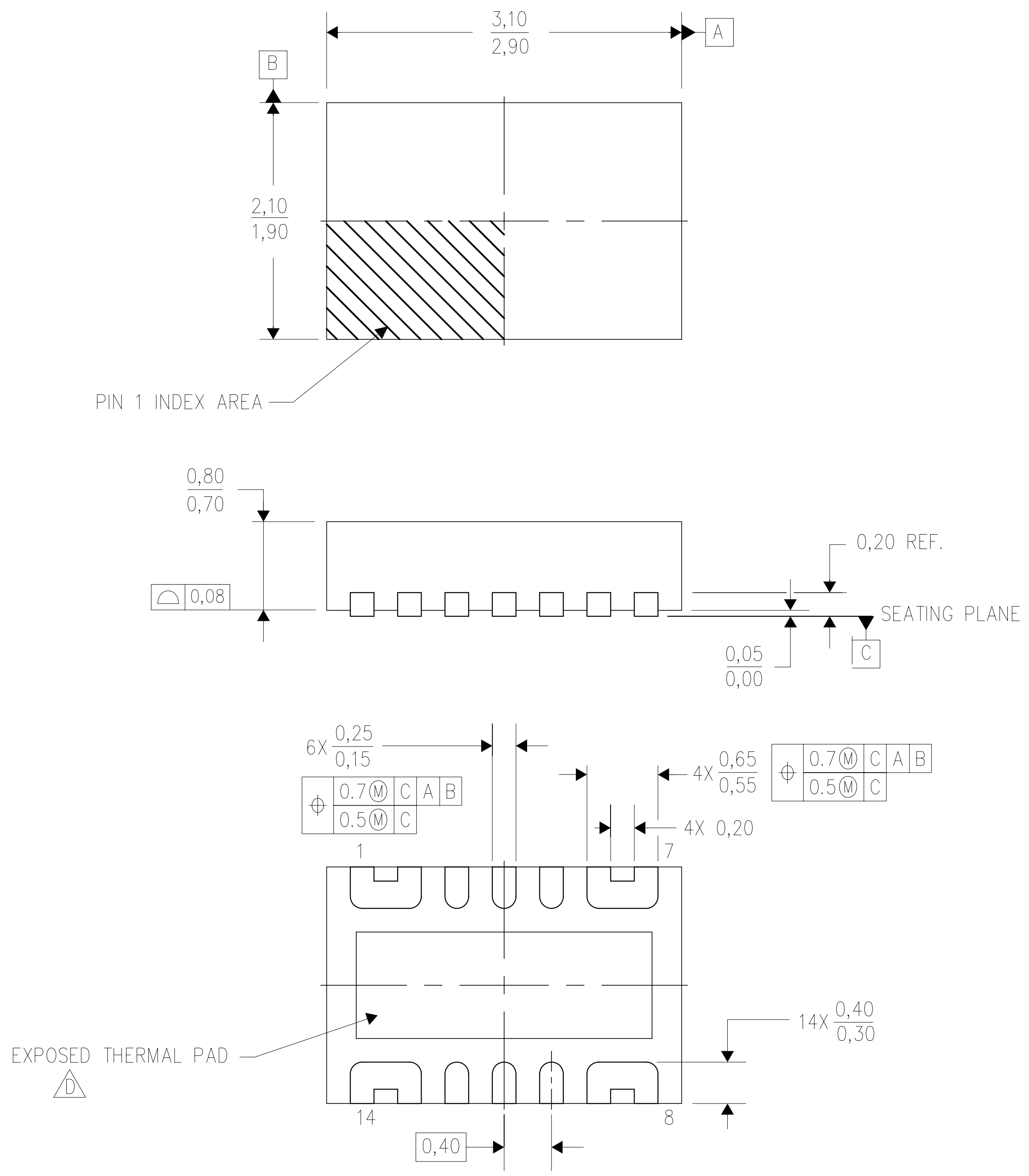
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22976ADPUR	WSON	DPU	14	3000	210.0	185.0	35.0
TPS22976DPUR	WSON	DPU	14	3000	210.0	185.0	35.0
TPS22976DPUT	WSON	DPU	14	250	210.0	185.0	35.0
TPS22976NDPUR	WSON	DPU	14	3000	210.0	185.0	35.0
TPS22976NDPUT	WSON	DPU	14	250	210.0	185.0	35.0
TPS22976NDPUT	WSON	DPU	14	250	210.0	185.0	35.0

DPU (R-PWSON-N14) PLASTIC SMALL OUTLINE NO-LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. This package is Pb-free.

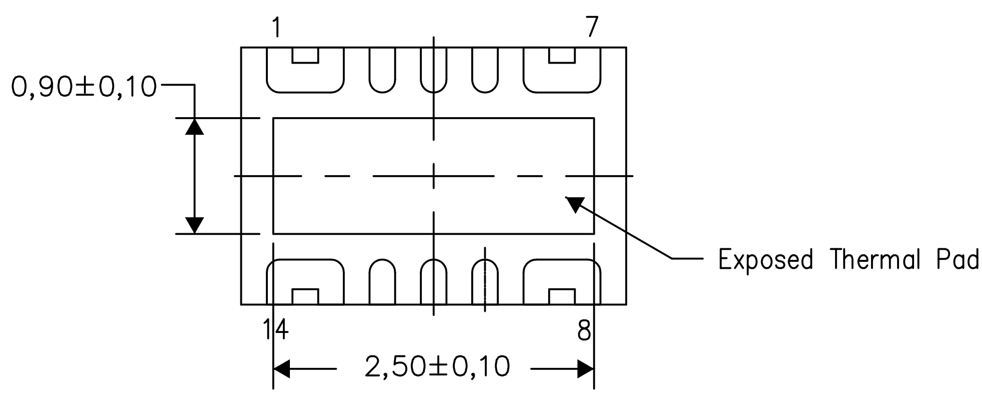
DPU (R-PWSON-N14) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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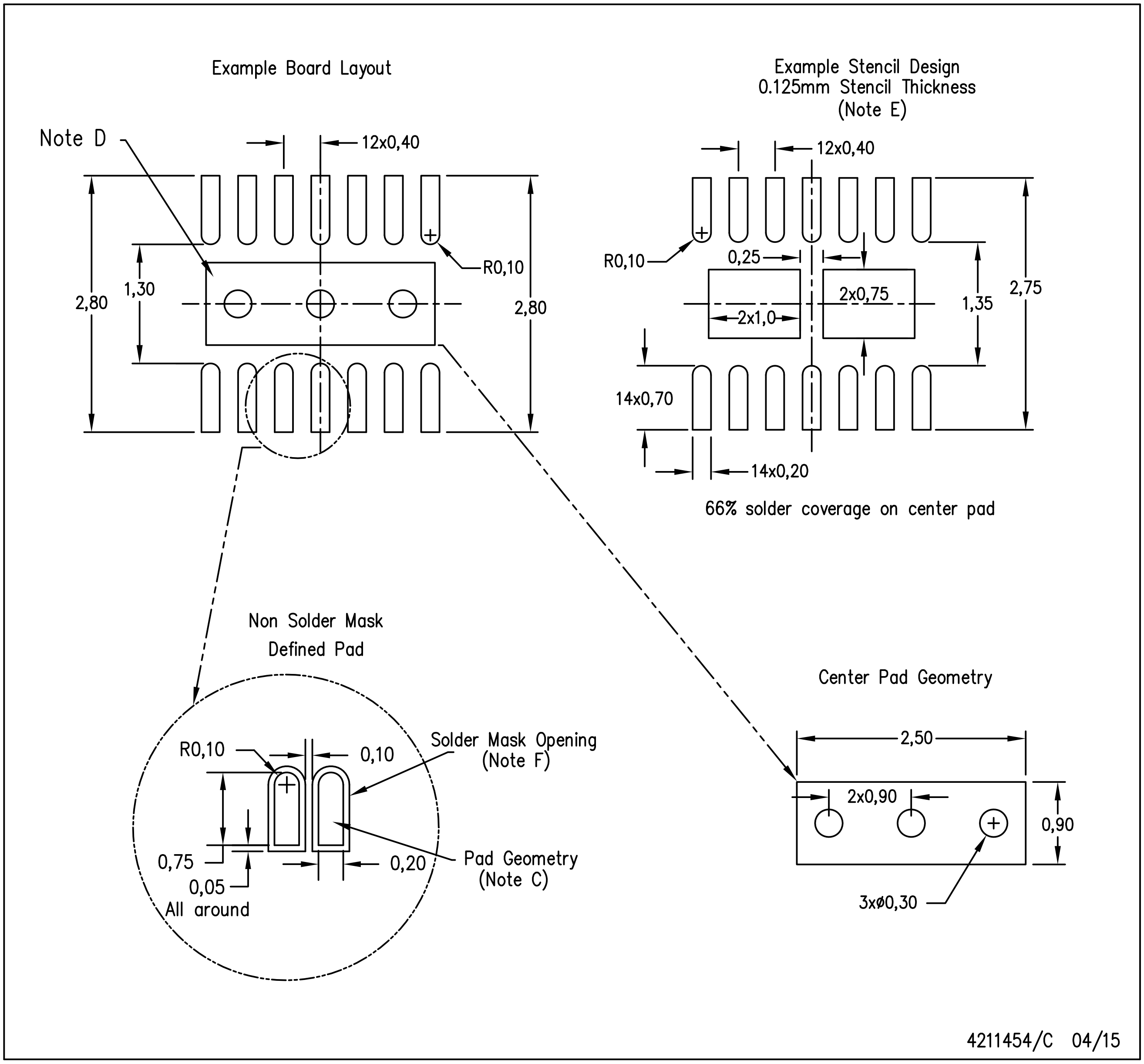
NOTE: All linear dimensions are in millimeters

DPU (R–PWSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

重要声明和免责声明

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