

VME64x Core Specifications

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1 Introduction

This document provides an overview of the features VME64x slave supports. All implemented functionalities conform to the standards defined by ANSI/VITA VME64x Standard [1] [2], but not all are implemented. It also provides an overview of the default power-up configuration and configuration procedure.

The implementation follows the design rules set by Design rules for custom VME modules in CMS [3].

2 VME64x features

This chapter lists and explains features that VME64x slave implements.

2.1 CR/CSR space

For the sake of a “plug and play” capability CR/CSR space is implemented as defined by ANSI/VITA Standards for VME64 Extensions [2].

In order to provide “plug and play” capability VME64x provides a mechanism very similar to PCI. A dedicated “Conf igure ROM / Control & Status Register” (CR/CSR) address space has been introduced. It consists of ROM and RAM regions with a set of well defined registers. It is addressed with the address modifier 0x2F in the A24 address space.

Every VME module occupies a 512 kB page in this address space. The location of this page in the A24 space is defined by geographical address lines on the backplane: each slot is provided with a unique geographical five bit address at the J1 connector (row d). From these bits A23...A19 of the CR/CSR page are derived. If the geographical address is not available (GA parity bit does not match), base address is set to 0x00, which indicates a faulty condition.

The CR/CSR space can be accessed with the data width D08(E0). Please note that in compliance with the CR/CSR definition, only every fourth location in the CR/CSR space is used.

Configuration ROM (CR) and Configuration RAM (CRAM) are implemented externally. Designers should see to it that data contained in the CR depicts the correct VME64x core specifications as presented in this document.

The layout of the configuration space is depicted in **Error! Reference source not found..** The location of the user defined CR and CSR regions as well as the CRAM region are programmable. For each of these, six bytes defining the start and the end address (with respect to the start of the configuration space) are reserved in the CR region. Designers are free to use these regions for module specific purposes. Dedicated software must deal with the content. If a user defined region is not implemented the start and end address must be set to 0x000000.

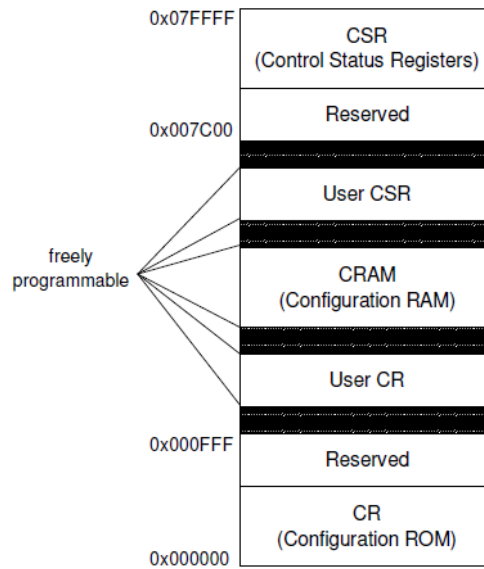


Figure 1: Configuration space organization in VME64x

Please refer to ANSI/VITA VME64 Extensions [2] for further information on the CR/CSR space.

2.2 Data types

This VME64x core supports D08(OE), D16, D32, D64 and unaligned data transfers. The implementation assumes that the target data memory is 8-bit wide. Upon D16 access, only every other byte is addressed, upon D32 every fourth and upon D64 data access only every eighth byte is addressed. Designers who do not need the 8-bit granularity and would prefer bigger data widths can choose to ignore least significant bits of the local address.

2.3 Addressing types

Table 1 list supported addressing types with their address modifier codes:

Mnemonic	AM code (hex)	Description
A24	3D	24-bit addressing
A24_BLT	3B	24-bit addressing block read/write (limited to 256 cycles)
A24_MBLT	3C	24-bit addressing multiplexed block read/write for D64 data access
A24_LCK	32	24-bit addressing ADOH lock cycle
A16	2D	16-bit addressing
A16_LCK	2C	16-bit addressing ADOH lock cycle
A32	0D	32bit addressing
A32_BLT	0F	32-bit addressing block read/write (limited to 256 cycles)
A32_MBLT	0C	32-bit addressing multiplexed block read/write for D64 data access
A32_LCK	05	32-bit addressing ADOH lock cycle
A64	01	64-bit addressing
A64_BLT	03	64-bit addressing block read/write (limited to 256 cycles)
A64_MBLT	03	64-bit addressing multiplexed block read/write for D64 data access
A64_LCK	04	64-bit addressing ADOH lock cycle
CR_CSR	2F	24-bit addressing for CR/CSR access

Table 1: Supported addressing types

Lock AHOH (address only with handshake) cycles are used to lock out the addressed resource for the period of the current VME bus grant (during which BBSY signal is low).

This implementation does not support extended address modifiers (XAMs).

2.4 Signals

This section focuses on functionality of certain VME bus signals.

2.4.1 RESET

RESET resets the entire core to the default configuration. Auto reset is performed on power-up.

2.4.2 BERR

BERR signal is used to signal a bus error. A transfer cycle is terminated with assertion of this signal if the VME64x slave does not recognize the data or addressing type used in the transfer cycle, if master attempts to write to a read-only memory (CR) or if error is received from the module which is addressed.

2.4.3 RETRY

RETRY signal terminates the transfer cycle if VME64x slave receives a retry request from the addressed module, signaling that the read/write request cannot be completed at this time.

2.5 Interrupts

Interrupt controller is a ROACK type controller.

VME64x core receives interrupt requests in a form of a 7-bit IRQ vector. Rising edge on any of these IRQ lines sets an associated bit in an internal IRQ register. The output of this registers drives the VME IRQ lines. Upon receiving an IRQ request on one or more of these lines, VME master responds to the request(s) by issuing an interrupt acknowledge cycle (IACK). Each of the pending interrupts is acknowledged separately, taking priority into an account. Upon receiving interrupt acknowledge, the correct bit in the IRQ register is cleared thus releasing the associated VME IRQ line. After each IACK cycle, 8-bit Status/ID register is presented on the data bus by the VME64x slave, which so far doesn't have any functionality and is constantly set to 0x00.

3 Configuration

Upon power-up or reset, module is disabled and only it's CR/CSR space can be accessed. Software must then first map the module memory in the 64-bit address space by setting Address Decoder Compare (ADER) registers in CSR, which, together with Address Decoder Mask (ADEM) registers in CR relocate the module memory to the desired address range. Please note that since 64-bit address space is supported, two consecutive ADEMs and ADERs form address relocation for one "function", so designers can implement up to four different memory relocations, but addressing which ever one of them will trigger a memory request to the module. Also note, that for the purpose of versatility of this VME64x core, the bits in the ADERs, that set to which AM the code the module should respond, are not taken into account, so users can access the module with all of the supported AMs (as long as of course they are aware which types of transfers are sensible for the module in question).

After the module has been placed in the desired address space, it can be enabled by writing into Bit Set Register in the CSR and thus setting the correct enable bit.

4 References

- [1] ANSI/VITA, American National Standard for VME64, April 1995.
- [2] ANSI/VITA, American National Standards for VME64 Extensions, October 1998.
- [3] VME64x in CMS, Design rules for custom VME modules in CMS, January 2004.