

Electronic Devices & Circuits

by

TEXTBOOK: J. Millman & C. Halkias "Electronic Devices & Circuits".

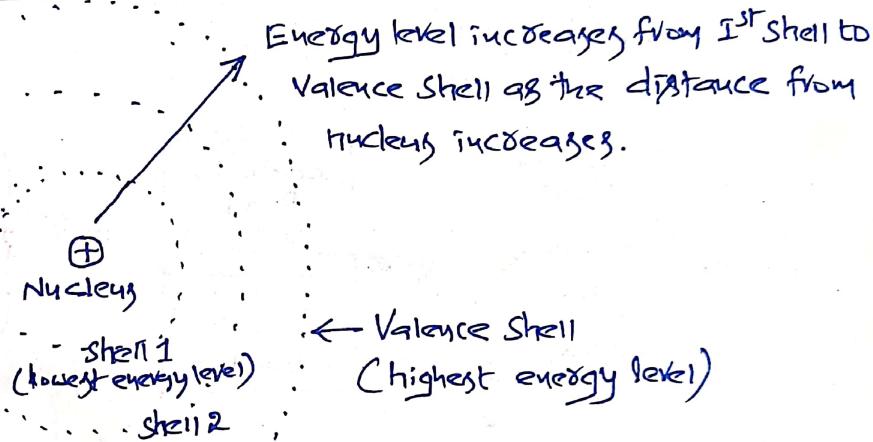
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UNIT - 1

PN JUNCTION DIODE & ITS APPLICATIONS

Review of Semiconductor Physics:

Structure of an atom:

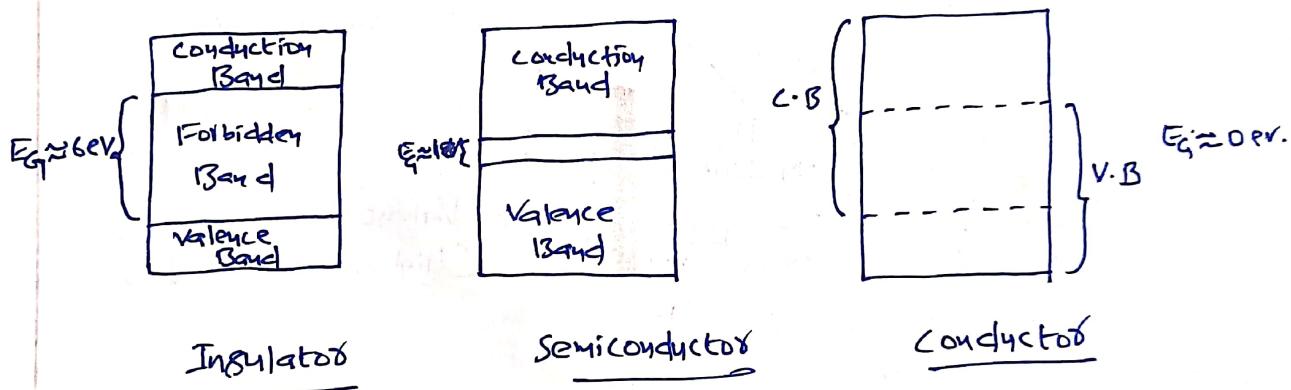


- The outermost shell is called Valence Shell and the electrons in this shell are called Valence electrons.
- An electron which is not subjected to the force of attraction of the nucleus is called a "free electron" such free electrons are basically responsible to the flow of current.
- Sharing of Valence electrons with other adjacent atoms is called "covalent bond".
- Energy levels of various electrons present in 1st orbit, 2nd orbit, merge to form various "energy levels".



Energy Band Theory:

- The Energy band formed due to merging of Energy levels associated with Valence electrons i.e; electrons in the last shell is called "Valence band".
- The Energy band formed due to merging of energy levels associated with the free electrons is called "Conduction Band".
- The Energy gap which is present separating the conduction band and the Valence band is called "Forbidden band (or) forbidden gap".



Insulator

→ Very poor conductor of electricity is called Insulator

Ex:- Diamond
carbon

Semiconductor

→ A substance whose conductivity lies in between Insulator & conductor is called a semiconductor

Ex:- Graphite

Practical Semiconductors are:- Silicon & Germanium; GaAs
These are insulators at low temperature.

Conductor

→ A very good conductor of electricity is called conductor

Ex:- Metal

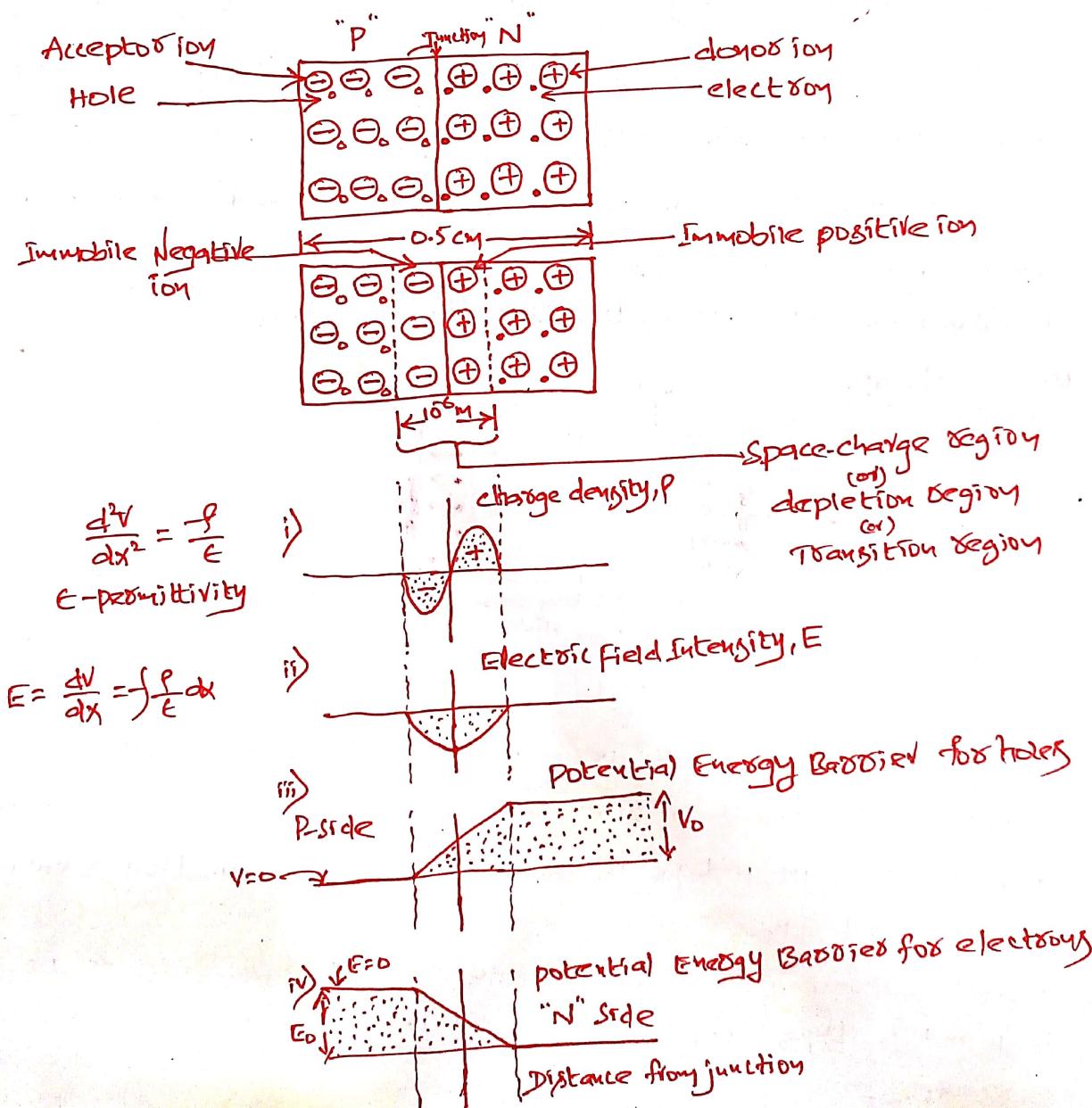
At 0K; E_g for silicon is $E_g = 1.12\text{ eV}$
for Germanium is $E_g = 0.785\text{ eV}$

At 300K; for silicon $E_g = 1.1\text{ eV}$

for Germanium $E_g = 0.72\text{ eV}$.

The P-N Junction : [open circuit]

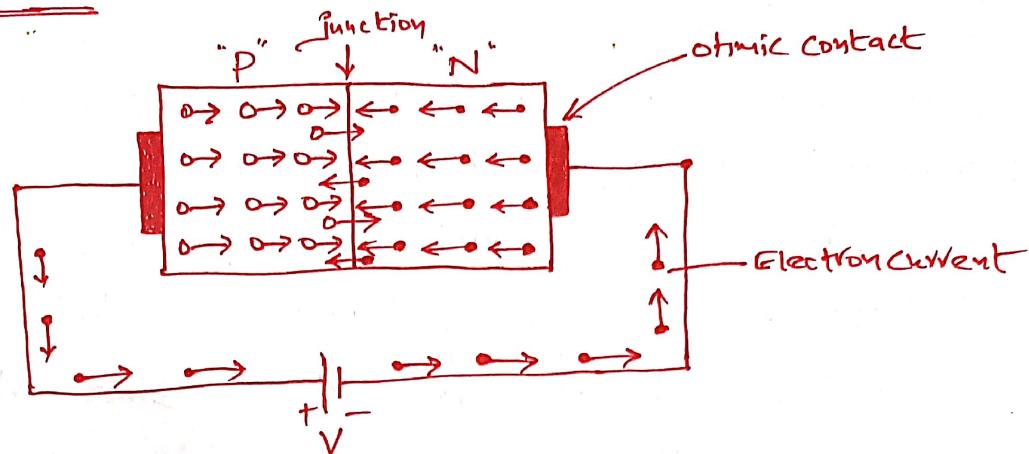
- Before the invention of diode there was vacuum diode which is bulky, costly and noisy. It takes more power and more time to start conducting because of thermionic emission and these limitations were solved by semiconductor junction diode.
- If donor impurities are doped into one side and acceptor impurities into the other side of a single crystal silicon then a P-N junction is formed, which is shown in below figure.



Biased P-N Junctions

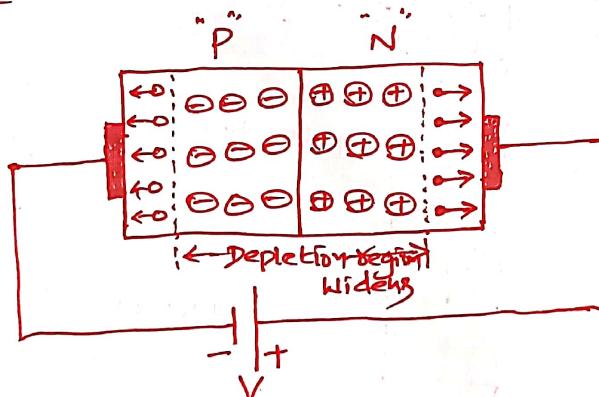
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Forward Bias:



- An external voltage applied with positive polarity to P-type and negative polarity to N-type is called a Forward Bias.
- In a Forward Bias the holes cross the junction from P-type to N-type and the electrons cross the junction in the opposite direction. These majority charge carriers travel around the closed circuit, and large current flows.
- Forward biasing narrows the depletion region.

Reverse Bias:



- In Reverse bias the -ve terminal of battery is connected to P-side and +ve terminal to N-side of the junction. All holes in P-type and electrons in N-type move away from the junction resulting zero current flow.
- A small current flows due to minority charge carriers present in P and N types and this current is called "Reverse Saturation current, I₀".

- This reverse current increase with increasing temperature and it is very small of the order of few micro amperes for Germanium and few nano amperes for silicon P-N Junction diodes.
- Reverse bias widens the depletion region.

The P-N Junction has two terminals called "electrodes", one each from P-region and N-region. Due to the two electrodes it is called "diode".

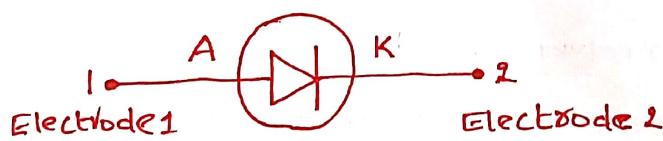
i.e; di-electrode = diode

To connect N and P regions to the external terminals, a metal is applied to the heavily doped N and P type semiconductors regions, such a contact is called "Ohmic contact". It has an important property that

- 1) It conducts current equally in both the directions
- 2) The drop across the contact is very small, which do not affect the performance of the device.

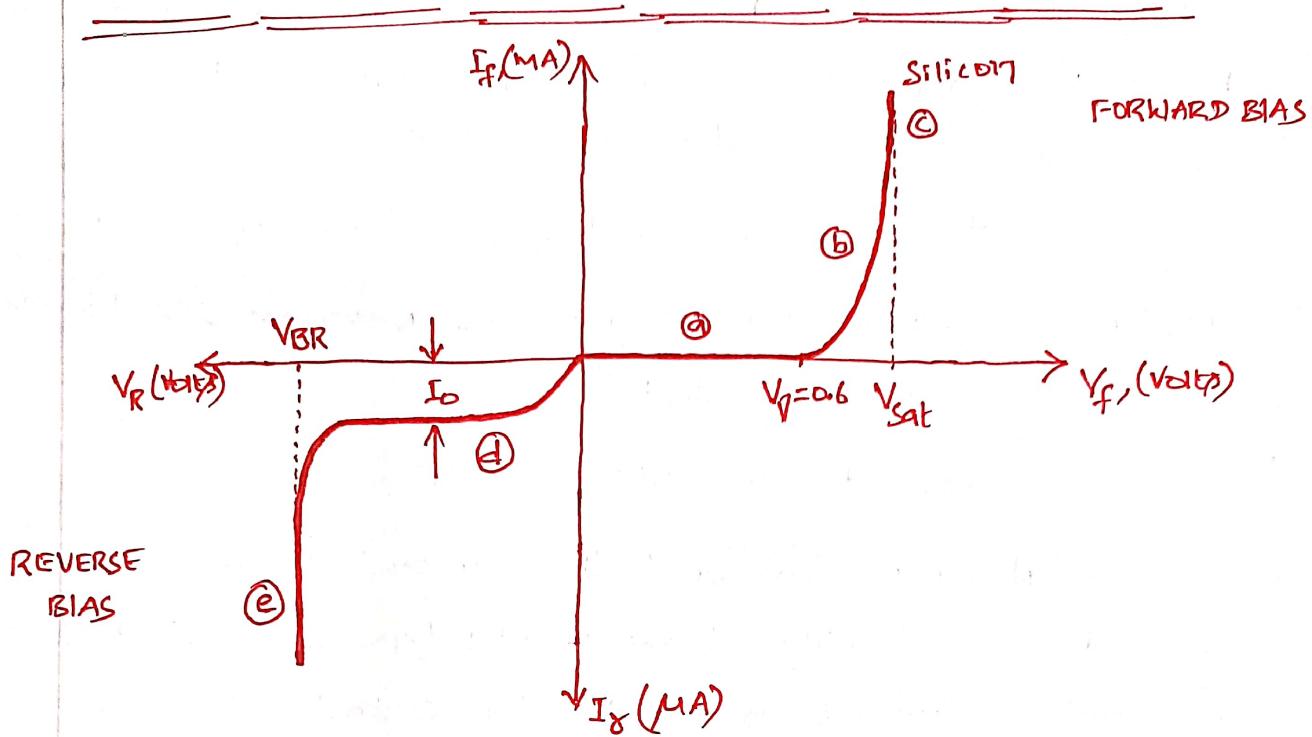
Thus ohmic contacts are used to connect N and P type regions to the electrodes.

Symbol:



The arrow head represents direction of hole current or conventional current.

VOLT- AMPERE (V-I) characteristics of p-N Diode:



FORWARD BIAS:-

- The diode is forward biased if 'V' is positive, indicating that the 'P'-side of the junction is positive with respect to N-side and the current flows from 'P' to 'N' side. For small change in forward voltage 'V' the current increases exponentially with voltage.
- There exists a "cut-in" or "offset" or "break-point" or "threshold voltage", V_p below which the current is very small (it is less than 1 percent of maximum rated value). Beyond V_p the current rises very rapidly.

From the figure the cut-in voltage for

$$\text{Germanium} \quad - V_p = 0.2V$$

$$\text{Silicon} \quad - V_p = 0.6V$$

In Forward Bias from the figure:

- ① $V_a < V_p$: As the applied potential is not sufficient to overcome the barrier, no current flows.
- ② $V_p < V_a < V_{sat}$: For every increase in junction voltage the current also increases so it is almost a exponential relationship between V and I .
- ③ $V_a \geq V_{sat}$: The carriers that are emitted due to external supply will collide with one another and create temperature. This temperature breaks the covalent bonds creating large amount of carriers which provides maximum current flow.

REVERSE BIAS:

The diode is reverse biased when 'P' side of the junction is negatively connected and 'N' side is positively connected.
From the figure:

- ④ $V_a < V_{BR}$: The electric field gives emission but it is very small because it is due to minority carriers.
 - ⑤ $V_a > V_{BR}$: The carriers that are emitted due to electric field will collide and create secondary emission at very high voltage which is called Avalanche multiplication (or) carrier multiplication producing large reverse saturation current and the diode will spoil in this breakdown region due to large heat produced in the reverse bias.
- The dynamic reverse resistance is very high at the order of Megohms.

P-N Diode Equation:

- If a forward bias is applied to the diode, holes are injected from the P-side into N-side.
- The concentration P_h of holes in the N-side is increased above its thermal equilibrium value P_{ho} and is given by

$$P_h(x) = P_{ho} + \bar{P}_h(0) e^{-x/l_p} \rightarrow ①$$

$$\bar{P}_h(0) = P_h(0) - P_{ho} \rightarrow ②$$

- The diffusion hole current in N-side is

given by $\bar{J}_{Ph} = -e D_p \frac{dP_h}{dx}$
 $I_{Ph} = -A e D_p \frac{dP_h}{dx} \quad [\because \bar{J}_{Ph} = \frac{I_{Ph}}{A}]$

$$I_{Ph}(x) = -A e D_p \frac{dP_h(x)}{dx} \rightarrow ③$$

Taking derivative of eq(1) and substituting in above expression ③

$$\frac{dP_h(x)}{dx} = 0 + \bar{P}_h(0) \cdot e^{-x/l_p} \cdot \left(-\frac{1}{l_p}\right) = -\frac{\bar{P}_h(0)}{l_p} \cdot e^{-x/l_p}$$

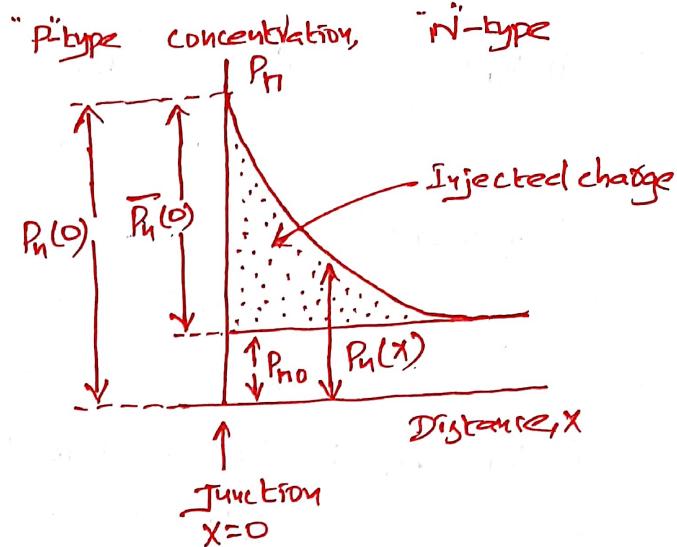
From eq(2)

$$\therefore I_{Ph}(x) = -A e D_p \cdot \frac{-\bar{P}_h(0)}{l_p} \cdot e^{-x/l_p}$$

$$I_{Ph}(x) = \frac{A e D_p}{l_p} \bar{P}_h(0) \cdot e^{-x/l_p} \rightarrow ③$$

This is the hole current which decreases exponentially with distance.

The injected carrier $\bar{P}_h(0)$ is a function of Voltage 'V' it is given as



l_p - diffusion length of holes

P_{ho} - thermal equilibrium holes

$\bar{P}_h(0)$ - injected concentration
at $x=0$.

According to "Law of Junction" the concentration of holes at the edge of the depletion layer, $x=0$ after applying an external voltage V is given as

$$V/V_T$$

$$P_h(0) = P_{h0} \cdot e^{V/V_T}$$

From equation (19)

$$\bar{P}_h(0) = P_h(0) - P_{h0}$$

$$= P_{h0} e^{V/V_T} - P_{h0}$$

$$\bar{P}_h(0) = P_{h0} \left[e^{V/V_T} - 1 \right]$$

From equation (3) hole current $I_{P_h}(0)$ crossing the junction into n-side with $x=0$ is

$$I_{P_h}(0) = \frac{AeD_p}{L_p} \bar{P}_h(0) \cdot e^0.$$

$$\therefore I_{P_h}(0) = \frac{AeD_p}{L_p} \cdot P_{h0} \left[e^{V/V_T} - 1 \right] \cdot 1 \rightarrow (4)$$

Similarly the electron current crossing the junction into p-side is

$$I_{n_p}(0) = \frac{AeD_n}{L_n} n_{p0} \left[e^{V/V_T} - 1 \right] \rightarrow (5)$$

Total diode current $I = I_{P_h}(0) + I_{n_p}(0)$

$$= \left[\frac{AeD_p}{L_p} P_{h0} + \frac{AeD_n}{L_n} n_{p0} \right] \left(e^{V/V_T} - 1 \right)$$

$$I = I_0 \left(e^{V/V_T} - 1 \right)$$

$$\text{where } I_0 = \frac{AeD_p P_{h0}}{L_p} + \frac{AeD_n n_{p0}}{L_n}$$

is called reverse saturation current.

$$\therefore \boxed{I = I_0 \left(e^{V/V_T} - 1 \right)}$$

$\eta=1$ for Germanium

$\eta=2$ for Silicon

$V_T = 26 \text{ mVolts}$

Temperature dependence of V-I characteristics of diode;

$$I = I_0 \left(e^{\frac{V}{kT}} - 1 \right)$$

In the above equation I_0 reverse saturation current depends on temperature while $V_T = \frac{kT}{q}$ is also temperature dependent.
 \therefore The overall diode characteristics are depends on temperature.

Effect of Temperature on I_0 :

Reverse saturation current I_0 is given as

$$I_0 = \frac{A e D_p P_{n0}}{L_p} + \frac{A e D_n N_{p0}}{L_n}$$

We know that from unity Action Law $P_{n0} = \frac{n_i^2}{N_D}$ & $N_{p0} = \frac{n_i^2}{N_A}$
& $n_i^2 = A_0 \cdot T^3 \cdot e^{-E_{Co}/kT}$.

$$\therefore I_0 = \frac{A e D_p n_i^2}{L_p N_D} + \frac{A e D_n n_i^2}{L_n N_A}$$

$$I_0 = \left[\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right] A \cdot e \cdot A_0 T^3 e^{-E_{Co}/kT}$$

In case of Germanium D_p & D_n are inversely proportional to Temperature

$$\text{i.e., } D_p \propto \frac{1}{T} ; D_n \propto \frac{1}{T}$$

$$D_p = \frac{k_p}{T} ; D_n = \frac{k_n}{T} \quad \text{where } k_p \& k_n \text{ are constants}$$

$$\therefore I_0 = \left[\frac{k_p}{L_p N_D} + \frac{k_n}{L_n N_A} \right] \cdot A \cdot e \cdot A_0 \cdot T^3 e^{-E_{Co}/kT}$$

$$I_0 = k_1 \cdot T^2 e^{-E_{Co}/kT} \rightarrow (1)$$

where $k_1 = \left(\frac{k_p}{L_p N_D} + \frac{k_n}{L_n N_A} \right) A \cdot e \cdot A_0$

In case of Silicon $I_o \propto n_i^{\frac{1}{2}}$

$$I_o \propto [n_i^{\frac{1}{2}}]^{1/2}$$

$$I_o = k_2 \cdot \left[A_0 T^3 e^{-E_{go}/kT} \right]^{\frac{1}{2}}$$

$$= k_2 \cdot A_0^{\frac{1}{2}} T^{\frac{3}{2}} e^{-E_{go}/2kT}$$

$$\boxed{I_o = k_2^{\frac{1}{2}} \cdot T^{\frac{3}{2}} e^{-E_{go}/2kT}} \rightarrow ②$$

Equations ① & ② can be written in general as :

$$\boxed{I_o = k' \cdot T^M \cdot e^{-E_{go}/\gamma kT} \quad (\text{or}) \quad I_o = k' \cdot T^M \cdot e^{-V_{go}/\gamma kT}} \rightarrow ③$$

where $V_{go} = \frac{E_{go}}{e}$; For $\underline{\text{Ge}}$ $\underline{\text{Si}}$
 $M = 2$ $M = \frac{3}{2} = 1.5$
 $\gamma = 1$ $\gamma = 2$
 $N_{go} = 0.785$ $V_{go} = 1.21$

k' is constant & E_{go} is forbidden-gap energy.

The relative co-efficient of temperature is defined as

$$\frac{1}{I_o} \frac{dI_o}{dT}$$

From eq ③ $I_o = k' \cdot T^M \cdot e^{-E_{go}/\gamma kT}$

Taking natural logarithm on both sides we get

$$\ln I_o = \ln k' + M \ln T - \frac{E_{go}}{\gamma \cdot k \cdot T}$$

Differentiating w.r.t Temperature 'T', we get

$$\frac{1}{I_0} \frac{dI_0}{dT} = 0 + \frac{M}{T} + \frac{k_{q0}}{q \cdot k \cdot T^2}$$

$$\therefore \boxed{\frac{1}{I_0} \frac{dI_0}{dT} = \frac{M}{T} + \frac{k_{q0}}{q \cdot k \cdot T^2}}$$

At 300K; for Ge $\frac{1}{I_0} \frac{dI_0}{dT} = \frac{2}{300} + \frac{0.785}{300 \times 1 \times 26 \times 10^{-3}} = 0.107 = 10.7/\text{C}$
 $= 11.1/\text{C}$

for "Si" $\frac{1}{I_0} \frac{dI_0}{dT} = \frac{312}{300} + \frac{1.21}{300 \times 12 \times 26 \times 10^{-3}} = 0.082 = 8.2/\text{C}$
 $= 8.1/\text{C}$.

∴ Theoretical variation of I_0 with Temperature T is $11.1/\text{C}$ for "Ge"
 and $8.1/\text{C}$ for Silicon.

- The experimental variation of I_0 is taken as $7.1/\text{C}$ for both Germanium & Silicon because in practice the diode is shunted by a layer of surface impurities which leaks some portion of current.
- Experimentally, I_0 gets multiplied by 1.07 with every 10°C .
 For 10°C rise the current gets multiplied by $(1.07)^{10} = 2$.
 We conclude that "the reverse saturation current I_0 approximately doubles for every 10°C rise in temperature".

- If I_{01} is reverse saturation current at Temperature T_1 and I_{02} is reverse saturation current at Temperature T_2 then

$$\boxed{I_{02} = I_{01} \cdot 2^{(T_2 - T_1)/10}}$$

ii) Temperature dependence of Forward Voltage:

The variation of forward voltage with temperature for constant current I can be derived by differentiating I w.r.t temperature.

$$I = I_0 (e^{\frac{V}{kT}} - 1)$$

$$I = I_0 \cdot e^{\frac{V}{kT}} \quad \text{for } V \gg kT.$$

Apply logarithm on both sides we get

$$V = kT \ln \frac{I}{I_0} \rightarrow 1$$

$$V = k \cdot \frac{T}{e} \cdot \ln \frac{I}{I_0}$$

$$\frac{dV}{dT} = \frac{k \cdot T}{e} \ln \frac{I}{I_0} + \frac{kT}{e} \left[\frac{1}{I} \times \frac{-I}{I_0^2} \cdot \frac{dI_0}{dT} \right]$$

$$= \frac{k \cdot T}{e} \ln \frac{I}{I_0} - kV_T \left[\frac{1}{I_0} \frac{dI_0}{dT} \right]$$

$$= \frac{k \cdot V_T}{T} \ln \frac{I}{I_0} - kV_T \left[\frac{M}{T} + \frac{V_{L0}}{T \cdot k \cdot V_T} \right] \quad \begin{matrix} \text{from eq(1)} \\ \text{& eq(1)} \end{matrix}$$

$$= \frac{V}{T} - \frac{kV_T M}{T} - \frac{V_{L0}}{T}$$

$$\boxed{\frac{dV}{dT} = \frac{V - (V_{L0} + kV_T M)}{T}} \rightarrow 2$$

consider a diode operating at 300K and just beyond the threshold voltage $V_j = 0.2V$ for "Ge"
 $= 0.6V$ for "Si" Then we find

for "Ge" $\frac{dV}{dT} = \frac{0.2 - (0.785 + 1 \times 2 \times 0.026)}{300} = -2.1 \text{ mV/C}$.

Si $\frac{dV}{dT} = \frac{0.6 - (1.21 + 2 \times 3.2 \times 0.026)}{300} = -2.3 \text{ mV/C}$.

$$\therefore \frac{dV}{dT} = \begin{cases} -2.1 \text{ mV/C} \\ -2.3 \text{ mV/C} \end{cases}$$

Or on average $\boxed{\frac{dV}{dT} = -2.2 \text{ mV/C}}$ to taken either for

Germanium or for Silicon at room temperature.

Static & Dynamic Resistances of a Diode:

i) DC (or) Static Resistance:

The static resistance, R of a diode is defined as the ratio of voltage to current.

$$R = \frac{V}{I}$$

In forward bias, the static resistance is low of the order of ohms.

In Reverse Bias the static resistance is very high of the order of "Mohm".

ii) AC (or) Dynamic Resistance:

The dynamic or incremental resistance is the reciprocal of slope of the伏特-安培 characteristic. i.e; $\gamma = \frac{dV}{dI}$.

$$I = I_0 (e^{\frac{V_{BAT}}{V_T}} - 1)$$

$$\frac{dI}{dV} = I_0 \cdot e^{\frac{V_{BAT}}{V_T}} \cdot \frac{1}{V_T} = \frac{I_0 e^{\frac{V_{BAT}}{V_T}}}{V_T} = \frac{I + I_0}{V_T} \quad \left[\because I = I_0 e^{\frac{V_{BAT}}{V_T}} \right]$$

$$\therefore \gamma = \frac{dV}{dI} = \frac{V_T}{I_0 e^{\frac{V_{BAT}}{V_T}}} = \frac{V_T}{I + I_0}$$

for forward bias $I \gg I_0$; $\gamma \approx \frac{V_T}{I}$ and it is "ohms".

Capacitance

If the voltage applied to a junction is changed, the charge distribution near the transition region must also change. There is a resultant current is developed due to rate of change of applied voltage, which is capacitive in nature. Hence we have attributed a certain capacitance to the pn junction.

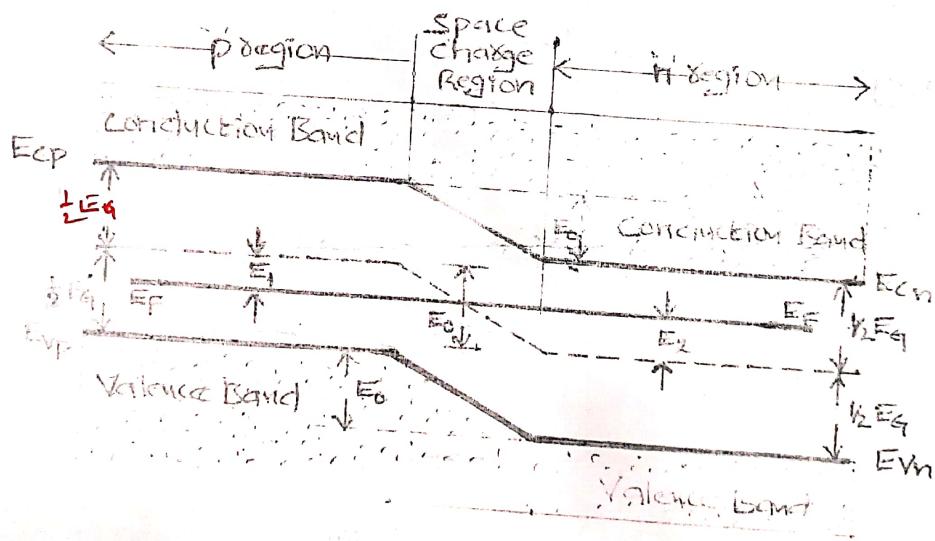
Junction capacitance

$$\text{Junction capacitance} = C_T + C_D$$

$$C_T = \frac{\epsilon A}{W}$$

$$C_D = \frac{\pi \epsilon}{4 V T}$$

Energy Band diagram of an open-circuited PN junction



Ideal Versus practical Diodes:

Ideal diode

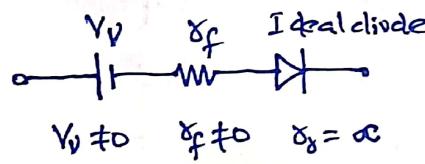
- 1) The cut-in Voltage is zero since there is no barrier potential and small forward bias voltage causes conduction through the device
- 2) The forward resistance is zero $R_f = 0$
- 3) The reverse resistance is infinity $\infty = \infty$
- 4) conducts in Forward bias and does not conduct in Reverse bias
- 5) Ideal diode acts as a fast-acting electronic switch

Practical diode

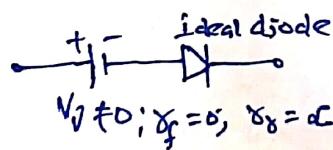
- 1) The cut-in Voltage $V_V = 0.2V$ for "Ge" and $V_V = 0.6V$ for "Si". to overcome potential barrier across the junction.
- 2) Forward resistance is in the range of few tens of ohms. ; $R_f = 10\Omega$
- 3) Reverse resistance is in the range of mega ohms. ; $\infty = M\Omega$.
- 4) conducts in Forward bias and a small reverse saturation current flows in Reverse bias
for Ge \rightarrow micro amps
Si \rightarrow nano amps.
- 5) This diode also acts as a fast-acting electronic switch.

Diode Equivalent circuit's

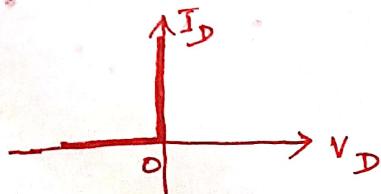
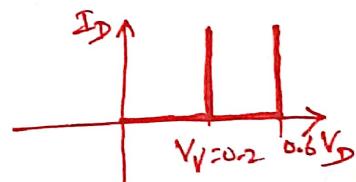
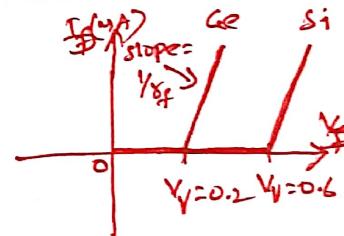
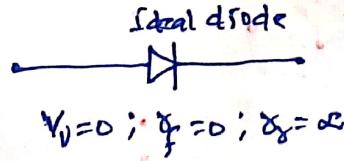
i) Piece wise linear model



ii) Simplified model



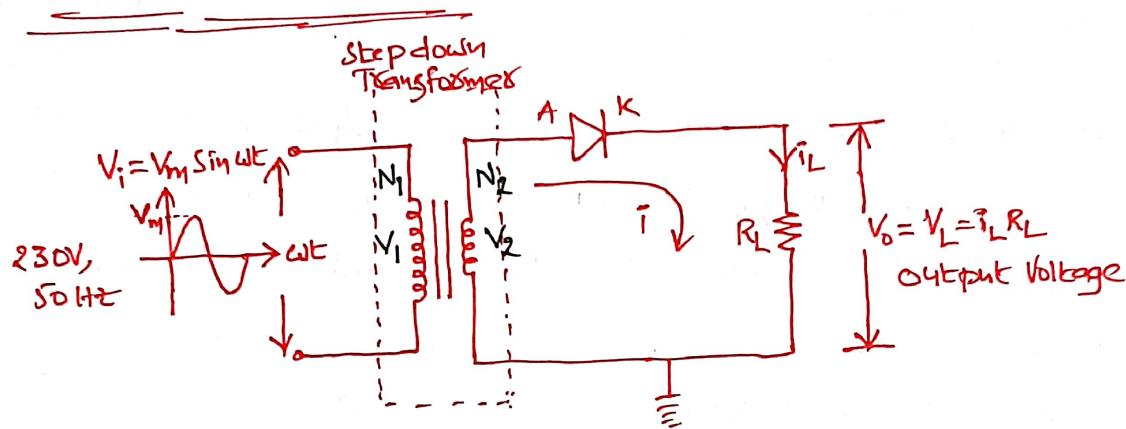
iii) Ideal model



RECTIFIERS AND FILTERS

A Rectifier is a device which converts a.c Voltage to pulsating d.c Voltage using one or more P-N Junction diodes.

D) Half-wave Rectifier:



N_1 — primary winding

N_2 — secondary winding

V_2 — secondary voltage

V_1 — primary voltage

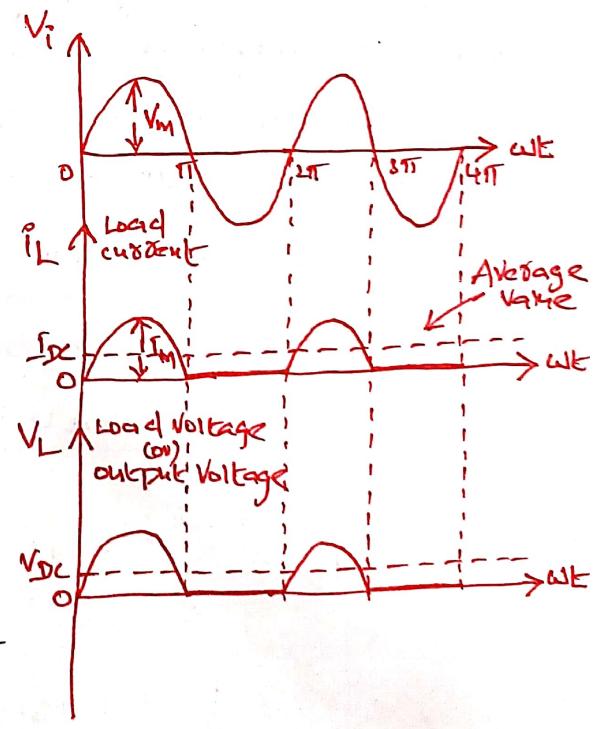
- A Transformer is a device which converts one form of current or voltage to other form without change in frequency

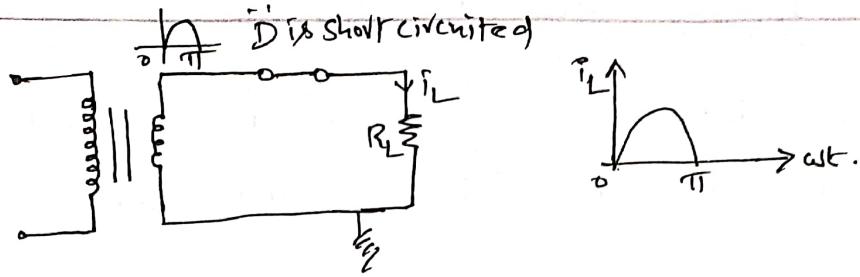
$$\frac{N_2}{N_1} = \frac{V_2}{V_1}$$

i) For positive cycle:

If positive cycle from 0 to π is given to input of diode then the diode is in forward bias condition and it is short circuited and current flows through the diode and through load resistance, R_L .

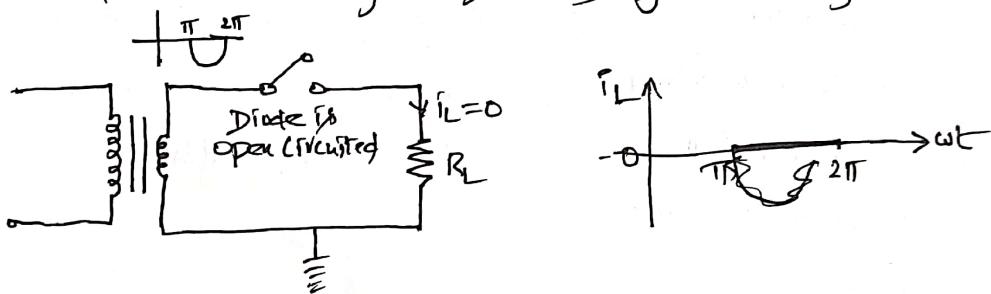
This current is represented in the wave-form from 0 to π duration and the load voltage also takes the same wave-form since $V_L = i_L R_L$.





ii) For Negative cycle:

- Negative cycle from π to 2π is given as input to the diode then diode 'D' is reverse biased and it is open circuited i.e. zero current flows through the diode and through load resistance, R_L .
- This current is represented in the waveform from π to 2π duration and load voltage also takes zero voltage since $V_L = i_L R_L$.



- Hence the output is discontinuous in nature and it is called pulsating dc.
- Hence it is necessary to calculate average value of load current and average value of output voltage.

Average DC Load current (I_{DC}):

Average or DC value is obtained by integration of alternating current

$$\text{Average Value} = \frac{\text{Area under the curve over one complete cycle; i.e., } 0-2\pi}{\text{Base, i.e., } 2\pi.}$$

$$\therefore I_{DC} = \frac{\int_0^{2\pi} i d(\omega t)}{2\pi}$$

where $i = I_m \sin \omega t$; $0 \leq \omega t \leq \pi$

$= 0$; $\pi \leq \omega t \leq 2\pi$

$$= \frac{1}{2\pi} \int_0^{2\pi} i d(\omega t).$$

" I_m is peak value of current

$$= \frac{1}{2\pi} \left[\int_0^{\pi} i d(\omega t) + \int_{\pi}^{2\pi} i d(\omega t) \right].$$

$$\begin{aligned}
 I_{DC} &= \frac{1}{2\pi} \left[\int_0^{\pi} I_m \sin \omega t d(\omega t) + \int_0^{\pi} 0 \right] \\
 &= \frac{I_m}{2\pi} [-\cos \omega t]_0^\pi = \frac{I_m}{2\pi} [1+1] = \frac{R I_m}{2\pi} = \frac{I_m}{\pi} \\
 \therefore I_{DC} &= \boxed{\frac{I_m}{\pi}}
 \end{aligned}$$

ii) Average (or) DC Load Voltage (V_{DC}):

$$\begin{aligned}
 V_{DC} &= I_{DC} \cdot R_L \\
 &= \frac{I_m}{\pi} \times R_L \\
 &= \frac{V_m}{\pi (R_L + R_f + R_s)} \times R_L \\
 &= \frac{V_m}{\pi \cdot R_L} \\
 \therefore V_{DC} &= \boxed{\frac{V_m}{\pi}}
 \end{aligned}$$

R_L - Load resistance
 R_f - Diode internal forward resist.
 R_s - Transformer secondary winding resistance

iii) RMS Value of Load current (I_{RMS}):

RMS means squaring, finding mean and then finding square root.

$$\begin{aligned}
 I_{RMS} &= \left[\frac{1}{2\pi} \int_0^{2\pi} i^2 d(\omega t) \right]^{1/2} \\
 &= \left[\frac{1}{2\pi} \left(\int_0^{\pi} i^2 d(\omega t) + \int_{\pi}^{2\pi} i^2 d(\omega t) \right) \right]^{1/2} \\
 &= \left[\frac{1}{2\pi} \left(\int_0^{\pi} I_m^2 \sin^2 \omega t d(\omega t) + 0 \right) \right]^{1/2} \\
 &= \left[\frac{I_m^2}{2\pi} \int_0^{\pi} \frac{1 - \cos 2\omega t}{2} d(\omega t) \right]^{1/2} = \frac{I_m}{2\sqrt{2\pi}} \left[\left(\frac{\omega t}{2} \right)_0^{\pi} - \left(\frac{\sin 2\omega t}{4} \right)_0^{\pi} \right]^{1/2} \\
 &= \frac{I_m}{2\sqrt{2\pi}} \left[\pi - 0 - 0 - 0 \right]^{1/2} = \frac{I_m}{2\sqrt{2\pi}} \sqrt{\pi} \Rightarrow \boxed{I_{RMS} = \frac{I_m}{2}}
 \end{aligned}$$

$$\text{RMS Value of output Voltage } (V_{LRMS}) \Rightarrow V_{LRMS} = I_{RMS} R_L \\ = \frac{I_m}{2} R_L \propto \frac{V_m \times R_L}{2(R_L + r_f + r_s)} = \frac{V_m}{2}$$

iv) Rectified Efficiency (η):

$$\eta = \frac{\text{D.C Output Power}}{\text{A.C Input Power}} = \frac{P_{DC}}{P_{AC}} = \frac{I_{DC}^2 R_L}{I_{AC}^2 (R_L + r_f + r_s)}$$

$$= \frac{\frac{I_m^2}{4} \pi^2 R_L}{I_m^2 / 4 [R_L]} \quad \because R_L \gg r_f + r_s \\ I_{AC} = I_{RMS} = \frac{I_m}{2} \\ I_{DC} = I_m / \pi$$

$$= \frac{4}{\pi^2}$$

$\eta = 0.406 = 40.6\%$

\therefore In HWR maximum 40.6% of a.c power gets converted to d.c power in the load. Remaining 60% of power is present in terms of ripples in the output.

v) Ripple Factor (δ):

The output of half wave rectified contains pulsating components called "Ripples". Measure of such ripples present in output is with the help of a factor called "Ripple Factor (δ)".

$$\delta = \frac{\text{R.M.S Value of a.c component of output}}{\text{Average (or) D.C component of output}}$$

I_{AC} = RMS value of a.c component present in output.

I_{DC} = RMS value of D.C component present in output

I_{RMS} = RMS value of total output current

$$I_{RMS}^2 = I_{AC}^2 + I_{DC}^2 \Rightarrow I_{RMS} = \sqrt{I_{AC}^2 + I_{DC}^2}$$

$$I_{AC} = \sqrt{I_{RMS}^2 - I_{DC}^2}$$

$$\delta = \frac{I_{AC}}{I_{DC}} = \frac{\sqrt{I_{RMS}^2 - I_{DC}^2}}{I_{DC}} = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - \frac{I_{DC}^2}{I_{RMS}^2}} = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1}$$

For Halfwave Rectifier $\delta = \sqrt{\left(\frac{I_{mL}}{I_{DC/\pi}}\right)^2 - 1} = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} = 1.211$

This indicates that Ripple content in output are 1.211 times the d.c component i.e; 121.1% of d.c component.

vi) Form factor (F.F):

$$F.F = \frac{I_{RMS}}{I_{DC}} = \frac{I_{mL}}{I_{DC/\pi}} = \frac{\pi}{2} = 1.57 \text{ --- for HWR}$$

vii) Peak factor (P.F):

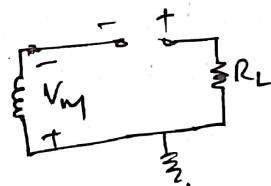
$$P.F = \frac{V_m}{V_{RMS}} = \frac{V_m}{V_m/\sqrt{2}} = \sqrt{2} = 1.414 = 2 \text{ for HWR}$$

$V_{RMS} = I_{DC} \times R_L = \frac{I_m}{2} R_L$

viii) Peak Inverse Voltage (PIV):

PIV is the peak voltage across the diode in the reverse direction i.e; when diode is reverse biased or not conducting.

For HWR $PIV = V_m$.



ix) Transformer Utilization Factor (TUF):

The factor which indicates how much is the utilization of the transformer in the circuit is called TUF.

$$TUF = \frac{P_{DC}}{P_{AC}} = \frac{I_{DC}^2 R_L}{V_{RMS} \times I_{RMS}} = \frac{\left(\frac{I_m}{2}\right)^2 R_L}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{2}}$$

For HWR $TUF = 0.287 = 28.7\%$.

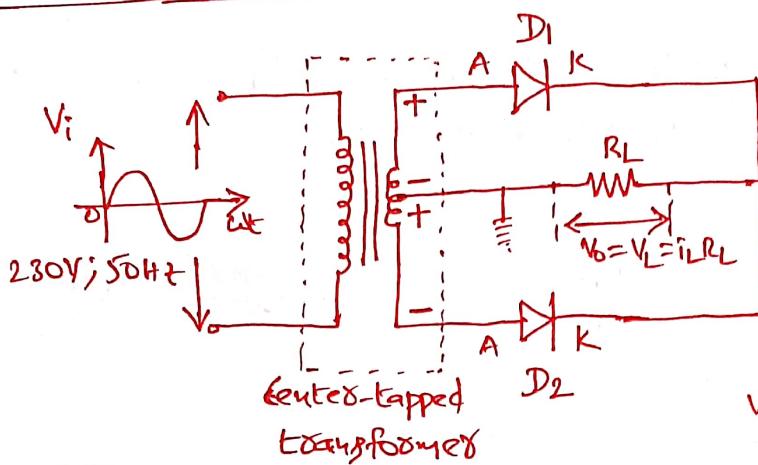
This shows that transformer is not fully utilized in HWR.

Disadvantages of HWR:

- 1) HWR conducts only for half cycle i.e; for positive cycle and does not conduct for negative cycle.
- 2) Ripple factor is high i.e; 1.211
- 3) Efficiency is 40%. Very low.
- 4) Transformer utilization factor TUF is low; i.e; 28.7%.

Advantages: 1) Simple circuit 2) Low cost

2) FULLWAVE RECTIFIERS



Operation:

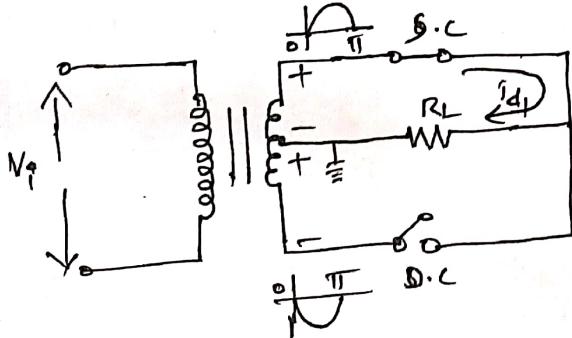
For positive half cycle:

When positive half cycle from 0 to π duration is given as input to diode D_1 then D_1 is forward biased and it is short circuited and current flows through the diode i.e. i_{d_1} .

In the second half of the circuit a negative waveform is given as input to diode D_2 in the $0-\pi$ duration then D_2 is reverse biased it is open-circuited and zero current flows i.e. $i_{d_2}=0$ in $0-\pi$ duration.

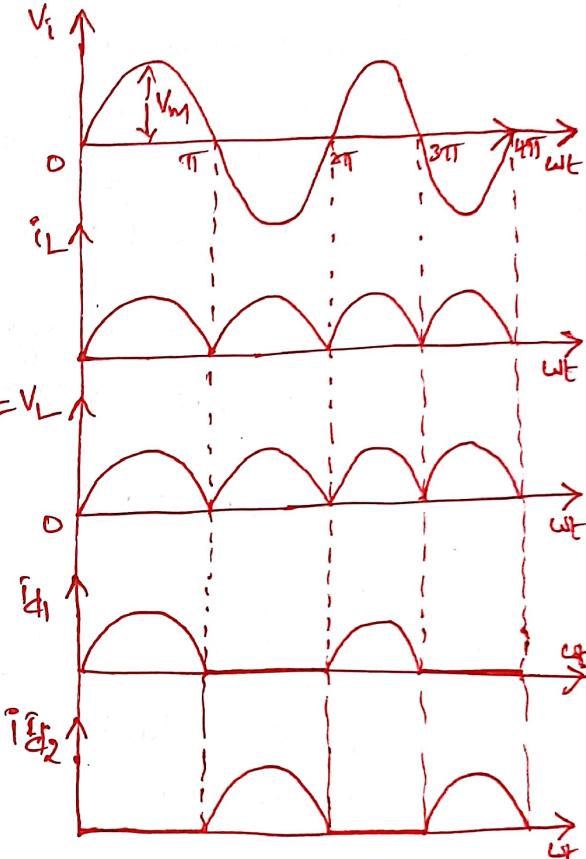
Then current flowing through R_L is i_L and voltage $V_L = i_L R_L$.

The circuit for positive half cycle is:



D_1 - Forward biased

D_2 - Reverse biased.



4.2.4 Characteristics:

1. Average DC Load Current (I_{DC})

Average or DC value is obtained by integration of alternating current.

$$\text{Average value} = \frac{\text{Area under the curve over one complete cycle i.e., } (0-2\pi)}{\text{Base i.e., } 2\pi}$$

$$I_{DC} = \frac{\int_0^{2\pi} i d(\omega t)}{2\pi} \quad (4.22)$$

Where $i = \begin{cases} I_m \sin \omega t; & 0 \leq \omega t \leq \pi \\ -I_m \sin \omega t; & \pi \leq \omega t \leq 2\pi \end{cases}$

$$\begin{aligned} I_{DC} &= \frac{1}{2\pi} \left[\int_0^{\pi} i d(\omega t) + \int_{\pi}^{2\pi} i d(\omega t) \right] \\ I_{DC} &= \frac{1}{2\pi} \left[\int_0^{\pi} I_m \sin \omega t d(\omega t) + \int_{\pi}^{2\pi} -I_m \sin \omega t d(\omega t) \right] \\ I_{DC} &= \frac{I_m}{2\pi} \left[[-\cos \omega t]_0^{\pi} - [-\cos \omega t]_{\pi}^{2\pi} \right] \\ I_{DC} &= \frac{I_m}{2\pi} [1 + 1 + 1 + 1] \\ I_{DC} &= \frac{2I_m}{\pi} \end{aligned} \quad (4.23)$$

2. Average DC Load Voltage (V_{DC})

$$V_{DC} = I_{DC} R_L$$

$$V_{DC} = \frac{2I_m}{\pi} R_L$$

$$\because I_m = \frac{V_m}{R_L + R_f + R_S} \quad \begin{cases} R_L = \text{load resistance} \\ R_f = \text{diode internal forward resistance} \\ R_S = \text{transformer secondary winding resistance} \end{cases}$$

$$V_{DC} = \frac{2V_m}{\pi(R_L + R_f + R_S)} R_L$$

$$\therefore R_L \gg (R_f + R_S)$$

$$V_{DC} = \frac{2V_m}{\pi R_L} R_L$$

$$V_{DC} = \frac{2V_m}{\pi} \quad (4.24)$$

3. RMS value of Load Current (I_{RMS})

RMS means squaring, finding mean and then finding square root.

$$\begin{aligned}
I_{RMS} &= \left[\frac{1}{2\pi} \int_0^{2\pi} i^2 d(\omega t) \right]^{1/2} \\
I_{RMS} &= \left[\frac{1}{2\pi} \left(\int_0^{\pi} i^2 d(\omega t) + \int_{\pi}^{2\pi} i^2 d(\omega t) \right) \right]^{1/2} \\
I_{RMS} &= \left[\frac{1}{2\pi} \left(\int_0^{\pi} I_m^2 \sin^2 \omega t d(\omega t) + \int_{\pi}^{2\pi} I_m^2 \sin^2 \omega t d(\omega t) \right) \right]^{1/2} \\
I_{RMS} &= \left[\frac{I_m^2}{2\pi} \left(\int_0^{\pi} \sin^2 \omega t d(\omega t) + \int_{\pi}^{2\pi} \sin^2 \omega t d(\omega t) \right) \right]^{1/2} \\
I_{RMS} &= \left[\frac{I_m^2}{2\pi} \left(\int_0^{\pi} \frac{1 - \cos 2\omega t}{2} d(\omega t) + \int_{\pi}^{2\pi} \frac{1 - \cos 2\omega t}{2} d(\omega t) \right) \right]^{1/2} \\
I_{RMS} &= \left[\frac{I_m^2}{4\pi} \left[(\omega t)_0^{\pi} - \left(\frac{\sin 2\omega t}{2} \right)_0^{\pi} + (\omega t)_{\pi}^{2\pi} - \left(\frac{\sin 2\omega t}{2} \right)_{\pi}^{2\pi} \right] \right]^{1/2} \\
I_{RMS} &= \left[\frac{I_m^2}{4\pi} (\pi - 0 + 2\pi - \pi - 0) \right]^{1/2} \\
I_{RMS} &= \frac{I_m}{\sqrt{2}}
\end{aligned} \tag{4.25}$$

4. RMS value of Load Voltage (V_{LRMS})

$$\begin{aligned}
V_{LRMS} &= I_{RMS} R_L \\
V_{LRMS} &= \frac{I_m}{\sqrt{2}} R_L \\
V_{LRMS} &= \frac{V_m}{\sqrt{2} (R_L + R_f + R_S)} R_L \\
V_{LRMS} &= \frac{V_m}{\sqrt{2} R_L} R_L \\
V_{LRMS} &= \frac{V_m}{\sqrt{2}}
\end{aligned} \tag{4.26}$$

5. Rectifier Efficiency (η)

$$\begin{aligned}
\eta &= \frac{DC \text{ Output power}}{AC \text{ Input Power}} \times 100\% \\
\eta &= \frac{P_{DC}}{P_{AC}} = \frac{I_{DC}^2 R_L}{\frac{1}{2\pi} \int_0^{2\pi} V_i i d(\omega t)} = \frac{I_{DC}^2 R_L}{\frac{1}{2\pi} \int_0^{2\pi} i (R_L + R_f + R_S) i d(\omega t)}
\end{aligned}$$

Since $V_i = i(R_L + R_f + R_S)$

$$\eta = \frac{I_{DC}^2 R_L}{\frac{1}{2\pi} \int_0^{2\pi} i^2 (R_L + R_f + R_S) d(\alpha)} = \frac{I_{DC}^2 R_L}{\frac{1}{2\pi} \left(\int_0^{\pi} i_m^2 \sin^2 \alpha (R_L + R_f + R_S) d(\alpha) + \int_{\pi}^{2\pi} i_m^2 \sin^2 \alpha (R_L + R_f + R_S) d(\alpha) \right)}$$

$$\eta = \frac{\left(\frac{2I_m}{\pi} \right)^2 R_L}{I_{RMS}^2 (R_L + R_f + R_S)} = \frac{\frac{4I_m^2}{\pi^2} R_L}{\frac{I_m^2}{2} R_L}$$

$$\eta = \frac{8}{\pi^2} = 0.8105 = 81.1\% \quad (4.27)$$

In FWR maximum 81.1% of A.C power gets converted to D.C power in the load. Remaining 19% of power is present in terms of ripples in the output.

6. Ripple Factor (r)

The output of half wave rectifier contains pulsating components called ‘ripples’. Measure of such ripples present in output is with the help of a factor called ‘Ripple Factor (r)’.

$$r = \frac{\text{RMS value of AC component of output}}{\text{Average (or) DC component of output}}$$

$$r = \frac{I_{AC}}{I_{DC}}$$

Output current is composed of AC component as well as DC component.

I_{AC} = RMS value of AC component present in output

I_{DC} = RMS value of DC component present in output

I_{RMS} = RMS value of total output current

$$I_{RMS}^2 = I_{AC}^2 + I_{DC}^2$$

$$I_{AC} = \sqrt{I_{RMS}^2 - I_{DC}^2}$$

$$r = \frac{I_{AC}}{I_{DC}} = \frac{\sqrt{I_{RMS}^2 - I_{DC}^2}}{I_{DC}} = \sqrt{\frac{I_{RMS}^2 - I_{DC}^2}{I_{DC}^2}} = \sqrt{\frac{I_{RMS}^2}{I_{DC}^2} - 1} = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1}$$

$$r = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1} = \sqrt{\left(\frac{I_m / \sqrt{2}}{2I_m / \pi}\right)^2 - 1}$$

$$r = \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1} = 0.483 \quad (4.28)$$

This indicates that ripple contents in output are 0.483 times the DC component i.e., 48.3% of DC component which is much less than that of the half wave rectifier.

7. Form Factor (FF)

$$FF = \frac{I_{RMS}}{I_{DC}} = \frac{I_m / \sqrt{2}}{2I_m / \pi} = \frac{\pi}{2\sqrt{2}} = 1.111 \quad (4.29)$$

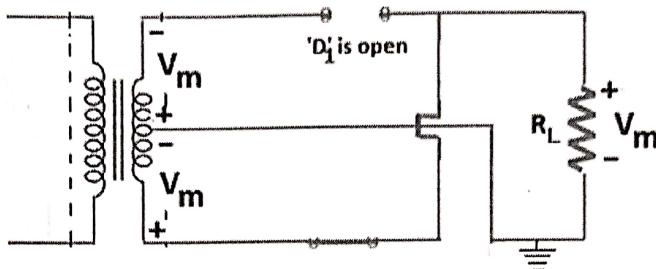
8. Peak Factor (PF)

$$PF = \frac{V_m}{V_{LRMS}} = \frac{V_m}{V_m / \sqrt{2}} = \sqrt{2} = 1.414 \quad (4.30)$$

9. Peak Inverse Voltage (PIV)

PIV is the peak voltage across the diode when the diode is reverse biased or non-conducting.

$$PIV = 2V_m \quad (4.31)$$



10. Transformer Utilization Factor (TUF)

The factor which indicates how much is the utilization of the transformer in the circuit is called TUF. In FWR the secondary current flows through each half separately in every half cycle. While primary of transformer carries current continuously. Hence, TUF is calculated for primary and secondary windings separately and then the average TUF is determined.

$$\text{Primary TUF} = \frac{\text{DC power delivered to the load}}{\text{AC power rating of primary of the transformer}}$$

$$\text{Primary TUF} = \frac{P_{DC}}{P_{AC}} = \frac{I_{DC}^2 R_L}{V_{SRMS} I_{RMS}} = \frac{(2I_m / \pi)^2 R_L}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}} = \frac{8}{\pi^2} = 0.811 = 81.1\%$$

The primary of transformer is feeding two half wave rectifiers separately. These two half wave rectifiers work independently of each other but feed a common load.

$$\text{Secondary TUF} = 2 \times \text{TUF of HWR}$$

$$\text{Secondary TUF} = 2 \times 0.287 = 0.574 = 57.4\%$$

$$\text{Average TUF for FWR} = \frac{\text{TUF of primary} + \text{TUF of secondary}}{2}$$

$$\text{Average TUF for FWR} = \frac{0.811 + 0.574}{2} = 0.693 = 69.3\% \quad (4.32)$$

Thus in FWR circuit, transformer gets utilized more than the half wave rectifier circuit.

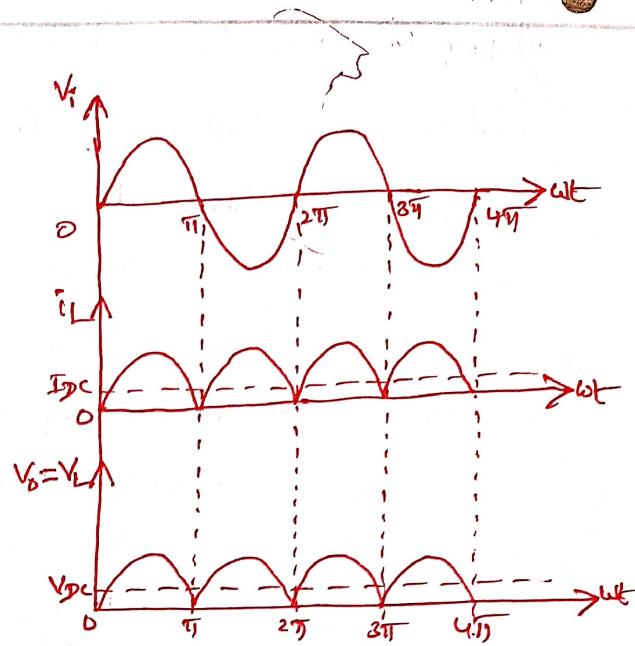
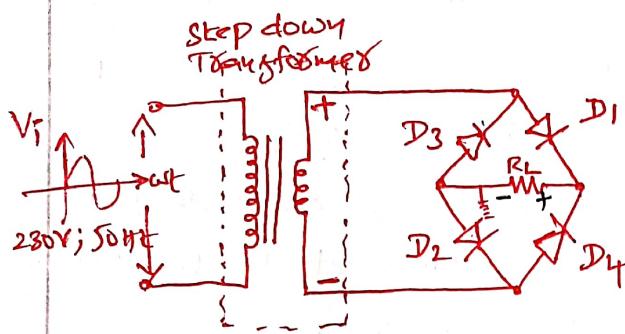
Advantages of FWR:

1. FWR Conducts for full cycle i.e., for positive cycle and for negative cycle.
2. Ripple Factor is low i.e., 0.483
3. Efficiency is high i.e., 81.1%
4. Transformer utilization factor is high i.e., 69.3%

Disadvantages of FWR:

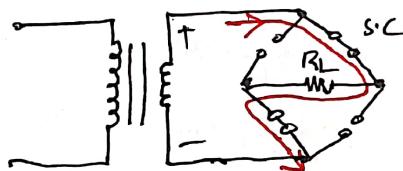
1. Cost is high as it uses center-tapped transformer.

Bridge Rectifier:



Operation for positive half cycle:

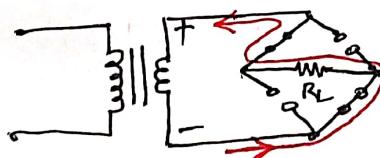
During positive cycle from $0\text{--}\pi$ duration diodes D_1 and D_2 are forward biased and are short circuited, current flows through D_1 entering the load at positive terminal, leaves the load at negative terminal and then flows through diode D_2 . During this cycle the diodes D_3 & D_4 are reverse biased and are open circuited and zero current flows through them.



current flow is represented by solid line.

Operation for Negative half cycle:

During negative half cycle the lower end of AC supply becomes positive diodes D_3 and D_4 become forward biased, current flows through D_3 entering the load at positive terminal, leaves the load at negative terminal and then flows through D_4 . During this cycle the diodes D_1 & D_2 are reverse biased and zero current flows through them.



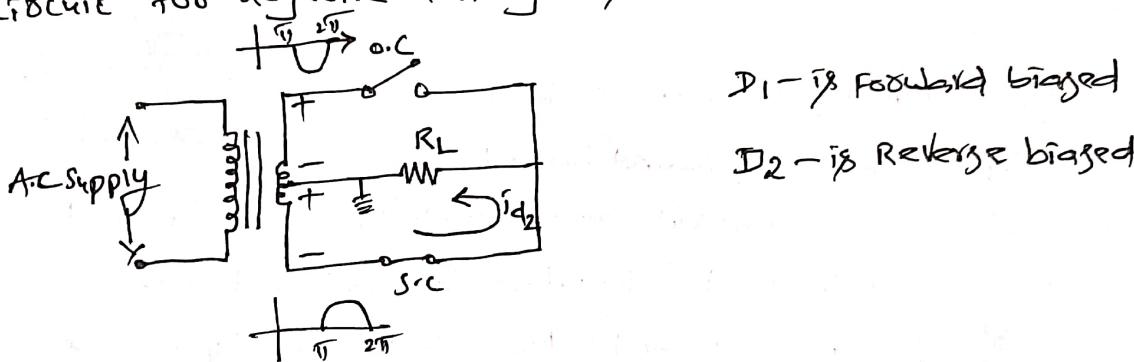
current flow is represented by solid line.

Thus the direction of flow of current through the load resistance R_L is same during both half cycles of the input supply voltage.

ii) For Negative half cycle:

When for negative half cycle from π to 2π duration is given as input to diode D_1 , then diode D_1 is reverse biased, open circuited and zero current flows through diode D_1 . i.e., $i_{D_1} = 0$.

- In the second half of the circuit, negative is converted to positive waveform from π to 2π duration then diode D_2 is forward biased, short circuited and current flows through D_2 .
- The circuit for negative half cycle is:



D_1 - is forward biased

D_2 - is Reverse biased

i) Average or DC load current, I_{DC} :

$$I_{DC} = \frac{1}{2\pi} \int_0^{2\pi} i_{D}(wt) dt \quad i = I_m \sin wt; \quad 0 \leq wt \leq \pi$$

$$= -I_m \sin wt; \quad \pi \leq wt \leq 2\pi$$

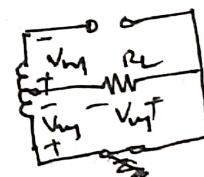
$$= \frac{1}{2\pi} \left[\int_0^{\pi} I_m \sin wt dt + \int_{\pi}^{2\pi} -I_m \sin wt dt \right]$$

$$\boxed{I_{DC} = \frac{2I_m}{\pi}}$$

$$\text{i)} V_{DC} = \frac{2V_m}{\pi}$$

$$\text{viii)} PIV = 2V_m$$

$$\text{ii)} I_{RMS} = \frac{I_m}{\sqrt{2}}; \quad V_{LRMS} = \frac{I_m}{\sqrt{2}} R_L$$



$$\text{iv)} \text{Efficiency, } \eta = 81.2\%$$

$$\text{ix)} TUF = 69.3\%$$

$$\text{v)} \text{Ripple factor, } \delta = 0.48$$

$$\text{vi)} \text{Form factor, F.F} = 1.11$$

$$\text{vii)} \text{Peak factor, P.F} = 1.414 = \frac{\text{Peak Value}}{\text{RMS Value}} = \frac{I_m}{I_m/\sqrt{2}} = \sqrt{2} = 1.414$$

4.3.4 Characteristics:

1. Average DC Load Current (I_{DC})

Average or DC value is obtained by integration of alternating current.

$$\text{Average value} = \frac{\text{Area under the curve over one complete cycle i.e., } (0-2\pi)}{\text{Base i.e., } 2\pi}$$

$$I_{DC} = \frac{\int_0^{2\pi} i d(\omega t)}{2\pi}$$

$$\text{Where } i = \begin{cases} I_m \sin \omega t; & 0 \leq \omega t \leq \pi \\ -I_m \sin \omega t; & \pi \leq \omega t \leq 2\pi \end{cases}$$

$$I_{DC} = \frac{1}{2\pi} \left[\int_0^{\pi} i d(\omega t) + \int_{\pi}^{2\pi} i d(\omega t) \right]$$

$$I_{DC} = \frac{1}{2\pi} \left[\int_0^{\pi} I_m \sin \omega t d(\omega t) + \int_{\pi}^{2\pi} -I_m \sin \omega t d(\omega t) \right]$$

$$I_{DC} = \frac{I_m}{2\pi} \left[[-\cos \omega t]_0^{\pi} - [-\cos \omega t]_{\pi}^{2\pi} \right]$$

$$I_{DC} = \frac{I_m}{2\pi} [1 + 1 + 1 + 1]$$

$$I_{DC} = \frac{2I_m}{\pi}$$

2. Average DC Load Voltage (V_{DC})

$$V_{DC} = I_{DC} R_L$$

$$V_{DC} = \frac{2I_m}{\pi} R_L$$

$$\because I_m = \frac{V_m}{R_L + 2R_f + R_S} \quad \begin{cases} R_L = \text{load resist} \tan ce \\ R_f = \text{diode internal forward resist} \tan ce \\ R_S = \text{transformer secondary winding resist} \tan ce \end{cases}$$

$$V_{DC} = \frac{2V_m}{\pi(R_L + 2R_f + R_S)} R_L$$

$$\therefore R_L \gg (2R_f + R_S)$$

$$V_{DC} = \frac{2V_m}{\pi R_L} R_L$$

$$V_{DC} = \frac{2V_m}{\pi}$$

3. RMS value of Load Current (I_{RMS})

RMS means squaring, finding mean and then finding square root.

$$I_{RMS} = \left[\frac{1}{2\pi} \int_0^{2\pi} i^2 d(\omega t) \right]^{1/2}$$

$$\begin{aligned}
I_{RMS} &= \left[\frac{1}{2\pi} \left(\int_0^{\pi} i^2 d(\omega t) + \int_{\pi}^{2\pi} i^2 d(\omega t) \right) \right]^{1/2} \\
I_{RMS} &= \left[\frac{1}{2\pi} \left(\int_0^{\pi} I_m^2 \sin^2 \omega t d(\omega t) + \int_{\pi}^{2\pi} I_m^2 \sin^2 \omega t d(\omega t) \right) \right]^{1/2} \\
I_{RMS} &= \left[\frac{I_m^2}{2\pi} \left(\int_0^{\pi} \sin^2 \omega t d(\omega t) + \int_{\pi}^{2\pi} \sin^2 \omega t d(\omega t) \right) \right]^{1/2} \\
I_{RMS} &= \left[\frac{I_m^2}{2\pi} \left(\int_0^{\pi} \frac{1 - \cos 2\omega t}{2} d(\omega t) + \int_{\pi}^{2\pi} \frac{1 - \cos 2\omega t}{2} d(\omega t) \right) \right]^{1/2} \\
I_{RMS} &= \left[\frac{I_m^2}{4\pi} \left[(\omega t)_0^\pi - \left(\frac{\sin 2\omega t}{2} \right)_0^\pi + (\omega t)_{\pi}^{2\pi} - \left(\frac{\sin 2\omega t}{2} \right)_{\pi}^{2\pi} \right] \right]^{1/2} \\
I_{RMS} &= \left[\frac{I_m^2}{4\pi} (\pi - 0 + 2\pi - \pi) \right]^{1/2} \\
I_{RMS} &= \frac{I_m}{\sqrt{2}}
\end{aligned}$$

4. RMS value of Load Voltage (V_{LRMS})

$$V_{LRMS} = I_{RMS} R_L$$

$$V_{LRMS} = \frac{I_m}{\sqrt{2}} R_L$$

$$V_{LRMS} = \frac{V_m}{\sqrt{2} (R_L + 2R_f + R_S)} R_L$$

$$V_{LRMS} = \frac{V_m}{\sqrt{2} R_L} R_L$$

$$V_{LRMS} = \frac{V_m}{\sqrt{2}}$$

5. Rectifier Efficiency (η)

$$\eta = \frac{DC \text{ Output power}}{AC \text{ Input Power}} \times 100\%$$

$$\eta = \frac{P_{DC}}{P_{AC}} = \frac{I_{DC}^2 R_L}{\frac{1}{2\pi} \int_0^{2\pi} V_i i d(\omega t)} = \frac{I_{DC}^2 R_L}{\frac{1}{2\pi} \int_0^{2\pi} i(R_L + 2R_f + R_S) i d(\omega t)}$$

Since $V_i = i(R_L + 2R_f + R_S)$

$$\eta = \frac{I_{DC}^2 R_L}{\frac{1}{2\pi} \int_0^{2\pi} i^2 (R_L + 2R_f + R_S) d(\omega t)}$$

$$\eta = \frac{I_{DC}^2 R_L}{\frac{1}{2\pi} \left(\int_0^\pi i_m^2 \sin^2 \alpha (R_L + 2R_f + R_S) d(\alpha) + \int_\pi^{2\pi} i_m^2 \sin^2 \alpha (R_L + 2R_f + R_S) d(\alpha) \right)}$$

$$\eta = \frac{\left(\frac{2I_m}{\pi} \right)^2 R_L}{I_{RMS}^2 (R_L + 2R_f + R_S)} = \frac{\frac{4I_m^2}{\pi^2} R_L}{\frac{I_m^2}{2} R_L}$$

$$\eta = \frac{8}{\pi^2} = 0.8105 = 81.1\%$$

In Bridge Rectifier maximum 81.1% of A.C power gets converted to D.C power in the load.

Remaining 19% of power is present in terms of ripples in the output.

6. Ripple Factor (r)

The output of half wave rectifier contains pulsating components called 'ripples'. Measure of such ripples present in output is with the help of a factor called 'Ripple Factor (r)'.

$$r = \frac{\text{RMS value of AC component of output}}{\text{Average (or) DC component of output}}$$

$$r = \frac{I_{AC}}{I_{DC}}$$

Output current is composed of AC component as well as DC component.

I_{AC} = RMS value of AC component present in output

I_{DC} = RMS value of DC component present in output

I_{RMS} = RMS value of total output current

$$I_{RMS}^2 = I_{AC}^2 + I_{DC}^2$$

$$I_{AC} = \sqrt{I_{RMS}^2 - I_{DC}^2}$$

$$r = \frac{I_{AC}}{I_{DC}} = \frac{\sqrt{I_{RMS}^2 - I_{DC}^2}}{I_{DC}} = \sqrt{\frac{I_{RMS}^2 - I_{DC}^2}{I_{DC}^2}} = \sqrt{\frac{I_{RMS}^2}{I_{DC}^2} - 1} = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1}$$

$$r = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1} = \sqrt{\left(\frac{I_m / \sqrt{2}}{2I_m / \pi}\right)^2 - 1}$$

$$r = \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1} = 0.483$$

This indicates that ripple contents in output are 0.483 times the DC component i.e., 48.3% of DC component which is much less than that of the half wave rectifier.

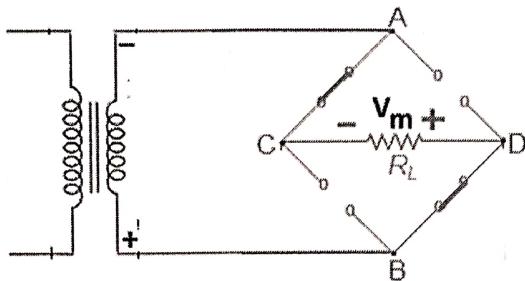
$$7. \text{ Form Factor (FF): } FF = \frac{I_{RMS}}{I_{DC}} = \frac{I_m / \sqrt{2}}{2I_m / \pi} = \frac{\pi}{2\sqrt{2}} = 1.111$$

$$8. \text{ Peak Factor (PF): } PF = \frac{V_m}{V_{LRMS}} = \frac{V_m}{V_m / \sqrt{2}} = \sqrt{2} = 1.414$$

9. Peak Inverse Voltage (PIV)

PIV is the peak voltage across the diode when the diode is reverse biased or non-conducting.

$$PIV = V_m \quad (4.33)$$



10. Transformer Utilization Factor (TUF)

The factor which indicates how much is the utilization of the transformer in the circuit is called TUF.

$$TUF = \frac{DC \text{ power delivered to the load}}{AC \text{ power rating of transformer}}$$

$$TUF = \frac{P_{DC}}{P_{AC}} = \frac{I_{DC}^2 R_L}{V_{SRMS} I_{RMS}} = \frac{(2I_m / \pi)^2 R_L}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}} = \frac{8}{\pi^2} = 0.811 \approx 81.1\% \quad (4.34)$$

Thus in Bridge Rectifier circuit, transformer gets utilized more than the half wave and full wave rectifier circuits.

Advantages of Bridge Rectifier:

1. No center-tapped transformer
2. Transformer is effectively utilized

Disadvantages of Bridge Rectifier:

1. Use of four diodes as compared to two diodes in FWR.

4.4 COMPARISON OF RECTIFIER CIRCUITS

S.No	Parameter	HWR	FWR	Bridge Rectifier
1.	Circuit	diagram	diagram	Diagram
2.	Number of diodes	1	2	4
3.	Average DC load current, I_{DC}	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$
4.	Average DC load voltage, V_{DC}	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2V_m}{\pi}$
5.	RMS value of load current, I_{RMS}	$\frac{I_m}{2}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$
6.	RMS value of load voltage, V_{LRMS}	$\frac{V_m}{2}$	$\frac{V_m}{\sqrt{2}}$	$\frac{V_m}{\sqrt{2}}$
7.	Efficiency, η	40.5%	81.1%	81.1%
8.	Ripple factor, r	1.211	0.483	0.483
9.	Form Factor, FF	1.57	1.111	1.111
10.	Peak Factor, PF	2	1.414	1.414
11.	Peak Inverse Voltage	V_m	$2V_m$	V_m
12.	TUF	28.7%	69.3%	81.1%

FILTERS

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Harmonic Components in Rectified Circuit

The analytical representation of output current wave in a rectifier is obtained by means of a Fourier series.

$$\text{For HWR} \Rightarrow i = I_m \left[\frac{1}{\pi} + \frac{1}{2} \sin \omega t - \frac{2}{\pi} \sum_{k=2,4,6,\dots} \frac{\cos k \omega t}{(k+1)(k-1)} \right]$$

$$\text{For FWR} \Rightarrow i = I_m \left[\frac{2}{\pi} - \frac{4}{\pi} \sum_{k=2,4,6,\dots} \frac{\cos k \omega t}{(k+1)(k-1)} \right]$$

A power supply must provide an essentially ripple-free source of power from an a.c. line.

From the above equations the output of rectifier contains ripple components in addition to a d.c. term. Hence it is necessary to include a filter between the rectifier and the load in order to attenuate these ripple components.

Inductor Filter

Filter is an electronic circuit composed of a capacitor, inductor or combination of both connected between the rectifier and the load so as to convert pulsating dc to pure dc.

i) For HWR's

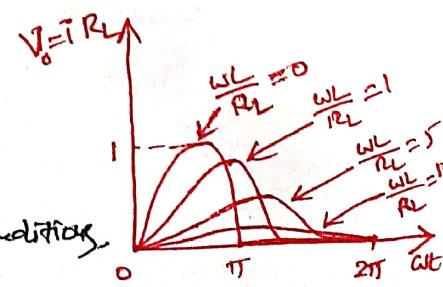
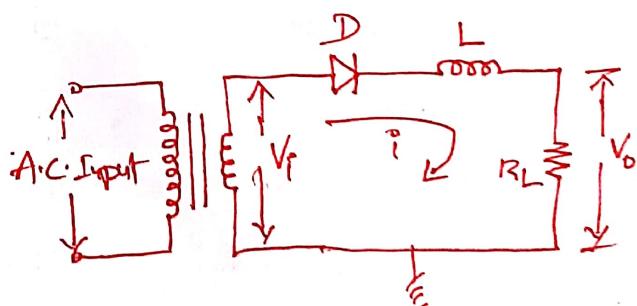
- In this the inductor (choke) is connected in series with the load.
- Inductor opposes any change of current that may flow through it.
- From the figure:

$$V_f = L \frac{di}{dt} + i R_L$$

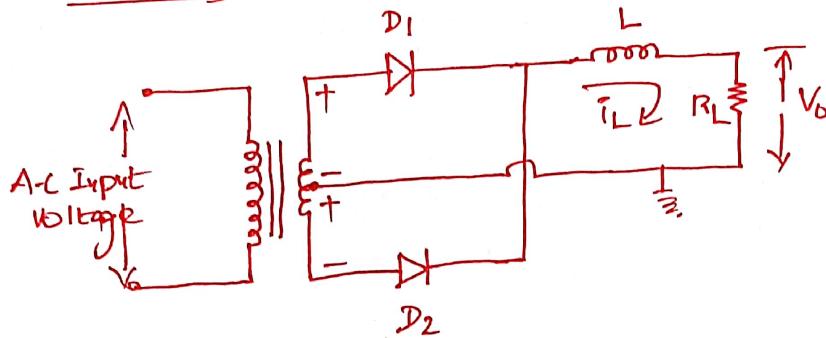
$$i = \frac{V_f}{R_L} = \frac{L \frac{di}{dt}}{R_L}$$

The above equation is plotted for three different conditions

- a) with no inductor $L=0$; $\frac{WL}{R_L} = 0$
- b) with inductor value $\frac{WL}{R_L} = 1, 5, 10$.



ii) FOR FWR:



The inductor offers high impedance to a.c. variations and the inductor blocks the a.c. component and allows only d.c. component.

Load current $i = \frac{2I_m}{\pi} - \frac{4I_m}{\pi} \sum_{k=2,4,6} \frac{\cos k\omega t}{(k+1)(k-1)}$

d.c. component $I_m = \frac{V_m}{R_L}$ $i = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi} \cos \omega t \rightarrow ①$

a.c. component $I_m = \frac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}}$

Substituting d.c & a.c terms in ① we get

$$i = \frac{2V_m}{\pi R_L} - \frac{4V_m}{3\pi \sqrt{R_L^2 + 4\omega^2 L^2}} \cos(\omega t - \phi)$$

where ' ϕ ' is the angle by which the load current lags behind the voltage. This is given by $\phi = \tan^{-1} \frac{2\omega L}{R_L}$.

Ripple Factor, $\delta = \frac{I_{ac, rms}}{I_{DC}}$; $I_{DC} = \frac{2V_m}{\pi R_L}$

$$\delta = \frac{\frac{4V_m}{3\pi\sqrt{2}\sqrt{R_L^2 + 4\omega^2 L^2}}}{\frac{2V_m}{\pi R_L}}$$

$$I_{ac, rms} = \frac{4V_m}{3\pi\sqrt{2}\sqrt{R_L^2 + 4\omega^2 L^2}}$$

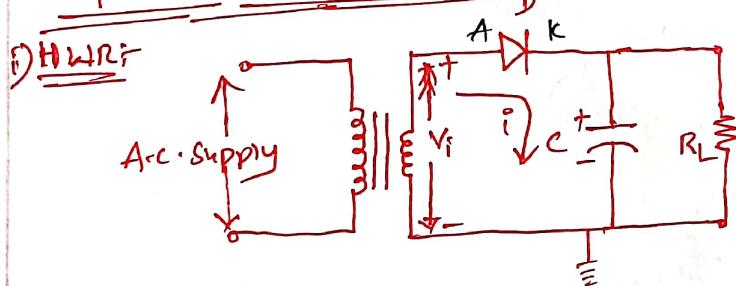
$$\delta = \frac{2}{3\sqrt{2}} \times \frac{R_L}{\sqrt{R_L^2 + 4\omega^2 L^2}} = \frac{2}{3\sqrt{2}} \sqrt{\frac{R_L^2}{R_L^2 + 4\omega^2 L^2}}$$

$$\text{if } \frac{4\omega^2 L^2}{R_L^2} \gg 1 \text{ then } \delta = \frac{2}{3\sqrt{2} \sqrt{1 + \frac{4\omega^2 L^2}{R_L^2}}} = \frac{2}{3\sqrt{2} \times \frac{2\omega L}{R_L}}$$

$$\boxed{\delta = \frac{R_L}{3\sqrt{2} \omega L}}$$

- i) At no load $R_L = \infty$ then $\delta = \frac{2}{3\sqrt{2}} = 0.47$ (use δ of FWR)
- ii) The expression for ripple factor shows that ripple varies inversely as the magnitude of inductance, and it is smaller for smaller values of R_L i.e; for high currents.
- Thyristor filters should be used when R_L is consistently small.

2) Capacitor Filters:



- The operation of capacitor stores energy during conduction period and delivers this energy to the load during non-conduction period.
- For positive input a.c signal the diode D is forward biased and it conducts, then the capacitor C quickly charges to peak value of input voltage V_m .
- When input starts decreasing below its V_m the diode is reverse biased since cathode voltage of diode becomes more positive than anode. (At cathode voltage is V_C which is more than anode voltage V_m).

- For Negative half cycle, capacitor discharges through R_L with a time constant of $T = R_L C$ which is large and hence capacitor discharges very little from V_m .

- In the next positive half cycle, when input signal becomes more than the capacitor voltage, the diode becomes forward biased and capacitor is charged back to V_m .

- (A) - (B) capacitor discharges diode is OFF.
- (B) - (C) capacitor charges diode is ON.

Ripple factor expression:

Let T_1 = time for which diode is conducting

T_2 = time for which diode is non conducting.

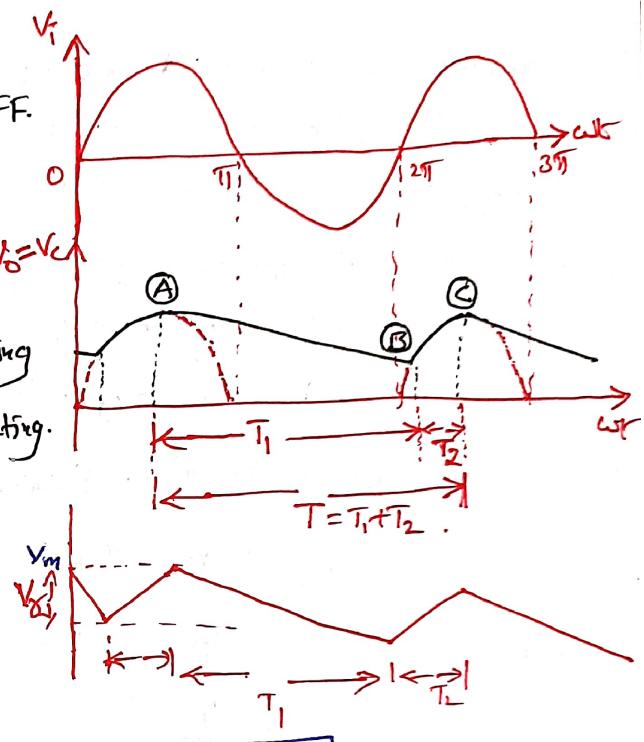
T = time period of a.c. input voltage

Let V_δ be peak to peak value of ripple

voltage which is triangular waveform.

- R.M.S value of triangular wave form

$$\text{so } V_{\text{rms}} = \frac{V_\delta}{2\sqrt{3}} \rightarrow 1$$



$$V_{\text{dc}} = V_m - \frac{V_\delta}{2} \quad \text{from the figure.}$$

During T_1 capacitor discharges. \therefore The charge lost is $Q = C \cdot V_\delta$

$$Q = C \cdot V_\delta \rightarrow 2$$

$$\text{But } i = \frac{dQ}{dt} \Rightarrow Q = \int_0^{T_1} i dt = I_{DC} T_1 \rightarrow 3$$

$$\text{From } 2 \text{ & } 3 \quad C \cdot V_\delta = I_{DC} T_1 \Rightarrow V_\delta = \frac{I_{DC} T_1}{C} \quad \because T_1 + T_2 = T$$

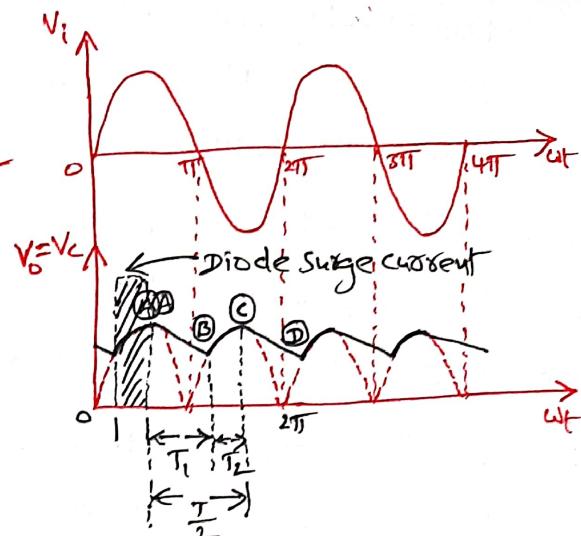
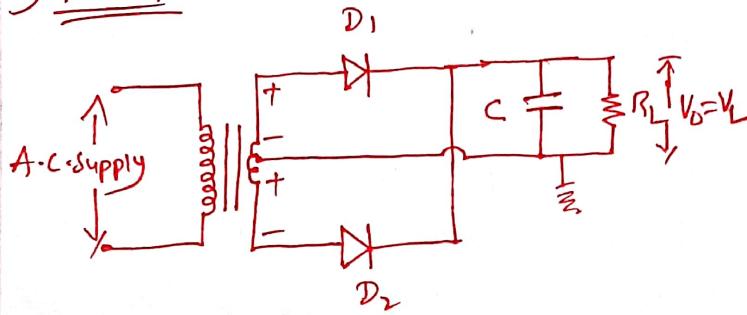
$$V_\delta = \frac{I_{DC} \cdot T}{C} = \frac{I_{DC}}{f \cdot C} \quad \because T = \frac{1}{f} \quad T_1 = T \quad (T_1 \gg T_2)$$

$$V_\delta = \frac{I_{DC}}{f \cdot C \cdot R_L} \quad \therefore I_{DR} = \frac{V_{DC}}{R_L}$$

$$\therefore \text{Ripple factor, } \gamma = \frac{V_{\text{rms}}}{V_{\text{dc}}} = \frac{V_\delta}{2\sqrt{3} \cdot V_\delta \cdot f \cdot C \cdot R_L} \Rightarrow \boxed{\gamma = \frac{1}{2\sqrt{3} f \cdot C \cdot R_L}}$$

\therefore As capacity increases ripples are reduced.

i) FWR:



- During positive cycle of ac input signal, diode D_1 is forward biased, capacitor C charges to peak value of V_m .
- In the next quarter cycle the capacitor starts discharging because D_1 is reverse biased and stops conducting. It discharges with $R_L C$ constant.
- In the next cycle D_2 is forward biased and charges capacitor to V_m .

$$\text{Here } T_1 + T_2 = T/2.$$

Ripple factor: since $T_1 \gg T_2 \Rightarrow T_1 = T/2$.

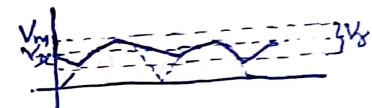
$$\therefore V_R = \frac{I_{DC} T_1}{C}$$

$$V_R = \frac{I_{DC} \cdot T}{2C} = \frac{I_{DC}}{2 \cdot f \cdot C} = \frac{V_{DC}}{2 \cdot f \cdot C \cdot R_L}$$

$$V_{Rms} = \frac{V_R}{2\sqrt{3}}$$

$$\therefore \delta = \frac{V_{Rms}}{V_{DC}} = \frac{V_R}{2\sqrt{3} \cdot V_{DC}} = \frac{V_{DC}}{2\sqrt{3} \cdot 2 \cdot f \cdot C \cdot R_L \cdot V_{DC}} = \frac{1}{4\sqrt{3} \cdot f \cdot C \cdot R_L}$$

$$\therefore \delta = \frac{1}{4\sqrt{3} \cdot f \cdot C \cdot R_L}$$



$$V_{DC} = V_m - \frac{V_R}{2}$$

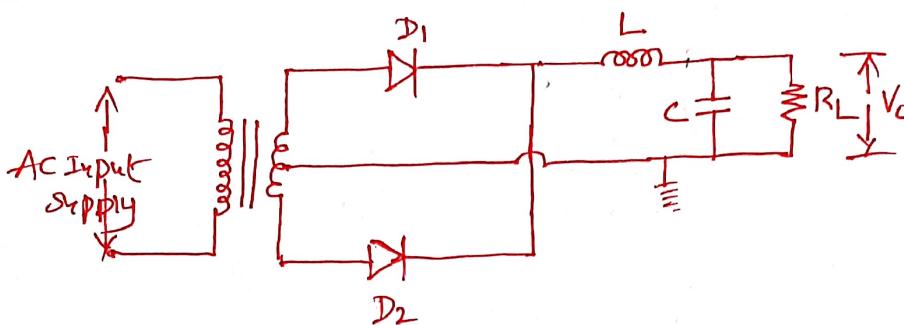
$$V_{DC} = V_m - \frac{I_{DC}}{4fC} \rightarrow \text{FWR}$$

$$V_{DC} = V_m - \frac{I_{DC}}{2fC} \rightarrow \text{HWR}$$

Surge current: In Full Wave & Bridge Rectifiers the forward resistance of diodes is very small and a large current flows through D_1 & D_2 instantaneously. This is called surge current. Such a peak surge current can destroy the diodes.

To limit these surge currents, a surge limiting Resistor R_s is used in the circuit.

3) L-section Filter (or) LC Filter:



- The series inductor filter and shunt capacitors filter are not much efficient to provide low ripple at all loads. Because, the inductor filter has low ripple at small loads ($\propto R_L$) whereas the capacitors filter has low ripple at heavy loads ($\propto 1/R_L$).
- The combination of these two filters may be selected to make the ripple independent of load resistance. The resulting filter is called L-section filter (or) LC filter (or) choke input filter.
- Capacitors shunting the load bypasses the harmonic currents because it offers very low reactance to a.c. ripple current while it appears as an open circuit to d.c. current.
- Inductors offers high impedance to the harmonic terms. In this way, most of the ripple voltage is eliminated from load voltage.

→ The a.c. current through 'L' ($X_L = 2\pi f L$ at second harmonic) is given by

$$I_{\text{oms;ac}} = \frac{4V_0}{3\pi\sqrt{2}} \times \frac{1}{X_L}$$

$$\left[\because i = \frac{2V_0}{\pi R_L} - \frac{4V_0}{3\pi X_L} \cos 2\omega t \right]$$

The a.c. voltage across the capacitor is:

$$V_{\text{oms;ac}} = I_{\text{oms;ac}} \times X_C$$

$$= \frac{4V_0}{3\pi\sqrt{2}} \times \frac{X_C}{X_L}$$

$$\text{Ripple factor, } \delta = \frac{V_{\text{rms; ac}}}{V_{\text{dc}}}$$

$$= \frac{\frac{4V_m}{3\pi\sqrt{2}} \frac{x_c}{x_L}}{\frac{V_{\text{dc}} \frac{2V_m}{\pi}}{x_L}} = \frac{2}{3\sqrt{2}} \frac{x_c}{x_L}$$

$$\text{Since } x_c = \frac{1}{2\omega C} \text{ and } x_L = 2\omega L$$

$$\delta = \frac{\sqrt{2}}{3} \frac{1}{2\omega C \times 2\omega L} \Rightarrow \boxed{\frac{1}{6\sqrt{2}\omega^2 LC} = \delta}$$

\therefore Ripple factor is independent of load.

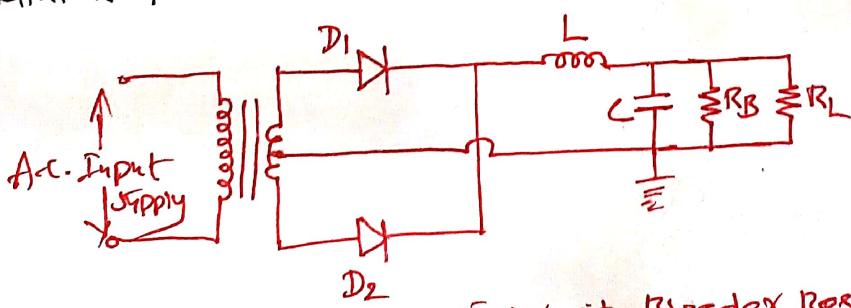
Bleeder Resistance, 'R_B'

The current through the choke (L) must be continuous and not interrupted. An interrupted current through the choke may develop a large ^{back}e.m.f (which is in excess of PIV rating of diodes)

This back e.m.f is harmful to diodes and capacitors. To eliminate back e.m.f developed across the choke, the current through it must be maintained continuous. This is ensured by connecting a bleeder resistance, 'R_B' across the output terminals. $R_B \geq 943L$ at 50Hz.

Critical Inductance, 'L_C'

The value of inductance 'L' must be kept above certain minimum value so that the current flows through the circuit all the time, this minimum value of inductance is called "critical inductance, L_C".

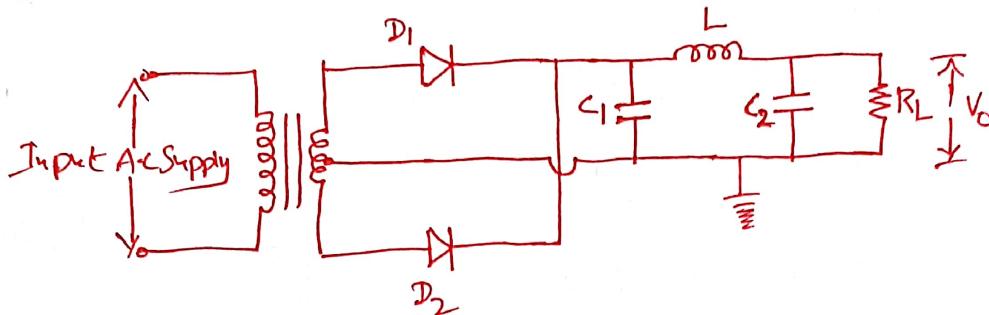


$$L_C \geq \frac{R_L}{943} \text{ at 50Hz}$$

$$\frac{4V_m}{3\pi x_L} \leq \frac{V_{\text{dc}}}{R_L}$$

Filter with Bleeder Resistance:

II-Section Filter (or) CLC Filter:



- This is capacitive filter followed by L-section filter.
- The ripple rejection capability of II-section filter is very good.
- The rectified output is given to capacitor \$C_1\$. This capacitor blocks d.c component and allows a.c. and bypasses all a.c.
- The a.c. then reaches to choke \$L\$ which passes d.c and blocks a.c component. The capacitor \$C_2\$ now allows remaining a.c component and almost pure d.c reaches to the load.

Ripple factor derivation:

The Fourier analysis of a triangular wave at output of capacitor \$C_1\$ is

$$V = V_{dc} - \frac{V_0}{\pi} \left(\sin 2\omega t - \frac{\sin 4\omega t}{2} + \frac{\sin 6\omega t}{3} - \dots \right)$$

$$\text{We know that } V_0 = \frac{I_{dc}}{2 \cdot C \cdot f} = \frac{I_{dc}}{2 \cdot C_1 \cdot f}$$

$$\text{RMS second harmonic Voltage is } V_{rms,ac} = \frac{V_0}{\sqrt{2}} = \frac{I_{dc}}{\sqrt{2} \pi f C_1 \sqrt{2}} = \sqrt{2} I_{dc} X_1$$

$$X_C = \frac{1}{2\omega C}$$

The Voltage \$V_{rms,ac}\$ is impressed on L-section now,

$$\text{the Ripple Voltage } V_{rms,ac}' = V_{rms,ac} \times \frac{X_2}{X_L}$$

$$= \sqrt{2} \cdot I_{dc} \cdot X_1 \cdot \frac{X_2}{X_L}$$

$$\text{Ripple factor } \delta = \frac{V_{\text{rms}, \text{ac}}}{V_{\text{dc}}}$$

$$= \frac{\sqrt{2} I_{\text{dc}} X_{C_1} \cdot X_{C_2}}{I_{\text{dc}} \cdot R_L \cdot X_L} \quad [\because V_{\text{dc}} = I_{\text{dc}} \cdot R_L]$$

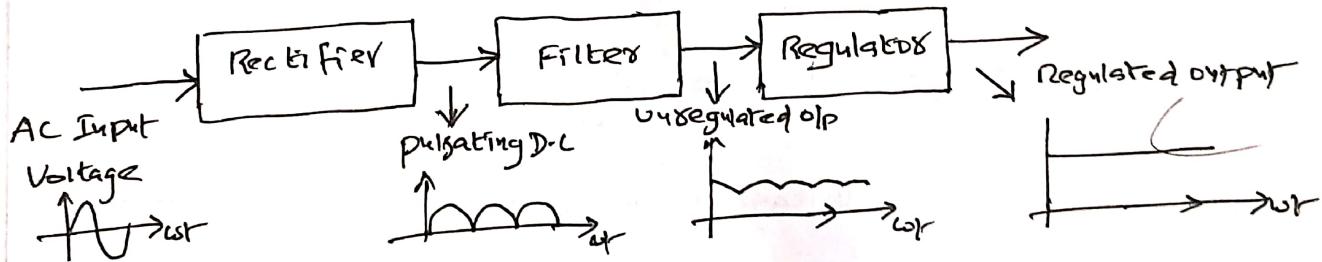
$$\boxed{\delta = \frac{\sqrt{2} X_{C_1} X_{C_2}}{R_L \cdot X_L}}$$

$$X_{C_1} = \frac{1}{2\omega C_1}; \quad X_{C_2} = \frac{1}{2\omega C_2}; \quad X_L = 2\omega L$$

$$\delta = \frac{\sqrt{2} \times 1}{2\omega C_1 \cdot 2\omega C_2 \cdot R_L \cdot 2\omega L} = \frac{\sqrt{2}}{8\omega^3 C_1 C_2 L R_L}$$

Use of Zener diode as a Voltage Regulator:

A Voltage Regulator is the one which is designed to keep the output voltage constant under varying input voltage and load.



Zener diode is used in Regulator because the zener diode is operated in the breakdown condition where the voltage across Zener is constant, irrespective of changes in zener current. So it can be used to regulate the voltage with varying input voltage or varying load conditions.

Special Semiconductor Diodes:-

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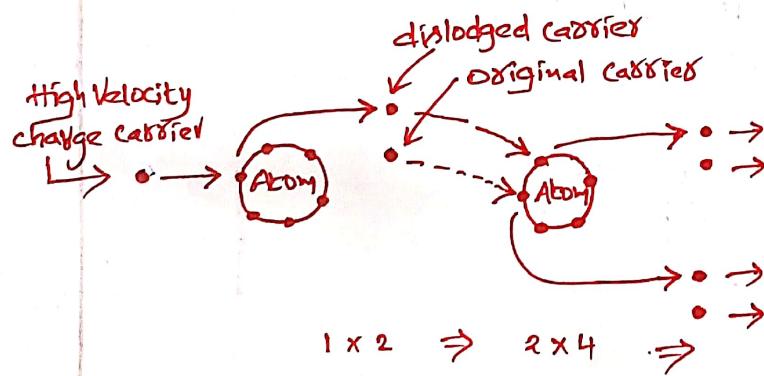
Breakdown Mechanisms in Semiconductor diodes:-

Diodes which are designed with adequate power dissipation capabilities to operate in breakdown region are known as "Avalanche Breakdown (or) Zener diodes".

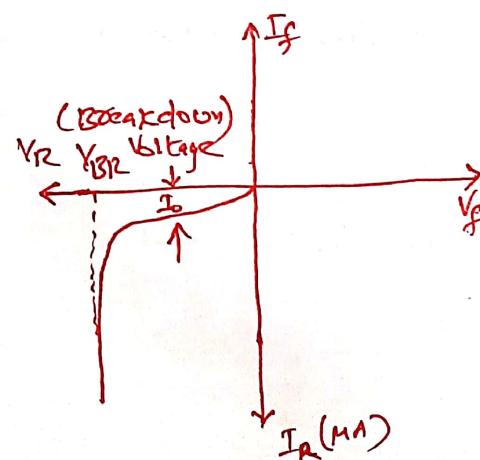


i) Avalanche Breakdown:

- In the P-N Junction diode in Reverse Bias a small reverse saturation current, I_0 flows due to movement of minority charge particles.
- As Reverse Voltage becomes larger the minority carriers increasingly accelerate. These carriers collide with the charge carriers present in covalent bond of crystal structure.
- These carriers in covalent bond acquire sufficient energy and come out from the bond creating new charge carriers.
- These new carriers in turn produce additional carriers again through the process of disrupting bonds this cumulative process is referred to as "Avalanche multiplication (or) carrier multiplication". This results in flow of large reverse currents and the diode finds itself in the region of "Avalanche Breakdown".

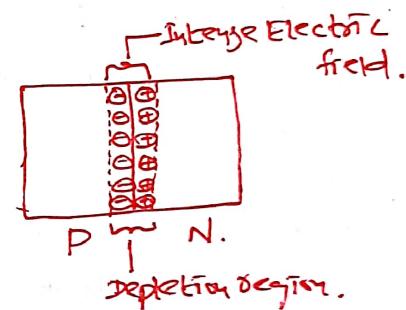
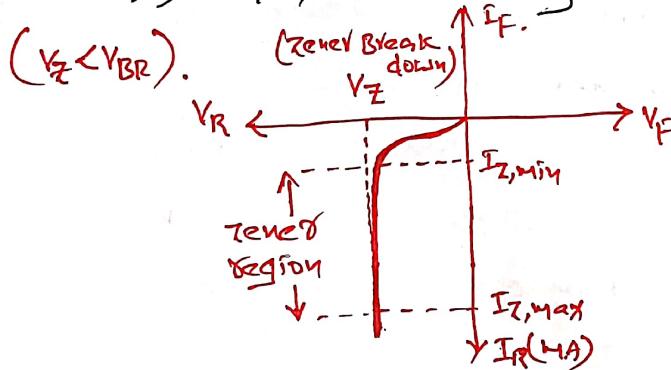


Avalanche Multiplication



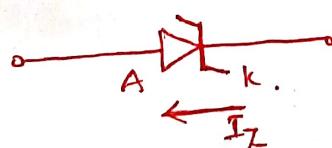
ii) Zener Breakdown:

- When a P-N Junction is heavily doped the depletion region becomes narrow.
- In Reverse bias conditions, the electric field across the depletion layer is very intense. This intense field pulls the charge carriers out of valence bands of stable atoms easily.
- Under these circumstances the minority carriers constitute very large current and the breakdown is referred to as "Zener Breakdown".
- Thus the Zener Breakdown voltage decreases as the temperature increases this is called "negative temperature coefficient".



Zener Diode Characteristics:

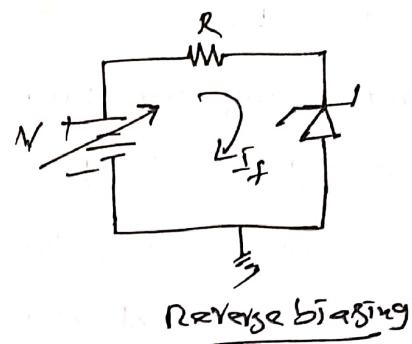
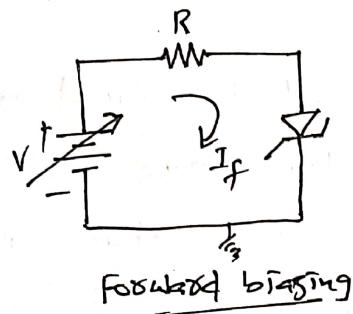
- Zener diode is a heavily doped PN junction semiconductor diode it is doped with 10^4 parts 1 part of impurity.
- In 1934, a physicist Carl Zener investigated the breakdown phenomenon.
- Zener diode is operated in "Reverse Breakdown Region".



Zener diode Symbol

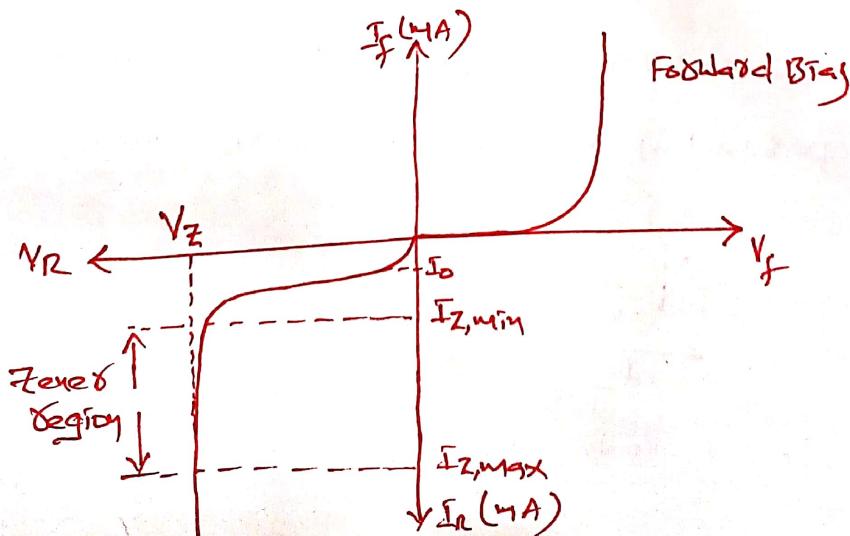
Forward bias:

In forward bias the normal diode and zener diode operate in similar fashion.



Reverse bias:

- In Reverse bias, the diode carries reverse saturation current, I_0 till $V_R < V_Z$. This current is very small in the order of few mA.
- At $V_R \geq V_Z$, current through zener diode increases rapidly. The current corresponding to knee point which change from low value to large value is called "Zener knee current" ($I_{Z,min}$).
- At this knee, a break down is said to occur in the device. The reverse voltage at which breakdown occurs is called "zener breakdown voltage, V_Z ".
- The maximum current a zener diode can carry safely is called "Zener maximum current, $I_{Z,max}$ ".
- Applications of zener diode are i) Voltage Regulators ii) Protection Circuits iii) Voltage limiters.



$$\text{Ripple factor } \delta = \frac{V_{\text{rms}, \text{ac}}}{V_{\text{dc}}}$$

$$= \frac{\sqrt{2} I_{\text{dc}} X_{C_1} \cdot X_{C_2}}{I_{\text{dc}} \cdot R_L \cdot X_L} \quad [\because V_{\text{dc}} = I_{\text{dc}} \cdot R_L]$$

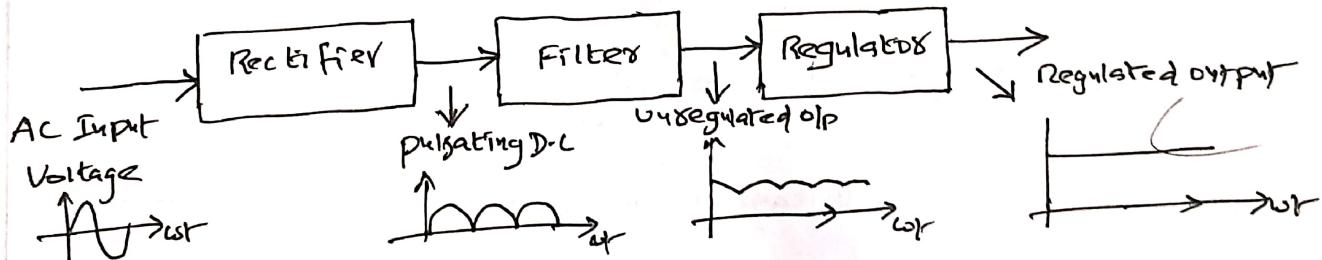
$$\boxed{\delta = \frac{\sqrt{2} X_{C_1} X_{C_2}}{R_L \cdot X_L}}$$

$$X_{C_1} = \frac{1}{2\omega C_1}; \quad X_{C_2} = \frac{1}{2\omega C_2}; \quad X_L = 2\omega L$$

$$\delta = \frac{\sqrt{2} \times 1}{2\omega C_1 \cdot 2\omega C_2 \cdot R_L \cdot 2\omega L} = \frac{\sqrt{2}}{8\omega^3 C_1 C_2 L R_L}$$

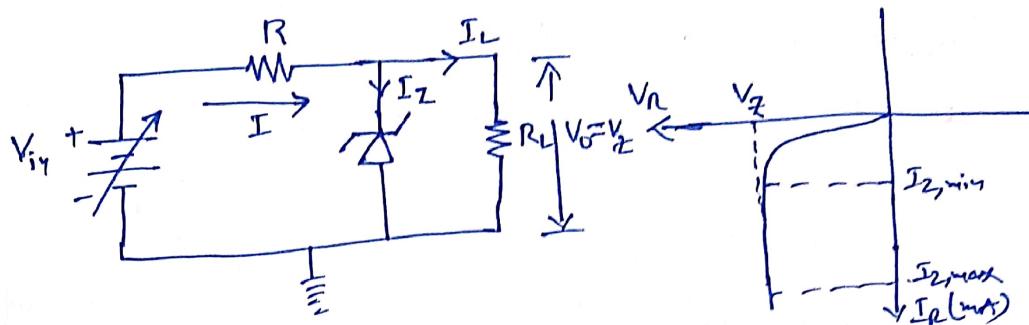
Use of Zener diode as a Voltage Regulator:

A Voltage Regulator is the one which is designed to keep the output voltage constant under varying input voltage and load.



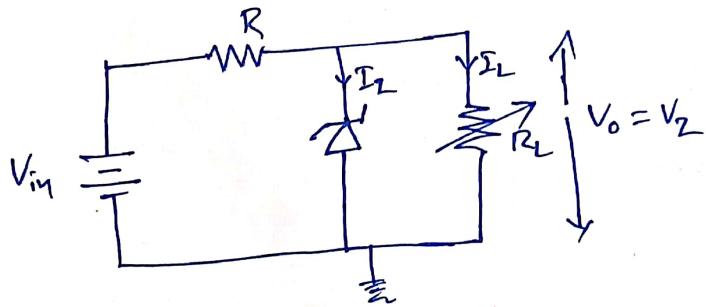
Zener diode is used in Regulator because the zener diode is operated in the breakdown condition where the voltage across Zener is constant, irrespective of changes in zener current. So it can be used to regulate the voltage with varying input voltage or varying load conditions.

i) Regulation with a Varying Input Voltage:



As input voltage increases, I_Z also varies accordingly, but the zener diode maintains constant voltage across the output terminals over a certain range. These limitations on the input variations are set by the minimum and maximum current values with which the zener can operate.

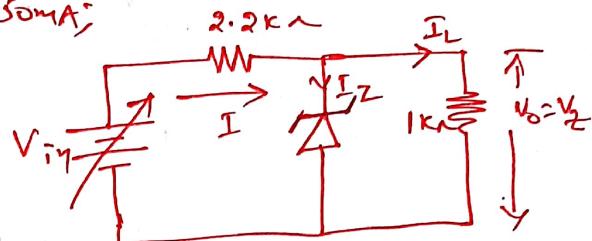
ii) Regulation with a Varying Load:



Zener diode maintains a constant voltage across R_L as long as the zener current is greater than $I_{Z,min}$ and less than $I_{Z,max}$. When the load current varies, the zener diode current adjusts itself so that its terminal voltage remains constant.

(P) For Zener Regulator shown in fig. calculate the range of input voltage for which output will remain constant.

Given $V_Z = 6.8V$; $I_{Z,\min} = 5mA$; $I_{Z,\max} = 50mA$



SOL: From KVL:

$$V_{in} = I \times 2.2k + V_Z$$

$$(V_{in})_{\min} = I_{\min} \times 2.2k + 6.8$$

$$= 11.8mA \times 2.2k + 6.8$$

$$\boxed{(V_{in})_{\min} = 32.76V}$$

KCL:

$$I = I_Z + I_L$$

$$I_{\max} = I_{Z,\max} + I_L$$

$$= 50mA + \frac{V_Z}{R_L}$$

$$I_{\max} = 50mA + \frac{6.8}{1k} = 50mA + 6.8mA = 56.8mA$$

$$(V_{in})_{\max} = I_{\max} \times 2.2k + 6.8$$

$$= 56.8mA \times 2.2k + 6.8$$

$$\boxed{(V_{in})_{\max} = 131.76V}$$

$$; I_{\max} = I_{Z,\max} + I_L$$

$$= 50mA + 6.8mA$$

$$I_{\max} = 56.8mA$$

\therefore Range of input voltage is 32.76V to 131.76V for which output will be constant.

Special purpose Electronic Devices

① TUNNEL DIODE :

A normal P-n junction diode has an impurity concentration of about 1 part in 10^8 . This much amount of doping has the depletion layer width of about 5 Microns (5×10^{-4} cm). The diodes in which the concentration of impurity atoms is greatly increased up to 1 part in 10^3 , to get completely changed characteristics, are called as "TUNNEL DIODES". These diodes are first introduced by Leo Esaki in 1958.

The Tunneling phenomenon :

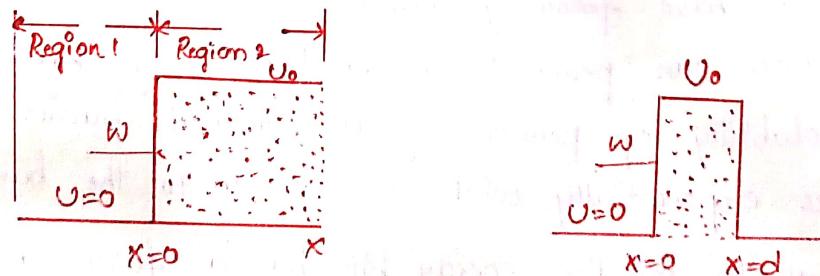
The width of the junction barrier varies inversely as the square root of the impurity concentration, and the width is reduced from 5 microns to less than 10^{-6} cm in Tunnel Diodes.

$$W \propto [\text{Impurity Concentration}]^{-1/2}$$

A particle must have an energy at least equal to the height of the potential energy barrier, if it is to move from one side of the barrier to the other. However, for barriers as thin as those in diodes introduced by Esaki, the Schrodinger equation indicates that there is a large probability that an electron will penetrate through the barrier. This quantum-mechanical behaviour is referred to as "Tunneling", and hence these high impurity-density P-n junction devices are called "TUNNEL DIODES".

Tunneling Effect :

Consider an electron of total energy w (Joules) moves in regions, where the potential energy may be taken as zero, $U=0$. At $x=0$, there is a potential-energy barrier of height $U_0 > w$ as shown in figure and potential energy remains constant in region 2 for $x > 0$.



Potential Energy Barrier of height U_0 :

Now we apply the Schrodinger equation for region 1 and region 2 to find the probability that an electron will penetrate through the barrier.

Region 1:

Schrodinger Equation is given by as

$$\frac{d^2\psi}{dx^2} + \frac{8\pi^2m}{h^2} (w) \psi = 0$$

Solution is $\psi = c e^{\pm j \left(\frac{8\pi^2 m w}{h^2} \right)^{1/2} x}$
where 'c' is constant.

The ' ψ ' and its complex conjugate ' ψ^* ' product gives the probability of finding an electron between x and $x+dx$.

$$\text{Since } \psi \cdot \psi^* = |\psi|^2 = \text{Constant},$$

The electron has an equal probability of being found anywhere in region 1. In other words, the electron is free to move in a region of zero potential energy.

Region 2:

In region 2, $x > 0$ the schrodinger equation is given as

$$\frac{d^2\psi}{dx^2} - \frac{8\pi^2m}{h^2} (v_0 - w) \psi = 0$$

Since $v_0 > w$ The solution is $\psi = A \cdot e^{-\left[\left(\frac{8\pi^2m}{h^2} \right) (v_0 - w) \right]^{1/2} x}$

$$\psi = A \cdot e^{-x/2 do} \text{ where } A \text{ is constant}$$

$$\text{and } do = \frac{1}{2} \left[\frac{h^2}{8\pi^2m(v_0 - w)} \right]^{1/2} = \frac{h}{4\pi} \left[\frac{1}{am(v_0 - w)} \right]^{1/2}$$

The Solution is actually of the form $\psi = A \cdot e^{-x/2 do} + B e^{x/2 do}$
However, $B=0$, since it is required that ' ψ ' be finite everywhere in region 2.

The probability of finding the electron between x and $x+dx$ in region 2 is $\psi \cdot \psi^* = A^2 e^{-x/do}$

From this we have following points:

- i) An electron can penetrate a potential-energy barrier.
- ii) The probability of penetrating a potential barrier by electron decreases exponentially with distance in to the barrier region.

Consider that the potential energy hill has a finite thickness 'd' as shown in fig (b). Then $x=d$ then

$$\psi \cdot \psi^* = A^2 \cdot e^{-d/do}.$$

Now, if

i) $d \gg d_0$: The probability that the electron will tunnel through the barrier is virtually zero.

ii) $d \rightarrow d_0$ ('d' approaches ' d_0 ') : $A^2 \cdot e^{-d/d_0}$ becomes large enough to represent an appreciable number of electrons which have tunneled through the barrier.

Energy Band structure of TUNNEL DIODE :

For lightly doped p-n diode, the Fermi level ' E_F ' lies inside the forbidden energy gap as given by equations below for n & p regions

$$P = N_V e^{-(E_F - E_V)/kT}$$

$$n = N_C e^{-(E_C - E_F)/kT}$$

$$N_A = N_V \cdot e^{-(E_F - E_V)/kT}$$

$$N_D = N_C e^{-(E_C - E_F)/kT}$$

$$E_F = E_V + kT \ln \frac{N_V}{N_A}$$

$$E_C = E_F + kT \ln \frac{N_C}{N_D}$$

For lightly doped diode :

$$N_A < N_V$$

$$N_D < N_C$$

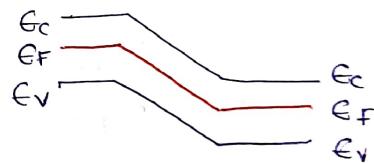
$$\ln \frac{N_V}{N_A} \text{ is positive}$$

$$\ln \frac{N_C}{N_D} \text{ is positive}$$

$$\therefore [E_F > E_V]$$

$$\therefore [E_C > E_F]$$

\therefore Fermi level lies inside the forbidden energy band.



For heavily doped diode :

$$N_A > N_V$$

$$N_D > N_C$$

$$\ln \frac{N_V}{N_A} \text{ is negative}$$

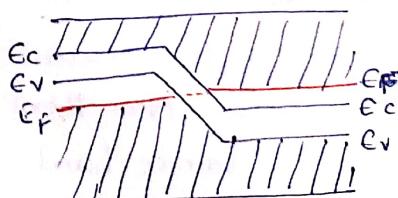
$$\ln \frac{N_C}{N_D} \text{ is negative}$$

$$[E_F < E_V]$$

$$[E_C < E_F]$$

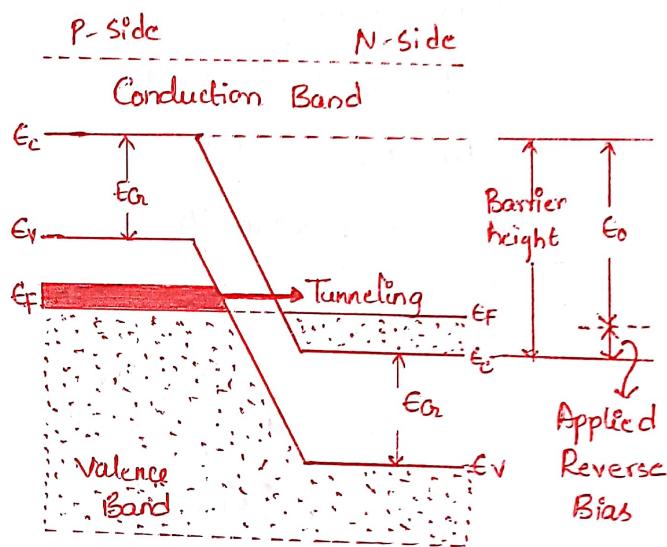
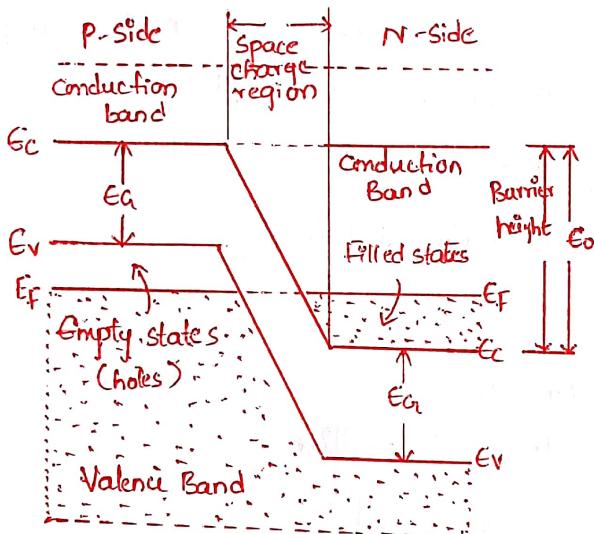
\therefore Fermi Level lies outside the forbidden energy band for heavily doped diode.

Since for p-type Fermi level lies in Valence band and for N-type Fermi level lies in Conduction Band.



Hence, under open-circuit conditions, the band structure of a heavily doped p-n junction is shown in figure (a) below.

The Fermi level ' E_F ' in the 'p' side is at the same energy as the Fermi level E_F in the 'n' side. As seen in the figure there are no filled states on one side of the junction which are at the same energy as empty allowed states on the other side. Hence there is no flow of charge in either direction across the junction and the current is zero for an open-circuited diode.



(a) Under Open-Circuited Conditions

(b) With an applied reverse Bias

Energy Bands in a heavily doped p-n diode:

The Volt-Ampere Characteristics :-

With energy-band picture of above figure and the concept of quantum-mechanical tunneling, the tunnel diode characteristics are explained below.

Consider that the 'p' material is grounded and that a voltage applied across the diode shifts the 'n' side with respect to the 'p' side.

If a Reverse-Bias Voltage is applied the height of the barrier is increased above the open circuit value ' E_0 '. Hence the n-side levels must shift downward with respect to the p-side levels as shown in figure (b). Now there are some energy states (heavily shaded region) in the valence band of the p-side which lie at the same level as allowed empty states in the conduction band of the 'n' side. Hence these electrons will 'tunnel' from 'p' to the 'n' side giving rise to

a reverse diode current. As the magnitude of reverse bias increases, the heavily shaded area grows in size, causing the reverse current to increase as shown in section ① of characteristic figure.

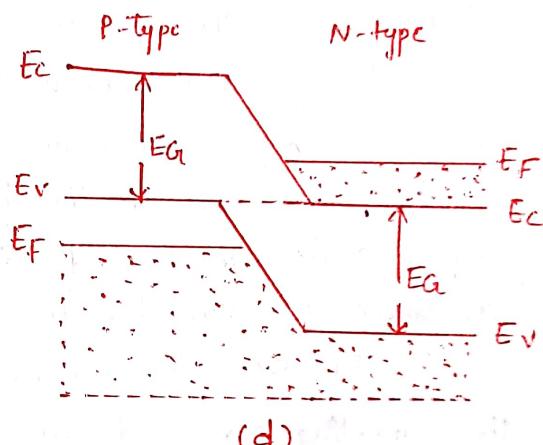
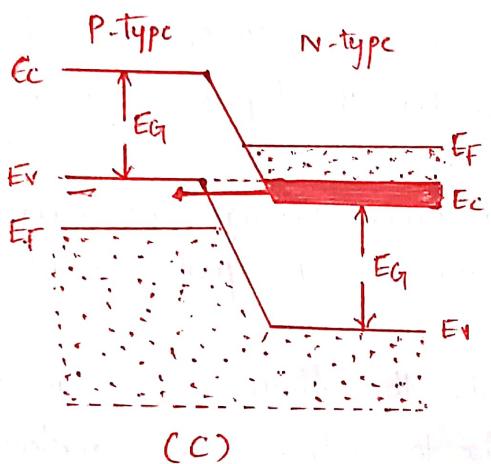
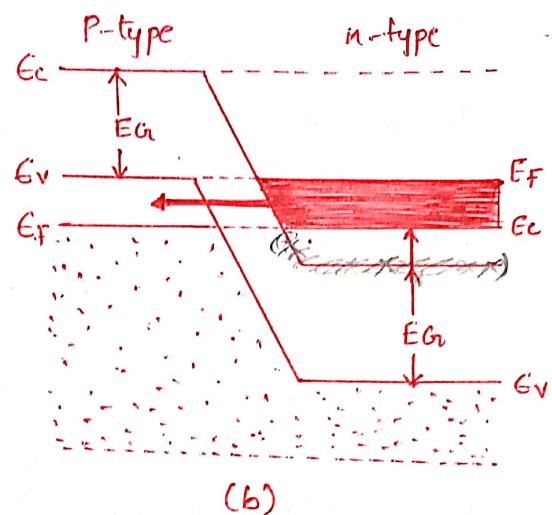
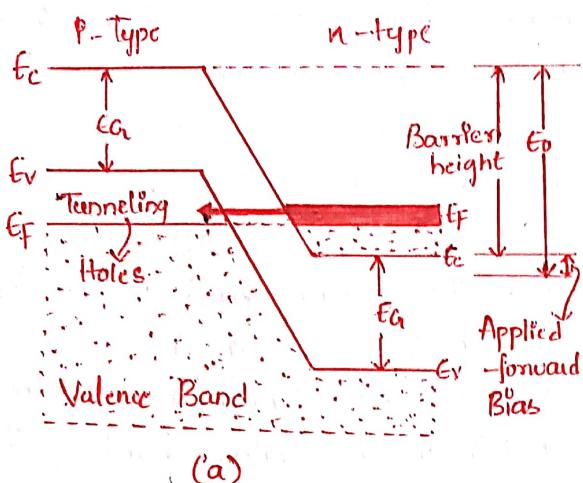
Now if a forward bias is applied to the diode the potential barriers is decreased below ' E_0 '. The n-side levels shift upward with respect to those on the p side, and the energy band picture is shown below. In the figure ② there are occupied states in the conduction band of the 'n' material (heavily shaded levels) which are at the same energy as allowed empty states (holes) in the valence band of the p side. Hence electrons will tunnel from the 'n' to the 'p' material, giving rise to the forward current of section ② in characteristic figure.

As forward bias is increased further, the figure ③ shown below is obtained. The maximum number of electrons leave the occupied states on the right side of the junction, and tunnel through the barrier to empty states on the left side, giving rise to the peak current ' I_p ' as shown in characteristic fig.

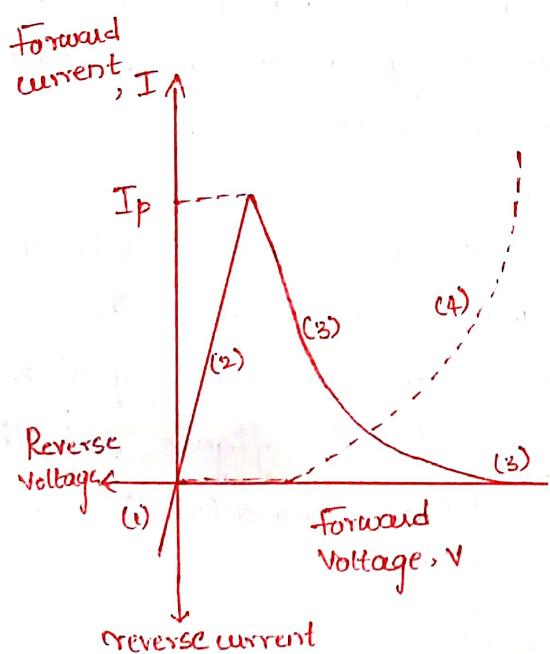
If more forward bias is applied, the figure ④ is obtained, and the tunneling current decreases, giving rise to section ④ of characteristic fig.

Finally, at an even larger forward bias, the band structure of fig ⑤ is shown is obtained, and there are no empty allowed states on one side of the junction at the same energy as occupied states on the other side, the tunneling current is dropped to zero.

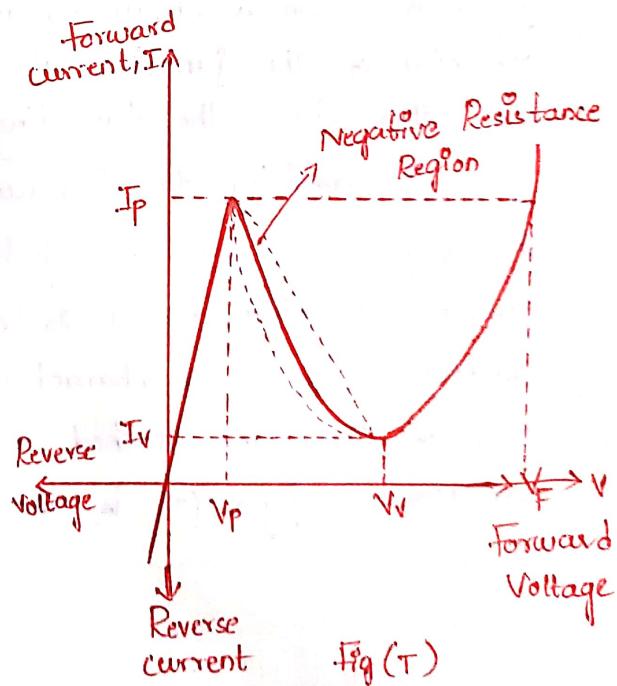
In addition to Quantum-Mechanical current described above, the regular p-n junction injection current is also being collected. This current is given by $I = I_0 (e^{\frac{q}{kT}} - 1)$ and is indicated by the dashed section ④ of characteristic figure. The curve in fig(T) is the sum of solid and dashed curves of characteristic figure and this resultant figure (T) is the "Tunnel-Diode" characteristic Curve.



The Energy Band pictures in a heavily doped p-n diode for a forward Bias



Tunneling current is solid,
Injection current is dashed curve.



Sum of solid & dashed curve gives
Tunnel diode Volt Ampere characteristic

The Tunnel diode exhibits a "Negative-resistance characteristic" between the peak current ' I_p ' and the minimum value ' I_v ', called the Valley current.

Applications :

- i) For currents whose values are between I_v and I_p , the curve is triple-valued, because each current can be obtained at three different applied voltages. This multivalued feature makes the tunnel diode useful in pulse and Digital circuitry.
- ii) Very high speed switch
- iii) High-frequency (microwave) oscillator

Most Common commercially available tunnel diodes are made from Germanium or Gallium Arsenide. It is difficult to manufacture a silicon tunnel diode with a high ratio of peak-to-valley current (I_p/I_v).

Advantages :

- i) low cost, low noise, simplicity, high speed, low power and Environmental Immunity.

Disadvantage :

Low output-Voltage swing because it is a two terminal device. Hence a tunnel diode and transistor may be combined advantageously.

Symbol of Tunnel Diode :



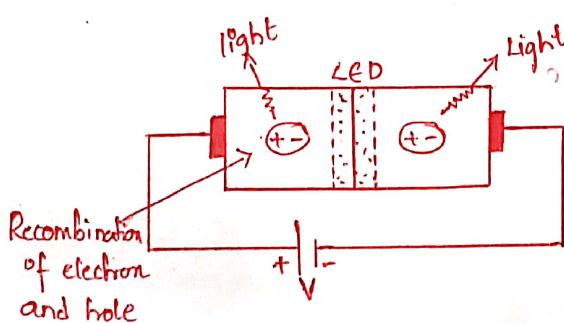
② Light Emitting Diode (LED):

The LED is an optical diode, which emits light when forward biased. The fig shows Symbol of LED which is similar to P-n junction diode apart from the two arrows indicating that the device emits the light energy.

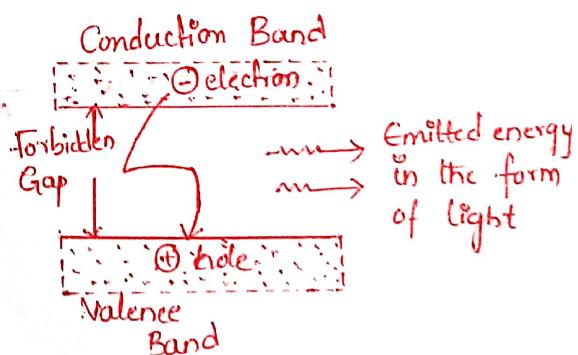
Operation:

When p-n junction is forward biased, the electrons cross the p-n junction from the n-type Semiconductor material and recombine with the holes in the p-type Semiconductor material. The free electrons in conduction band which are at higher energy level falls from conduction band to a valence band to recombine with hole. The energy corresponding to the difference between higher level and low level is released by an electron which travelling from conduction band to valence band.

In Normal diodes this energy released is in the form of heat. But LED is made up of some special material which release this energy in the form of "photons" which emit the light energy. Such diodes are called Light Emitting Diodes. This process is called "Electroluminescence". The fig. shows the basic principle of this process.



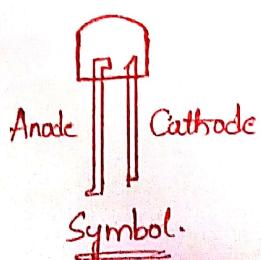
LED Forward Biased



Process of Electroluminescence

LED's use materials like :

GaAs	P	→ Red or Yellow ; Visible
GaP		→ Red or Green ; Visible
GaAs		→ Infrared ; Invisible

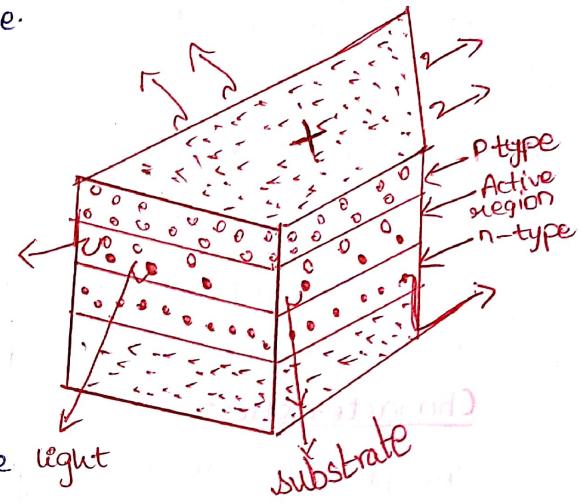


Construction of LED:-

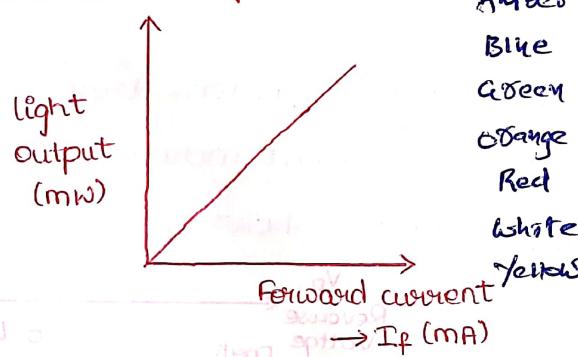
Method used for LED construction is to deposit three semiconductor layers on the substrate as shown in figure below.

In between P-type and N-type Active region is present which emits light when electron and hole recombine.

In this particular structure, the LED emit light all the way around the layered structure. Thus the basic layered structure is placed in a tiny reflective cup and the light from the active region reflects towards the desired direction. This is shown in figure light above.



Output characteristics of LED:

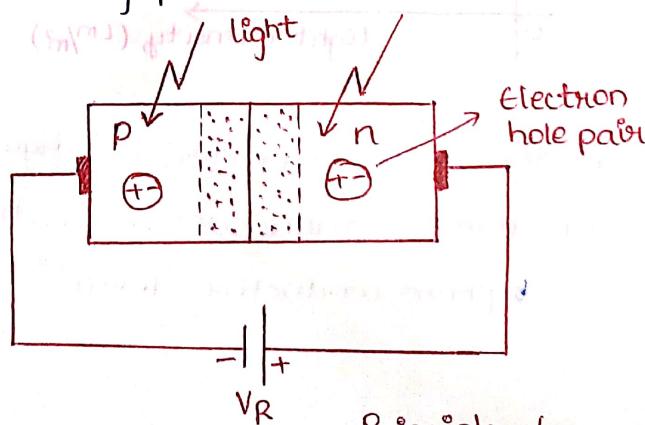
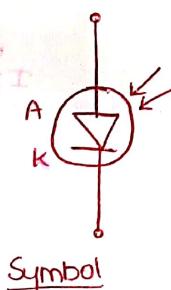


color	composition	Forward Voltage
Amber	AlInGaP	2.1
Blue	GaN	5
Green	GaP	2.2
Orange	GaAsP	2
Red	GaAsP	1.8
White	GaN	4.1
Yellow	AlInGaP	2.1

③

PHOTO DIODE:

A photo Diode is a semiconductor P-n junction device whose region of operation is limited to the reverse biased region. The figure shows symbol of photo diode and working principle.



Principle of operation

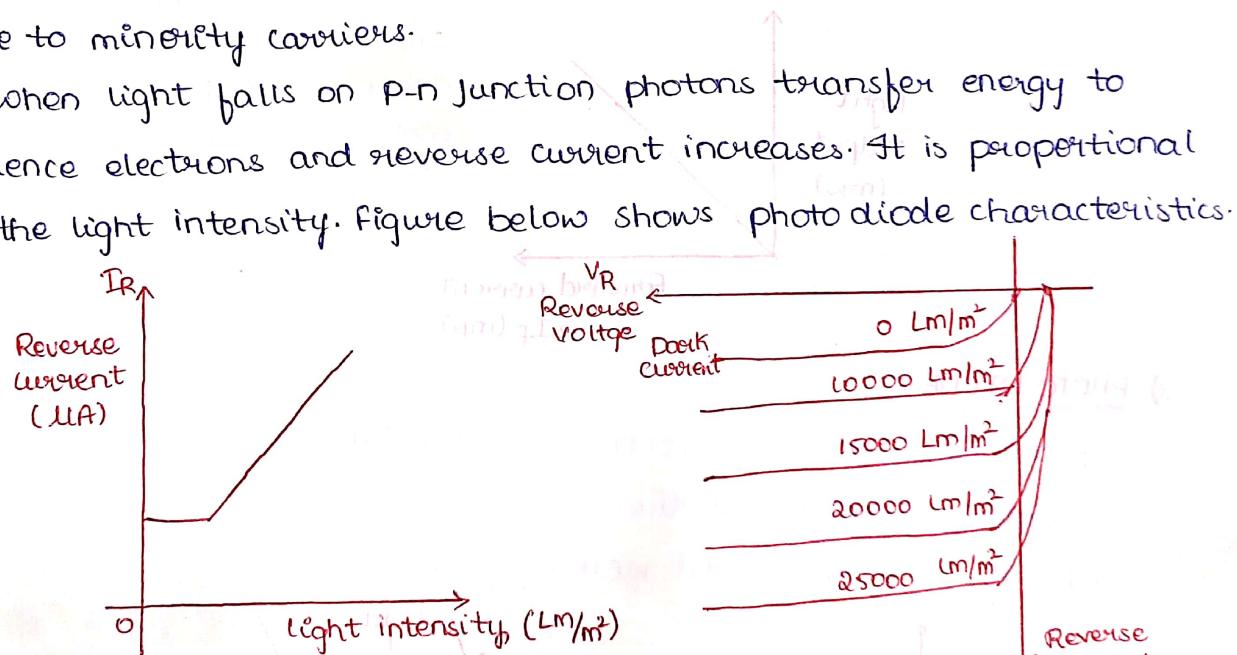
The photodiode is connected in reverse biased condition. The depletion region width is large. Under normal condition, it carries small reverse current due to minority charge carriers.

When light is incident through glass windows on the P-n junction photons in the light bombard the P-n junction and some energy is imparted to the valence electrons. Due to this, valence electrons are dislodged from the covalent bonds and become free electrons. Thus more electron-hole pairs are generated and total number of minority charge carriers increase and hence reverse current increases. This is basis principle of operation of photo diode.

Characteristics:

The photo diode is designed such that it is sensitive to the light. When there is no light, the reverse biased photo diode carries a current which is very small and called "Dark current". It is purely due to minority carriers.

When light falls on P-n junction photons transfer energy to valence electrons and reverse current increases. It is proportional to the light intensity. Figure below shows photo diode characteristics.



From the above characteristics figure the photodiode can be used as a "variable resistance device" controlled by light intensity. It is also called "photo conductive device".

Advantages:-

- (i) can be used as variable resistance device
- (ii) highly sensitive to light.
- (iii) speed is very high

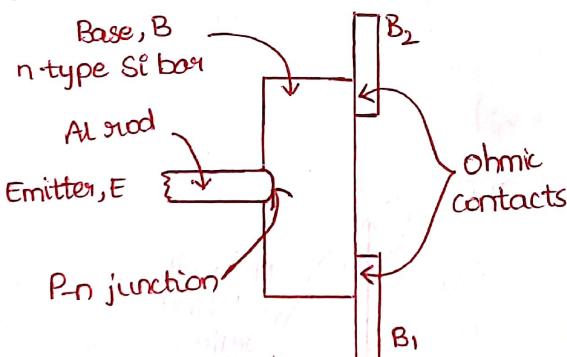
Applications:

- (i) Burglar Alarm System
- (ii) counting System

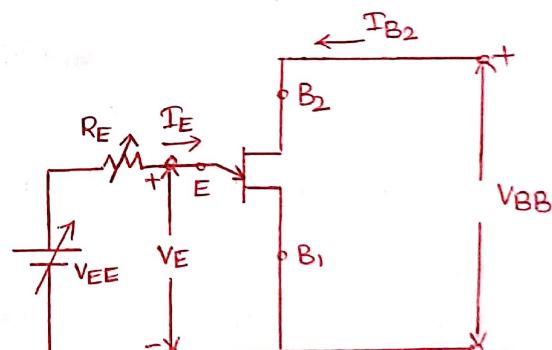
④ UJT (Uni Junction Transistor):-

The device whose construction is similar to that of FET is Uni junction Transistor. A bar of high-resistivity n-type silicon called Base 'B', has attached to it at opposite ends two ohmic contacts, B_1 and B_2 .

A Aluminium wire, called emitter 'E', is alloyed to the base to form a P-n rectifying junction. This device was originally described in the literature as "Double-base Diode", but is now commercially available under the name "Uni Junction Transistor" (UJT).



UJT constructional Details



UJT circuit symbol

Note that emitter arrow is inclined and point towards B_1 whereas the ohmic contacts B_1 and B_2 are brought out at right angles to the line which represents the 'Base'. This arrow indicates the direction of flow of conventional current. When the UJT is forward biased.

Internal resistances of two bases are R_{B_1} and R_{B_2} . Emitter 'E' is closer to B_2 . Hence R_{B_1} is more than the resistance R_{B_2} .

when $I_E = 0$ then resistance between two bases is called "Interbase Resistance", R_{BB} ". ie

$$R_{BB} = R_{B1} + R_{B2}$$

Voltage drop across R_{B1} is

$$V_{RB1} = \frac{R_{B1} \times V_{BB}}{R_{B1} + R_{B2}} = \eta V_{BB} \text{ when } I_E = 0$$

η is called "Intrinsic stand off ratio" = $\frac{R_{B1}}{R_{B1} + R_{B2}}$

$$\therefore \eta = \frac{R_{B1}}{R_{BB}}$$

Operation:

The potential of 'A' is equal to $V_A = \eta V_{BB}$

Case i): If $V_E < V_A$

As long as $V_E < V_A$, P-n junction is reverse biased Hence emitter current I_E will not flow. Thus UJT is said to be "OFF"

Case ii): If $V_E > V_A + V_f$

$$\text{ie } V_E > V_p \quad (V_A + V_f = V_p)$$

$$(V_p = \eta V_{BB} + V_f)$$

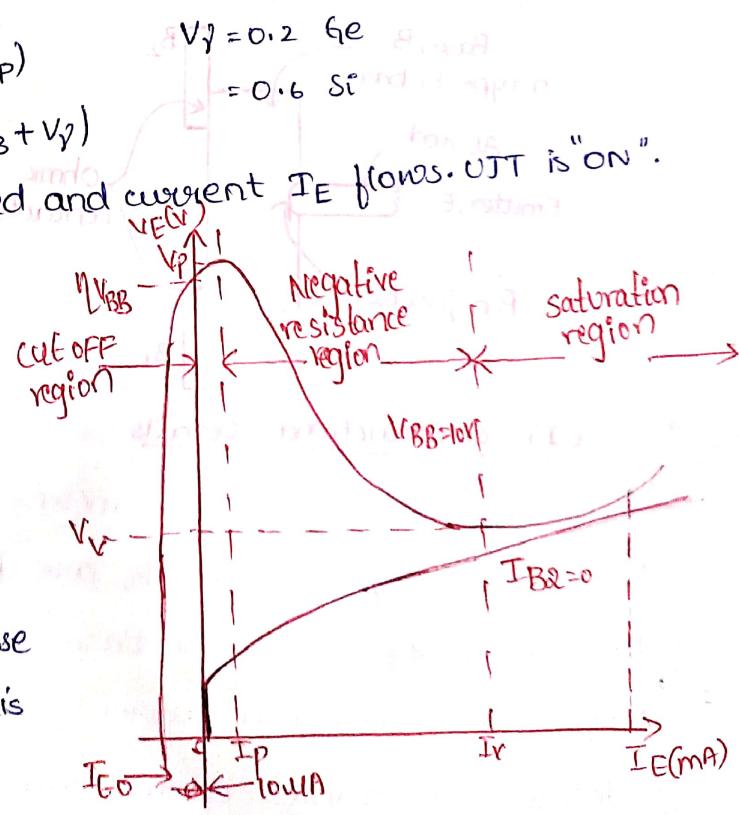
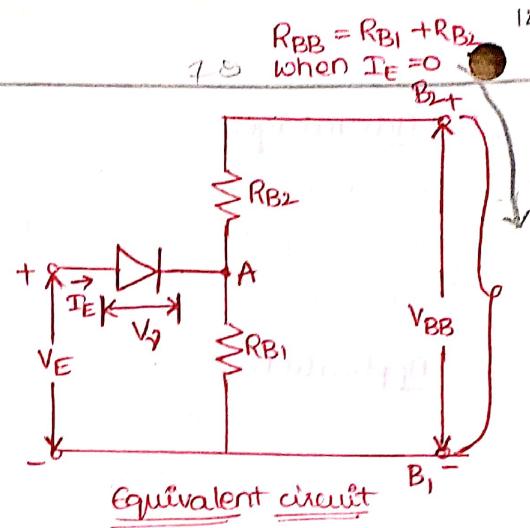
P-n junction is forward biased and current I_E flows. UJT is "ON".

Case iii):

If B_2 is open circuited so that $I_{B2} = 0$, then the relationship V-I is same as p-n junction diode as shown in the figure.

Case iv):

If $V_E < \eta V_{BB}$ P-n junction is reverse biased and I_E is negative and this negative current is I_{EO} which is of the order of 10 mA.



Input characteristics of UJT:

LIQUID CRYSTAL DISPLAY (LCD)

A liquid crystal display or LCD draws its definition from its name itself. It is combination of two states of matter, the solid and the liquid. LCD uses a liquid crystal to produce a visible image. Liquid crystal display screen works on the principle of blocking light rather than emitting light. LCD's requires backlight as they do not emit light by them.

Construction of LCD:

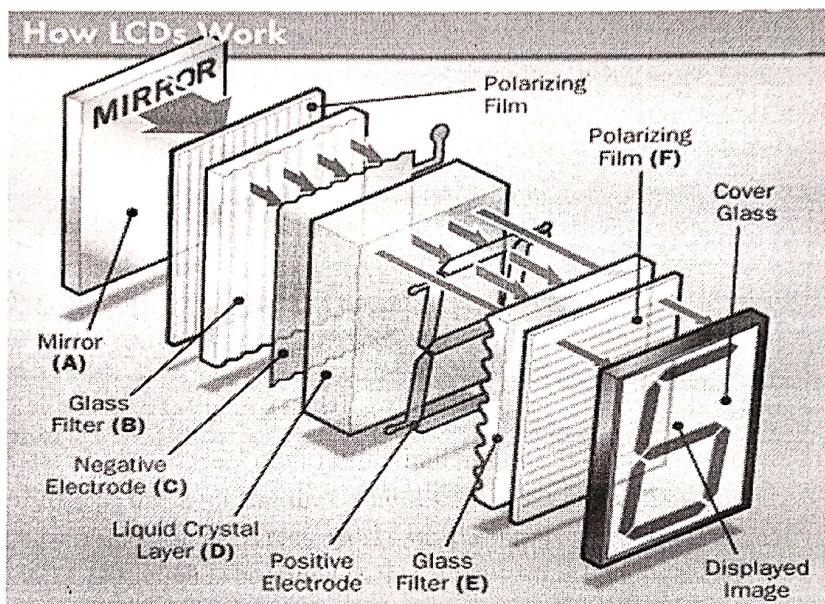


Fig.3.13: LCD Layered Diagram

The basic structure of LCD shown in figure 3.13 should be controlled by changing the applied current. Polarized light is used in LCD. As mentioned above two polarized glass pieces are used in the making of the liquid crystal. The glass which does not have a polarized film on the surface of it must be rubbed with a special polymer which will create microscopic grooves on the surface of the polarized glass filter. The grooves must be in the same direction of the polarized film. Now, a coating of pneumatic liquid phase crystal is added on one of the polarized filter of the polarized glass. The microscopic channel cause the first layer molecule to align with filter orientation. When the right angle appears at the first layer piece, then a second piece of glass is added with the polarized film. The first filter will be naturally polarized as the light strikes it at the starting stage.

Thus the light travels through each layer and guided on the next with the help of molecule. The molecule tends to change its plane of vibration of the light in order to match their angle. When the light reaches to the far end of the liquid crystal substance, it vibrates at the same angle as that of the final layer of the molecule vibrates. The light is allowed to enter into the device only if the second layer of the polarized glass matches with the final layer of the molecule.

Working Principle of LCD:

The principle behind the LCD's is that when an electrical current is applied to the liquid crystal molecule, the molecule tends to untwist. This causes the angle of light which is passing through the molecule of the polarized glass and also cause a change in the angle of the top polarizing filter. As a result a little light is allowed to pass the polarized glass through a particular area of the LCD. Thus that particular area will become dark compared to other.

The LCD works on the principle of blocking light. While constructing the LCD's, a reflected mirror is arranged at the back. An electrode plane is made of indium-tin oxide which is kept on top and a polarized glass with a polarizing film is also added on the bottom of the device. The complete region of the LCD has to be enclosed by a common electrode and above it should be the liquid crystal matter.

Next comes to the second piece of glass with an electrode in the form of the rectangle on the bottom and, on top, another polarizing film. It must be considered that both the pieces are kept at right angles. When there is no current, the light passes through the front of the LCD it will be reflected by the mirror and bounced back. As the electrode is connected to a battery the current from it will cause the liquid crystals between the common-plane electrode and the electrode shaped like a rectangle to untwist. Thus the light is blocked from passing through. That particular rectangular area appears blank.

Applications of LCD:

1. Liquid crystal technology has major applications in the field of science and engineering as well on electronic devices.
2. Liquid crystal thermometer
3. The liquid crystal display technique is also applicable in visualization of the radio frequency waves in the waveguide.
4. Used in the medical applications.

Advantages of LCD:

1. LCD's consumes less amount of power compared to CRT and LED
2. LCD's are consist of some microwatts for display in comparison to some milli watts for LED's
3. LCDs are of low cost
4. Provides excellent contrast
5. LCD's are thinner and lighter when compared to cathode ray tube and LED

Disadvantages of LCD:

1. Require additional light sources
2. Range of temperature is limited for operation
3. Low reliability
4. Speed is very low

SILICON CONTROLLED RECTIFIER (SCR)

SCR is a three terminal four layer three junction semiconductor device. Three terminals are Anode (A), cathode (K) and Gate (G) which is connected to inner p-type layer and the function of Gate is to control the firing of SCR. Three junctions J₁, J₂ and J₃ with junctions J₁ and J₃ operate in forward direction while middle junction J₂ operates in the reverse direction. In normal operating conditions Anode is positive with respect to cathode. Silicon was chosen because of its high temperature and power capabilities.

SCR is cut into two transistors; the base of PNP is joined to the collector of NPN transistor while collector of PNP is joined to the base of NPN transistor. The gate is brought out from the Base of NPN material.

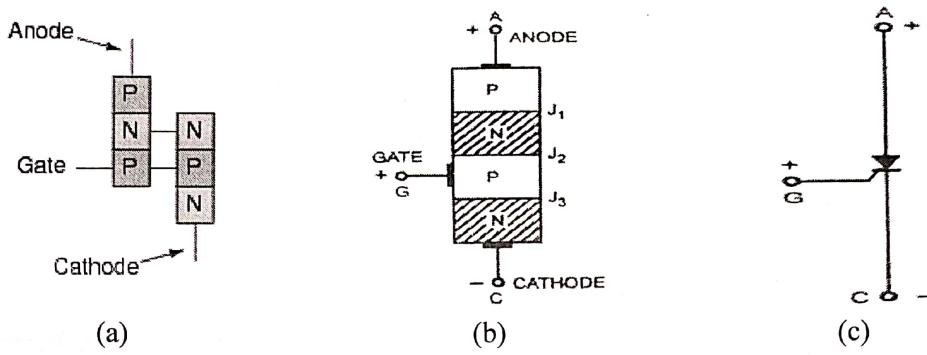


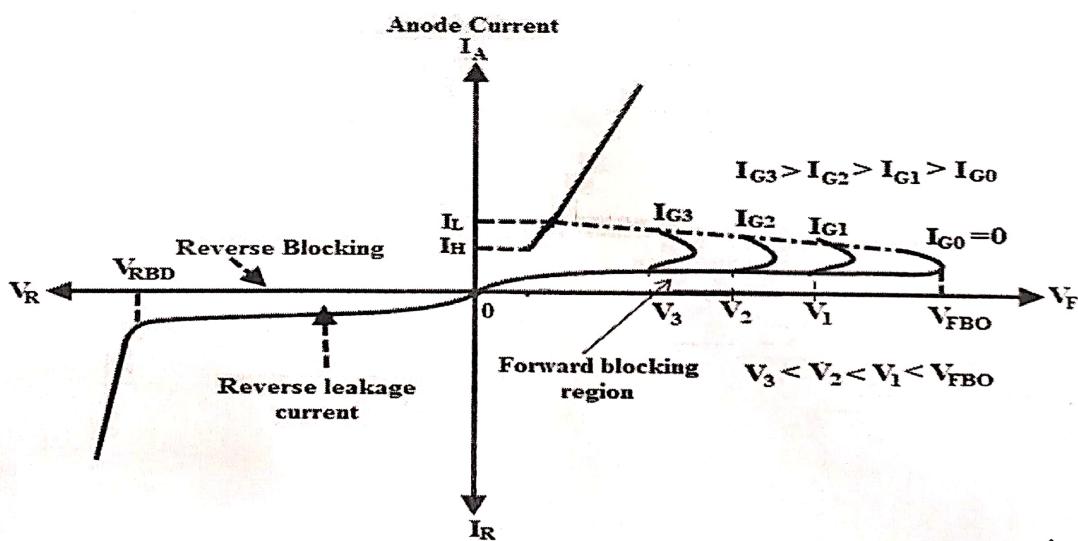
Fig.3.16:SCR a) split transistors b) Basic structure c) schematic symbol

V-I characteristics

- When the anode is positive with respect to cathode i.e., when SCR is in forward mode the SCR does not conduct unless the forward voltage exceeds certain value called the Forward Break Over Voltage (V_{FBO}).
- If a positive Gate current is supplied the SCR becomes conducting at a voltage much lesser than forward break over voltage. The larger the gate current, lower the break over voltage. Once SCR is switched on, the forward voltage drop across it is suddenly reduced to very small value.
- A minimum forward current that is contained to keep SCR in conducting state is called 'Hold Current (I_H)'. If current through SCR is reduced below I_H the SCR turns 'OFF'.
- When SCR is turned ON from OFF state the resulting forward current is called 'Latch current (I_L)'. I_L is slightly higher than I_H .
- If Anode is negative w.r.t cathode the device enters into the reverse blocking region. The negligible current flows. As the voltage is increased at a particular value Avalanche breakdown occurs and large current flows through the device. This is called Reverse breakdown and the voltage at which it happens is called 'Reverse break down voltage, V_{RBD} '. The V-I characteristics of SCR are shown in figure 3.17.

Applications of SCR

- It is used as a Switch and in AC voltage stabilizers
- It is used as a Inverter and Chopper



V-I characteristics of SCR

VARACTOR DIODE

A diode which has a capacitance that varies as a function of the voltage applied across its terminals is called a varactor diode (or) varicap diode (or) variable capacitance diode (or) variable reactance diode (or) tuning diode.

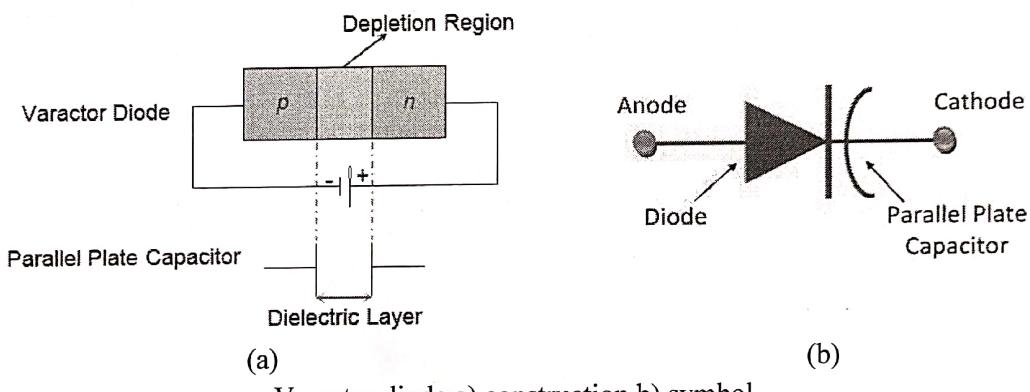
Varactors are operated in reverse-bias so no current flows, but the thickness of depletion region varies with the applied bias voltage, where the capacitance of the diode can be varied. The depletion region thickness is proportional to the square root of the applied voltage generally,

$$W \propto \sqrt{V_a} \quad (3.5)$$

Capacitance is inversely proportional to depletion region thickness

$$C \propto \frac{1}{W} \quad (3.6)$$

$$C \propto \frac{1}{\sqrt{V_a}} \quad (3.7)$$



Varactor diode a) construction b) symbol

Applications

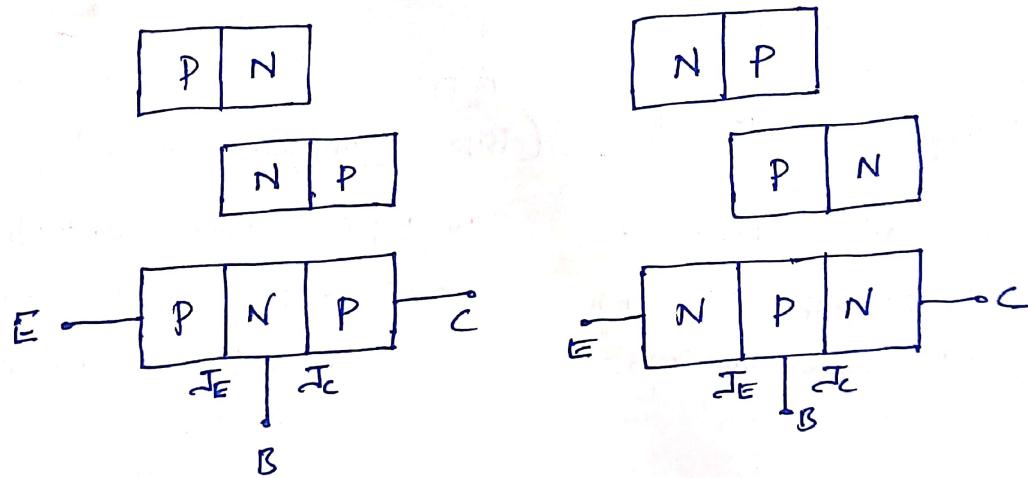
1. Voltage-controlled capacitors
2. Voltage-controlled oscillators
3. Tuners of television sets to electronically tune the receiver to different stations
4. Parametric Amplifiers

TRANSISTOR AND FET CHARACTERISTICS

- Before invention of Transistor, Vacuum tube is present which is Bulky, costly and takes more time to conduct. To overcome all these in the year 1947, Transistor was invented by William Shockley. The major advantages of Transistor are:
 - i) Amplify electronic signals such as Radio & T.V
 - ii) It has low operating Voltage
 - iii) small size & ruggedness
 - iv) higher efficiency.

Transistor Construction

- One PN diode and NP diode are joined back to back which forms a PNP and NPN transistors.



- Transistor is a three terminal device which has Emitter, Base and collector. It has low resistance (maximum current) at input and high resistance (less current) at output of transistor. So Transistor came from the word

'TRANSFER RESISTOR' → TRANSISTOR.

- Transistor:

	<u>Emitter</u>	<u>Base</u>	<u>Collector</u>
Size :	medium	small	large
Doping :	Heavily	lightly	Moderately

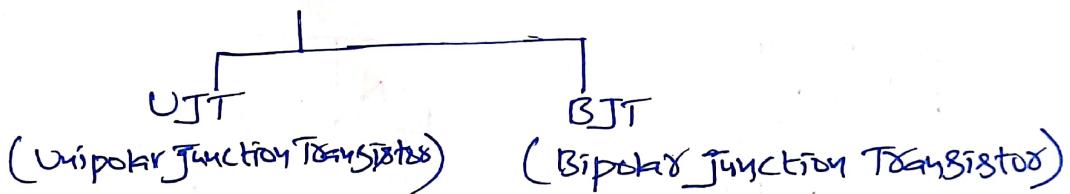
Collector size is large because collector region has to handle more power than the Emitter and therefore more surface area is required for heat dissipation.

- There are two junctions in a transistor I_E & I_C .

I_E - It is between Emitter & Base and it is called Emitter-Base junction or Emitter junction.

I_C - It is between Base & Collector and it is called Collector-Base junction or Collector junction.

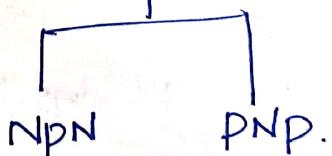
- There are two types of transistors



In UJT current conduction is only due to one type of carriers i.e., majority charge carriers.

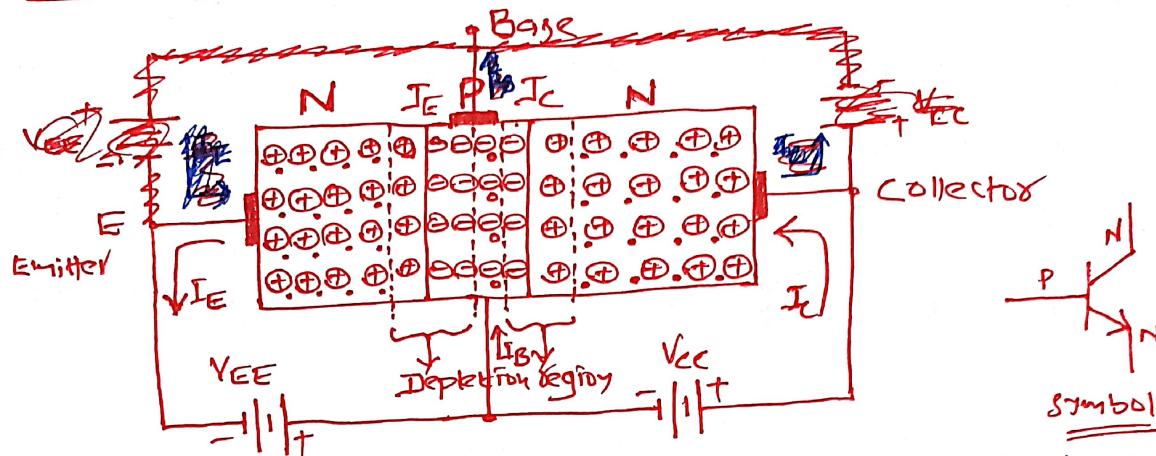
In BJT current conduction is due to both types of charge carriers i.e., majority & minority charge carriers.

Types of BJT's



BJT Operation:

i) operation of NPN Transistor:



— During Diffusion, depletion region penetrates more deeply into the lightly doped side i.e; Base in order to include an equal number of impurity atoms in the each side of the junction.

— For a biased transistor, it is necessary to correctly bias the two P-N junctions with external voltages. Depending upon external bias voltage polarities used, the transistor works in one of the three regions-

<u>Region</u>	<u>Emitter-Base Junction (JE)</u>	<u>Collector-Base junction (Jc)</u>
i) Active	Forward biased	Reverse biased
ii) Saturation	Forward biased	Forward biased
iii) Cut-off	Reverse biased	Reverse biased
iv) Reverse Active	Reverse biased	Forward biased

— With D.C source V_{EE} forward biased the depletion region ΔL_{JE} is reduced and with V_{CC} reverse biased ΔL_{JC} , depletion region is increased. The forward biased E-B junction causes electrons in N-type to flow towards base constituting emitter current, I_E .

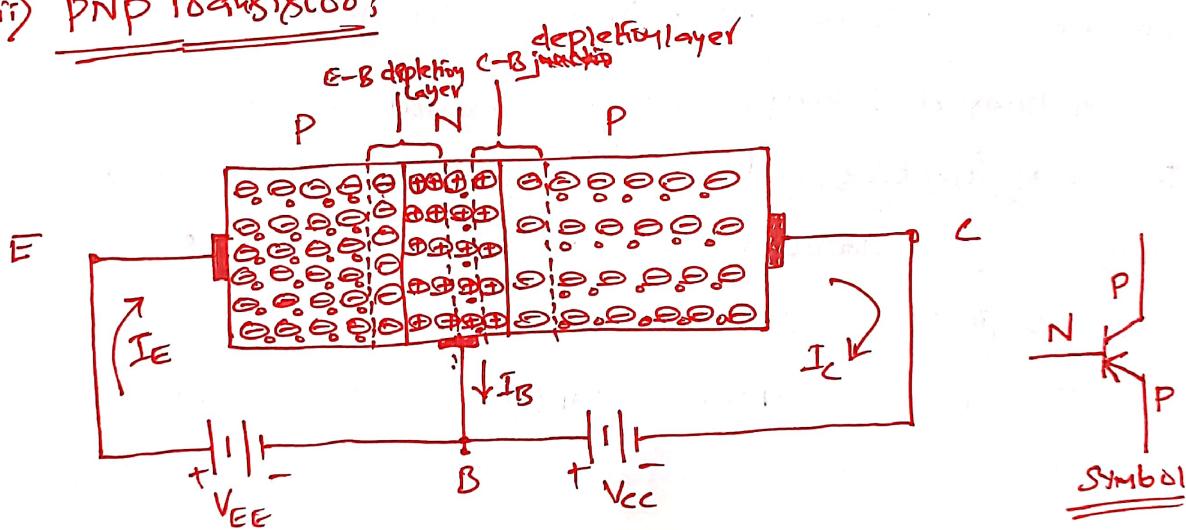
As e-B junction is reverse biased no current flows through the junction. The Emitter current I_E diffuse through JE junction and enters into base where some electrons gets recombined in base and before all electrons get recombined the electrons cross the IC junction and enters into collector because of base small size.

∴ A small current is focus in base and a large current in collector.

∴ For NPN Transistor

$$I_E = I_B + I_C$$

i) PNP Transistor's



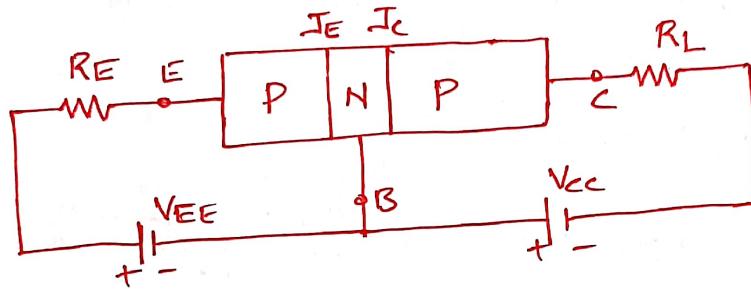
- As Base-Emitter junction is forward biased the majority carriers emitted by P-type emitter flow towards base and constitutes emitter current, I_E .
- As base is N-type there is a chance of recombination of holes emitted by the emitter with the electrons in base. But as base is very thin and lightly doped only few electrons recombine with holes the remaining charge carriers cross over into the collector region to constitute the collector current.

$$\therefore I_E = I_B + I_C$$

Transistor as an Amplifier:

The main utility of a transistor is it amplifies the weak signals.

The weak signal is applied at input terminals and the amplified output is obtained across the output terminals.



The input circuit is forward biased and has low resistance. A small change in input voltage causes ΔV_i causes a large change in Emitter current ΔI_E . This causes the same change in collector current and ΔI_C flows through a high load resistance R_L and a large voltage is developed across R_L .

$$\text{Voltage Amplification } A = \frac{\Delta V_{out}}{\Delta V_{in}}$$

$$= \frac{R_L \cdot \Delta I_C}{R_E \cdot \Delta I_E}$$

$$= \frac{R_L \cdot \alpha \cdot \Delta I_E}{R_E \cdot \Delta I_E}$$

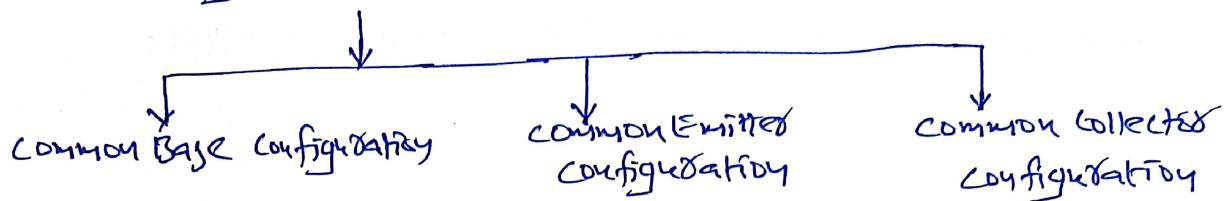
$$\Rightarrow A = \frac{\alpha \cdot R_L}{R_E}$$

where α is a fraction of current change which is collected.

$\therefore A > 1$ and transistor acts as an amplifier.

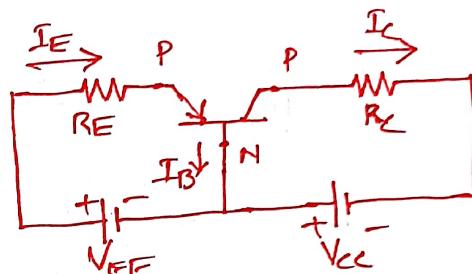
Transistor Configurations:

The Transistor can be connected in a circuit in the following three configurations.



i) Common Base Configuration:

The circuit shows common base configuration as Base is common to Emitter and collector terminals.



$$\text{From the figure: } I_C = \alpha I_E + I_{CBO}$$

$$\text{since } I_E = I_B + I_C.$$

$$I_C = \alpha (I_B + I_C) + I_{CBO}$$

$$I_C = \alpha I_B + \alpha I_C + I_{CBO}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CBO}$$

$$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \left(\frac{\alpha}{1-\alpha} \right) I_B + \left(\frac{1}{1-\alpha} \right) I_{CBO}$$

αI_E — current due to majority carriers

I_{CBO} — current due to minority carriers

where α is called current amplification factor in CB configuration.

and
$$\alpha = \frac{I_C}{I_E}$$
 when no signal is applied.

$\therefore \alpha < 1$. It ranges from 0.95 to 0.995 typical α_{NPN} is 0.98.

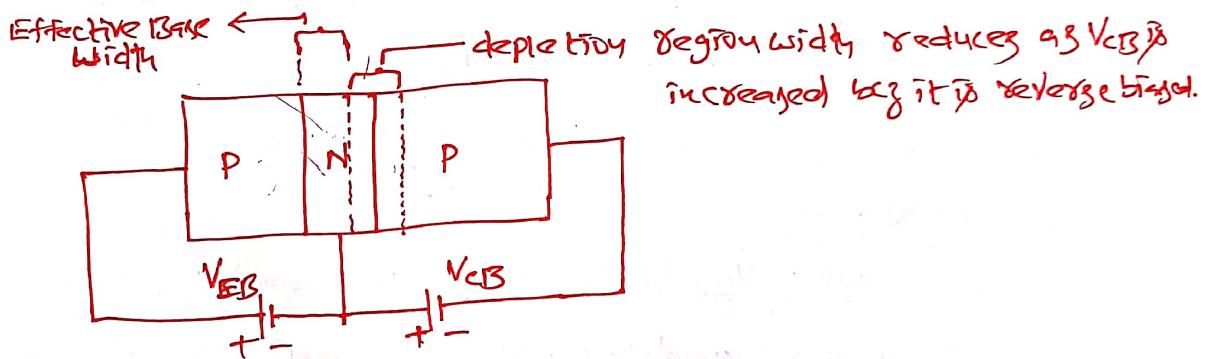
Input characteristics

It is the curve between input current (I_E) and input voltage (V_{EB}) at constant V_{CB} .

The I_E is taken on Y-axis and V_{EB} on X-axis.

From the characteristics we have:

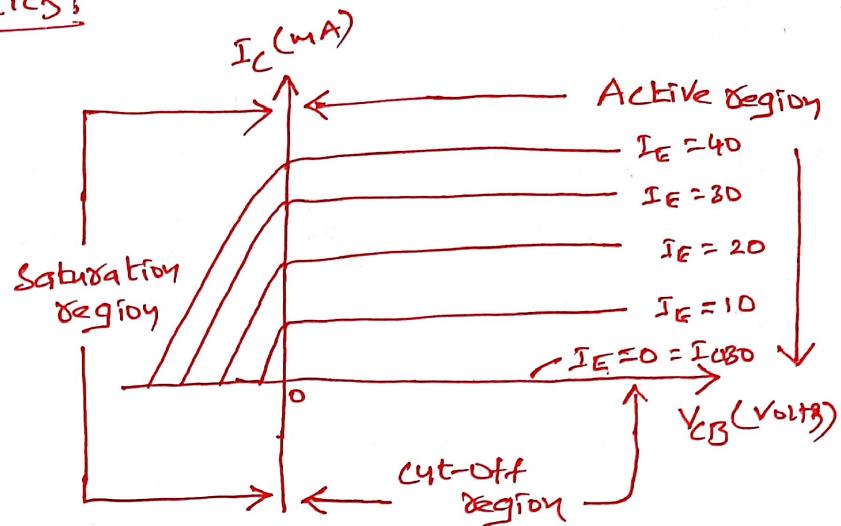
- After cut-in Voltage $V_V = 0.2V$ for Ge & $V_V = 0.6V$ for Si, the current I_E increases as V_{EB} increases i.e; input resistance is small.
- With increase in V_{CB} the width of depletion region (B-C) also increases gradually because V_{CB} is reverse biased and the effective base width decreases which increases I_E current.



This reduction of effective base width is called "Early Effect" or "Base width modulation".

- This decrease in base width has two consequences:
 - i) less chance of recombination in base region
 - ii) The charge gradient is increased within the base.
- The transistor breakdown occurs when V_{CB} increases beyond certain limit because as V_{CB} increases effective base width becomes zero since depletion region spreads completely across base and reaches the emitter junction i.e where emitter and collector are shorted. This causes large increase in emitter current resulting breakdown. This breakdown is known as "punch-through" or "Reach Through".

Output characteristics:



→ It is the curve between collector current, I_c and collector base voltage V_{CB} at constant Emitter current, I_E .

Output characteristics has three basic regions.

- Active Region
- Saturation Region
- Cut-off Region.

i) Active Region:

In this region V_{EB} is forward biased and V_{CB} is reverse biased and I_c is approximately equal to I_E and transistor works as an amplifier.

ii) Saturation Region:

In this region V_{EB} and V_{CB} are forward biased and this curve is represented as left of $V_{CB} = 0$ Volts. There is an exponential increase in collector current I_c as V_{CB} increases towards 0 Volts.

iii) Cut-off Region:

In this region V_{EB} and V_{CB} are reverse biased. If $I_E = 0$ then $I_c = I_{CBO}$ a reverse leakage current shown in figure. The region below this $I_E = 0$ is known as cut-off region where collector current is nearly zero.

2) Common Emitter configuration:

In this configuration

Emitter is common to both
Base and collector and hence
the name Common Emitter
configuration.

We know that

$$I_C = \left(\frac{\alpha}{1-\alpha} \right) I_B + \left(\frac{1}{1-\alpha} \right) I_{CBO}$$

$$\boxed{I_C = \beta \cdot I_B + (1+\beta) I_{CBO}}$$

$$\therefore \beta = \frac{\alpha}{1-\alpha}; 1+\beta = \frac{1}{1-\alpha}$$

$\beta \cdot I_B$ is called forward current and

$(1+\beta) I_{CBO}$ is called "reverse leakage current" in CE configuration
and it is denoted as I_{CEO} .

$$\text{i.e., } I_{CEO} = (1+\beta) I_{CBO}$$

$$I_{CEO} \gg I_{CBO}$$

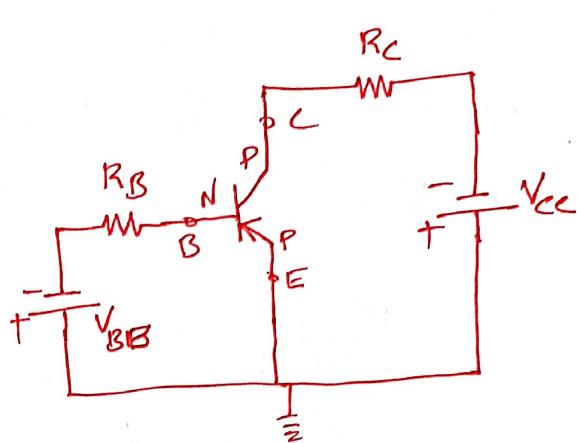
$$\& I_{CEO} \ll \beta \cdot I_B.$$

$$\therefore I_C = \beta \cdot I_B + I_{CEO} \quad [\text{neglecting } I_{CBO}]$$

$$\boxed{I_C = \beta \cdot I_B} \quad [\text{neglecting } I_{CEO} = 0]$$

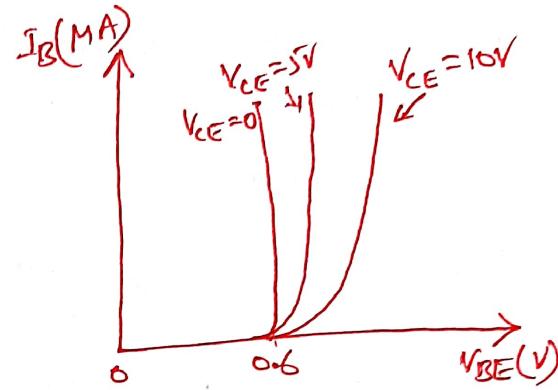
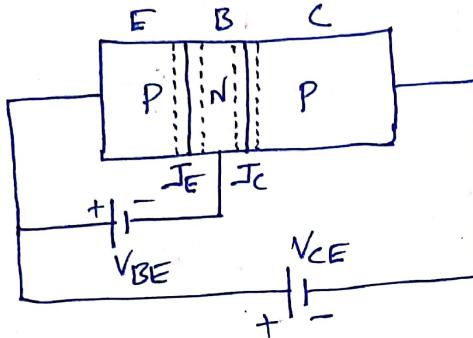
$\therefore \beta$ is called current amplification factor for CE configuration.

and $\boxed{\beta = \frac{I_C}{I_B}}$ and $\beta > 1$.



i) Input characteristics:

IE is the curve drawn between Input current I_B (Base current) and input voltage V_{BE} (Base-Emitter Voltage) keeping output voltage V_{CE} (Collector to Emitter Voltage) constant.



→ For $V_{CE}=0$ Volts and as V_{BE} is increased the transistor is forward biased and after cut-off Voltage I_B increases rapidly.

→ For $V_{CE}=5V$; since I_C is reverse biased the depletion region increases and effective base width reduces and less recombination takes place in base region reducing base current I_B shown in fig. above.

ii) Output characteristics:

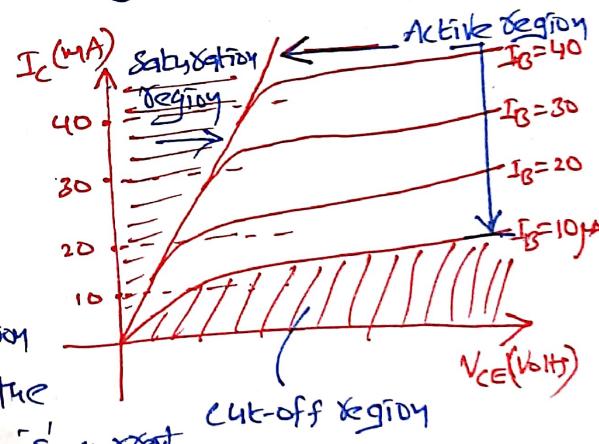
→ It is diagram between V_{CE} and I_C keeping input current I_B constant.

Active Region:

In this collector junction I_C is reverse biased. As V_{CE} increases depletion region increases and base decreases reducing the chance of recombination in the base and I_C current rises more sharply.

→ Saturation Region: when both I_C & I_E junctions are forward biased the transistor operates in saturation region shown in fig. above.

→ Cut-off Region: when $I_B=0$; there is no base and collector current is reverse leakage current I_{CE0} which is shown in figure.



3) common collector configuration:

- In this collector is common to both Base and Emitter and hence it is named common collector configuration.

- We know that

$$I_C = \alpha I_E + I_{CBO}$$

$$\& I_E = I_B + I_C$$

$$I_E = I_B + \alpha I_E + I_{CBO}$$

$$I_E - \alpha I_E = I_B + I_{CBO}$$

$$I_E(1-\alpha) = I_B + I_{CBO}$$

$$I_E = \left(\frac{1}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}$$

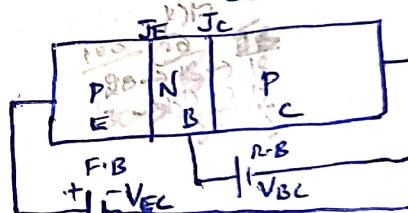
$$I_E = V I_B + V I_{CBO}$$

$$I_E = V I_B$$

$$V = \frac{I_E}{I_B}$$

neglecting leakage current I_{CBO} then

where $V = 1 + \beta$.

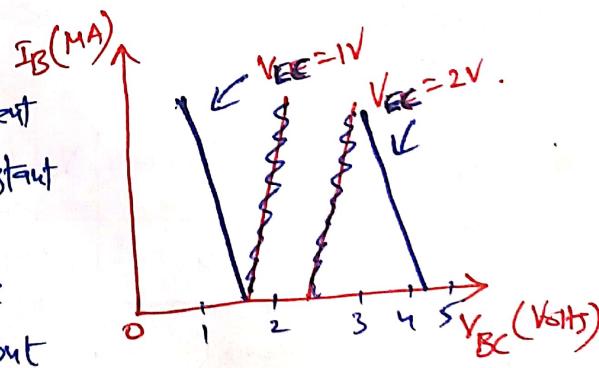


Where 'V' is called current amplification factor for CC configuration.

i) Input characteristics:

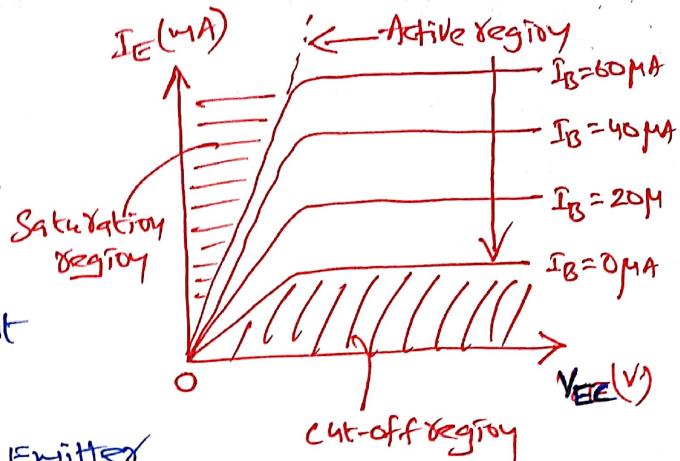
- It is the graph between input current I_B varying input voltage V_{BC} at constant V_{EE} .

- These characteristics are quite different than CB & CE due to input voltage V_{BC} which is largely determined by the level of collector to Emitter V_{EE} voltage.



Output characteristics:

The Emitter current I_E is taken along Y-axis and V_{EE} along X-axis. Since I_C is approximately equal to I_E , the common collector output characteristics are practically similar to those of the common emitter characteristics.



Comparison of CE, CB and CC Configurations:

	<u>CE</u>	<u>CB</u>	<u>CC</u>
i) Voltage gain, A_V	High	High	Low
ii) Current gain, A_I	High	Low	High
iii) Input Resistance, R_i	Medium	Low	High
iv) Output Resistance, R_o	Medium	High	Low
v) Amplification factor	$\beta = \frac{I_C}{I_B}$	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_E}{I_B}$
vi) Application	Audio Signal Amplification	Input Stage of Multi-Stage Amplifier	Impedance Matching.

Why BE config?

Transistor junction Voltage Values:

Type	V_{BE} (cutoff)	V_{BE} (cut-in)	V_{BE} (Active)	V_{BE} (saturation)
Silicon, Si	0.0	0.5	0.6	0.7
Gallium, Ge	-0.1	0.1	0.2	0.3

BJT is a "current controlled current source" because output current is controlled by input current.

Why CE configuration is widely used in Amplifier circuits?

- i) CE configuration is the only configuration which provides both voltage gain as well as current gain greater than unity.
- ii) In CE the ratio of R_o to R_i is small which makes configuration an ideal for coupling between various transistor stages. Maximum power is transferred from stage 1 to stage 2, when R_o of stage 1 is equal to R_i of stage 2.

Relation between α and β :

We know that $\beta = \frac{I_c}{I_B}$ & $\alpha = \frac{I_c}{I_E}$

$$\& I_E = I_B + I_C \Rightarrow I_B = I_E - I_C$$

$$\beta = \frac{I_c}{I_B}$$

$$\beta = \frac{I_c}{I_E - I_c} = \frac{I_c / I_E}{I_E - I_c / I_E} = \frac{\frac{I_c}{I_E}}{\frac{I_E}{I_E} - \frac{I_c}{I_E}} = \frac{\alpha}{1 - \alpha}$$

$$\boxed{\beta = \frac{\alpha}{1 - \alpha}}$$

$$\underline{\beta > 1}$$

$$\beta(1 - \alpha) = \alpha$$

$$\beta - \alpha\beta = \alpha$$

$$\beta = \alpha + \alpha\beta$$

$$\beta = \alpha(1 + \beta)$$

$$\boxed{\alpha = \frac{\beta}{1 + \beta}}$$

$$\underline{\alpha < 1}$$

Limits of operation of BJT & its Specifications:

- For each transistor there is a region of operation on the characteristics which will ensure that the maximum ratings are not being exceeded and the output signal exhibits minimum distortion.
- All of these limits of operation are defined on a typical transistor specification sheet designed by engineers.
- Some of the limits of operation are:

maximum collector current: $I_{CEO} \leq I_C \leq I_{Cmax}$

specification sheet values: $7.5mA \leq I_C \leq 200mA$

maximum collector to Emitter Voltage: $V_{CEsat} \leq V_{CE} \leq V_{CEmax}$

specification sheet values: $0.3V \leq V_{CE} \leq 30V$

maximum power dissipation: $P_{Cmax} \geq V_{CE} I_C$

specification sheet values: $650mW \geq V_{CE} I_C$

In common Base Voltage Configuration

Collector - Base Voltage V_{CB} : $V_{CB} = 25V \text{ to } 80V$.

Transistor Biasing and Stabilization

The basic function of Transistor is to do Amplification.

The process of raising the strength of a weak signal without any change in its shape is known as faithful amplification.

For faithful amplification, the following three conditions must be satisfied.

- i) The Emitter-Base junction should be forward biased
- ii) The Collector-Base junction should be Reverse biased
- iii) There should be proper zero signal collector current.
(i.e; operating point of transistor)

The proper flow of zero signal collector current (proper operating point of a transistor) and maintenance of proper collector-emitter Voltage during the passage of signal is known as "Transistor Biasing".

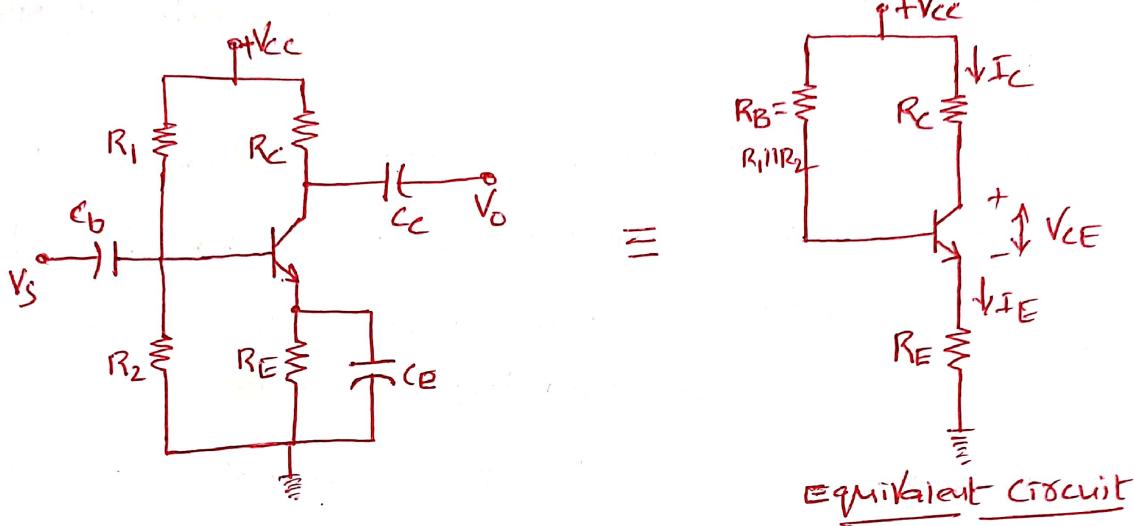
When a transistor is not biased properly, it works inefficiently and produces distortion in the output signal. Hence a transistor is to be biased properly and correctly. A transistor is biased either with the help of battery (or) an associating circuit with the transistor. The circuit with the transistor is generally employed and it is known as biasing circuit.

In order to produce distortion-free output in amplifier circuits, the Supply Voltages and Resistances in the circuit must be suitably chosen. These establish V_{CE} , I_C to operate transistor in Active Region. This point Q (V_{CE}, I_C) is called Quiescent point (or) operating point of transistor.

The process of giving proper supply voltages and resistances for obtaining the desired Q-point is called biasing.

D.C Load Line:

Consider a common Emitter configuration circuit shown below.



In the absence of a.c signal, the capacitors provide very high impedance, i.e; open circuited. \therefore Equivalent circuit for CE config

Applying KVL to the collector circuit of fig① we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CC} - V_{CE} = I_C [R_C + R_E] \quad \because I_C \approx I_E$$

$$I_C = \frac{-V_{CE}}{R_C + R_E} + \frac{V_{CC}}{R_C + R_E} \quad \text{let } R = R_C + R_E$$

$I_C = -\frac{1}{R} V_{CE} + \frac{V_{CC}}{R}$

→ ①

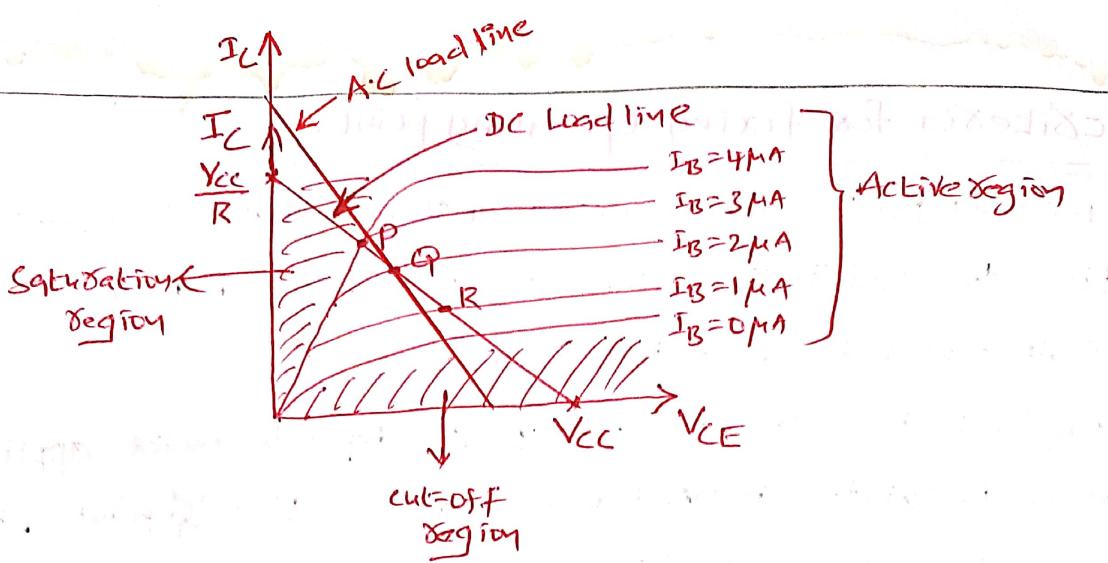
Comparing this equation with equation of straight line $y = mx + c$

$$y = mx + c$$

on Y-axis I_C is taken ; slope of line $m = -1/R$

X-axis V_{CE} is taken

$$\text{constant } c = \frac{V_{CC}}{R}$$



These are the output characteristics of CE configuration.

A straight line can be drawn on the graph of I_C vs V_{CE} with slope m and intercept 'c'. From eq(1)

i) At $I_C = 0$; $V_{CE} = V_{CC}$ on X-axis.

ii) At $V_{CE} = 0$; $I_C = \frac{V_{CC}}{R}$ on Y-axis.

The line drawn between these points is called "dc load line".

This line intersects the output characteristic curves at a point called the "operating point". This point is fixed point and it is called "Quiescent point (or) Q-point". Quiescent means quiet, still, inactive.

A.C Load line:

If load resistance R_L is considered (i.e; $R_L \neq \infty$) then $R'_L = R_L // R_C$

must be drawn through the operating point 'Q'. This a.c load line is indicated in the above figure, where we observe that the input signal may swing a maximum of approximately 2mA around 'Q'.

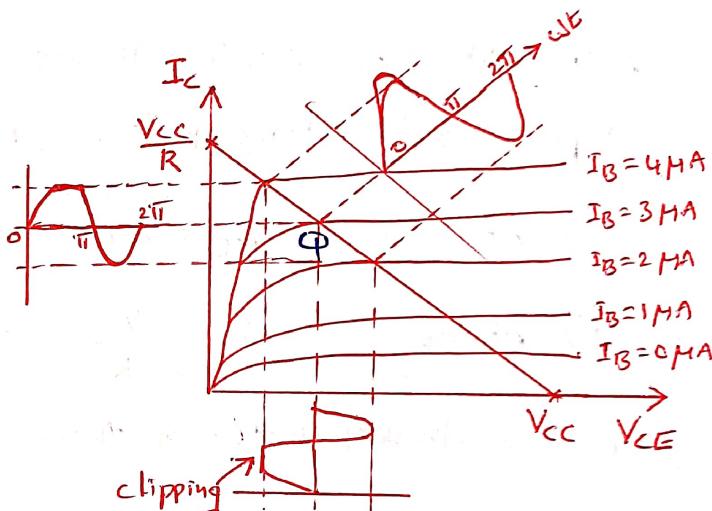
Criteria for fixing Operating point:

Operating point can be selected at three different positions on the d.c load line: i) near saturation region ii) Near cut-off region iii) At center i.e; in active region.

The selection of operating point depends on its application. When transistor is used as an amplifier, the 'Q' point should be at center of d.c load line to prevent any possible distortion in amplified output signal.

Case(i):

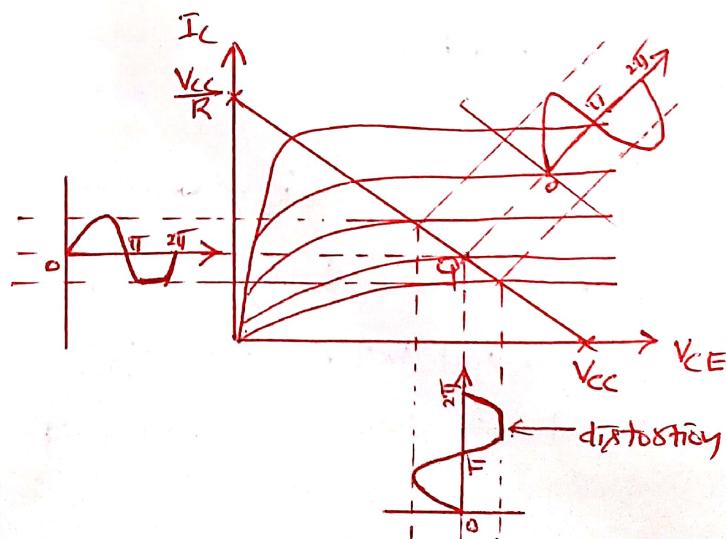
Biasing circuit is designed to fix operating point near to saturation region shown in figure. I_B is a sinusoidal signal but output collector current, I_C is clipped at positive half cycle i.e; distortion is present at output. So this is not a suitable operating point.



Case(ii):

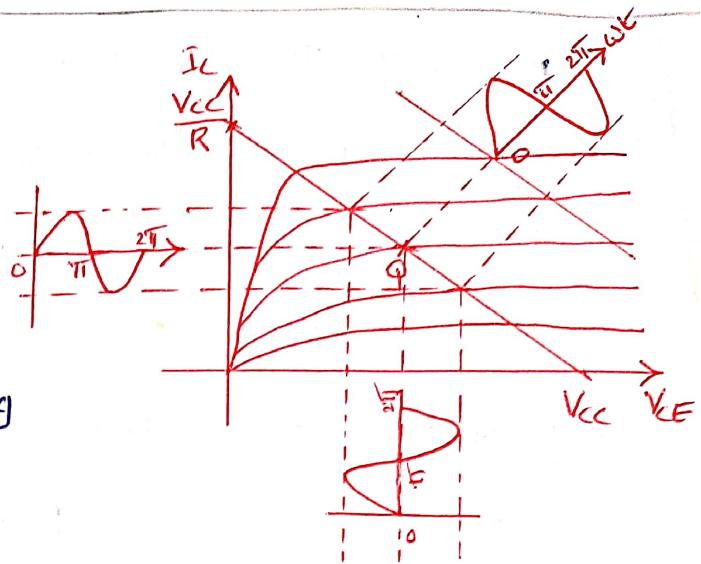
'Q' point is fixed near to cut-off region shown in figure. The collector current, I_C is clipped at negative cycle.

∴ This is not a suitable operating point.



case(iii):

If point Q is fixed at center of active region. The output signal is sinusoidal waveform without any distortion. Thus this point Q is the best operating point.



Factors affecting on operating point:

Important factors that are considered while designing the biasing circuit which are responsible for shifting the operating point.

i) Temperature:-

ii) Reverse Saturation Current, I_{CEO}:

Reverse saturation current doubles for every 10°C rise in temperature i.e;

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

$$I_C = \beta I_B + I_{CEO}$$

$$\therefore I_{CEO} = (1+\beta) I_{CBO}$$

As I_{CBO} doubles, I_{CEO} also increases which in turn increase I_C . The increase in collector current, I_C shifts the operating point into saturation region.

ii) Forward Voltage, V_{BE}:

Base to Emitter Voltage, V_{BE} changes with temperature at the rate of $2.5\text{mV}/^{\circ}\text{C}$. Base current, I_B depends upon V_{BE} since from the Base Circuit

$$I_B = \frac{V_{CC} - V_{BE} - I_{CBO}}{R_B}$$

and I_C is also depends on I_B from $I_C = \beta I_B$.

Therefore, I_C depends on V_{BE} . And it changes with temperature.

The change in I_C change or shifts the operating point.

iii) Amplification factor, β

β of transistor is also temperature dependent. As β varies I_C also varies since $I_C = \beta I_B$. As I_C changes the operating point also changes.

∴ To avoid thermal instability, the biasing circuit should be designed to provide a degree of thermal stability i.e; even though there are temperature changes the changes in transistor parameters (V_{CE} , I_C , P_D) should be less.

Requirements of biasing circuit

- i) Emitter Base junction (J_E) must be forward biased and collector Base junction (J_C) must be reverse biased i.e; the transistor must operate in middle of active region.
- ii) The circuit design should provide a degree of temperature stability.
- iii) Operating point should be made independent of transistor parameters (V_{CE} , I_C , β).

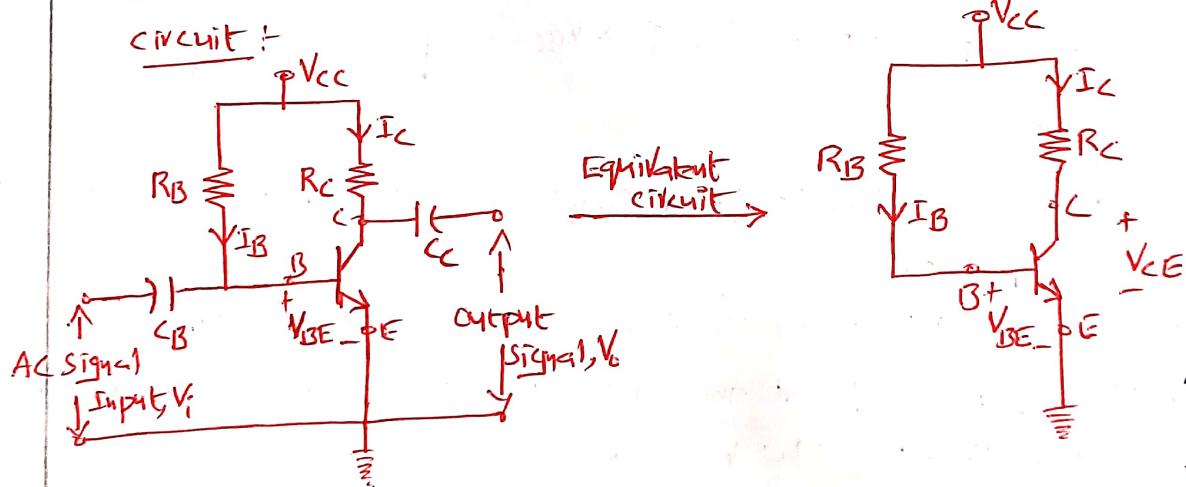
The following techniques are normally used to maintain operating point stable: They are - i) Stabilization techniques ii) Compensation techniques.

Stabilization techniques refers to the use of resistive biasing circuits which allow base current, I_B to vary so as to keep collector current I_C relatively constant with variations in I_C , β & V_{BE} .

Compensation techniques refers to the use of temperature sensitive devices such as diodes, transistors, thermistors etc which provide compensating voltages and currents to maintain operating point stable.

Methods of Bias Stabilization

> Fixed Bias



The figure above shows Fixed Bias circuit. For d.c analysis we can replace capacitors with an open circuit because the reactance of a capacitor for d.c is $X_C = \frac{1}{2\pi f C}$ and for d.c ($f=0$)

$$\therefore X_C = \frac{1}{f} = \infty.$$

The d.c equivalent circuit for fixed bias is shown in right side figure.

Base circuit: Applying KVL to base circuit above we get,

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \rightarrow ① \quad \because V_{CC} \gg V_{BE}$$

$$I_B = \frac{V_{CC}}{R_B}$$

Since I_B is independent of I_C , V_{BE} & β , so it is a fixed one.

Collector circuit:

Applying KVL to collector circuit of above figure we get,

$$V_{CC} = I_C R_C + V_{CE}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \rightarrow ②$$

$\therefore I_C$ is independent of I_C , β & V_{BE} .

$$V_{CE} = V_C - V_E$$

$$V_{CE} = V_C \quad \text{since } V_E = 0$$

$$V_{BE} = V_B - V_E$$

$$V_{BE} = V_B \quad \text{since } V_E = 0$$

$$V_{BC} = V_B - V_C$$

Advantages:

- 1) This fixed bias circuit is a simple circuit which uses very few components.
- 2) It provides maximum flexibility in the design since we can fix the operating point anywhere in active region characteristics simply by changing the value of R_B .

Disadvantages:

- 1) Thermal stability is not provided by this circuit since collector current increases as temperature is increased.
- 2) Since $I_C = \beta I_B$ as I_B is fixed from Base circuit, I_C depends on β which changes and shifts the operating point. Thus stabilization of operating point is very poor in fixed bias circuit.

Stability Factors:

Stability factor is defined as the degree of change in operating point due to variation in temperature.

There are three variables which are temperature dependent, they are:

$$\text{i)} S = \frac{\partial I_C}{\partial T_{CO}} \quad | \quad V_{BE}, \beta = \text{constant}$$

$$\text{ii)} S' = \frac{\partial I_C}{\partial V_{BE}} \quad | \quad I_{CO}, \beta = \text{constant}$$

$$\text{iii)} S'' = \frac{\partial I_C}{\partial \beta} \quad | \quad I_{CO}, V_{BE} = \text{constant}$$

Ideally stability factor should be zero to keep operating point stable.

General equation for stability factor using common emitter configuration is derived as follows:

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

partial differentiating above equation w.r.t I_C we have

$$\frac{\partial I_C}{\partial I_C} = \beta \cdot \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CBO}}{\partial I_C}$$

since β & V_{BE} are constant in deriving 'S'

$$1 - \beta \frac{\partial I_B}{\partial I_C} = (1+\beta) \frac{\partial I_{CBO}}{\partial I_C}$$

$$= (1+\beta) \times \frac{1}{S}$$

$$S = \frac{1+\beta}{1-\beta \left(\frac{\partial I_B}{\partial I_C} \right)} \rightarrow ③$$

Stability factor 'S' is defined as "The rate of change of collector current with respect to reverse saturation current, keeping V_{BE} & β constant".

Stability factors for fixed bias

i) \underline{S} : For fixed bias circuit we have $I_B = \frac{V_{CC} - V_{BE}}{R_B}$

Here, $\frac{\partial I_B}{\partial I_C} = 0$ because I_C is not there in above equation.

$$\therefore S = \frac{1+\beta}{1-\beta \left(\frac{\partial I_B}{\partial I_C} \right)} = \frac{1+\beta}{1-\beta(0)} = 1+\beta \Rightarrow \boxed{S = 1+\beta}$$

\therefore For $\beta=50$; $S = 1+50 = 51$

$\therefore I_C$ increases 51 times as fast as I_{C0} . ($\because S = \frac{I_C}{I_{C0}} = 51$)

such a large value of 'S' makes 'Thermal Runaway' ($I_C = 51 I_{C0}$)

ii) $\underline{S'} \therefore S' = \frac{\partial I_C}{\partial V_{BE}}$ | I_{C0}, β are constants.

From CE configuration we have $I_C = \beta I_B + (1+\beta) I_{CBO}$

differentiating w.r.t V_{BE} ; $I_C = \beta \left[\frac{V_{CC} - V_{BE}}{R_B} \right] + (1+\beta) I_{CBO}$

(From eq(1))

$$\frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_B} + 0 \Rightarrow$$

$$\boxed{S' = \frac{-\beta}{R_B}}$$

iii) $\underline{S''} \therefore S'' = \frac{\partial I_C}{\partial \beta}$ | V_{BE}, I_{C0} are constants.

We know that, $I_C = \beta I_B + (1+\beta) I_{CBO}$

$$= \beta \left[\frac{V_{CC} - V_{BE}}{R_B} \right] + (1+\beta) I_{CBO}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{V_{CC} - V_{BE}}{R_B} + I_{CBO}$$

$$S'' = I_B + I_{CBO} \Rightarrow \begin{cases} S'' = I_B \\ S'' = \frac{I_C}{\beta} \end{cases} \quad (\because I_B \gg I_{CBO})$$

$$\therefore I_C = \beta I_B; I_B = \frac{I_C}{\beta}$$

Self Bias (or) Emitter Bias

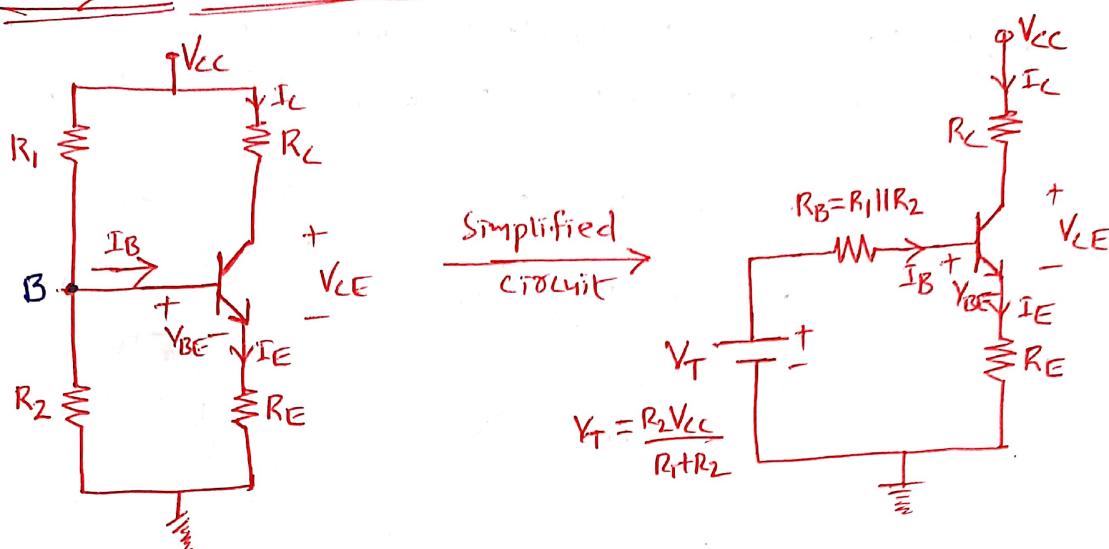


Figure shows Voltage divided bias circuit in which biasing is provided by three resistors R_1 , R_2 & R_E .

R_1 & R_2 act as a potential divider giving a fixed voltage to point B, which is Base.

In previous biasing techniques I_c and V_{CE} are a function of β . Since β is temperature sensitive then it is desirable to develop a bias circuit that is less sensitive to temperature and such circuit is called Voltage-Divider Bias (circuit, or) Self Bias or Emitter Bias.

$$\text{The Thevenin's Voltage } V_t \text{ across } R_2 \text{ is } V_t = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$\text{and base resistance, } R_B = R_1 || R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Base circuit:

Applying KVL to Base circuit we get

$$V_t = R_B I_B + V_{BE} + I_E R_E \rightarrow ①$$

$$V_t = R_B I_B + V_{BE} + (1+\beta) I_B R_E$$

$$\therefore I_B = \frac{V_t - V_{BE}}{R_B + (1+\beta) R_E}$$

$$\begin{aligned} I_E &= I_B + I_C \\ &= I_B + \beta I_B \\ &= (1+\beta) I_B \end{aligned}$$

Collector Circuit

Applying KVL to collector circuit we get

$$V_{CC} = I_C R_C + V_{LE} + I_E R_E \quad \text{Eqn ②}$$

$\because I_E \approx I_C$

$$\begin{aligned} V_{CC} &= I_C R_C + V_{LE} + I_C R_E \\ &= I_C [R_C + R_E] + V_{LE} \end{aligned}$$

$$\therefore I_C = \frac{V_{CC} - V_{LE}}{R_C + R_E}$$

Stability factors for ~~Wheatstone bridge~~ Bias (GT) Emitter follower

i) $S \doteq$ From figure : $V_T = I_B R_B + V_{BE} + I_E R_E$

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

partial differentiating w.r.t I_C .

$$0 = \frac{\partial I_B}{\partial I_C} R_B + 0 + \left(\frac{\partial I_B}{\partial I_C} + 1 \right) R_E$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E}$$

$$S = \frac{1+\beta}{1-\beta \left(\frac{\partial I_B}{\partial I_C} \right)}$$

$$= \frac{1+\beta}{1-\beta \left(\frac{-R_E}{R_B + R_E} \right)} = \frac{1+\beta}{1+\beta \frac{R_E}{R_B + R_E}} = \frac{(1+\beta) \left(1 + \frac{R_B}{R_E} \right)}{1+\beta + \frac{R_B}{R_E}}$$

a) If $\frac{R_B}{R_E} \ll 1$ then $S = \frac{1+\beta}{1+\beta} = 1 \quad \therefore \boxed{S=1}$

b) To keep $\frac{R_B}{R_E}$ small, we can keep R_B small, this means R_1, R_2 must be small. Due to small values of R_1 & R_2 more current is drawn from V_{CC} reducing life of battery.

$$V_E = I_E R_E$$

$$V_{CE} = V_C - V_E$$

$$V_C = V_{CE} + V_E$$

From ③

~~Assume~~

$$V_C = V_{CC} - V_{LE} - I_C R_C - I_E R_E + V_E + V_{CE}$$

$$V_C = V_{CC} - I_C R_C$$

$$V_{BE} = V_B - V_E$$

$$V_B = V_{BE} + V_E$$

From ①

$$V_B = V_{CC} - I_B R_B - I_E R_E + V_E$$

$$V_B = V_{CC} - I_B R_B$$

∴ while designing the circuit the resistance $R_1 \gg R_2$ is kept then $R_B = R_1 || R_2$ is small drawing less current from V_{CC} .

∴ stability factor's for Voltage divider bias is less compared to other biasing circuits. So this circuit is most commonly used.

$$\text{ii) } \underline{\underline{s'}} : \quad s' = \frac{\partial I_C}{\partial V_{BE}} \quad | \quad I_{CO}, \beta \text{ are constants.}$$

$$V_T = I_B R_B + V_{BE} + I_E R_E$$

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

we know that

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

$$I_B = I_C - \frac{(1+\beta) I_{CBO}}{\beta}$$

$$V_{BE} = V_T - I_B [R_B + R_E] - I_C R_E$$

$$= V_T - \left[\frac{I_C - (1+\beta) I_{CBO}}{\beta} \right] [R_B + R_E] - I_C R_E$$

$$= V_T - \frac{I_C}{\beta} [(1+\beta) R_E + R_B] + \frac{(R_E + R_B)(1+\beta) I_{CBO}}{\beta}$$

partially differentiating w.r.t V_{BE}

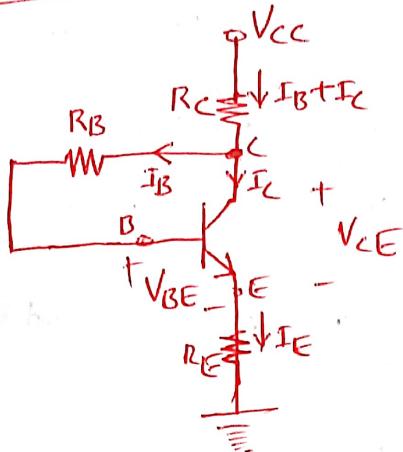
$$1 = 0 - \frac{\partial I_C}{\partial V_{BE}} \frac{[(1+\beta) R_E + R_B]}{\beta} + 0$$

$$1 = 0 - s' \frac{[(1+\beta) R_E + R_B]}{\beta}$$

$$\Rightarrow s' = \frac{-\beta}{(1+\beta) R_E + R_B}$$

$$\text{iii) } \underline{\underline{s''}} :$$

Collector to Base Bias



An improvement in stability is obtained by introducing a feedback path from collector to base shown in figure above.

Although the Q-point is not totally independent of β , the sensitivity to changes in β or temperature variations is normally less than encountered for the fixed bias or self bias circuits.

Base circuit: Applying KVL to base circuit, we get

$$\begin{aligned} V_{CC} &= (I_B + I_C)R_C + I_B R_B + V_{BE} + I_E R_E \\ &= (I_B + \beta I_B)R_C + I_B R_B + V_{BE} + I_C R_E \quad \because I_E \approx I_C \\ &= (I_B + \beta I_B)R_C + I_B R_B + V_{BE} + \beta I_B R_E \end{aligned}$$

$$V_{CC} = I_B [(1 + \beta)R_C + R_B + \beta R_E] + V_{BE} \quad \because \beta \gg 1$$

$$V_{CC} - V_{BE} = I_B [R_C + R_B + \beta R_E]$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta (R_C + R_E)}$$

In general the equation for I_B can be written as $I_B = \frac{V'}{R_B + \beta R'}$
where $V' = V_{CC} - V_{BE}$; $R' = R_C + R_E$

$$\text{Since } I_C = \beta I_B$$

$$I_C = \frac{\beta V^I}{R_B + R_L} \quad \because \beta R_L \gg R_B$$

$$\therefore I_C = \frac{\beta V^I}{\beta R_L} = \frac{V^I}{R_L}$$

$\therefore I_C$ is independent of value of β , the sensitivity to variations in β is less.

Collector Circuit Applying KVL to the collector circuit we get

$$V_{CC} = R_C (I_C + I_B) + V_{CE} + I_E R_E$$

$$I_E \approx I_C$$

$$V_{CC} = R_C (I_C + I_B) + V_{CE} + I_C R_E$$

$$V_{CC} = I_C (R_C + R_E) + I_B R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) - I_B R_C$$

In this circuit R_B appears across input base and output collector so "negative feedback" exists in the circuit.

Stability Factor:

$$\begin{aligned} \Rightarrow \underline{S} &= \text{From Figure: } V_{CC} = (I_C + I_B) R_C + I_B R_B + V_{BE} + I_E R_E \\ &= (I_C + I_B) R_C + I_B R_B + V_{BE} + I_C R_E \quad (\because I_E \approx I_C) \\ &V_{CC} = I_C (R_C + R_E) + I_B (R_B + R_C) + V_{BE} \end{aligned}$$

partial differentiating w.r.t I_C

$$0 = (R_C + R_E) + \frac{\partial I_B}{\partial I_C} (R_B + R_C) + 0$$

$$\frac{\delta I_B}{\delta I_C} = \frac{-(R_{CT} + R_E)}{R_B + R_C}$$

$$\therefore \text{Stability factor } S = \frac{1+\beta}{1-\beta \left(\frac{\delta I_B}{\delta I_C} \right)} = \frac{1+\beta}{1-\beta \left(-\frac{(R_{CT} + R_E)}{R_B + R_C} \right)}$$

$$S = \frac{1+\beta}{1+\beta \frac{(R_{CT} + R_E)}{(R_B + R_C)}}$$

This collector to base bias circuit provides lesser stability factor than for fixed bias circuit, then this circuit provides better stability than fixed bias circuit.

ii) S' : $S' = \frac{\delta I_C}{\delta V_{BE}} \quad | \quad I_C, \beta \text{ are constants}$

From Fig. we have $I_B \approx \frac{V_{CC} - V_{BE}}{R_B + R_E}$ $V_{CC} = (I_B + I_C)R_C + I_B R_B + V_{BE}$
 $I_E \approx I_C$

$$V_{CC} = I_B(R_C + R_E) + I_C(R_C + R_E) + V_{BE} \quad (\because I_E \approx I_C)$$

$$V_{CC} = \frac{I_C}{\beta} (R_C + R_E) + I_C(R_C + R_E) + V_{BE}$$

$$I_C \left[\frac{1}{\beta} (R_C + R_E) + (R_C + R_E) \right] = V_{CC} - V_{BE}$$

$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_C + R_E + \beta(R_C + R_E)}$$

$$\therefore \frac{\delta I_C}{\delta V_{BE}} = \frac{-\beta}{R_C + R_E + \beta(R_C + R_E)} \Rightarrow$$

$$S' = \frac{-\beta}{R_E + R_E + (1+\beta)R_L}$$

iii) S'' : $S'' = \frac{\delta I_C}{\delta \beta} \quad | \quad I_C, V_{BE} = \text{constants}$

From above derivation we have $I_C = \frac{\beta(V_{CC} - V_{BE})}{\beta R_E + R_E + (1+\beta)R_L}$

partial differentiate wrt β .

$$\frac{\partial I_C}{\partial \beta} = \frac{[\beta R_E + R_B + (1+\beta)R_C] [V_{CC} - V_{BE}] - \beta (V_{CC} - V_{BE}) \cdot (R_E + R_C)}{[\beta R_E + R_B + (1+\beta)R_C]^2}$$

$$= \frac{(V_{CC} - V_{BE}) (\beta R_E + R_B + (1+\beta)R_C - \beta R_E - \beta R_C)}{[\beta R_E + R_B + (1+\beta)R_C]^2}$$

$$= \frac{(V_{CC} - V_{BE}) (R_B + R_C)}{[\beta R_E + R_B + (1+\beta)R_C] [\beta R_E + R_B + (1+\beta)R_C]}$$

$$\beta'' = \frac{I_C}{\beta} \cdot \frac{(R_B + R_C)}{[\beta R_E + R_B + (1+\beta)R_C]}$$

problem 8:

Calculate operating point $Q'(V_{CE}, I_C)$ for the given circuit.

Sol: Apply KVL to Base circuit

$$12 = 10k(I_C + I_B) + 100kI_B + V_{BE}$$

$$12 = 10k(\beta I_B + I_B) + 100kI_B + 0.7$$

$$12 - 0.7 = I_B [10k(100+1) + 100k]$$

$$I_B = 10.18 \mu A ; I_C = \beta I_B = 100 \times 10.18 \mu A = 1.018 \text{ mA.}$$

Apply KVL to collector circuit

$$12 = 10k(I_C + I_B) + V_{CE}$$

$$V_{CE} = 12 - 10k(1.018 \text{ mA} + 10.18 \mu \text{A}) = 1.71 \text{ V.}$$

Operating point is $Q'(1.71, 1.018 \text{ mA})$.

Calculate stability factor 'S' for the given circuit

Sol: It is a fixed bias circuit.

$$\therefore S = 1 + \beta.$$

Apply KVL to collector

$$10 = 2kI_C + 4$$

$$I_C = \frac{10-4}{2k} = 3 \text{ mA}$$

KVL to Base

$$10 = 100kI_B + V_{BE}$$

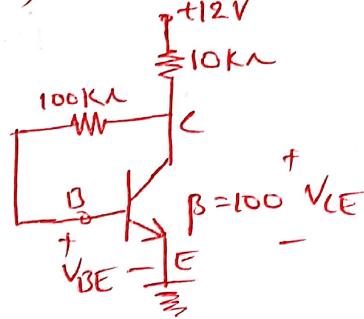
$$10 = 100kI_B + 0.7$$

$$I_B = \frac{10-0.7}{100k} = \frac{9.3}{100k} = 93 \mu \text{A}$$

$$I_C = \beta I_B$$

$$\beta = \frac{I_C}{I_B} = \frac{3 \text{ mA}}{93 \mu \text{A}} = 32.258. \quad \therefore S = 1 + \beta$$

$$= 1 + 32.258 = 33.258$$



THERMAL RUNAWAY :

The power dissipated within a transistor is predominantly the power dissipated at its collector Base junction. Thus maximum power is limited by the temperature that the collector Base junction can withstand. For silicon transistor this temperature is in the range 150 to 225°C and for Germanium it is between 60 to 100°C.

Collector - Base junction temperature may rise because of two reasons.

1. Due to rise in Ambient temperature
2. Due to self-heating.

Self heating : The increase in collector current increases the power dissipated at the collector junction, in turn increases the temperature of the junction & hence increases the collector current. This process is cumulative & it is referred to as "SELF HEATING". The excess heat produced at C-B junction may even burn & destroy the transistor. This situation is called "THERMAL RUNAWAY" of the transistor.

THERMAL RESISTANCE :-

The steady state temperature rise at the collector junction is proportional to the power dissipated at the junction.

i.e $T_j - T_A \propto P_D$

$$T_j - T_A = \Theta P_D$$

$$\therefore \Theta = \frac{T_j - T_A}{P_D} \text{ } ^\circ\text{C/watt}$$

T_j = junction temperature

T_A = Ambient temperature

P_D = power dissipated at collector junction

Θ = Thermal resistance

T_A = Temperature in a room (or) temperature surrounding an object.

Condition for Thermal Runaway (Thermal stability):

Required condition is that "the rate at which heat is released at the collector junction must not exceed the rate at which the heat can be dissipated."

$$\text{i.e. } \frac{\partial P_c}{\partial T_j} < \frac{\partial P_D}{\partial T_j}$$

$$T_j - T_A = \Theta P_D$$

Differentiating w.r.t T_j

$$1 - 0 = \Theta \frac{\partial P_D}{\partial T_j}$$

$$\therefore \frac{\partial P_D}{\partial T_j} = \frac{1}{\Theta}$$

$$\therefore \frac{\partial P_c}{\partial T_j} < \frac{1}{\Theta}$$

This condition must be satisfied to prevent Thermal Runaway.

By suitable circuit design it is possible to ensure that the transistor cannot runaway below a specified ambient temperature or even under any conditions. Such an analysis is made below.

Thermal Stability:

Consider voltage divider Bias circuit for analysis.

From the figure :

P_C = heat generated at collector junction

= DC power input to circuit -
the power lost as $I^2 R$
in R_C & R_E

$$\therefore P_C = V_{CC} \times I_C - I_C^2 R_C - I_E^2 R_E$$

$$\therefore I_C \approx I_E$$

$$P_C = V_{CC} I_C - I_C^2 [R_C + R_E]$$

Differentiating w.r.t ' I_C ' we get

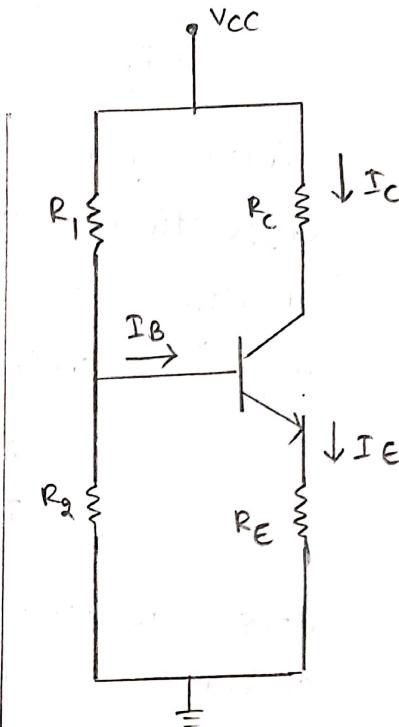
$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2I_C (R_C + R_E) \quad -(1)$$

Condition to avoid thermal runaway can be written as

$$\frac{\partial P_C}{\partial T_j} < 1/0 \Rightarrow \frac{\partial P_C}{\partial I_C} \times \frac{\partial I_C}{\partial T_j} < 1/0 \quad -(2)$$

we know that as junction temperature affects collector current by affecting I_{CO} , V_{BE} , β

$$\frac{\partial I_C}{\partial I_{CO}} \times \frac{\partial I_{CO}}{\partial T_j} + \frac{\partial I_C}{\partial V_{BE}} \times \frac{\partial V_{BE}}{\partial T_j} + \frac{\partial I_C}{\partial \beta} \times \frac{\partial \beta}{\partial T_j}$$



voltage divider
Bias circuit.

$$\therefore \frac{\partial I_C}{\partial T_j} = S \cdot \frac{\partial I_{CO}}{\partial T_j} + S' \frac{\partial V_{BE}}{\partial T_j} + S'' \frac{\partial \beta}{\partial T_j}$$

$$\frac{\partial I_C}{\partial T_j} = S \cdot \frac{\partial I_{CO}}{\partial T_j} + S' \frac{\partial V_{BE}}{\partial T_j} + S'' \frac{\partial \beta}{\partial T_j}$$

since junction temp. affects collector current by affecting I_{CO} , V_{BE} , β . But as we are doing analysis for thermal runaway the effect of I_{CO} dominates.

$$\therefore \frac{\partial I_C}{\partial T_j} = S \cdot \frac{\partial I_{CO}}{\partial T_j}$$

As reverse saturation current I_{CO} for both silicon & Germanium increases about 7 percent per $^{\circ}\text{C}$, we can write

$$\frac{\partial I_{CO}}{\partial T_j} = 0.07 I_{CO}$$

$$\therefore \frac{\partial I_C}{\partial T_j} = S \times 0.07 I_{CO}$$

— (3)

Substituting (1) & (3) in eq. (2) we have

$$[V_{CC} - \frac{1}{2} I_C (R_C + R_E)] S \times 0.07 I_{CO} < 10$$

As S , I_{CO} , θ are positive, we see that the inequality in above eq. is always satisfied provided that the quantity in square bracket is negative.

$$\therefore V_{CC} - 2I_C(R_C + R_E) < 0$$

$$V_{CC} < 2I_C(R_C + R_E)$$

$$\boxed{\frac{V_{CC}}{2} < I_C(R_C + R_E)} \quad - (4)$$

Apply KVL to collector circuit of figure:
we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\because I_C \approx I_E$$

$$V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$V_{CC} - V_{CE} = I_C (R_C + R_E)$$

substitute it in eq. (4)

$$\frac{V_{CC}}{2} < V_{CC} - V_{CE}$$

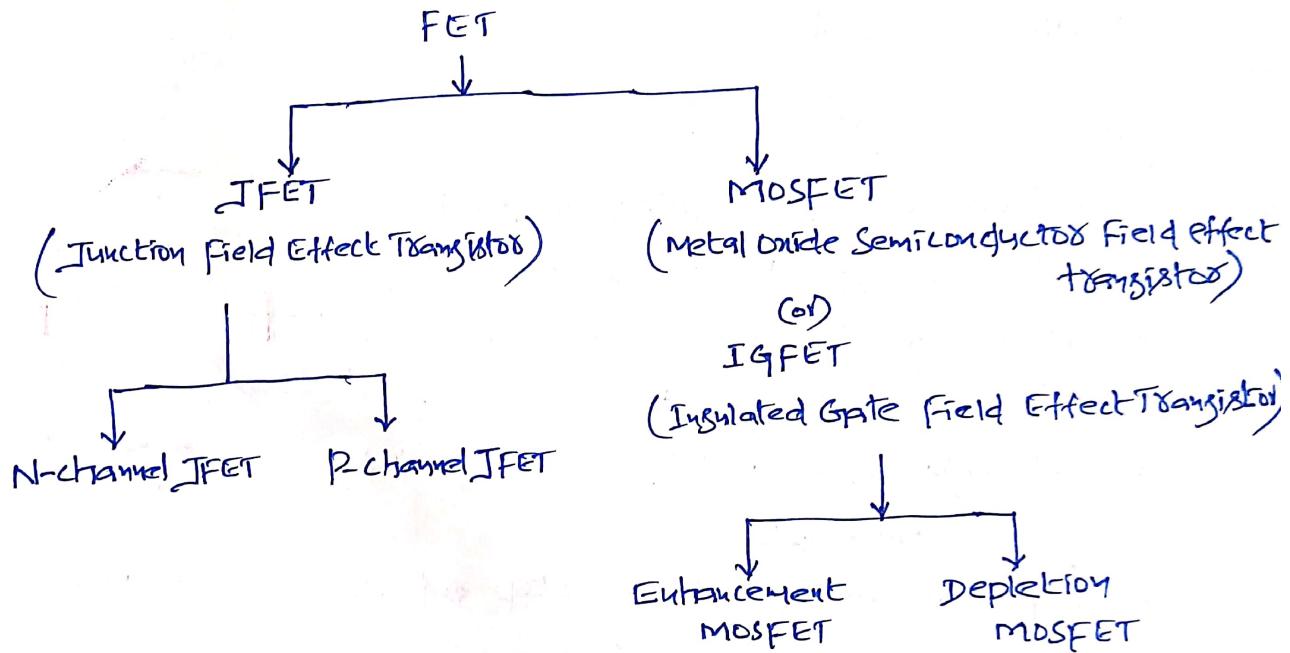
$$V_{CE} < V_{CC} - \frac{V_{CC}}{2}$$

$$\boxed{V_{CE} < \frac{V_{CC}}{2}}$$

If $V_{CE} < \frac{V_{CC}}{2}$ the stability is ensured.

Field Effect Transistor :-

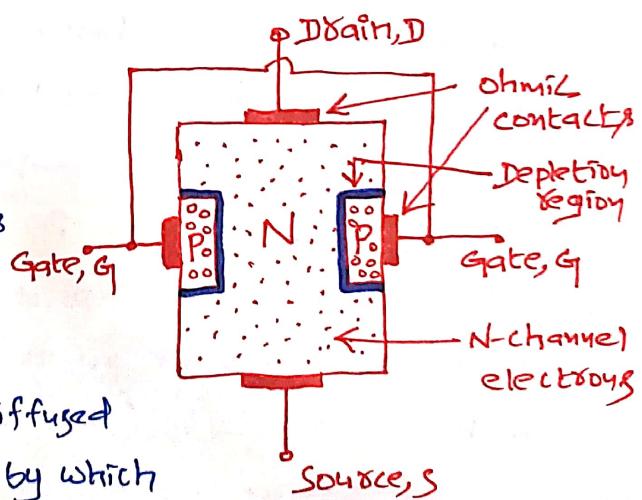
- FET is a semiconductor device which depends for its operation on the control of current by an electric field.
- FET is a unipolar device, in which current flows only due to majority carriers whereas BJT is a Bipolar device.
- FET is a three terminal device which contains source (S), Drain (D), Gate (G) and current is controlled by voltage at Gate terminal.



N-channel JFET :-

construction :

- It consists of N-type bar which is made of silicon and ohmic contacts are connected with terminals Source and Drain.
- A heavily doped P-type silicon is diffused on both sides of N-type silicon bar by which PN junctions are formed. These layers are joined together and called Gate, G.



Source: Source is a terminal through which majority carriers enter the bar.

Drain: It is the terminal through which majority carriers leave the bar.

Gate: Heavily doped 'P' regions of acceptor impurities on both sides of N-type bar have formed.

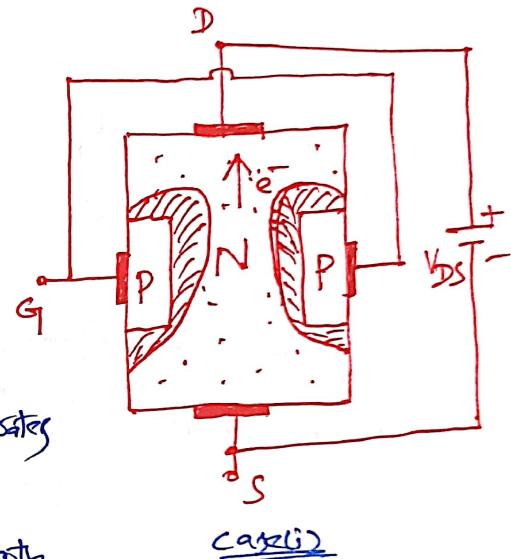
channel: The region between two Gate-regions is channel through which majority carriers move from Source to Drain.

substrate (or) shield: To protect FET from Electromagnetic fields.

Principle of Operation:

Case(I): $V_{GS} = 0$ Volt.

- When there is no Gate potential applied and with V_{DS} applied between Drain and source electrons start to flow from Source to drain creating drain current, I_D . As P is heavily doped depletion region penetrates heavily into N-channel.



- This depletion region is wider at the top of both P-type material and it's narrow at bottom. This is due to reverse biasing at top side with respect to V_{DS} and forward biasing at bottom side and due to this the shape of depletion region is like wedge shape shown in fig.

Case(II): As the Voltage V_{DS} is increased from 0 to a few Volts, the current will increase as determined by Ohm's law.

As V_{DS} reaches to V_P (Pinch-off Voltage) the current is almost constant and this region is called "pinch-off region". The region from 0 to V_P in the graph is called "Ohmic Region" and in this region JFET acts like "Voltage Variable Resistor (VVR)".

Case(ii): $V_{GS} < 0 \text{ Volts}$

— when a negative $V_{GS} = -1 \text{ V}$ is applied the depletion increases and current reduces than when it is at $V_{GS} = 0 \text{ Volt}$ and comes to saturation at lower voltages of V_{DS} .

→ As V_{GS} is increased more i.e., $V_{GS} = -5 \text{ V}$ both the depletion regions touch at intrinsic zero current flows in the device.

Volt-Ampere characteristics of JFET:

There are two characteristics of JFET they are:

- i) Drain (Output) characteristics
- ii) Transfer characteristics

Drain (output) characteristics:

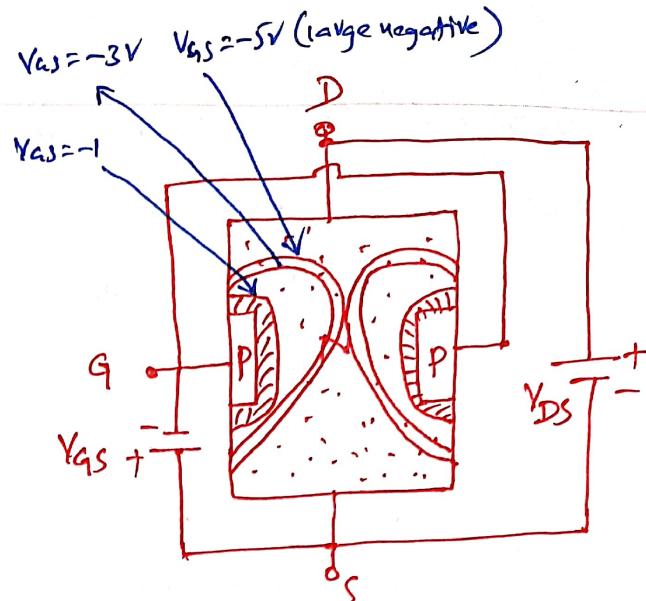
— From the figure as voltage V_{DS} increases then current I_D also increases for small values of V_{DS} .

This region is called "Ohmic Region".

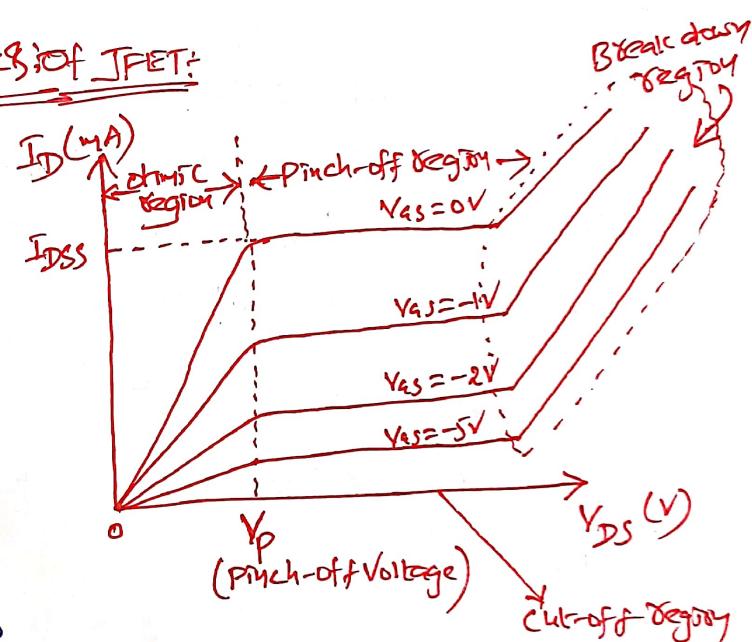
and FET acts as a "Voltage Variable Resistor (VVR)".

— As V_{DS} increases the current I_D reaches to its constant level called "Pinch-off Voltage, V_p " or constant current region.

— As V_{DS} is increased beyond "pinch-off" voltage, V_p the drain current I_D remains constant upto certain values of V_{DS} and hence space charge region could not oppose the carriers and suddenly current



Small V_{GS} :



Drain characteristics

increases and this region is called "Breakdown Region." At this point I_D increases rapidly and the device may be destroyed.

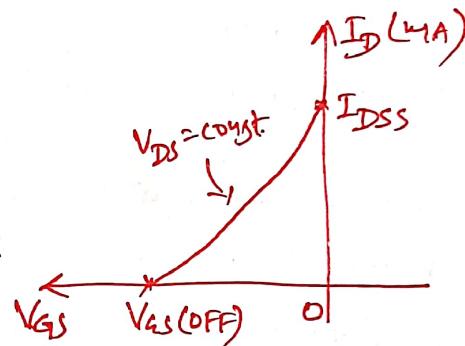
- For N-channel JFET more negative V_{GS} cause $I_D = 0$ where depletion regions completely touches with each other and the channel closes. The value of V_{GS} at the cut-off point is designated as $V_{GS(OFF)}$.

Pinch-off Voltage, $V_p \rightarrow$ constant I_D

Cut-off Voltage, $V_{GS(OFF)} \rightarrow I_D = 0$.

i) Transfer characteristics:

- The curve represents transfer characteristics of N-channel JFET drawn between I_D and V_{GS} keeping V_{DS} constant.



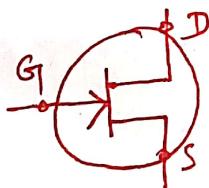
- From the characteristics we have

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

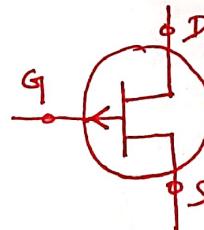
which is non linear and the relationship is defined by "Shockley's" equation.

point at bottom where $I_D = 0$ is $V_{GS(OFF)}$ and at top of curve on I_D axis represents I_{DSS} (Drain-source saturation current) at $V_G = 0$.

Symbols:



N-channel JFET



P-channel JFET

Parameters of JFET:

i) Transconductance (g_m):

$g_m = \frac{\text{Variation in drain current}}{\text{Variation in Gate Source Voltage}}$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad | V_{DS} = \text{constant}$$

$$\therefore g_m = -\frac{2I_{DSS}}{V_p} \left(1 - \frac{V_{GS}}{V_p}\right)$$

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_p}\right)$$

Units are "Micro Ampere per volt"
or
"MICROSIRAMENS"

$$g_{m0} = -\frac{2I_{DSS}}{V_p}$$

$$\text{ii) Drain Resistance, } \delta_d : \quad \delta_d = \frac{\text{drain voltage}}{\text{drain current}} = \frac{\Delta V_{DS}}{\Delta I_D} \quad | V_{GS} = \text{constant.}$$

iii) Amplification factor, μ :

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \quad | I_D = \text{constant}$$

$$= \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} = \delta_d \cdot g_m \quad \therefore \boxed{\mu = g_m \delta_d}$$

Comparison of BJT and FET:

BJT

- 1) Current controlled current source
- 2) Bipolar device because current flows due to majority & minority.
- 3) Input resistance, R_i is low
- 4) Bigger in size
- 5) More noisy
- 6) Cheaper
- 7) "Offset" or cut-in Voltage exists
- 8) There is Thermal Runaway
- 9) R_o increases as output junction is reverse biased

FET

- 1) Voltage controlled ~~current~~ source
- 2) Unipolar device; current flows due to majority carriers.
- 3) Input resistance, R_i is high.
- 4) Smaller in size used in Integrated Circuits.
- 5) Less noisy than BJT
- 6) Costly
- 7) No off-set Voltage exists so it is good for signal chopping.
- 8) No Thermal Runaway.
- 9) R_o decreases as current passes through the channel.

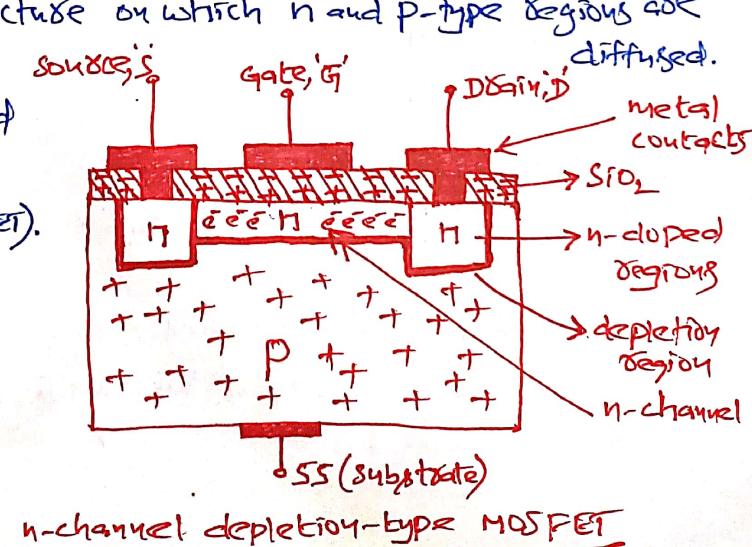
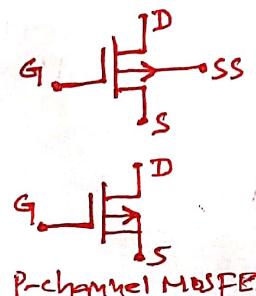
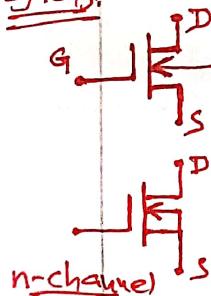
MOSFET :- (Metal Oxide Semiconductor FET) (or) IGFET:

MOSFETs are broken into depletion type and Enhancement type.

Depletion MOSFET :- [n-channel]

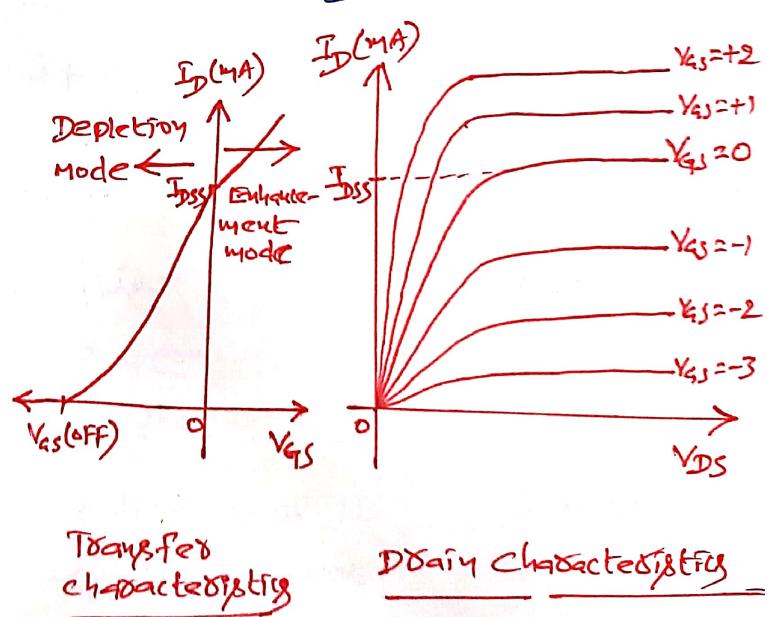
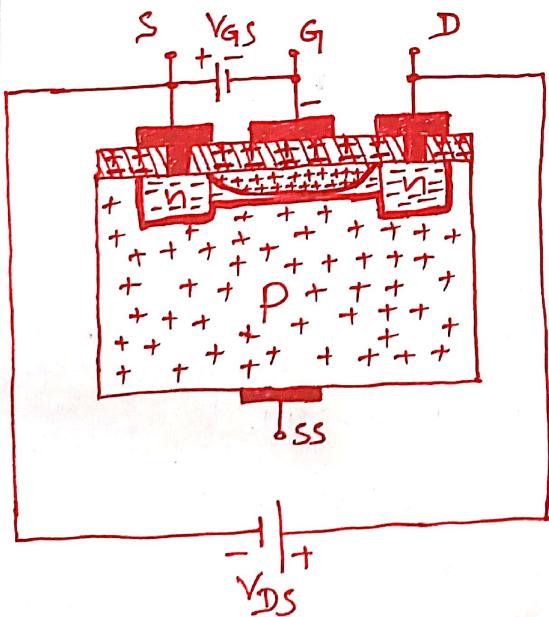
Construction :-

- The basic construction of the n-channel depletion-type MOSFET is provided in figure below.
- A slab of p-type material is formed from a silicon base and is referred to as the "substrate, ss".
- The source and drain terminals are connected through metallic contacts to n-type doped regions linked by an n-channel.
- The gate is also connected to a metal contact surface but being insulated from the n-channel by a very thin silicon dioxide (SiO_2) layer.
- SiO_2 is an insulator referred to as "dielectric" that sets up opposing electric fields within the dielectric when exposed to externally applied field. This SiO_2 provides "direct connection between Gate terminal and channel of a MOSFET."
- The reason for label "Metal-Oxide-Semiconductor FET" :-
metal - for source, drain and gate connections to proper surface oxide - for silicon dioxide insulating layer
semiconductor - for basic structure on which n and p-type regions are diffused.
- The insulating layer between source, gate, and drain has resulted in another name for the device called Insulated-Gate FET (IGFET).



Operation and characteristics

<u>V_{GS}</u>	<u>Effect</u>	<u>I_D [Drain Current]</u>
i) zero	If voltage V_{DS} is applied across drain-source current slowly increases from source to drain because electrons in n-type departs at source travels through the channel and are attracted at drain. As V_{DS} is increased Drain current also increases shown in figure.	Increases from zero to maximum value, I_{DS} .
ii) Negative	The negative potential at gate attract holes from P-type substrate and repel electrons. Depending on magnitude of V_{GS} (-ve) recombination takes place and reduce electrons in n-channel.	Drain current decreases
iii) Positive	The positive gate draws additional electrons from P-type substrate increasing electrons in n-channel. This is called "Enhancement Region".	still increases

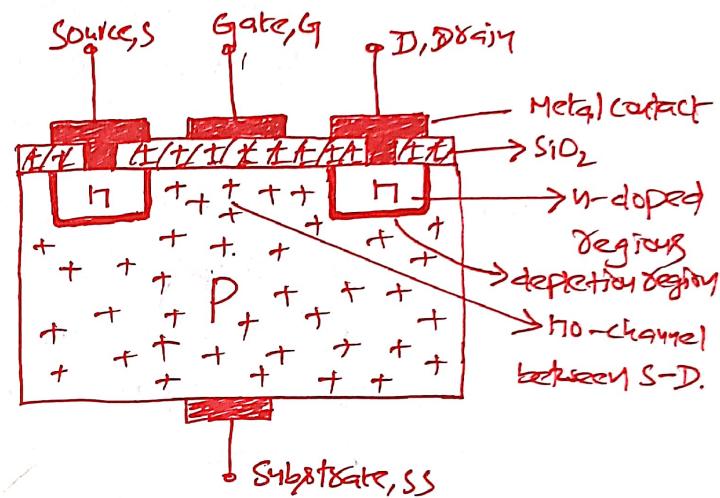
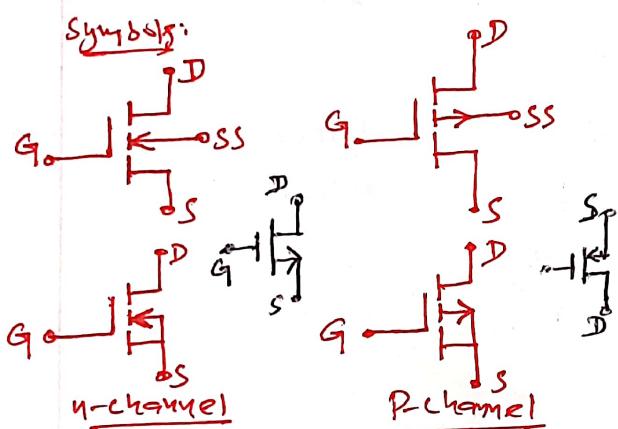


ii) Enhancement MOSFET (N-channel)

Construction:-

- A slab of p-type material is formed from a Silicon base and is referred to as the substrate.
- The construction is same as that of Depletion MOSFET (N-channel) but there is an absence of a channel between the two n-doped regions. This is the primary difference between the constructions of two MOSFET's.

Operation and characteristics



Operation and characteristics

V_{GS}

Effect

I_D (Drain current)

i) zero

If V_{GS} is applied between Gate to Source then in the absence of channel there are no charge carriers moving from Source to Drain.

Zero current flows.

ii) Negative

If V_{DS} is negative between Source to Drain then V_S is negative there is no channel with electrons in between Source to Drain.

Zero current flows.

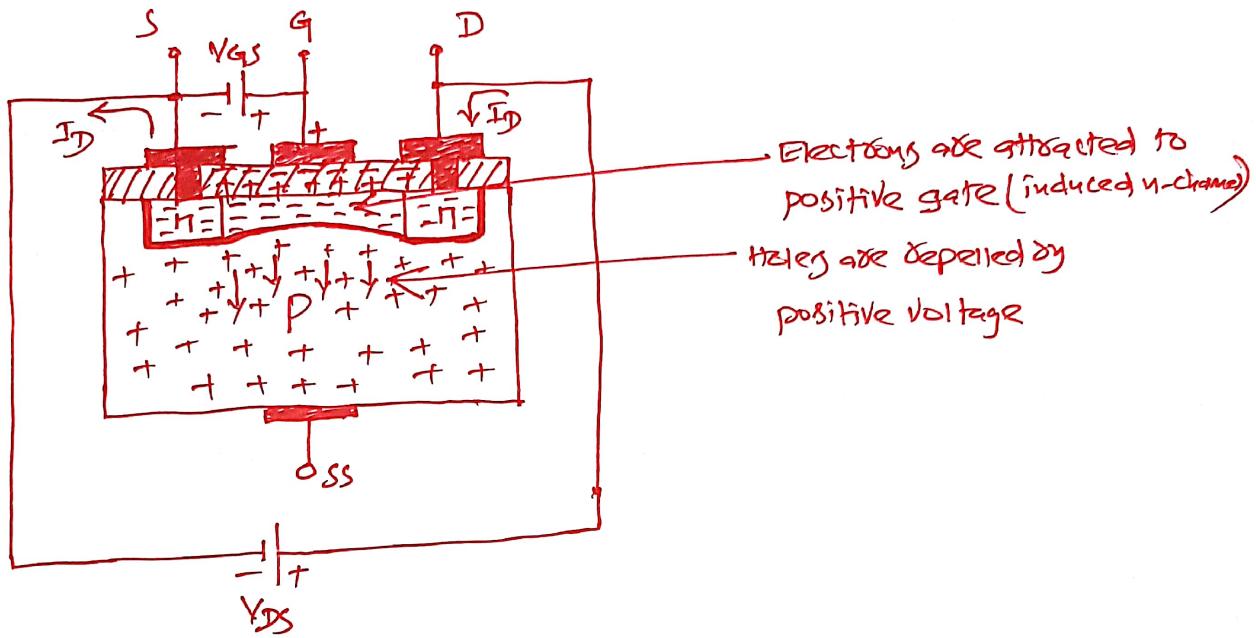
iii) Positive

If V_{GS} is positive then all negative carriers present in p-substrate are attracted towards the Gate and a negative channel with electrons is formed between Source to Drain. Then current flows from Source to Drain.

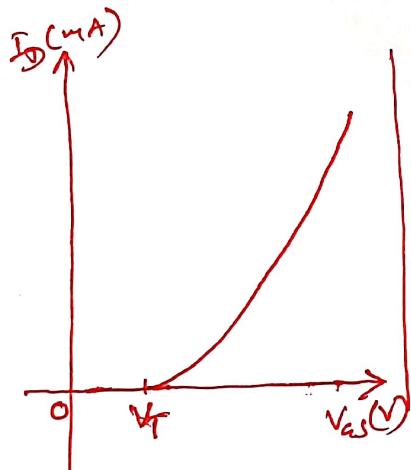
Increases from zero to maximum value.

45

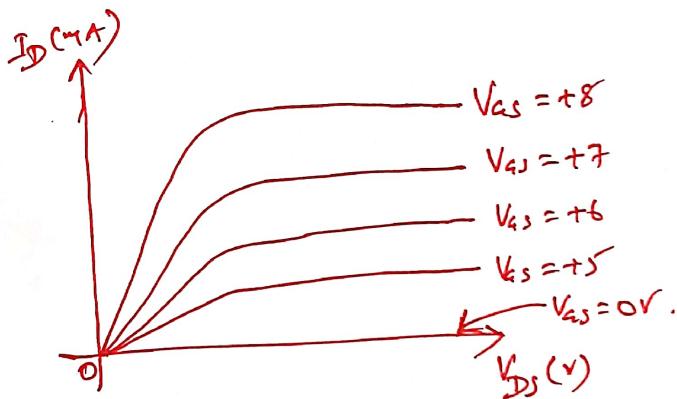
Thus drain current is "Enhanced" by the positive gate voltage and such a device is called an "Enhancement-type metal-oxide semiconductor."



n-channel Enhancement MOSFET :



Transfer Characteristics



Drain characteristics

Comparison of JFET and MOSFET

JFET	MOSFET
1. The input resistance is High it is in the range of $10^8 \Omega$	The input resistance is Very High it is in the range of 10^{10} to $10^{15} \Omega$.
2. Output Drain resistance is higher ($1 M\Omega$)	Output Drain resistance is lower than JFET ($50k\Omega$)
3. Operated only in the depletion mode	Operated in both depletion and Enhancement mode
4. Gate leakage current is of the order of $10^{-9} A$	Gate leakage current is of the order of $10^{-12} A$
5. The output characteristics are flatter	The output characteristics are not flatter
6. Used in VLSI circuits.	Widely used in VLSI circuits than JFET

From the MOSFET,

$$\text{Capacitance is given as, } C_{ox} = \frac{\epsilon_{ox}}{L}$$

ϵ_{ox} - thickness of oxide.

ϵ_{ox} - Oxide permittivity

$$\epsilon_{ox} = 3.9 \epsilon_0$$

ϵ_0 - permittivity of free space

$$\epsilon_{ox} = 3.9 \times 8.854 \times 10^{-12} F/m$$

$$\epsilon_{ox} = 3.45 \times 10^{-11} F/m.$$

Drain current in Triode region (Non-saturation region) is given as:

$$i_D = \frac{Mn C_{ox} W}{L} \left[(V_{ds} - V_T) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

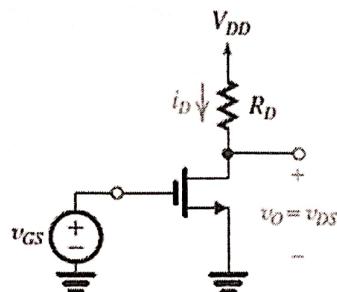
Drain current in saturation region at $V_{ds} = V_{ds} - V_T$ is given as:

$$i_D = \frac{Mn C_{ox} W}{2L} (V_{ds} - V_T)^2$$

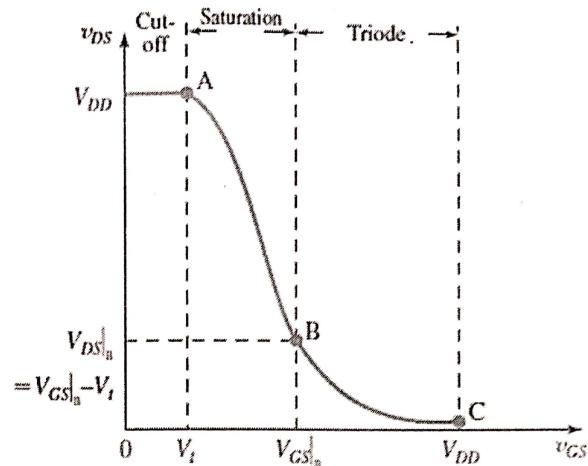
Here, $k_m = Mn C_{ox}$ - is called "process transconductance parameter" A_{V2}

$$k_m = \frac{Mn C_{ox} W}{2L} - \text{is called "conductance parameter".}$$

MOSFET as an Amplifier:



MOSFET Amplifier Circuit



Voltage Transfer Characteristics

A simple way to convert a transconductance amplifier to a voltage amplifier is to pass the output current through a resistor and take the voltage across the resistor as the output. Doing this for a MOSFET results in the simple amplifier circuit shown in figure above.

Here V_{GS} is the input voltage, R_D is known as a load resistance where it converts the drain current i_D to a voltage $i_D R_D$, and V_{DD} is the supply voltage that powers up the amplifier and, together with R_D establishes operation in the saturation region.

In the amplifier circuit of Fig (a) the output voltage is taken between the drain and ground. This is done because of the need to maintain a ground reference throughout the circuit.

Apply KVL to the drain circuit, we get

$$V_{DD} = i_D R_D + V_{DS}$$

The output voltage V_{DS} is given by

$$V_{DS} = V_{DD} - i_D R_D$$

A very useful tool that yields great insight into the operation of an amplifier circuit is its voltage transfer characteristic (VTC). This is simply a plot of the output voltage V_{DS} versus the input voltage V_{GS} .

Case (i): $V_{GS} < V_t$ – transistor is cut-off i.e., $i_D=0$, therefore from the above equation, $V_{DS}=V_{DD}$.

Case (ii): $V_{GS} > V_t$ – transistor is ON i.e., i_D increases but V_{DS} decreases as shown in fig (b).

Case (iii): $V_{GS} > B$ – transistor is in Triode region, i_D double increase and V_{DS} decreases more.

The VTC in fig(b) indicates that the segment of greatest slope that is potentially the largest amplifier gain is that labeled AB, which corresponds to operation in the saturation region.

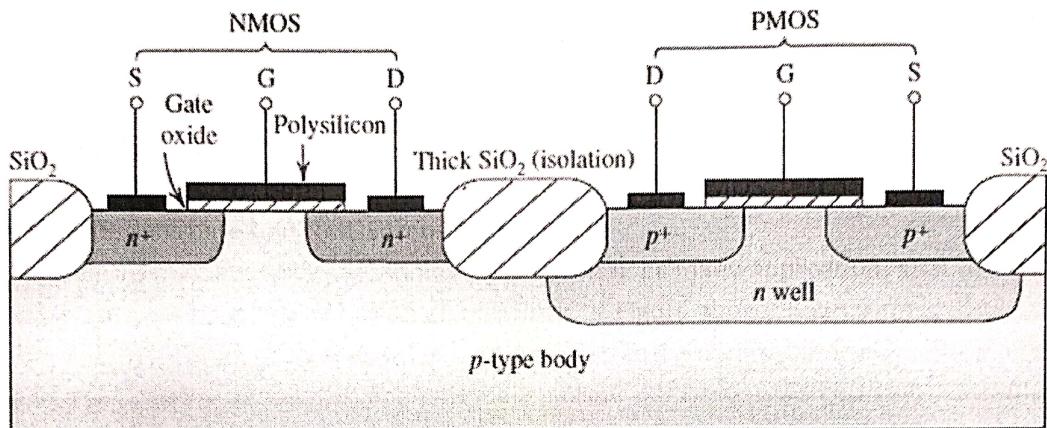
An expression for the segment AB can be obtained by substituting for i_D by its saturation-region value

$$i_D = k_n(V_{GS} - V_t)^2$$

$$\text{Therefore, } V_{DS} = V_{DD} - k_n R_D (V_{GS} - V_t)^2$$

$$\text{Voltage Gain, } A_V = V_{DS}/V_{GS}$$

Complementary Metal Oxide Semiconductor (CMOS):



CMOS Circuit

A technology was developed that permits the fabrication of both NMOS and PMOS transistors on the same chip that is called **Complementary Metal Oxide Semiconductor (CMOS)**. This technology is currently the dominant electronics technology.

As the name implies, Complementary MOS technology employs MOS transistors of both polarities. Although CMOS circuits are somewhat more difficult to fabricate than NMOS, the availability of complementary devices makes possible many powerful circuit configurations. Indeed, at the present time CMOS is the most widely used of all the IC technologies. This statement applies to both analog and digital circuits. CMOS technology has virtually replaced designs based on NMOS transistors alone.

Furthermore, by 2009 CMOS technology had taken over many applications that just a few years earlier were possible only with bipolar devices. Figure above shows a cross section of a CMOS chip illustrating how the PMOS and NMOS transistors are fabricated. Observe that while the NMOS transistor is implemented directly in the p -type substrate, the PMOS transistor is fabricated in a specially created n region, known as an **n well**. The two devices are isolated from each other by a thick region of oxide that functions as an insulator. Not shown on the diagram are the connections made to the p -type body and to the n well. The latter connection serves as the body terminal for the PMOS transistor.

Biasing in MOS Amplifier Circuits:

The main step in the design of a MOSFET amplifier circuit is the establishment of an appropriate dc operating point for the transistor to produce faithful amplification. This is known as biasing or bias design.

For this the operating point (I_D, V_{DS}) should be operated in saturation region for all input signals.

i) Biasing by fixing V_{GS} without source resistance:-

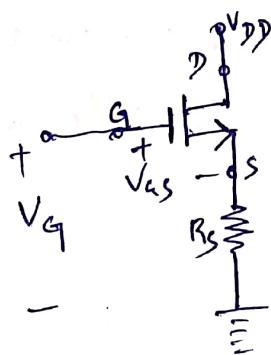
Biasing a MOSFET is to fix gate-to-source voltage (V_{GS}) to provide desired I_D .

From the equation of drain current in saturation region:

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_t)^2$$

If V_{GS} is fixed, but both V_t and μ_n depend on temperature and drain current I_D changes, making operating point unstable.

ii) Biasing by fixing V_{GS} with connecting a source resistance:-



$$\text{From the circuit: } V_g = V_{GS} + I_D R_S$$

(i) If $V_g > V_{GS}$, V_{GS} is neglected, then

$$V_g = I_D R_S \Rightarrow I_D = \frac{V_g}{R_S}$$

(ii) If $V_g < V_{GS}$, then V_g is neglected,

$$-V_{GS} = I_D R_S \Rightarrow I_D = -\frac{V_{GS}}{R_S}$$

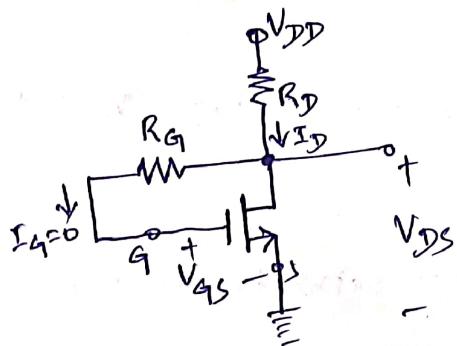
Resistor R_S provides "negative feedback", which stabilizes I_D .

case iii) If V_g is constant, V_{ds} will have to decrease, this in turn decreases drain current ' I_D ' starting the operating point.

thus R_g works to keep I_D as constant as possible.

The negative feedback action of R_g gives the name "degeneration resistance".

iii) Biasing using a Drain-to-Gate Feedback Resistor



Here, the larger feedback resistance R_g produce gate current $I_g = 0$.

$$\therefore V_{ds} = V_{dd} \quad (\because I_g = 0).$$

Apply KVL we get,

$$V_{dd} = I_D R_D + V_{ds}$$

$$V_{ds} = V_{dd} - I_D R_D$$

$$V_{gs} = V_{dd} - I_D R_D$$

$$\therefore \boxed{V_{dd} = V_{gs} + I_D R_D.}$$

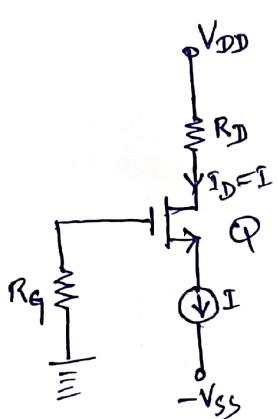
Here as I_D increased for some reason, then V_{gs} must decrease.

The decrease in V_{gs} in turn decreases I_D to keep it as constant.

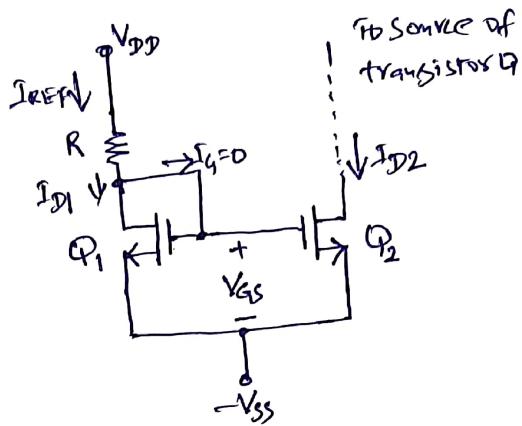
thus Negative feedback or degeneration provided by R_g works to keep the value of I_D as constant as possible.

v) Biasing using a constant-current source:

This is the most effective method for biasing a MOSFET amplifier.



Biasing MOSFET using a constant-current source, I



Implementation of constant-current source I using a current mirror.

→ The transistor Q_1 is in saturation region. ($\because I_g = 0, \therefore S = D$)

$$\therefore I_{D1} = \frac{k_n'}{2} \left(\frac{W}{L} \right)_1 (V_{GS} - V_t)^2 \quad | \quad I_{D1} = I_{REF}.$$

→ The Q_2 transistor has same V_{GS} and assume it is operating in saturation region, then

$$I_{D2} = \frac{k_n'}{2} \left(\frac{W}{L} \right)_2 (V_{GS} - V_t)^2 \quad | \quad I_{D2} = I.$$

$$\frac{I_{D2}}{I_{D1}} = \frac{\left(\frac{W}{L} \right)_2}{\left(\frac{W}{L} \right)_1} \Rightarrow \boxed{I_{D2} = I_{D1} \times \frac{\left(\frac{W}{L} \right)_2}{\left(\frac{W}{L} \right)_1}}$$

$$\therefore I = I_{REF} \frac{\left(\frac{W}{L} \right)_2}{\left(\frac{W}{L} \right)_1}$$

This circuit is known as "current mirror" and is very popular in design of IC MOS amplifiers.

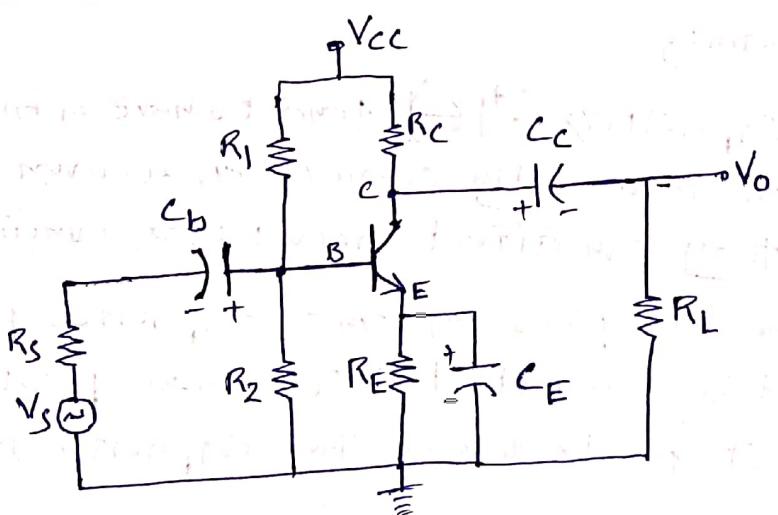
ANALYSIS OF TRANSISTOR AMPLIFIER AT LOW FREQUENCY

Small Signal High Frequency Transistor Amplifier Models

Introduction:-

V-I characteristics of BJT are non-linear. The analysis of non-linear device is complex. To simplify the analysis of BJT, its operation is restricted to the linear V-I characteristics around the Q-point in the Active Region. This approximation is possible only with small input signals. The term small signal amplifier refers to the use of signal that takes up a relatively small percentage of an amplifier's operational range. With small input signals, the transistor can be replaced with small signal linear model. This model is also called "small signal Equivalent circuit".

Common Emitter (CE) Amplifier circuit:



From the above circuit:-

- Resistances R_1, R_2, R_C, R_E forms the Voltage divided bias circuit for CE amplifier. It sets the proper operating point for CE amplifier and provides faithful amplification of input signal.

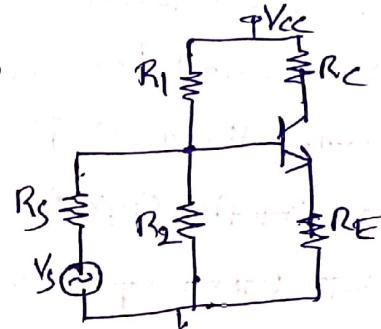
Blocking capacitor

ii) Input capacitor, C_b : It couples the input signal to the base of the transistors. It blocks any DC component present in the signal and allows (passes) only AC signal for amplification.

If ' C_b ' is not connected in the circuit then source is directly connected to circuit as shown in the figure below.

The bias voltage is altered to

$$\text{so } V_{R_2} = \frac{V_{CC} \cdot (R_S || R_L)}{R_1 + (R_S || R_2)}$$



Instead of $V_{R_2} = \frac{V_{CC} B_2}{R_1 + R_2}$

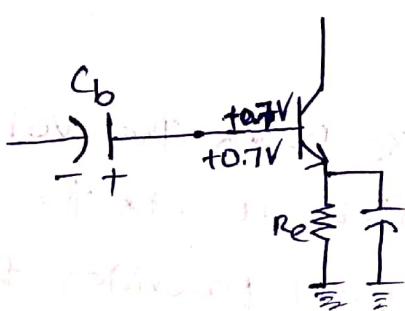
Then the circuit bias conditions will be altered and the operating point is unstable.

1. Blocking capacitor, C_b is required to keep operating point stable

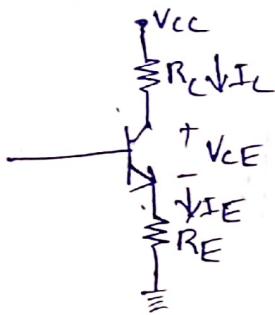
Capacitor polarity:

Electrolytic capacitors ($+/-$) tend to have a high leakage current when incorrectly connected, so even if they do not explode, they can affect circuit bias conditions.

i.e., to overcome this problem the capacitor positive terminal must be connected to the more positive of the two circuit points where the capacitor is installed.



iii) Emitter Bypass Capacitor (C_E): It is placed parallel with R_E to provide a low reactance path to the amplified a.c. signal. If it is not placed, the amplified a.c. signal passing through R_E will cause a voltage drop across it. This will reduce the output voltage, reducing the gain of amplifier.

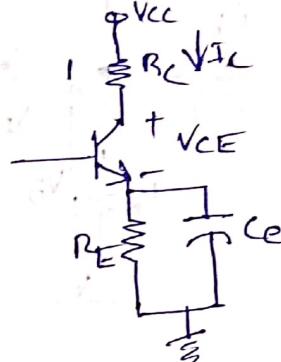


$$V_{CC} = I_c R_C + V_{CE} + I_E R_E$$

$$I_c R_C = V_{CC} - V_{CE} - I_E R_E$$

As $I_E R_E \uparrow$ $I_c R_C \downarrow$

\therefore Voltage gain decreases.



$$V_{CC} = I_c R_C + V_{CE} + I_E [R_E || X_{CE}]$$

$$I_c R_C = V_{CC} - V_{CE} - I_E \left[\frac{R_E}{(I_E R_E) + R_E} \right]$$

As $I_E [R_E || X_{CE}] \downarrow$ $I_c R_C \uparrow$
 \therefore Voltage gain increases.

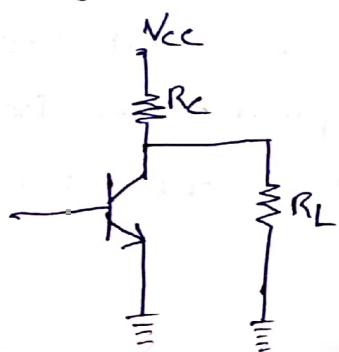
iv) Coupling capacitor (C_C):

This capacitor couples the output of the amplifier to the load or to the next stage of the amplifier. It blocks d.c. and passes only a.c. part of amplified signal.

If it is connected then R_L is directly coupled to the circuit output and the collector supply voltage is reduced from V_{CC} to $\frac{V_{CC} R_L}{R_C + R_L}$ and collector resistance becomes $(R_C || R_L)$.

This affects the circuit d.c. loadline and Q-point.

If capacitor C_C is kept then it passes a.c. output waveform to the load without affecting the circuit bias conditions.



COMMON COLLECTOR AMPLIFIER CIRCUIT

26

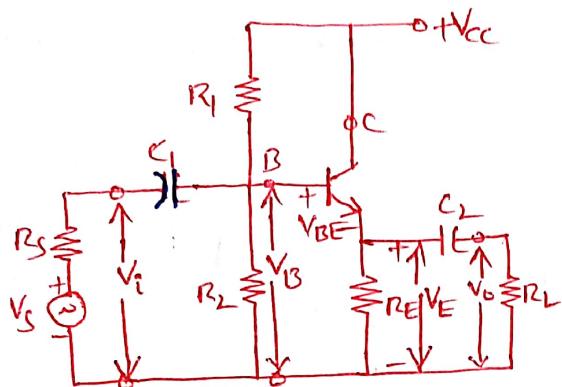


Figure shows common collector circuit. The DC biasing is provided by R_1, R_2 and R_E . From the fig:

$$V_B = V_{BE} + V_E$$

$$\therefore V_E = V_B - V_{BE}$$

consider V_{BE} fairly constant, variation in V_B occurs at Emitter and Emitter voltage V_E will vary same as base voltage, V_B . In CC circuit Emitter terminal follows the signal voltage applied to the Base. Hence CC circuit is also called as "EMITTER FOLLOWER".

I H-parameter representation of a Transistor?

TWO-PORT NETWORK:



If current i_1 & voltage V_2 are independent and if the two-port is linear, we have

$$V_1 = h_{11} i_1 + h_{12} V_2$$

$$i_2 = h_{21} i_1 + h_{22} V_2$$

The quantities $h_{11}, h_{12}, h_{21}, h_{22}$ are called the 'H or hybrid' parameters because they are not all alike dimensionally.

The h -parameters are defined as follows:

$$h_{11} = \frac{V_1}{I_1} \Big| V_2=0 = \text{input resistance with output short-circuited. (ohms)}$$

$$h_{12} = \frac{V_1}{V_2} \Big| I_1=0 = \text{reverse-open circuit voltage amplification (dimensionless)}$$

$$h_{21} = \frac{i_2}{V_1} \Big| V_2=0 = \text{current gain with output short-circuited. (dimensionless)}$$

$$h_{22} = \frac{i_2}{V_2} \Big| I_1=0 = \text{output conductance with input open-circuited (mhos)}$$

IEEE standards for notation:-

$i=11$ = input ; $o=22$ = output

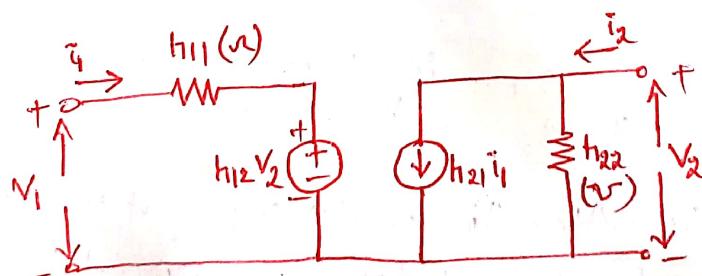
$f=21$ = forward transfer ; $\delta=12$ = reverse transfer

In case of transistors:-

$h_{Tb} = h_{11b}$ = input resistance in common-Base configuration

$h_{fe} = h_{21e}$ = short-circuit forward current gain in CE circuit.

Hybrid Model :-



Applying KVL and KCL for input and output ports we have,

$$V_1 = h_{11}i_1 + h_{12}V_2.$$

$$i_2V_2 = h_{21}i_1 + h_{22}V_2.$$

Transistor Hybrid Model:

- The h-parameters are:
- i) Real numbers at audio frequencies
 - ii) Easy to measure
 - iii) Can also be obtained from the transistor static characteristic curves
 - iv) Convenient to use in circuit analysis and design.

i) Common-Emitter connection:

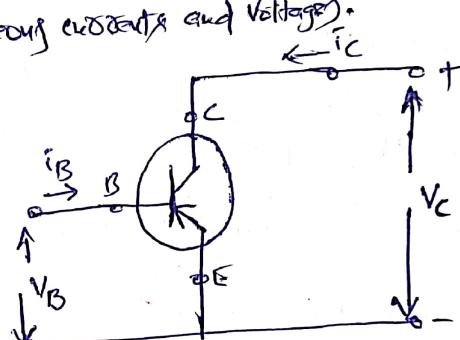
i_B, i_C, V_B, V_C represent total instantaneous currents and voltages.

V_B is a function f_1 of i_B and V_C &

i_C is another function f_2 of i_B and V_C .

$$\therefore V_B = f_1(i_B, V_C) \rightarrow ①$$

$$i_C = f_2(i_B, V_C) \rightarrow ②$$



Making Taylor's series expansion of ① & ② around the quiescent point I_B, V_C and neglecting higher-order terms, we obtain

$$\Delta V_B = \left. \frac{\partial f_1}{\partial i_B} \right|_{V_C=\text{const}} \Delta i_B + \left. \frac{\partial f_1}{\partial V_C} \right|_{I_B=\text{const}} \Delta V_C$$

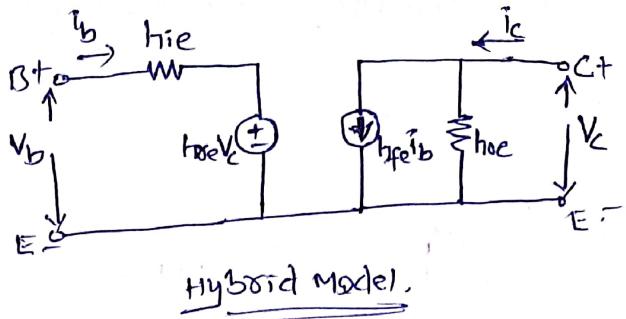
$$\Delta i_C = \left. \frac{\partial f_2}{\partial i_B} \right|_{V_C=\text{const}} \Delta i_B + \left. \frac{\partial f_2}{\partial V_C} \right|_{I_B=\text{const}} \Delta V_C$$

The quantities ΔV_B , ΔV_C , Δi_B and Δi_C represent the small-signal incremental base and collector voltages and currents. We may represent them with the symbols v_b , v_c , i_b and i_c .

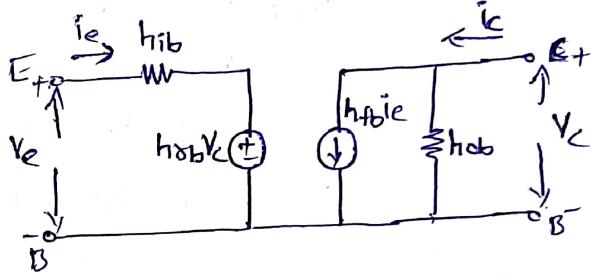
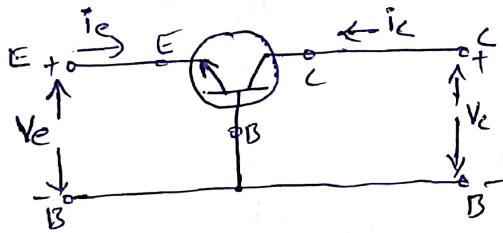
Now ① & ② can be written as: v_b vs i_b :

$$V_b = h_{ie} i_b + h_{oe} V_c$$

$$i_c = h_{fe} i_b + h_{oe} V_c$$



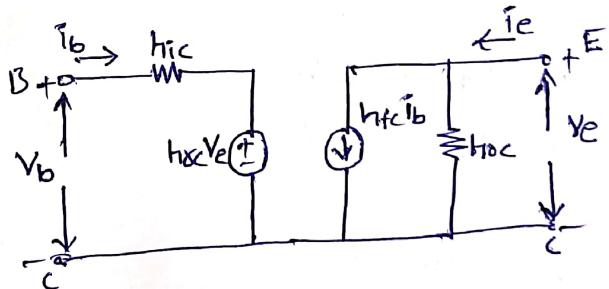
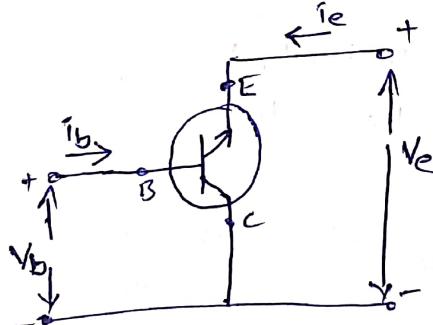
i) Common-Base connection:



$$V_e = h_{ib} i_e + h_{ob} V_c$$

$$i_c = h_{fb} i_e + h_{ob} V_c$$

ii) Common-Collector connection:



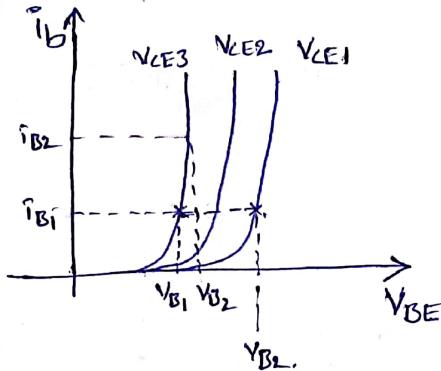
$$V_b = h_{ic} i_b + h_{oc} V_e$$

$$i_e = h_{fc} i_b + h_{oc} V_e$$

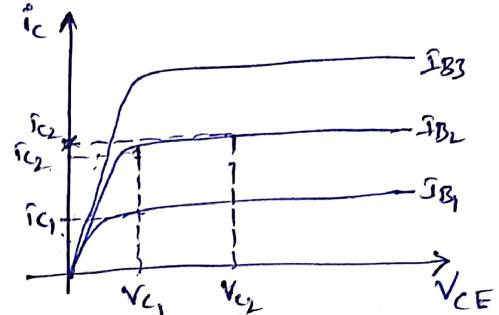
Determination of H-parameters from the characteristics

CE characteristics

Input:



Output:



$$V_B = h_{fe} i_B + h_{oe} V_C$$

$$i_C = h_{fe} i_B + h_{oe} V_C$$

$$h_{fe} = \frac{\Delta V_B}{\Delta i_B} = \frac{V_{B2} - V_{B1}}{i_{B2} - i_{B1}}$$

$$h_{oe} = \frac{\Delta V_B}{\Delta V_C} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$$

$$h_{fe} = \frac{\Delta i_C}{\Delta i_B} = \frac{i_{C2} - i_{C1}}{i_{B2} - i_{B1}}$$

$$h_{oe} = \frac{\Delta i_C}{\Delta V_C} = \frac{i_{C2} - i_{C1}}{V_{C2} - V_{C1}}$$

CB characteristics

$$V_e = h_{fb} i_e + h_{ob} V_C$$

$$i_C = h_{fb} i_e + h_{ob} V_C$$

Input:

$$h_{fb} = \frac{\Delta V_e}{\Delta i_e} = \frac{V_{e2} - V_{e1}}{i_{e2} - i_{e1}}$$

$$h_{ob} = \frac{\Delta V_e}{\Delta V_C} = \frac{V_{e2} - V_{e1}}{V_{C2} - V_{C1}}$$

Output:

$$h_{fb} = \frac{\Delta i_C}{\Delta i_e} = \frac{i_{C2} - i_{C1}}{i_{e2} - i_{e1}}$$

$$h_{ob} = \frac{\Delta i_C}{\Delta V_C} = \frac{i_{C2} - i_{C1}}{V_{C2} - V_{C1}}$$

CC characteristics

$$V_B = h_{ic} i_B + h_{oc} V_C$$

$$i_C = h_{ic} i_B + h_{oc} V_C$$

Input:

$$h_{ic} = \frac{\Delta V_B}{\Delta i_B} = \frac{V_{B2} - V_{B1}}{i_{B2} - i_{B1}}$$

$$h_{oc} = \frac{\Delta V_B}{\Delta V_C} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$$

Output:

$$h_{fIC} = \frac{\Delta i_C}{\Delta i_B} = \frac{i_{C2} - i_{C1}}{i_{B2} - i_{B1}}$$

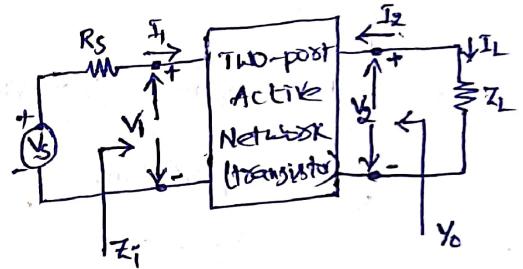
$$h_{oc} = \frac{\Delta i_C}{\Delta V_C} = \frac{i_{C2} - i_{C1}}{V_{C2} - V_{C1}}$$

Typical h-parameter Values for Transistor

	<u>CE</u>	<u>CB</u>	<u>CC</u>
$h_{11} = h_T$	1100Ω	21.6Ω	1100Ω
$h_{12} = h_\delta$	2.5×10^{-4}	2.9×10^{-4}	≈ 1
$h_{21} = h_f$	50	-0.98	-51
$h_{22} = h_o$	$25\mu\text{A/V}$	0.49 mA/V	$25\mu\text{A/V}$
$\frac{1}{h_{22}} = \frac{1}{h_o}$	40K	2.04 M	40K

Analysis of a Transistor Amplifier circuit using h-parameters

To form a transistor Amplifier it is only necessary to connect an external load and signal source as indicated in fig. and to bias the transistor properly.



Basic Amplifier Circuit

Current Gain (or) Current Amplification (A_I)

$$A_I = \frac{\text{O/p current}}{\text{i/p current}}$$

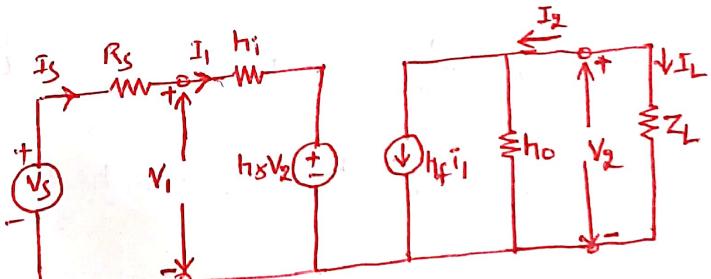
$$= \frac{I_L}{I_1} = \frac{-I_2}{I_1} \quad (\because I_L = -I_2)$$

We have $I_2 = h_T I_1 + h_o V_2$

$$= h_f I_1 + h_o (-I_2 Z_L) \quad [\because V_2 = I_2 Z_L = -I_2 Z_L]$$

$$I_2 + h_o I_2 Z_L = h_f I_1$$

$$I_2 [1 + h_o Z_L] = h_f I_1 \Rightarrow \frac{I_L}{I_1} = \frac{h_f}{1 + h_o Z_L}$$



Small Signal Analysis

$$A_I = \frac{-h_f}{1 + h_o Z_L}$$

2) Input Impedance (Z_i):

$$Z_i = \frac{V_1}{I_1}$$

From input circuit we have $V_1 = h_T I_1 + h_{o2} V_2$

$$Z_i = \frac{h_T I_1 + h_{o2} V_2}{I_1}$$

$$= h_T + \frac{h_{o2} V_2}{I_1}$$

$$\left[\because V_2 = -I_2 Z_L = -\frac{I_2}{I_1} I_1 Z_L = A_I I_1 Z_L \right]$$

$$= h_T + h_{o2} \cdot A_I Z_L$$

$$= h_T + h_{o2} \cdot A_I Z_L$$

$$Z_i = h_T - \frac{h_{o2} h_T Z_L}{1 + h_{o2} Z_L}$$

$$\Rightarrow Z_i = h_T - \frac{h_T h_{o2}}{Z_L + h_{o2}}$$

3) Voltage Gain (or) Voltage Amplification (A_V):

$$A_V = \frac{\text{Op Voltage}}{\text{Input Voltage}} = \frac{V_2}{V_1} = \frac{A_I I_1 Z_L}{V_1} = \frac{A_I Z_L}{Z_i}$$

$$A_V = \frac{A_I Z_L}{Z_i}$$

4) Output Admittance (Y_o): [Voltage source is shorted and current source is opened]

$$Y_o = \frac{I_2}{V_2} \quad \text{with } V_S = 0. \quad \left[\because I_2 = h_T I_1 + h_{o2} V_2 \right]$$

$$Y_o = \frac{h_T I_1 + h_{o2} V_2}{V_2} = h_{o2} + \frac{h_T I_1}{V_2}$$

From the figure: with $V_S = 0$; $R_S I_1 + h_T I_1 + h_{o2} V_2 = 0 \Rightarrow \frac{I_1}{V_2} = \frac{-h_{o2}}{h_T + R_S}$.

$$\therefore Y_o = h_{o2} + \frac{-h_T h_{o2}}{h_T + R_S}$$

$$\therefore Y_o = h_{o2} - \frac{h_T h_{o2}}{h_T + R_S}$$

5) Voltage Amplification (A_{VS}) (taking into source resistance R_S of source):

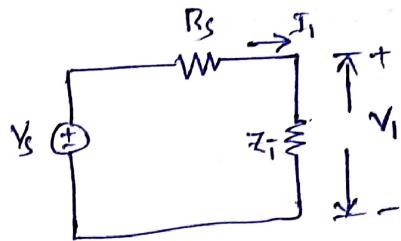
$$A_{VS} = \frac{V_2}{V_S}$$

$$= \frac{V_2}{V_1} \times \frac{V_1}{V_S}$$

$$= A_V \cdot \frac{V_1}{V_S}$$

$$= A_V \cdot \frac{V_S Z_i}{V_S (Z_i + R_S)}$$

$$A_{VS} = \frac{A_V Z_i}{Z_i + R_S}$$



$$-V_S + R_S I_1 + Z_i I_1 = 0$$

$$I_1 = \frac{V_S}{(R_S + Z_i)}$$

$$\therefore V_1 = I_1 Z_i = \frac{V_S Z_i}{Z_i + R_S}$$

If $R_S = 0$; then $A_{VS} = A_V$

Where A_V is voltage gain for an ideal voltage source.

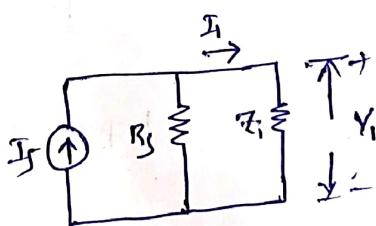
6) Current Amplification (A_{IS}) (taking into account source resistance, R_S):

$$A_{IS} = \frac{I_L}{I_S}$$

$$= -\frac{I_2}{I_S} = -\frac{I_2}{I_1} \times \frac{I_1}{I_S} = A_I \cdot \frac{I_1}{I_S}$$

$$\therefore A_{IS} = \frac{A_I \cdot R_S \frac{I_S}{Z_i}}{\frac{I_S}{Z_i} (R_S + Z_i)}$$

$$\therefore A_{IS} = \frac{A_I R_S}{R_S + Z_i}$$



$$I_1 = \frac{R_S I_S}{R_S + Z_i}$$

If $R_S = \infty$; then $A_{IS} = A_I$

Where A_I is current gain for an ideal current source.

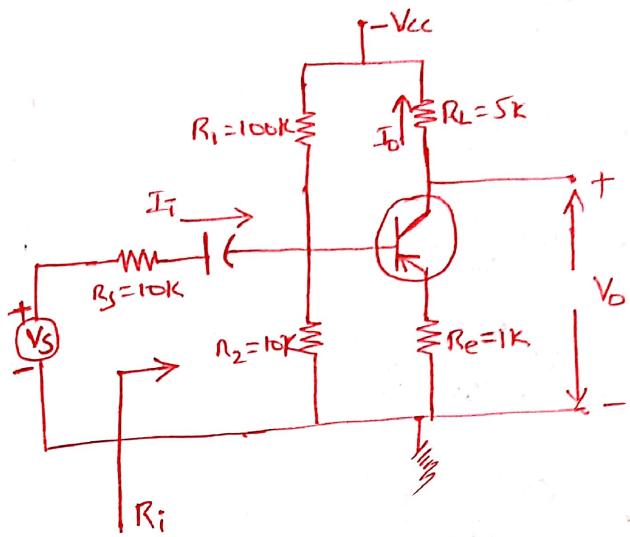
Where

7) Power Gain (A_P):

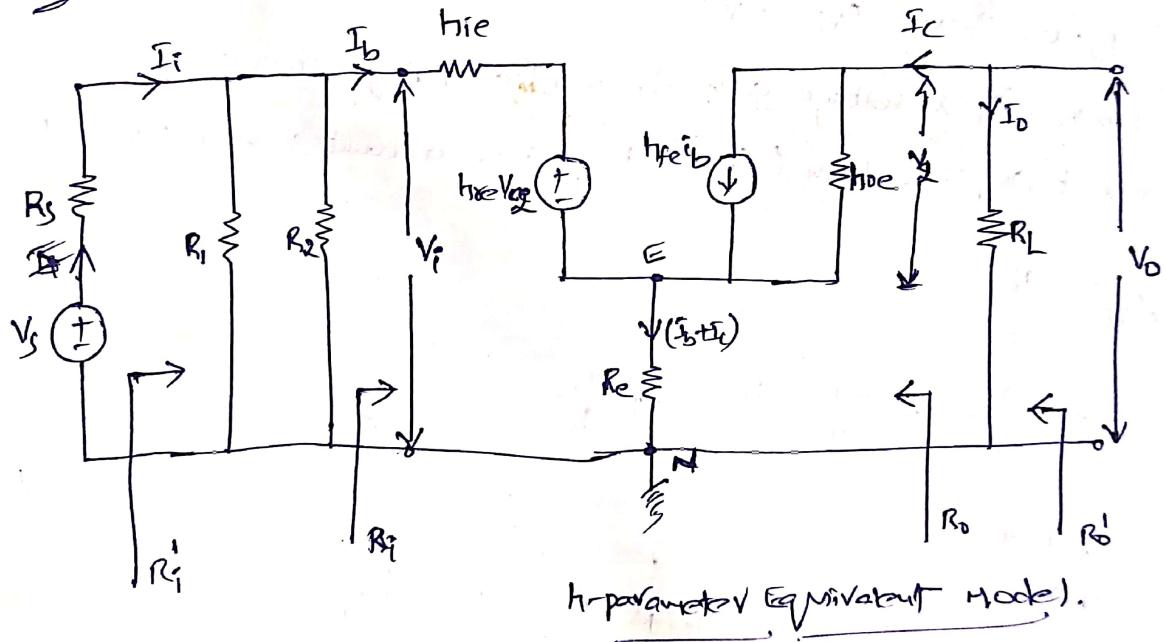
$$A_P = \frac{P_2}{P_1} = \frac{-V_2 I_2}{V_1 I_1} = A_V \cdot A_I = \frac{A_I I_L \cdot A_I}{Z_i Z_i} \Rightarrow$$

$$A_P = \frac{A_I^2 \cdot Z_L}{Z_i}$$

(P) For the Transistor Amplifier shown below, compute $A_I = \frac{I_o}{I_i}$, A_V , A_{VS} and R_I . Assume $h_{ie} = 1100\Omega$, $h_{fe} = 50$, $h_{oe} = 2.5 \times 10^4$, $h_{re} = 24 \text{ mA/V}$.



Sol:



h-parameter Equivalent Model.

$$c) \underline{\text{Current Gain}} \quad A_I = \frac{I_o}{I_i} = \frac{-I_c}{I_b}$$

From fig: $\dot{I}_c = h_{fe} i_b + h_{oe} V_2$

$$\dot{I}_c = h_{fe} i_b + h_{oe} (-\dot{I}_c R_L - R_E (i_b + \dot{I}_c))$$

$$\therefore \dot{I}_c [1 + h_{oe}(R_L + R_E)] = h_{fe} i_b - h_{oe} R_E i_b \\ = i_b (h_{fe} - h_{oe} R_E)$$

From output loop we have:

$$V_o = V_2 + R_E (i_b + \dot{I}_c)$$

$$I_o R_L = V_2 + R_E (i_b + \dot{I}_c)$$

$$-\dot{I}_c R_L = V_2 + R_E (i_b + \dot{I}_c)$$

$$-V_2 = -\dot{I}_c R_L - R_E (i_b + \dot{I}_c)$$

$$\therefore i_c [1 + h_{oe}(R_L + R_E)] = i_b (h_{fe} - h_{oe} R_E)$$

$$\frac{i_c}{i_b} = \frac{h_{fe} - h_{oe} R_E}{1 + h_{oe} (R_L + R_E)}$$

$$\therefore A_I = \frac{-i_c}{i_b} = \frac{-(h_{fe} - h_{oe} R_E)}{1 + h_{oe} (R_L + R_E)} \Rightarrow A_I = \frac{-h_{fe} + h_{oe} R_E}{1 + h_{oe} (R_L + R_E)}$$

$$\therefore A_I = \frac{-50 + 25 \times 10^6 \times 1k}{1 + 25 \times 10^6 (5k + 1k)} = -43.45.$$

b) Input Resistance $R_i = \frac{V_i}{i_b}$

$$\therefore V_i = h_{ie} i_b + h_{oe} V_2 + R_e (i_b + i_c)$$

$$= i_b [h_{ie} + R_e + R_e \frac{i_c}{i_b} + \frac{h_{oe} V_2}{i_b}]$$

$$R_i = \frac{V_i}{i_b} = h_{ie} + R_e - R_e A_I + \frac{h_{oe} V_2}{i_b}$$

$$\begin{aligned} R_i &= h_{ie} + R_e (1 - A_I) + \frac{h_{oe}}{i_b} [-i_c R_L - R_e (i_b + i_c)] \\ &= h_{ie} + R_e (1 - A_I) + h_{oe} A_I R_L - h_{oe} R_e (1 + \frac{i_c}{i_b}) \end{aligned}$$

$$R_i = h_{ie} + R_e (1 - A_I) + h_{oe} A_I R_L + h_{oe} R_e (A_I - 1)$$

$$R_i = 1100 + 1k (1 + 43.45) + 2.5 \times 10^{-4} (-43.45) 5k + 2.5 \times 10^{-4} \times 1k (-43.45 - 1)$$

$$\therefore R_i = 45.48 \text{ k}\Omega.$$

$$R_T' = R_T \parallel R_1 \parallel R_2$$

$$= 45.48K \parallel 100K \parallel 10K = 7.576K\Omega.$$

c) Voltage Gain, A_V :- (without R_S)

$$A_V = \frac{V_o}{V_i}$$

$$= \frac{V_o}{I_b} \times \frac{I_b}{V_i} = \frac{V_o}{I_b \times R_T'} = \frac{I_o R_L}{I_b \times R_T'} \Rightarrow \boxed{\frac{A_I R_L}{R_T'} = A_V}$$

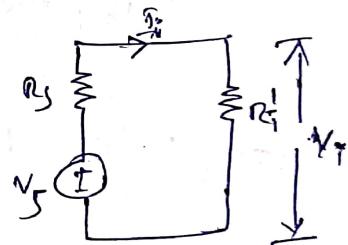
$$\therefore A_V = \frac{-43.45 \times 5K}{45.48K} = -4.77.$$

d) Overall Voltage Gain A_{VS} :- (taking R_S)

$$A_{VS} = \frac{V_o}{V_S}$$

$$= \frac{V_o}{V_i} \times \frac{V_i}{V_S} = A_V \cdot \frac{V_i}{V_S}$$

$$\boxed{A_{VS} = A_V \cdot \frac{R_S'}{R_S + R_T'}}$$



$$\therefore V_S = R_S I_S + I_S R_S'$$

$$V_S = I_S (R_S + R_S')$$

$$\therefore A_{VS} = -4.77 \times \frac{7.576K}{10K + 7.576K}$$

$$\boxed{A_{VS} = -2.056}$$

$$V_S = \frac{V_i}{R_T'} [R_S + R_S']$$

$$\boxed{\frac{V_P}{V_S} = \frac{R_S'}{R_S + R_S'}}$$

c) overall current gain (A_{IS}) (taking R_S)

$$A_{IS} = \frac{I_o}{I_s}$$

$$= \frac{I_o}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_i}$$

$$= \frac{-I_c}{I_c} \times 43.45 \times \frac{I_b}{I_i}$$

$$\left[\because I_o = -I_c \quad \& \quad A_I = -\frac{I_c}{I_b} \right]$$

$$\frac{I_c}{I_b} = 43.45$$

From fig: $I_b = \frac{I_s R_B}{R_B + R_I}$

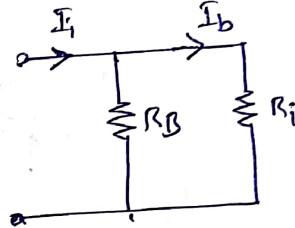
$$\frac{I_b}{I_s} = \frac{R_B}{R_B + R_I}$$

$$= \frac{100k/11}{100k+110k} = \frac{100k \cdot 11}{110k}$$

$$= \frac{100k \cdot 11}{110k}$$

$$= \frac{100k}{10}$$

$$\frac{I_b}{I_s} = 0.1666$$



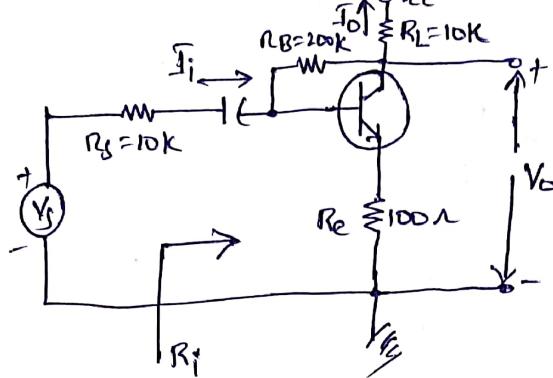
$$R_B = R_1 || R_2 = 100k \cdot 110k$$

$$\therefore A_{IS} = -1 \times 43.45 \times 0.1666 = \underline{\underline{-7.24}}$$

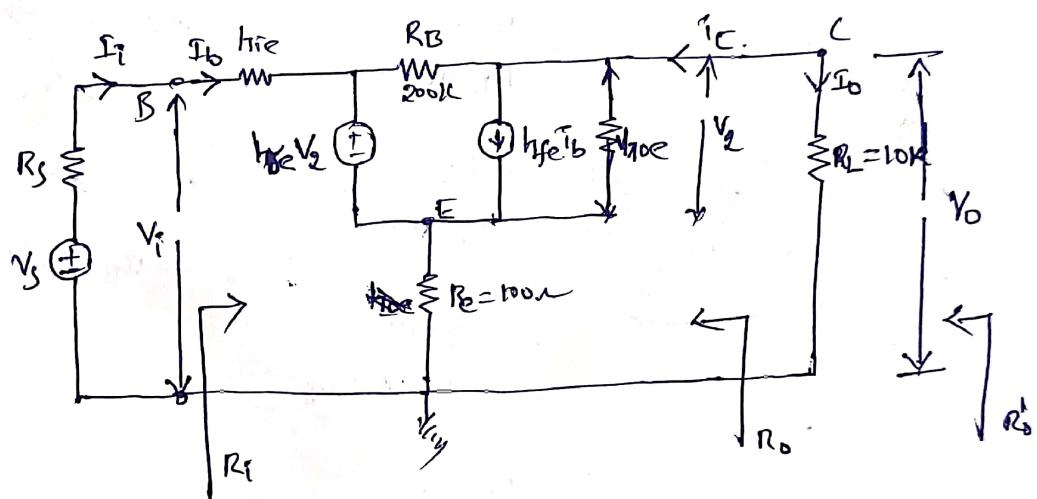
f) output resistance (r_o):

$$r_o = \frac{V_o}{I_o}$$

(P2) For the transistor amplifier shown below, compute $A_I = \frac{I_o}{I_s}$, A_V , A_{VS} , and R_i . Assume $h_{RE} = 1100\Omega$, $h_{FE} = 50$, $h_{RO} = 2.5 \times 10^{-4}$, $h_{OE} = 29(\text{mA})/\text{V}$.

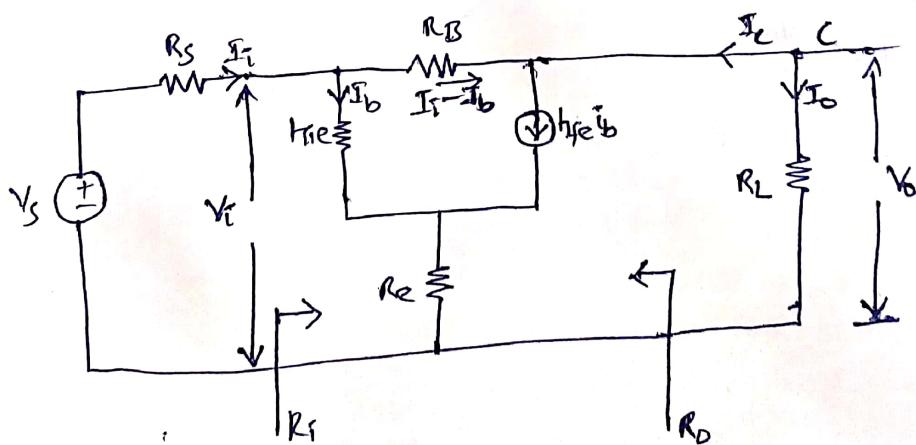


Sol:



to calculate A_I : $A_I = \frac{I_o}{I_s}$

neglecting h_{RE} and h_{RO} and draw equivalent model

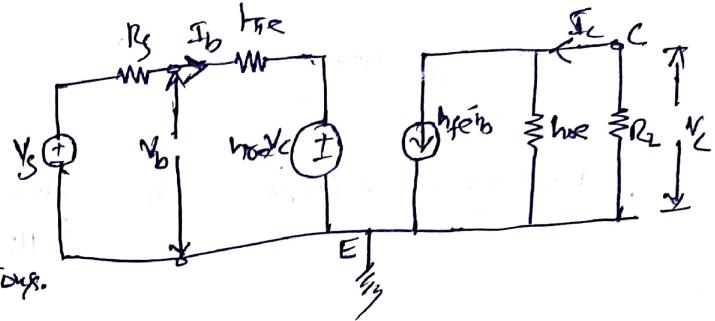


(approximate)

Analysis of Transistor Amplifier circuit using Simplified Hybrid Model

i) CE circuit Analysis:

- It is necessary to calculate approximate values of A_I , A_V , R_i , R_o & A_p rather than to carryout exact lengthy calculations.



- $\frac{1}{h_{oe}} \parallel R_L$ if $\frac{1}{h_{oe}} \gg R_L$ then

$$\frac{\frac{1}{h_{oe}} \times R_L}{\frac{1}{h_{oe}} + R_L} = R_L \text{ then } h_{oe} \text{ is neglected provided } h_{oe} \cdot R_L \ll 1.$$

\therefore neglecting h_{oe} ; $I_C = h_{fe}I_b$.

$$- |h_{oe}V_{ce}| = h_{oe}I_C R_L$$

$$= h_{oe} \cdot h_{fe}I_b R_L$$

since $h_{oe}h_{fe} \approx 0.01$ this voltage is neglected compared with $h_{fe}I_b$.

\therefore if R_L is small; neglecting h_{oe} and h_{ie} in the circuit.

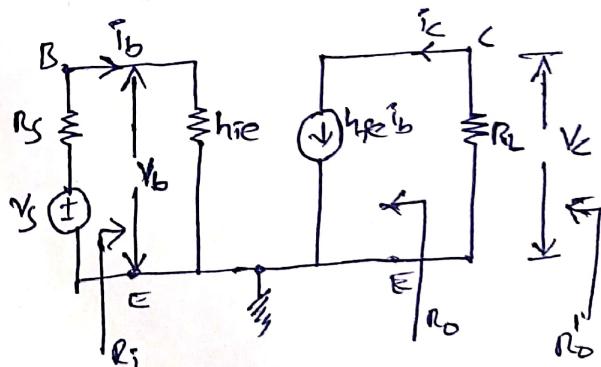
Approximate CE Model:

i) Current Gain (A_I)

$$A_I = \frac{-h_{fe}}{1 + h_{oe}R_L}$$

h_{oe} is neglected for approximation

$\therefore A_I = -h_{fe}$



ii) Input Resistance (R_i):

$$R_i = h_{ie} + h_{oe} A R_L$$

h_{oe} is neglected

$$\therefore R_i = h_{ie}$$

iii) Voltage Gain, (A_V):

$$A_V = \frac{A I R_L}{R_i} \Rightarrow \frac{-h_{fe} \times R_L}{h_{ie}} = A_V$$

iv) Output Impedance (r_o):

$$r_o = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} h_{re}}$$

neglecting h_{oe} & h_{re}

$$\therefore r_o = 0$$

$$\therefore R_o = 1/r_o = \infty$$

open circuit \rightarrow current source ($h_{fe} i_b$)

short circuit \rightarrow voltage source (V_o)

$$R_o' = R_o || R_L$$

$$= \frac{R_o \cdot R_L}{R_o + R_L} = R_L$$

$$\boxed{R_o' = R_L}$$

i) CB Simplified Model

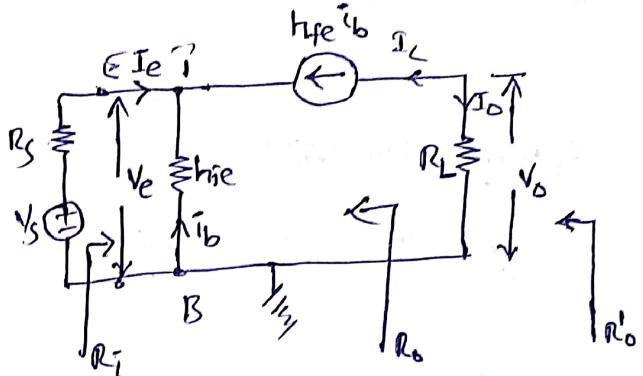
i) Current Gain (A_I)

$$A_I = \frac{I_D}{I_e} = -\frac{I_L}{I_e}$$

$$= \frac{h_{fe} i_b}{i_b(1+h_{fe})}$$

$$\therefore A_I = \frac{h_{fe}}{1+h_{fe}}$$

$\therefore A_I < 1$.



Apply KCL at 'i' we have

$$i_e + i_b + h_{fe}i_b = 0$$

$$i_e + i_b(1+h_{fe}) = 0 \Rightarrow i_e = -i_b(1+h_{fe})$$

ii) Input Resistance (R_i)

$$R_i = \frac{V_e}{i_e} = \frac{h_{fe} i_b}{i_b(1+h_{fe})}$$

$$\Rightarrow R_i = \frac{h_{fe}}{1+h_{fe}}$$

R_i is low compared to CE & CC.

iii) Voltage Gain, (A_V)

$$A_V = \frac{V_o}{V_e} = \frac{I_D R_L}{I_e R_i} = \frac{A_I R_L}{R_i} = \frac{\frac{h_{fe}}{1+h_{fe}} R_L}{\frac{h_{fe}}{1+h_{fe}}} = R_L$$

$$\Rightarrow A_V = \frac{h_{fe} R_L}{h_{fe}}$$

iv) Output Resistance, (R_o)

open circuit current source $h_{fe}i_b = 0$; $i_c = 0$.

$$R_o = \frac{V_o}{I_o}$$

$$= \frac{V_o}{-I_L} = \frac{V_o}{0} = \infty \quad \therefore R_o = \infty$$

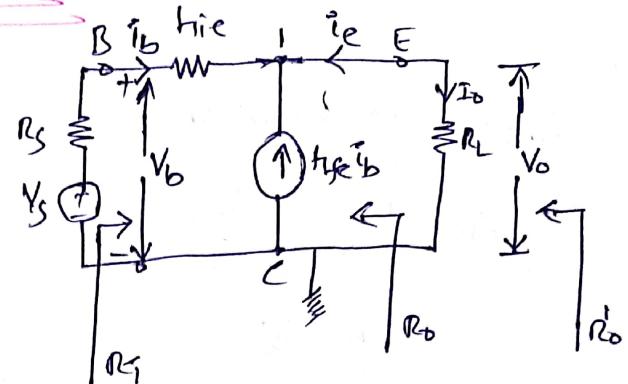
$$R'_o = R_o || R_L \Rightarrow R'_o = R_L$$

iii) CC Simplified Hybrid Model :

i) Current Gain, (A_I) :

$$A_I = \frac{I_o}{I_b} = -\frac{i_e}{i_b} = +\frac{i_b(1+h_{fe})}{i_b}$$

$$\therefore A_I = 1+h_{fe}.$$



at Node 'E' $i_e = -i_b(1+h_{fe}).$

ii) Input Resistance (R_i) :

$$R_i = \frac{V_b}{i_b}$$

Apply KVL to outer loop we have

$$V_b = h_{ie}i_b + I_o R_L$$

$$+i_b \left[h_{fe} + \frac{I_o}{i_b} R_L \right]$$

$$\frac{V_b}{i_b} = h_{ie} + A_I R_L = h_{ie} + (1+h_{fe}) R_L.$$

iii) Voltage Gain, (A_V) :

$$A_V = \frac{V_o}{V_b} = \frac{I_o R_L}{i_b R_i} = \frac{A_I R_L}{R_i} = \frac{(1+h_{fe}) R_L}{h_{ie} + (1+h_{fe}) R_L}$$

$$\therefore A_V = \frac{(1+h_{fe}) R_L}{(1+h_{fe}) R_L} \approx 1.$$

$$\because (1+h_{fe}) R_L \gg h_{ie}.$$

but it is always less than unity.

iv) Output Resistance, (R_o) :

$$R_o = \frac{V_o}{i_e}$$

short circuit - voltage source ($V_s = 0$)
open circuit - current source ($h_{fe}i_b$)

Applying KVL :

$$V_s = i_b R_i + h_{fe} i_b + V_o.$$

$$V_o = i_b [R_i + h_{ie}] \quad \& \quad i_e = -i_b (1+h_{fe}).$$

$$\therefore R_o = \frac{-i_b (R_i + h_{ie})}{-i_b (1+h_{fe})}$$

$$\therefore R_o = \frac{R_i + h_{ie}}{1+h_{fe}}$$

&

$$R_o' = R_o || R_L,$$

(P) The Transistor of figure shown is connected as a common emitter amplifier, and the h-parameters are given in table. If $R_L = R_S = 1000\Omega$, find the gains A_I , A_{IS} , A_V , A_{VS} and input and output Z_i , Z_o impedances and power gain A_P .

~~Ques~~

$$A_I = \frac{-h_{FE}}{1 + h_{OE}R_L} = \frac{-50}{1 + 2.5 \times 10^6 \times 10^3} = -48.8$$

$$R_I = h_{IE} + h_{RE} A_I R_L = 1100 + 2.5 \times 10^{-4} \times 48.8 \times 10^3 = 1088\Omega$$

$$A_V = \frac{A_I R_L}{R_I} = \frac{-48.8 \times 10^3}{1088 \times 10^3} = -44.8$$

$$A_{VS} = \frac{A_V R_I}{R_I + R_S} = -44.8 \times \frac{1088}{2108} = -23.3$$

$$A_{IS} = \frac{A_I R_S}{R_I + R_S} = \frac{-48.8 \times 10^3}{2108} = -23.3$$

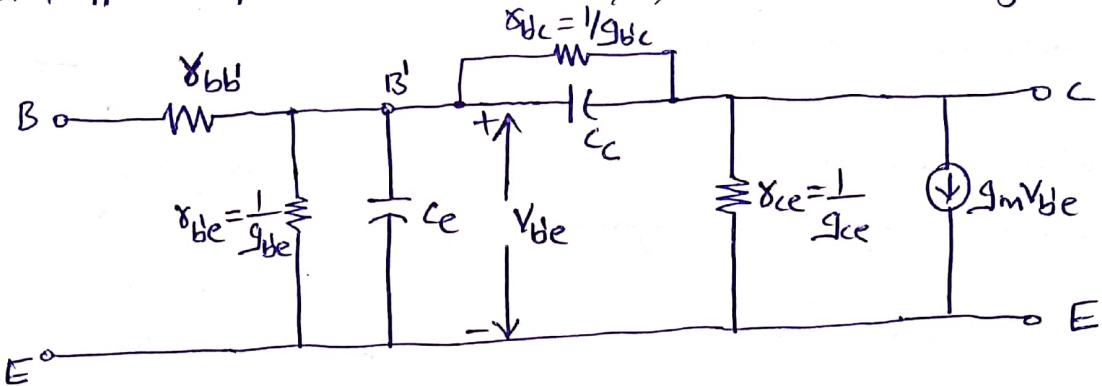
$$Y_o = h_{OE} - \frac{h_{FE} h_{RE}}{h_{IE} + R_S} = 2.5 \times 10^{-6} - \frac{50 \times 2.5 \times 10^{-4}}{2108} = 19 \times 10^{-6} \text{ mho}$$

$$Z_o = 1/Y_o = 52.6 \text{ k}\Omega$$

$$A_P = A_V \cdot A_I = 44.8 \times 48.8 = 2190.$$

The Hybrid- π (Π) Common Emitter Transistor Model:

Hybrid- Π or Giacobello model is shown in below figure.



γ_{BB} — The ohmic base-spreading resistance between actual base B and Virtual Base B' .

$g_m V_{BE}$ — For small changes in voltage V_{BE} across the emitter junction, the excess minority-carrier concentration injected into base is proportional to V_{BE} and results in small signal collected current and accounts for current generated $g_m V_{BE}$.

$g_{BE} = \frac{1}{\gamma_{BE}}$ — Increase in minority carriers in Base increases base current and this effect is taken by inserting g_{BE} between B' and E.

C_e — Diffusion capacitance accounts for storage of excess minority carriers in the base.

$g_{BC} = \frac{1}{\gamma_{BC}}$ — feedback between output and input is taken with g_{BC} .

$\gamma_{CE} = 1/g_{CE}$ — conductance between collector and Emitter.

Typical values of Hybrid- Π parameters at room temperature are!

$$g_m = 50 \text{ mA/V} \quad \gamma_{BB} = 100 \Omega \quad \gamma_{BE} = 1 \text{ k}\Omega \quad \gamma_{BC} = 4 \text{ M}\Omega$$

$$\gamma_{CE} = 80 \text{ k}\Omega \quad C_L = 3 \text{ pF} \quad C_e = 100 \text{ pF}$$

The Hybrid- π Model :-

i) Transistor Transconductance (g_m):

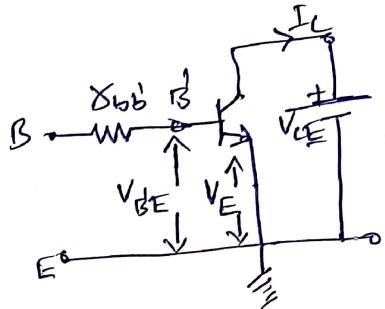
In Active Region, the collector current is given by

$$I_C = \alpha I_E + I_{CEO} \quad \rightarrow ①$$

From the circuit, $I_L = g_m V_{BE}$

$$g_m = \frac{I_L}{V_{BE}}$$

$$g_m = \frac{\partial I_L}{\partial V_{BE}}$$



part(i) differentiating equation ① with respect to V_{BE} , we get

$$\frac{\partial I_C}{\partial V_{BE}} = \alpha \frac{\partial I_E}{\partial V_{BE}} + \text{d}$$

$$g_m = \alpha \cdot \frac{\partial I_E}{\partial V_E}$$

$\because V_{BE} = V_E$ from the circuit

$$g_m = \alpha \cdot r_e$$

$\therefore r_e = \frac{\partial I_E}{\partial V_E}$ - dynamic resistance

$$g_m = \frac{\alpha I_E}{V_T}$$

$$r_e = \frac{V_T}{I_E} = \frac{V_T}{\alpha I_E} \quad (\alpha=1).$$

$$g_m = \frac{I_C - I_{CEO}}{V_T}$$

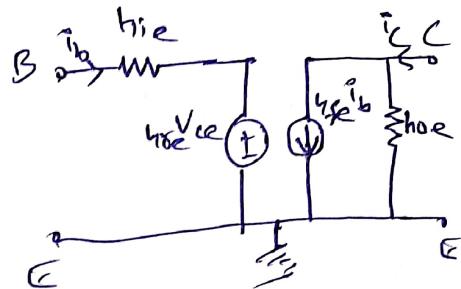
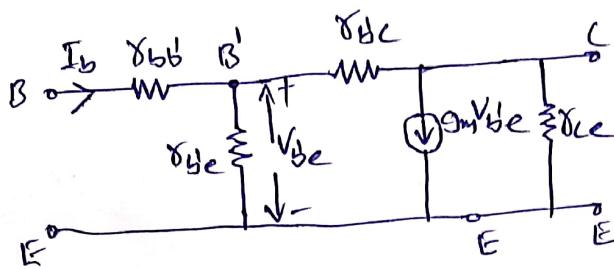
{ From equation ① }

$$g_m = \frac{|I_L|}{V_T}$$

$\because I_C \gg I_{CEO}$

$\therefore g_m$ is directly proportional to current and inversely proportional to temperature.

i) Input Resistance at Emitter (γ_{be}):



We know that, $I_c = g_m V_{be}$

$$I_c = g_m (\gamma_{be} i_b) \quad [\because \gamma_{fe} \gg \gamma_{be}]$$

i_b flows only
into γ_{be} .

$$\frac{I_c}{I_b} = g_m \gamma_{be}$$

$$\gamma_{fe} = g_m \gamma_{be} \quad [\because h_{fe} = \frac{I_c}{I_b}]$$

$$\therefore \boxed{\gamma_{be} = \frac{h_{fe}}{g_m}}$$

γ_{be} is directly proportional to temperature and inversely proportional to current.

ii) Input Resistance at Base (γ_{bb}):

Here V_{CE} output is shorted and $\gamma_{bc} \parallel \gamma_{be} \approx \gamma_{be}$.

$$\therefore \text{Input resistance} = \frac{V_{BE}}{I_b}$$

$$\text{But } V_{BE} = i_b \gamma_{bb} + i_b \gamma_{be}$$

$$V_{BE} = i_b (\gamma_{bb} + \gamma_{be})$$

$$\frac{V_{BE}}{I_b} = \gamma_{bb} + \gamma_{be} \quad [\because h_{ie} = \frac{V_{BE}}{I_b}]$$

$$h_{ie} = \gamma_{bb} + \gamma_{be}$$

$$\boxed{\gamma_{be} = h_{ie} - \gamma_{bb}}$$

iv) Voltage Gain (h_{re}):

With input open circuited ($i_{b}=0$), h_{re} is defined as

$$h_{re} = \frac{V_{be}}{V_{ce}} \quad \left[\text{from } V_{be} = h_{re} i_b + h_{re} V_{ce} \right]$$

$$h_{re} = \frac{\gamma_{be} \gamma_c}{(\gamma_{be} + \gamma_{bc}) \gamma_c} \quad \left[\because V_{be} = \gamma_{be} i_L \text{ & } V_{ce} = (\gamma_{ce} + \gamma_{bc}) i_L \right]$$

$$h_{re} = \frac{\gamma_{be}}{\gamma_{be} + \gamma_{bc}}$$

$$h_{re} (\gamma_{be} + \gamma_{bc}) = \gamma_{be}$$

$$h_{re} \gamma_{be} + h_{re} \gamma_{bc} = \gamma_{be}$$

$$h_{re} \gamma_{bc} = \gamma_{be} - h_{re} \gamma_{be}$$

$$h_{re} \gamma_{bc} = \gamma_{be} (1 - h_{re})$$

$$h_{re} \gamma_{bc} = \gamma_{be}$$

$$\left[\because h_{re} \approx 1 \Rightarrow h_{re} = 2.5 \times 10^{-4} \right]$$

$$\therefore h_{re} = \boxed{\frac{\gamma_{be}}{\gamma_{bc}}}.$$

FET AMPLIFIERS

FET amplifiers are divided into three categories: they are i) common source amplifier ii) common drain amplifier iii) common gate amplifier

ANALYSIS OF COMMON SOURCE (CS) AMPLIFIER

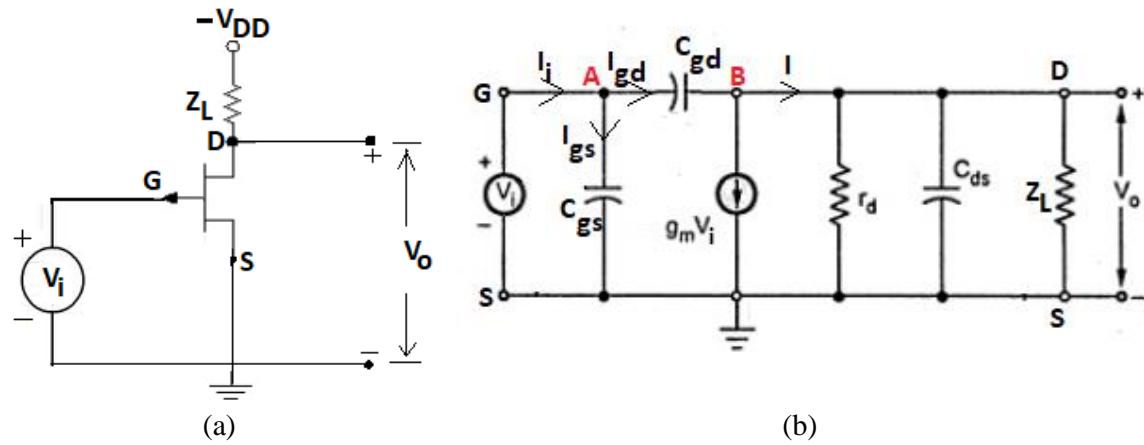


Fig.7.12: a) common source amplifier circuit b) small signal equivalent circuit

i) Voltage Gain (\$A_V\$):

$$A_V = \frac{\text{Output voltage}}{\text{Input voltage}} = \frac{V_o}{V_i}$$

From the fig.7.12 (b) the output voltage is given as

$$\begin{aligned} V_o &= I \times (r_d \parallel X_{C_{ds}} \parallel Z_L) \\ V_o &= I \times \frac{1}{\frac{1}{r_d} + \frac{1}{X_{C_{ds}}} + \frac{1}{Z_L}} \\ V_o &= \frac{I}{g_d + Y_{ds} + Y_L} \end{aligned} \quad (7.39)$$

$$\therefore g_d = \frac{1}{r_d} = \text{conductance of } r_d$$

$$\therefore Y_{ds} = \frac{1}{X_{C_{ds}}} = j\omega C_{ds} = \text{admittance of } C_{ds}$$

$$\therefore Y_L = \frac{1}{Z_L} = \text{admittance of } Z_L$$

To calculate current I in the circuit apply KCL at node 'B' we get

$$\begin{aligned} I + g_m V_i &= I_{gd} \\ I &= I_{gd} - g_m V_i \end{aligned} \quad (7.40)$$

I_{gd} is the current passing through gate-drain capacitance C_{gd} and it is given by

$$\begin{aligned} I_{gd} &= \frac{V_i - V_o}{X_{C_{gd}}} \\ I_{gd} &= Y_{gd}(V_i - V_o) \end{aligned} \quad (7.41)$$

Substituting I_{gd} in eq. (7.40), we get

$$I = Y_{gd}(V_i - V_o) - g_m V_i$$

$$I = V_i(Y_{gd} - g_m) - Y_{gd}V_o$$

Substituting current I in the eq. (7.39), we get

$$\begin{aligned} V_o &= \frac{V_i(Y_{gd} - g_m) - Y_{gd}V_o}{g_d + Y_{ds} + Y_L} \\ V_o &= \frac{V_i(Y_{gd} - g_m)}{g_d + Y_{ds} + Y_L} - \frac{Y_{gd}V_o}{g_d + Y_{ds} + Y_L} \\ V_o + \frac{Y_{gd}V_o}{g_d + Y_{ds} + Y_L} &= \frac{V_i(Y_{gd} - g_m)}{g_d + Y_{ds} + Y_L} \\ \frac{V_o(g_d + Y_{ds} + Y_L) + Y_{gd}V_o}{g_d + Y_{ds} + Y_L} &= \frac{V_i(Y_{gd} - g_m)}{g_d + Y_{ds} + Y_L} \\ V_o(g_d + Y_{ds} + Y_L + Y_{gd}) &= V_i(Y_{gd} - g_m) \\ \frac{V_o}{V_i} &= \frac{Y_{gd} - g_m}{g_d + Y_{ds} + Y_L + Y_{gd}} \end{aligned}$$

Therefore, voltage gain at high frequencies is given by

$$A_V = \frac{Y_{gd} - g_m}{g_d + Y_{ds} + Y_L + Y_{gd}} \quad (7.42)$$

At low frequencies FET capacitances are neglected i.e., $Y_{gd}=Y_{ds}=0$

$$\therefore A_V = \frac{-g_m}{g_d + Y_L} = \frac{-g_m}{\frac{1}{r_d} + \frac{1}{Z_L}}$$

$$A_V = -g_m \times (r_d \parallel Z_L) = -g_m \times Z_L' \quad (\because Z_L' = r_d \parallel Z_L) \quad (7.43)$$

ii) Input Admittance (Y_i):

$$Y_i = \frac{\text{Input Current}}{\text{Input voltage}} = \frac{I_i}{V_i}$$

To calculate current I_i in the circuit apply KCL at node 'A' we get

$$I_i = I_{gd} + I_{gs}$$

From the circuit $I_{gs} = \frac{V_i}{X_{C_{gs}}} = Y_{gs} V_i$ and from eq. (7.41); $I_{gd} = Y_{gd}(V_i - V_o)$ substituting

these equations in the above equation we get

$$\begin{aligned} I_i &= Y_{gd}(V_i - V_o) + Y_{gs}V_i \\ I_i &= V_i[Y_{gs} + Y_{gd}(1 - \frac{V_o}{V_i})] \\ \frac{I_i}{V_i} &= Y_{gs} + Y_{gd}(1 - A_V) \\ Y_i &= Y_{gs} + Y_{gd}(1 - A_V) \end{aligned} \quad (7.44)$$

At low frequencies FET capacitances are neglected i.e., $Y_{gs}=Y_{gd}=0$

$$\therefore Y_i = 0$$

iii) Output Resistance (R_o):

Output resistance is given by the parallel combination of all impedances and resistances at the output of the circuit. That is

$$R_o = r_d \parallel X_{C_{ds}} \parallel Z_L$$

At low frequencies all capacitances are neglected. Therefore, we get

$$R_o = r_d \parallel Z_L = \frac{r_d Z_L}{r_d + Z_L} \quad (7.45)$$

7.12 ANALYSIS OF COMMON DRAIN (CD) AMPLIFIER

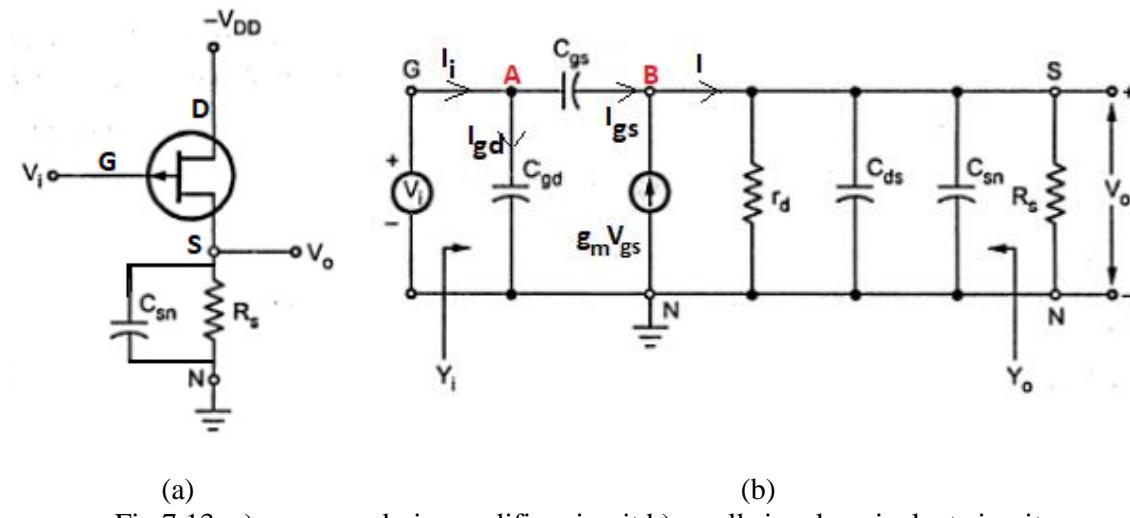


Fig.7.13: a) common drain amplifier circuit b) small signal equivalent circuit

In common drain amplifier drain is common to input gate and output source terminals. An additional capacitance C_{sn} is added in the equivalent circuit which represents the capacitance from source to ground.

i) Voltage Gain (A_V):

$$A_V = \frac{\text{Output voltage}}{\text{Input voltage}} = \frac{V_o}{V_i}$$

From the fig.7.13 (b) the output voltage is given as

$$\begin{aligned} V_o &= I \times (r_d \parallel X_{C_{ds}} \parallel X_{C_{sn}} \parallel R_s) \\ V_o &= I \times \frac{1}{\frac{1}{r_d} + \frac{1}{X_{C_{ds}}} + \frac{1}{X_{C_{sn}}} + \frac{1}{R_s}} \\ V_o &= \frac{I}{g_d + Y_{ds} + Y_{sn} + g_s} \end{aligned} \quad (7.46)$$

$$\therefore g_d = \frac{1}{r_d} = \text{conductance of } r_d$$

$$\therefore Y_{ds} = \frac{1}{X_{C_{ds}}} = j\omega C_{ds} = \text{admittance of } C_{ds}$$

$$\therefore Y_{sn} = \frac{1}{X_{C_{sn}}} = j\omega C_{sn} = \text{admittance of } C_{sn}$$

$$\therefore g_s = \frac{1}{R_s} = \text{conductance of } R_s$$

To calculate current I in the circuit apply KCL at node 'B' we get

$$\begin{aligned} I &= I_{gs} + g_m V_{gs} \\ I &= I_{gs} + g_m (V_i - V_o) \end{aligned} \quad (7.47)$$

I_{gs} is the current passing through gate-source capacitance C_{gs} and it is given by

$$\begin{aligned} I_{gs} &= \frac{V_i - V_o}{X_{C_{gs}}} \\ I_{gs} &= Y_{gs}(V_i - V_o) \end{aligned} \quad (7.48)$$

Substituting I_{gs} in eq. (7.47), we get

$$\begin{aligned} I &= Y_{gs}(V_i - V_o) + g_m (V_i - V_o) \\ I &= V_i(Y_{gs} + g_m) - V_o(Y_{gs} + g_m) \end{aligned}$$

Substituting current I in the eq. (7.46), we get

$$\begin{aligned} V_o &= \frac{V_i(Y_{gs} + g_m) - V_o(Y_{gs} + g_m)}{g_d + Y_{ds} + Y_{sn} + g_s} \\ V_o &= \frac{V_i(Y_{gs} + g_m)}{g_d + Y_{ds} + Y_{sn} + g_s} - \frac{V_o(Y_{gs} + g_m)}{g_d + Y_{ds} + Y_{sn} + g_s} \\ V_o &+ \frac{V_o(Y_{gs} + g_m)}{g_d + Y_{ds} + Y_{sn} + g_s} = \frac{V_i(Y_{gs} + g_m)}{g_d + Y_{ds} + Y_{sn} + g_s} \\ \frac{V_o(g_d + Y_{ds} + Y_{sn} + g_s) + V_o(Y_{gs} + g_m)}{g_d + Y_{ds} + Y_{sn} + g_s} &= \frac{V_i(Y_{gs} + g_m)}{g_d + Y_{ds} + Y_{sn} + g_s} \\ V_o(g_d + Y_{ds} + Y_{sn} + g_s + Y_{gs} + g_m) &= V_i(Y_{gs} + g_m) \\ \frac{V_o}{V_i} &= \frac{Y_{gs} + g_m}{g_d + Y_{ds} + Y_{sn} + g_s + Y_{gs} + g_m} \end{aligned}$$

Therefore, voltage gain at high frequencies is given by

$$A_V = \frac{Y_{gs} + g_m}{g_d + Y_{ds} + Y_{sn} + g_s + Y_{gs} + g_m} \quad (7.49)$$

At low frequencies FET capacitances are neglected i.e., $Y_{gs}=Y_{ds}=Y_{sn}=0$

$$\therefore A_V = \frac{g_m}{g_m + g_d + g_s}$$

$$A_V = \frac{g_m}{g_m + g_d + \frac{1}{R_s}}$$

$$A_V = \frac{g_m}{g_m + g_d} \quad (\because (g_m + g_d) \gg \frac{1}{R_s})$$

$$A_V = \frac{g_m}{g_m + \frac{1}{r_d}} = \frac{g_m \cdot r_d}{g_m r_d + 1}$$

$$A_V = \frac{\mu}{1 + \mu} \quad (\because g_m r_d = \mu) \quad (7.50)$$

Therefore, amplification is positive and has a value less than unity.

ii) Input Admittance (Y_i):

$$Y_i = \frac{\text{Input Current}}{\text{Input voltage}} = \frac{I_i}{V_i}$$

To calculate current I_i in the circuit apply KCL at node 'A' we get

$$I_i = I_{gd} + I_{gs}$$

From the circuit, $I_{gd} = Y_{gd}V_i$ and from eq. (7.48); $I_{gs} = \frac{V_i - V_o}{X_{C_{gs}}} = Y_{gs}(V_i - V_o)$ substituting

these equations in the above equation I_i we get

$$\begin{aligned} I_i &= Y_{gd}V_i + Y_{gs}(V_i - V_o) \\ I_i &= V_i[Y_{gd} + Y_{gs}(1 - \frac{V_o}{V_i})] \\ \frac{I_i}{V_i} &= Y_{gd} + Y_{gs}(1 - A_V) \\ Y_i &= Y_{gd} + Y_{gs}(1 - A_V) \end{aligned} \quad (7.51)$$

At low frequencies FET capacitances are neglected i.e., $Y_{gs} = Y_{gd} = 0$

$$\therefore Y_i = 0$$

iii) Output Resistance (R_o):

Output resistance is given by the parallel combination of all impedances and resistances at the output of the circuit. That is

$$R_o = r_d \parallel X_{C_{ds}} \parallel X_{C_{sn}} \parallel R_s$$

At low frequencies all capacitances are neglected. Therefore, we get

$$R_o = r_d \parallel R_s = \frac{r_d R_s}{r_d + R_s} \quad (7.52)$$