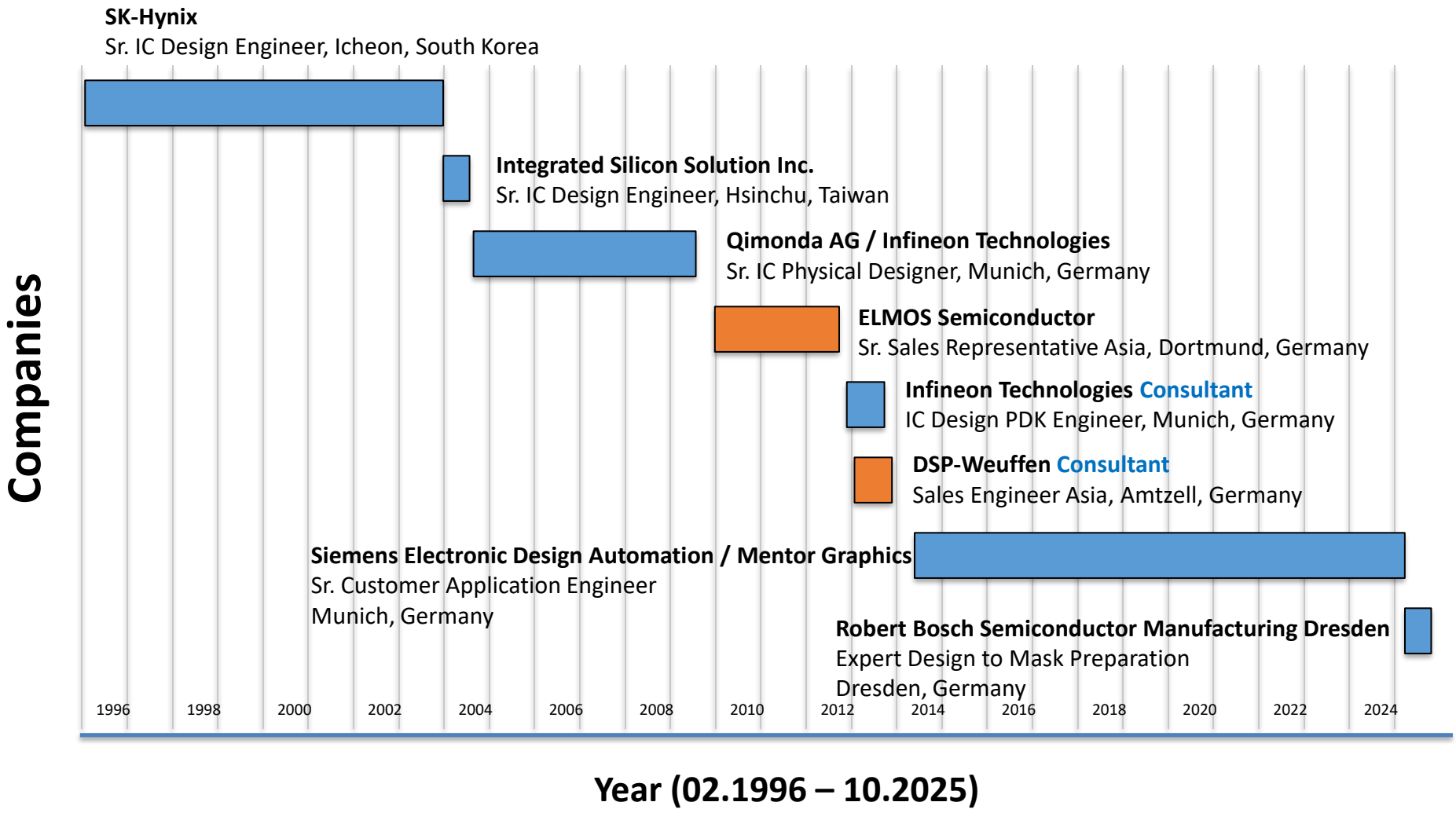
Be Joyful always pray continually
Give thanks in all circumstance

Career Timeline



CAREER SNAPSHOT

Kyung Wook Park — Senior Semiconductor Expert
Nearly 3 decades — IC Design • Physical Design • Verification • Tape-Out • EDA • Sales

Munich, Germany

DAUERAUFENTHALT–EU

TECHNICAL EXPERTISE

- Design-to-Mask & Tape-Out: OPC/RET, MDP, mask assembly, DFM, 300mm fab integration (Bosch)
- Physical Verification (Calibre): DRC | LVS | PERC | OPC RET | SmartFILL | Pattern Matching
- Memory & Mixed-Signal: DDR1/DDR2, bank-cell arrays, PLL/timing, I/O, Sense Amps, Voltage Generators
- Advanced Processes: TSMC N3E/N7/N16/N28, GF 45/28/22, Intel nodes, Samsung 14nm FinFET
- EDA & Automation: Siemens Calibre, Cadence Virtuoso, Pegasus, SKILL, Synopsys ICC2 P&R;, Python, TCL

CUSTOMER & BUSINESS IMPACT

- Siemens EDA (Calibre CAE): Customer support, training, tool adoption (Intel, GF, Infineon, Apple, ST)
- ELMOS Senior Sales Manager Asia: Tier-1 customers; €15M revenue in ultrasonic ICs
- DSP-Weuffen (ADAS Sales): Developed China/Korea market for multi-camera SoCs
- Cross-functional leadership: Sales, Product, Design, QA, Logistics, Finance coordination
- Secured key accounts and led successful annual price negotiations, maintaining and growing revenue stream

ACHIEVEMENTS & RECOGNITION

- Patents: 2 US + 12 Korean patents (DRAM & design automation)
- Awards: Key Talent Award (€20,000), Outstanding Achievement, Best Product Award
- Recognized expert: Memory design simulation, verification, DFM SmartFILL/OPC/DRC writer, physical design methodologies, ASICs

GLOBAL EXPERIENCE & CORE STRENGTHS

- Global footprint: Germany, Korea, Taiwan, China; EU/Asia customer engagements
- Languages: English (C2), Korean (native), German (B2)
- Core strengths: End-to-End lifecycle, cross-functional leadership, automation & problem-solving

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Generated: 2025-12-04 UTC

Kyung Wook Park

Munich, Germany | EU Long-Term Residence Permit
English (C2) • German (B2) • Korean (Native) • Japanese (A2)
GitHub: https://junowedd.github.io/technotespark/

PROFESSIONAL SUMMARY

Senior semiconductor professional with **29+ years of experience across EMEA and APAC**, spanning advanced IC design, EDA verification, design-to-mask preparation, and **long-cycle, high-value B2B engagements.**
Proven in aligning customer business priorities with **advanced semiconductor and EDA solutions**, bridging design, verification, and manufacturing readiness for complex programs, including safety-critical automotive products.
Combines strong commercial leadership and **APAC sales experience** with deep technical credibility, collaborating closely with senior managers, directors, engineering teams, and leading **global foundries** to enable technology adoption, mitigate risk, and deliver successful tape-outs and **sustained revenue growth**.

KEY ACHIEVEMENTS

• **Drove multi-million-euro semiconductor sales and business development programs across APAC**, securing Tier-1 customer relationships in Korea, Japan, China, Taiwan, and Singapore, and supporting long-cycle, high-value B2B engagements.

• **Generated €15M in revenue** for automotive ultrasonic parking sensor ICs at ELMOS through direct engagement with OEMs and Tier-1 customers, aligning technical solutions with customer business requirements.

• **Enabled production-ready tape-outs for safety-critical automotive and advanced semiconductor products**, including Bosch's 300mm automotive chip, by leading photomask preparation, OPC/RET, manufacturability validation, and data integrity assurance.

• **Supported PDK development and validation** for leading foundries including TSMC, Intel, GlobalFoundries, Samsung, Infineon, and ST, acting as a trusted technical and commercial advisor to ensure successful customer outcomes across Europe and APAC.

• **Developed automation frameworks and verification flows** (SKILL-based PCells, TCL/SVRF/TVF scripts, standard libraries), improving verification throughput, accuracy, and customer sign-off turnaround time.

• **Bridged engineering, manufacturing, and customer teams**, translating complex design, sign-off, and yield considerations into clear execution plans that reduced program risk and accelerated adoption.

• **Recognized with multiple industry and company awards**, including SK Hynix Key Talent Award, Outstanding Achievement Award, Best Product Award, and GlobalFoundries Recognition Award.

• **Authored 14 patents (2 U.S., 12 Korean)** in DRAM memory circuit design and physical design, reinforcing technical credibility in customer and executive discussions.

CORE PROFESSIONAL COMPETENCIES

• **Enterprise Sales, Negotiation & Go-To-Market Strategy**, negotiation and deal execution
• Regional Sales Leadership & Cross-Cultural Stakeholder Management
• **Customer Success & Account Enablement** (technical advisory, EMEA & APAC)

• **Semiconductor Solution Positioning** (Memory, ASIC, Analog & Mixed-Signal)
• Foundry Partnership & Ecosystem Collaboration (TSMC, Intel, GF, Samsung, ST)
• **R&D–Customer Alignment & Cross-Functional Leadership**

• **EDA / DFM / Verification Expertise** supporting customer evaluations and adoption
• Tape-Out, Full-Chip Sign-Off & Mask Data Preparation (OPC/RET, Kerf)
• **Yield, Manufacturability & Reliability Optimization** aligned with business outcomes
• Design Automation & Workflow Optimization to accelerate customer sign-off

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PROFESSIONAL EXPERIENCE (Expert Track – Semiconductor / Manufacturing / EDA)

Robert Bosch Semiconductor Manufacturing Dresden, Dresden, Germany
Expert, Design-to-Mask Preparation | 2025.04 – 2025.10

• **Led end-to-end tape-out and photomask preparation** for a 300mm automotive semiconductor program, ensuring manufacturability, data integrity, and compliance with automotive quality standards.

• **Identified and mitigated manufacturing-readiness risks** during technology transfer (TI / TSMC 45nm) by implementing reticle, kerf, and alignment optimizations, reducing re-spin exposure.

• **Coordinated cross-functional stakeholders** across design, lithography, manufacturing, and mask vendors to deliver a production-ready mask set under strict schedule constraints.

Impact: Enabled on-time production release of a **safety-critical automotive semiconductor** by mitigating tape-out and manufacturability risks under strict quality, yield, and schedule constraints.

Siemens EDA (Electronic Design Automation, Mentor Graphics), Munich, Germany
Senior Customer Application Engineer (Calibre Portfolio) | 2014.06 – 2025.03

• Served as a **trusted technical advisor** to Tier-1 semiconductor companies (Intel, TSMC, GlobalFoundries, ST, Infineon, Apple), supporting **strategic decisions** across verification, manufacturability, and sign-off.

• Led **customer engagements end-to-end** from **problem framing and solution benchmarking** to **implementation, automation, and tape-out readiness**, directly influencing project outcomes and schedules.

• Designed and deployed **custom verification and automation flows** (DRC/LVS/DFM/PERC/OPC), eliminating recurring bottlenecks and reducing late-stage design and manufacturing risk.

• Delivered executive-level briefings and technical workshops, **and enablement sessions**, aligning engineering teams and decision-makers on adoption of advanced verification and manufacturability solutions.

Impact: Drove adoption contributing to multi-year enterprise agreements of **Calibre verification and DFM solutions** across multiple Tier-1 customers, strengthening long-term strategic partnerships and accelerating customer time-to-market.

DSP-Weuffen GmbH, Amtzell, Germany
Consultant Sales Engineer (Asia Market) | 2013.02 – 2013.11

• **Led technical sales engagements** for ADAS, multi-camera, MCU, and DSP platforms across China and Korea, supporting customer evaluations and design-in decisions.
• **Developed and managed Tier-1 automotive accounts** including Delphi, Mando, Hyundai Mobis, and Desay, acting as the primary technical and commercial interface.
• **Delivered system-level HW/SW demonstrations** (surround-view and vision systems) and supported customer benchmarking and feasibility assessments.

Impact: Accelerated evaluations shortening sales cycles and design-in discussions for automotive electronics platforms across **APAC** by translating system-level capabilities into customer-specific value.

Infineon Technologies AG, Munich, Germany
Consultant – IC Package / PDK Engineer | 2012.12 – 2013.09

• Developed **Calibre-based DRC rule decks** for **wire-bond BGA, TSSOP, and MQFP LF packages**, supporting standardized package verification flows.

• Created **test cases and validation frameworks** to ensure rule-deck accuracy, production readiness, and proper documentation.

• Coordinated **OSAT alignment** with **Amkor Technology and ASE**, ensuring consistency between design rules, package implementation, and manufacturing constraints.

***Impact*:** Enabled production-ready package verification flows and smoother OSAT integration, reducing risk during package qualification and manufacturing ramp-up.

ELMOS Semiconductor SE, Dortmund, Germany
Senior Sales Representative (APAC) | 2010.01 – 2012.09

• Managed **sales operations and distributor networks** across **Singapore, Korea, China,** Japan, and Taiwan, serving as the primary interface for OEM / Tier-1 automotive customers.

• Generated **€15M in revenue** for **ultrasonic parking sensor ICs** by driving customer engagement, design-in activities, and long-term account development.

• Led **contract and pricing negotiations** with major customers including **Hyundai Mobis, Panasonic, Delphi, and Alpine**, balancing technical requirements with commercial objectives.

• Delivered **end-to-end technical and commercial design-in support** for automotive ASIC projects spanning **sensing, power management, motor control, and in-vehicle networking (CAN, LIN-SBC, FlexRay)**.

***Impact*:** Secured multiple **long-term automotive design wins** and €15M in revenue by aligning customer technical requirements with commercial strategy across APAC Tier-1 accounts.

Qimonda AG / Infineon Technologies AG, Munich, Germany
Senior IC Physical Designer – DRAM (DDR2/DDR3) & Mixed-Signal | 2004.09 – 2009.07

• Led **full-custom physical design and sign-off** for **DDR2/DDR3 DRAM and mixed-signal products**, covering **DRC/LVS compliance** and tape-out readiness.

• Executed **analog, mixed-signal, and power layout** across **90nm → 45nm CMOS nodes**, ensuring manufacturability, yield optimization, and device-matching precision.

• Performed **digital P&R (ICC2)**, parasitic extraction, and **IR-drop / EM / antenna checks**, supporting robust timing and reliability sign-off.

• Improved **design-cycle efficiency** by integrating digital blocks through **PCell-based methodologies and Virtuoso XL**, reducing manual layout effort.

• Authored **technical guidelines** and contributed to **global analog layout methodologies**, enabling consistency and reuse across design teams.

***Impact*:** Delivered **tape-out-ready DDR memory and mixed-signal silicon on schedule** while improving layout robustness, yield, and design-cycle efficiency across multiple technology nodes.

Integrated Silicon Solution Inc. (ISSI), Hsinchu, Taiwan
Senior IC Design Engineer | 2004.01 – 2004.07

• Executed **mask revisions and layout optimization** for a **256Mb LP-SDRAM** product, covering RTL-to-GDS implementation and verification.

• Supported **manufacturability improvements and sign-off quality**, ensuring alignment with **TSMC PRRM** requirements.

***Impact*:** Enabled tape-out-ready LP-SDRAM design with improved verification robustness and manufacturability, reducing risk during foundry sign-off.

SK-Hynix Semiconductor, Icheon, South Korea
Senior IC Design Engineer – DRAM Circuit & Physical Design | 1996.02 – 2003.12

• Led **DRAM and SRAM circuit design and chip architecture definition**, covering high-speed clocks, sense amplifiers, power management, I/O, refresh, and control logic, with full-chip simulation and **JEDEC-compliant timing sign-off**.

• Coordinated **physical design teams** through floor-planning, tape-out, and full-chip sign-off, ensuring alignment across circuit, layout, and manufacturing interfaces.

• Designed and verified **critical layout blocks** (I/O, ESD/latch-up protection, core arrays, power routing), performing **RC extraction, IR-drop, DRC/LVS/ERC/OPC sign-off**, and implementing **dummy-fill and CMP-aware optimizations** to improve wafer yield.

• Led development of **design automation and P&R flows**, authoring **Hercules and Assura rule decks** and supporting post-layout **SI and timing sign-off** using StarRC.

• Authored **2 U.S. and 12 Korean patents** in DRAM design and received multiple internal innovation awards.

***Impact*:** Supported multiple **high-volume DRAM product launches** by integrating circuit design, physical implementation, and automation flows, improving yield, sign-off robustness, and scalability in production.

EDUACTION

Bachelor of Science, Electronics Engineering
University of Ulsan, South Korea (1989.03 – 1996.02)
Completed 29 months of mandatory **military service** with the Republic of Korea Army Infantry while pursuing degree studies (1991.01 – 1993.06).

German Language Training (Professional Integration Track)
Completed a series of certified German language programs supporting professional integration, technical communication, and customer-facing responsibilities in Germany:

• **B2** Level (2013.12–2014.05), CBZ München **| Berlitz Level 4** (2010.11–2011.04), Berlitz Dortmund **| B1** Level (2009.08–2009.12), Münchener Volkshochschule

Japanese Language Course in Dortmund (2010.02~ 2011.05), in KOR(1996.03~ 1996.08)

Additional Training:
• Advanced IC Physical Design & ICC P&R (Synopsys, Munich) (2018.03)
• Calibre SVRF / PERC / OPC Training (Siemens EDA, Munich) (2014.09)
• Microcontroller with infrared optical sensor (ELMOS, Karlsruhe) (2010.06 & 2011.09)

Interests
Machine Learning/AI, cloud-based EDA innovation, and European historical studies.

Hobbies
Long-distance running, hiking, cycling to support a balanced and healthy daily routine.

TECHNICAL HIGHLIGHTS (Selected – Supporting Sales & Customer Engagement)

Foundry Technology Coverage
Hands-on exposure to advanced semiconductor process nodes (≈45nm to 3nm-class) across major foundries including TSMC, GlobalFoundries, Intel, and STMicroelectronics

Manufacturing & Mask Data Preparation
Lithography simulation • SRAF / RET evaluation • OPC / MEBES • JobDeck preparation
Multi-patterning strategies • End-to-end mask data preparation pipelines (litho ModelFlow)
Experience with FinFET and CMOS technologies

CRM & Enterprise Systems
• Salesforce • SAP CRM
Data & Markup Formats
• HTML • JSON • XML • CSV
Design Data & Configuration Management
• Git • GitHub • Bitbucket • Visual Studio Code
Programming & Automation
• Python • Tcl • Java • C++ • Perl • awk • Shell (bash/csh)
Operating Systems
• Linux(RHEL) • Unix • Windows • High-performance computing (cloud-enabled)

Selected EDA & Semiconductor Tools
Analog / Mixed-Signal Design & Simulation
• HSPICE, Spectre, FastSpice (HSIM / NanoSim)
Physical Design, Verification & Full-Chip Sign-Off
• Cadence Virtuoso XL, Synopsys ICC2, (DRC / LVS / DFM / PERC / OPC / Lithography)

Siemens / Mentor Calibre — Deep Expertise
Advanced DFM and yield analysis; **PERC (ESD / latch-up);** OPC simulation and verification; Smart-Fill / ECO-Fill; **antenna and reliability checks**; EM/IR analysis; pattern matching; auto-waivers; **advanced debug workflows**, including 2.5D/3D IC and chiplet analysis.
