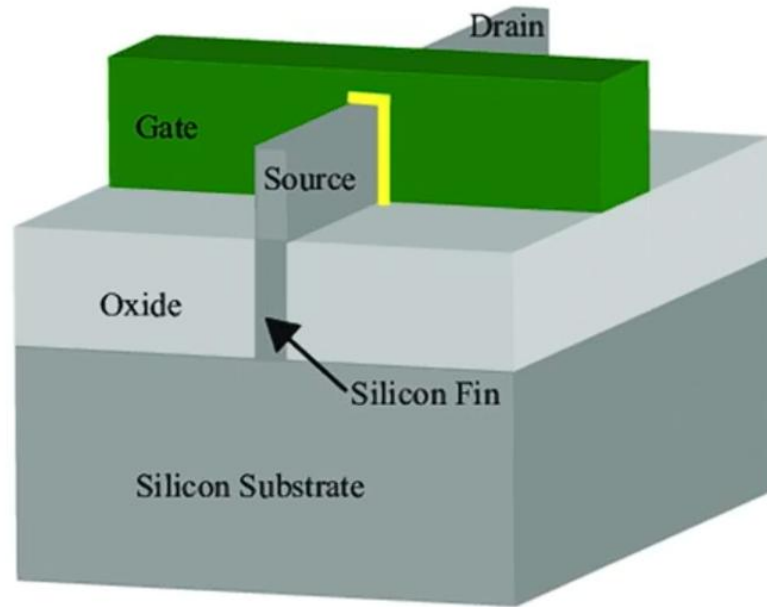
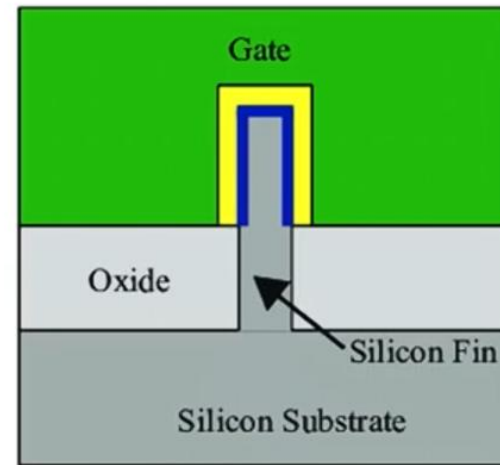


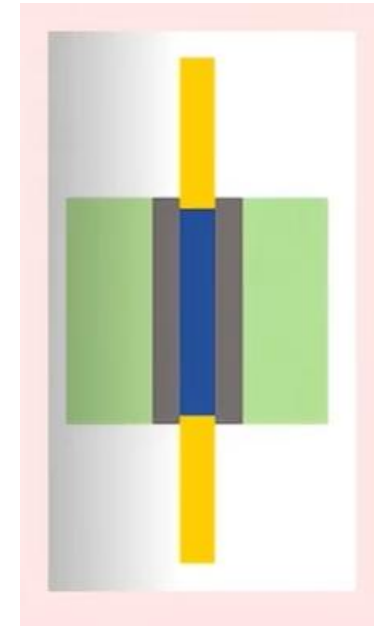
## FinFET (22nm/14nm Processes ~)



(a) 3D Structure



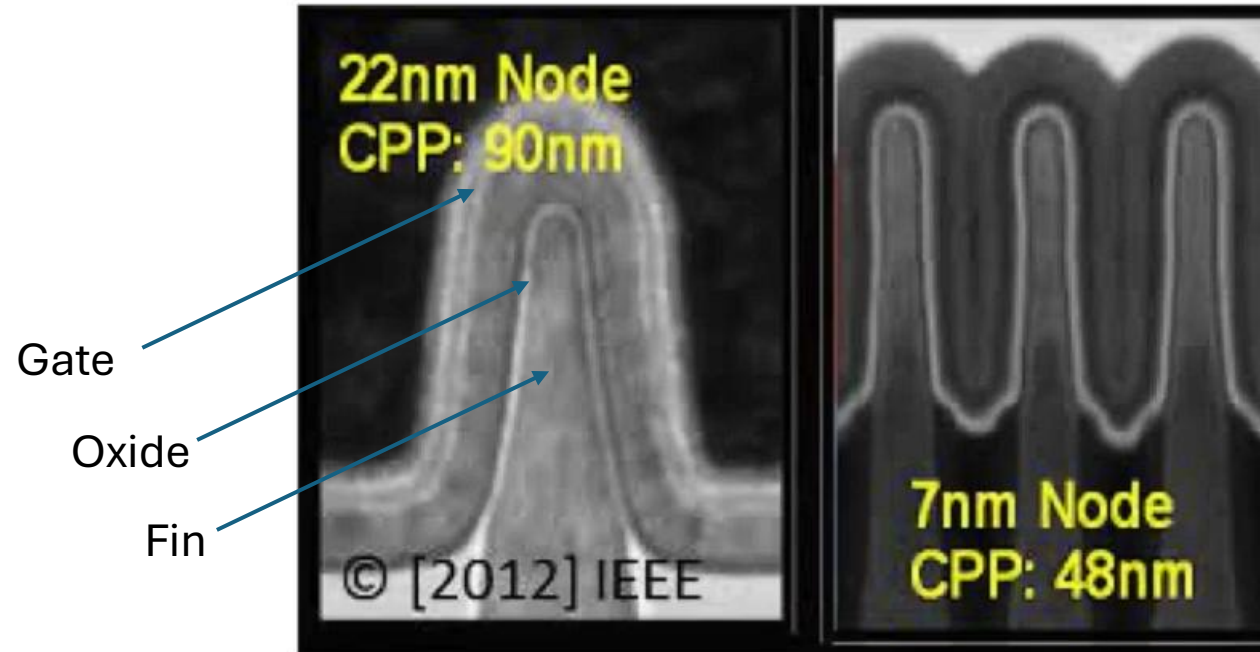
(b) Cross-sectional View



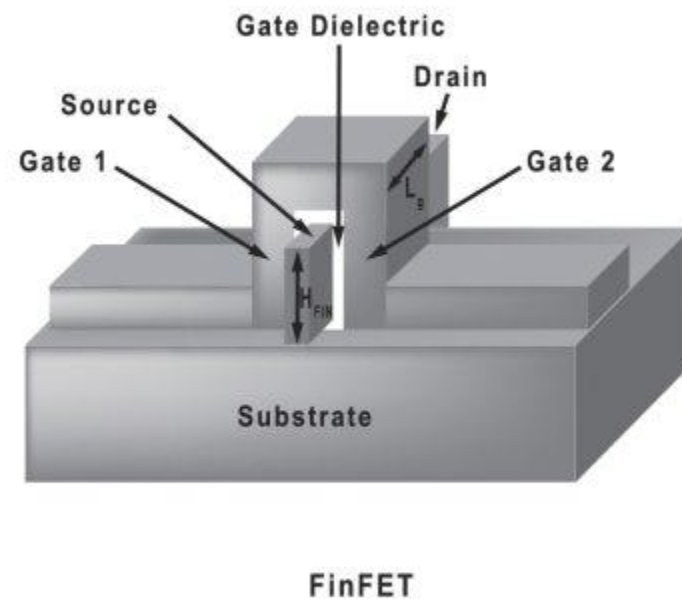
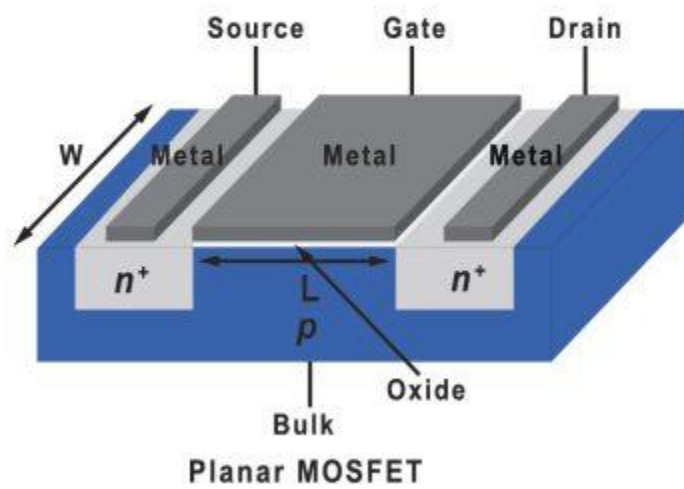
(c) Cross-section Top View

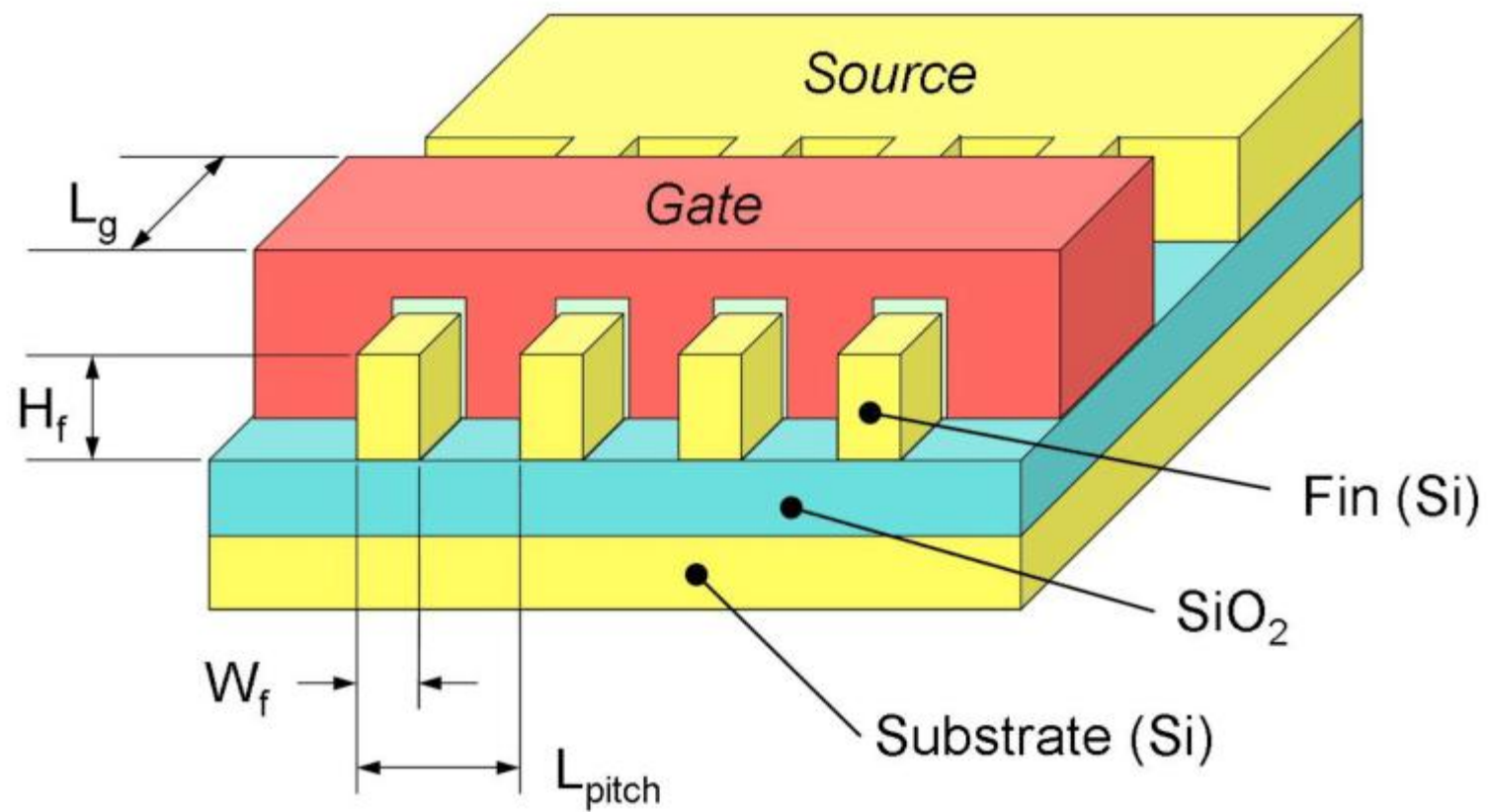
© Intel inc.

FinFET = "Double-gated" MOSFET

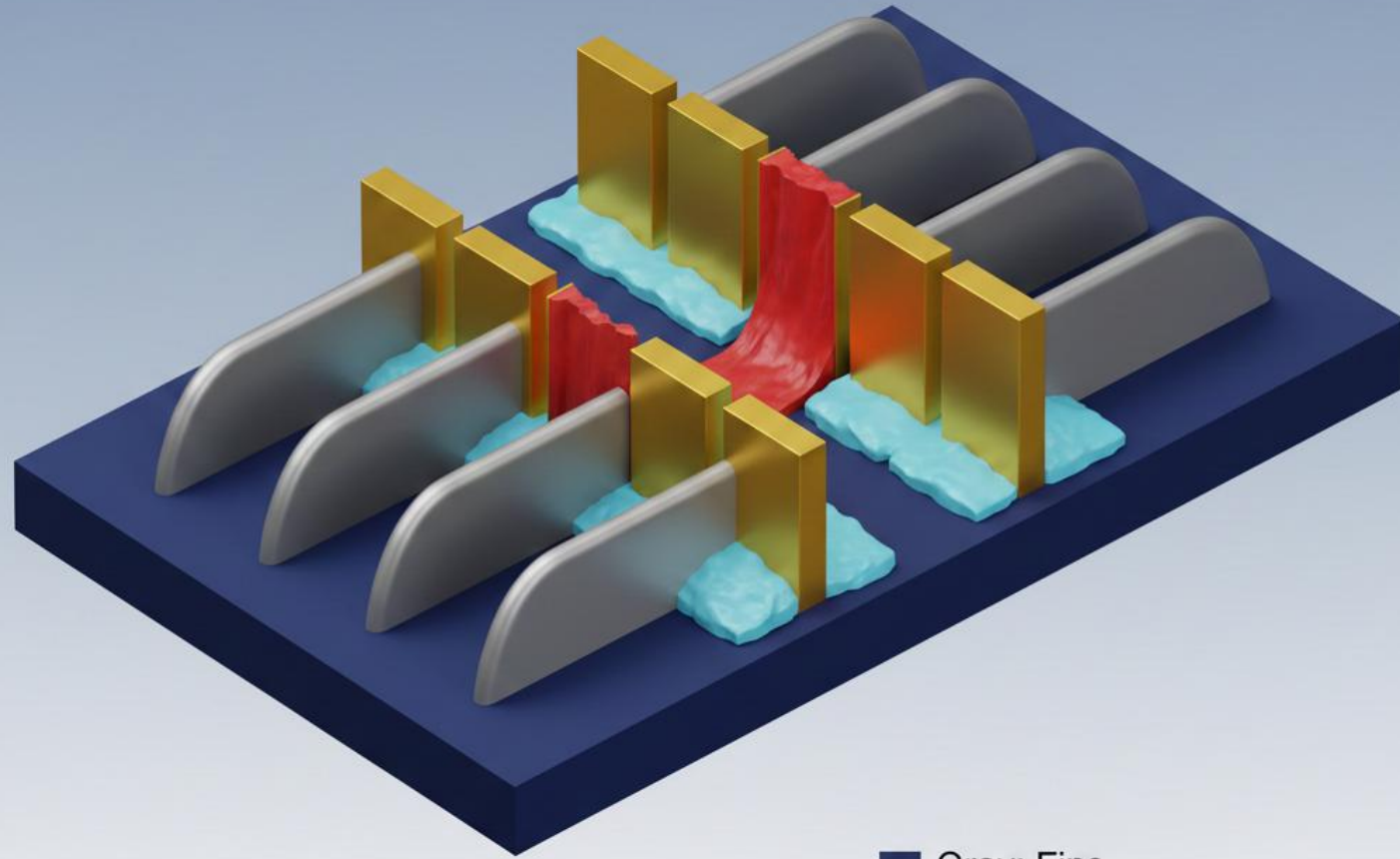


Contact Poly Pitch  
90nm vs. 48nm





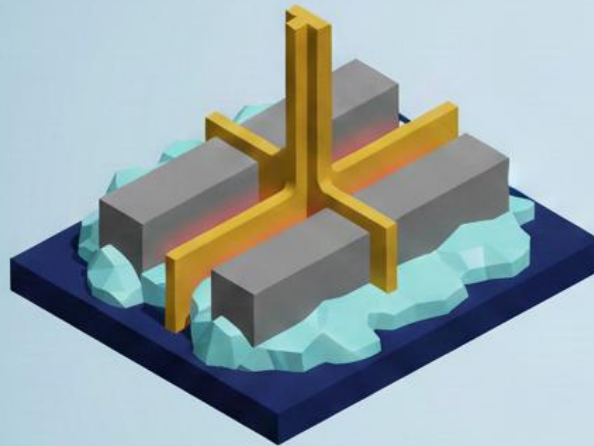
## FinFET 3D Structure with Color-Coded FinCut



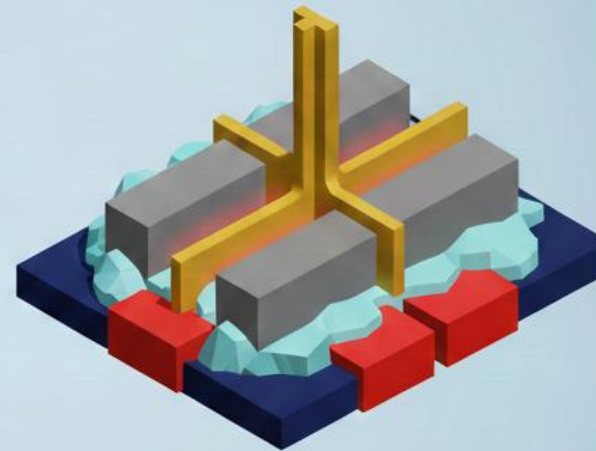
- Gray: Fins
- Gold: Gate
- Red: FinCut Region
- Blue Isolation (STI)

## FinFET Transistor Comparison: 2-Fin vs 4-Fin with FinCut

Dual-Fin FinFET Transistor



Quad-Fin FinFET Transistor

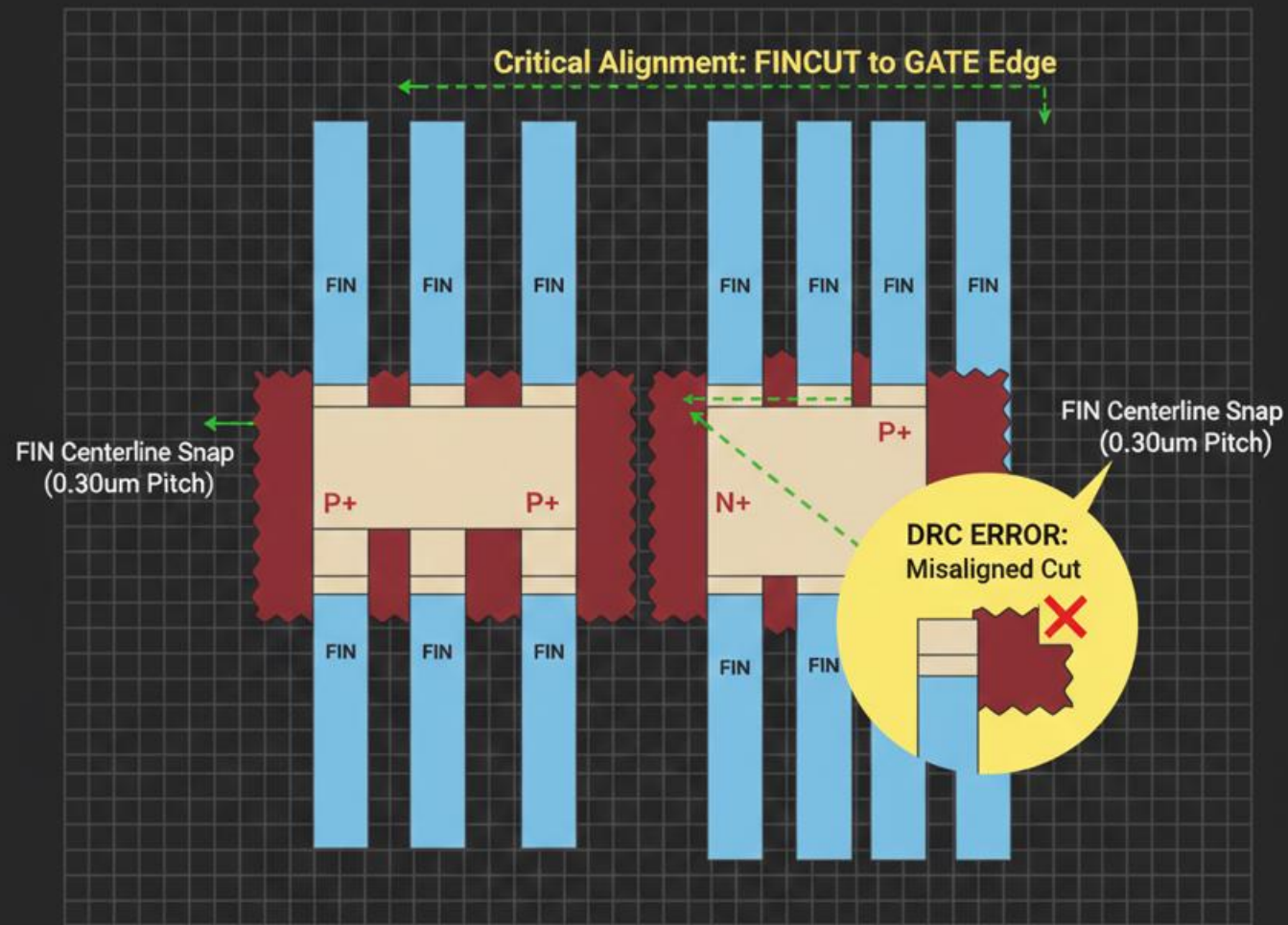


- Gray: Fins
- Gold: Gate
- Red: Active Channel Region
- Blue: Shallow Trench Isolation (STI)
- Substrate:
- Substrate

Note: A 4-fin transistor has approximately twice drive current (and thus is functionally 'larger/larger') than a 2-fin transistor due to increased channel width.

# Fin-to-FinCut 배화도 (Alignment Diagram)

Critical FinFET Cut Layer Alignment





## Double FINCUT Operation

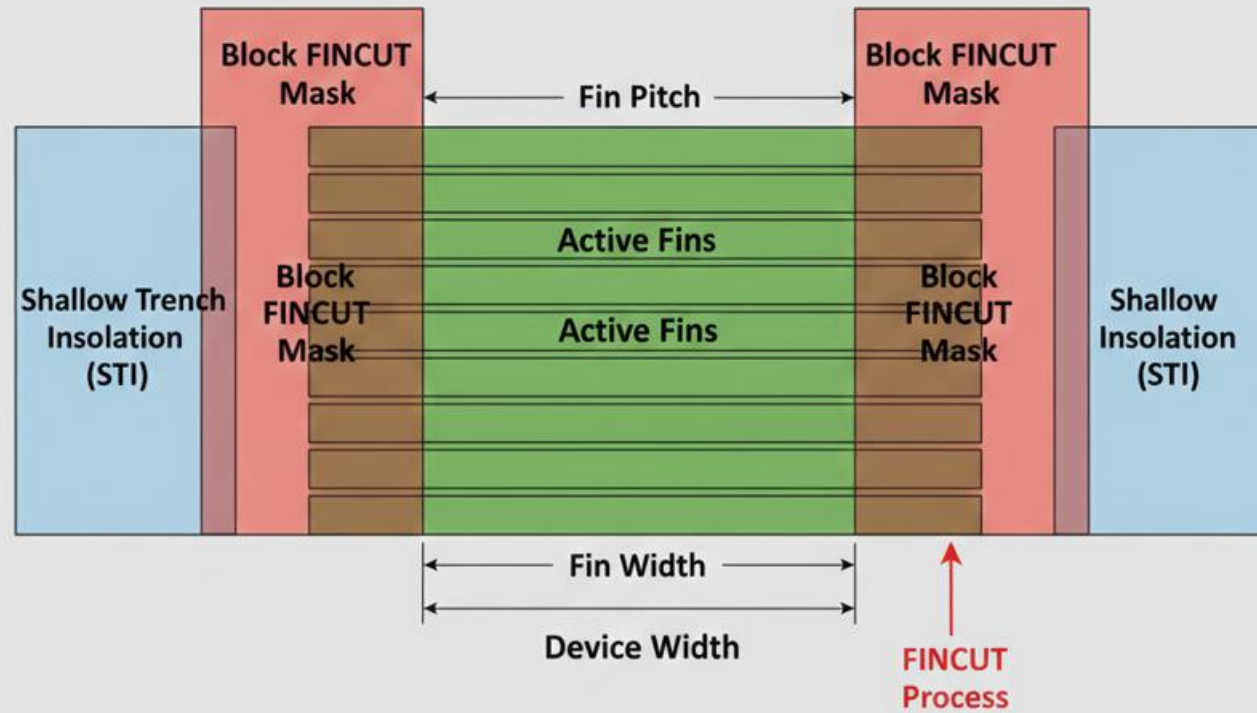




Figure 2. Aggressive use of cut shapes reduces parasitic gate-diffusion capacitance.

