Hobbies & Interests

Long-distance running

Hiking

Cycling

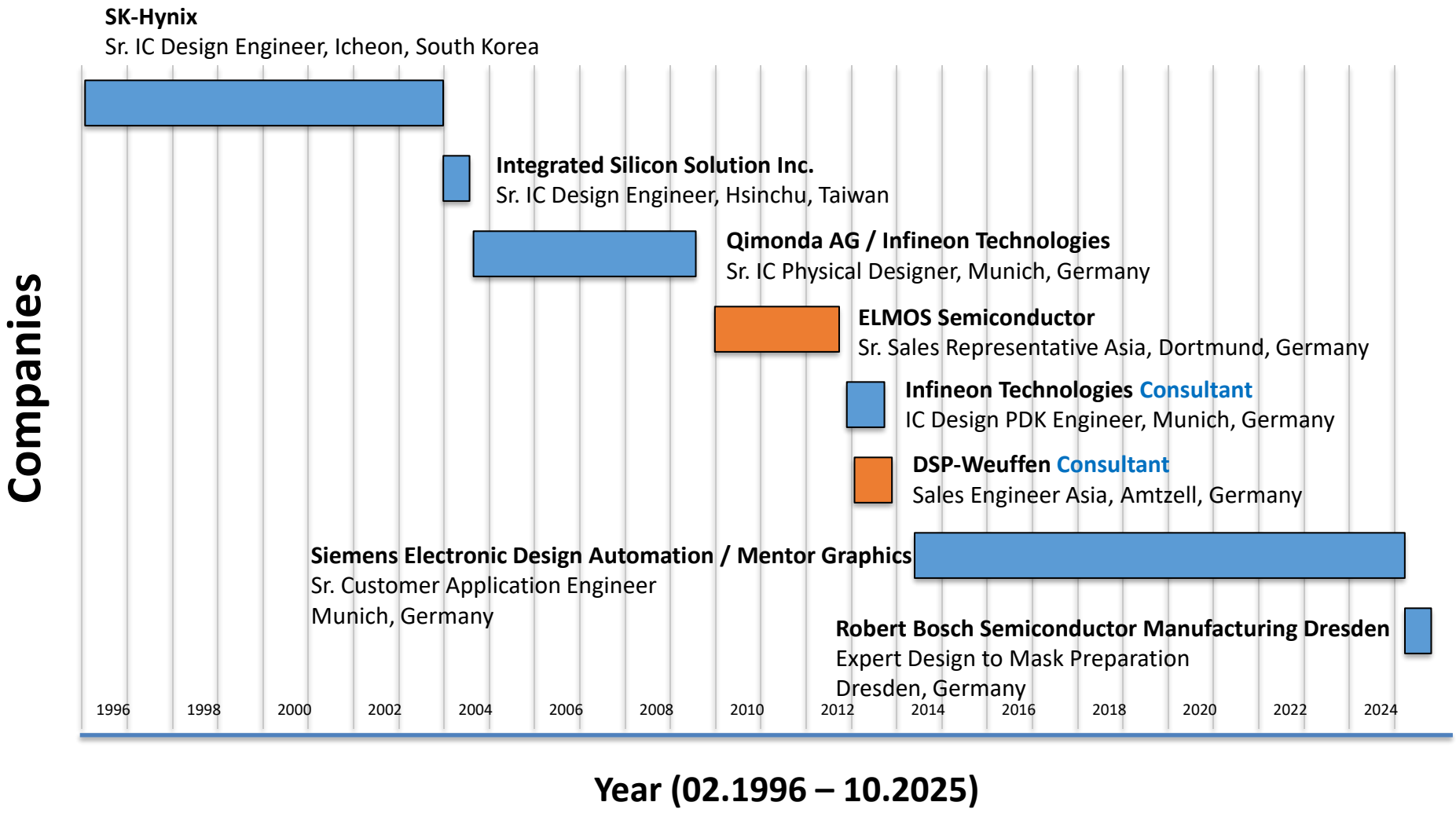
European history

Happy

Dream big

Be Joyful always pray continually
Give thanks in all circumstance

Career Timeline



CAREER SNAPSHOT

Kyung Wook Park — Senior Semiconductor Expert
Nearly 3 decades — IC Design • Physical Design • Verification • Tape-Out • EDA • Sales

Munich, Germany

DAUERAUFENTHALT–EU

TECHNICAL EXPERTISE

- Design-to-Mask & Tape-Out: OPC/RET, MDP, mask assembly, DFM, 300mm fab integration (Bosch)
- Physical Verification (Calibre): DRC | LVS | PERC | OPC RET | SmartFILL | Pattern Matching
- Memory & Mixed-Signal: DDR1/DDR2, bank-cell arrays, PLL/timing, I/O, Sense Amps, Voltage Generators
- Advanced Processes: TSMC N3E/N7/N16/N28, GF 45/28/22, Intel nodes, Samsung 14nm FinFET
- EDA & Automation: Siemens Calibre, Cadence Virtuoso, Pegasus, SKILL, Synopsys ICC2 P&R;, Python, TCL

CUSTOMER & BUSINESS IMPACT

- Siemens EDA (Calibre CAE): Customer support, training, tool adoption (Intel, GF, Infineon, Apple, ST)
- ELMOS Senior Sales Manager Asia: Tier-1 customers; €15M revenue in ultrasonic ICs
- DSP-Weuffen (ADAS Sales): Developed China/Korea market for multi-camera SoCs
- Cross-functional leadership: Sales, Product, Design, QA, Logistics, Finance coordination
- Secured key accounts and led successful annual price negotiations, maintaining and growing revenue stream

ACHIEVEMENTS & RECOGNITION

- Patents: 2 US + 12 Korean patents (DRAM & design automation)
- Awards: Key Talent Award (€20,000), Outstanding Achievement, Best Product Award
- Recognized expert: Memory design simulation, verification, DFM SmartFILL/OPC/DRC writer, physical design methodologies, ASICs

GLOBAL EXPERIENCE & CORE STRENGTHS

- Global footprint: Germany, Korea, Taiwan, China; EU/Asia customer engagements
- Languages: English (C2), Korean (native), German (B2)
- Core strengths: End-to-End lifecycle, cross-functional leadership, automation & problem-solving

Kyung Wook Park | Munich, Germany | +49 176 2119 5934 | junowedd@gmail.com

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Kyung Wook Park

Senior Semiconductor Leader | EMEA & APAC Leadership | Customer Success & Application
EDA & Manufacturing | IC Design | Physical Verification | Advanced Packaging
Email: junowedd@gmail.com | Phone: +49 176 2119 5934 | Munich, Germany
EU Long-Term Residence Permit | English (C2) • German (B2) • JPN (A2) • Korean (Native)
Nationality: South Korea | Date of Birth: 06 Dec 1970 | Place of Birth: Jinhae, South Korea
Family: Married, 3 children (25, 21, 19)

PROFESSIONAL SUMMARY

Senior semiconductor engineer with 29+ years of experience spanning IC design, DDR and SRAM memory development, mixed-signal integration, EDA/CAD verification, and design-to-mask preparation. Skilled in circuit simulation, physical layout, timing analysis, PDK development, full-chip sign-off, OPC/RET, and advanced-node manufacturing readiness. Strong track record of bridging design, verification, and photomask data preparation while collaborating with leading foundries such as TSMC, Intel, GF, Samsung, and ST. Brings cross-domain expertise across automotive, ASICs, and high-performance products—combining deep technical capability with customer-facing and regional sales experience to support technology adoption, business expansion, and successful tape-outs across EMEA and APAC.

KEY ACHIEVEMENTS

• Supported Bosch's 300mm automotive chip tape-out with photomask operations and OPC/RET, ensuring production readiness and data integrity.

• Delivered PDK rule-deck development and validation for TSMC, Infineon, Intel, GF, and ST, enabling successful customer projects across Europe as a Customer Application Engineer.

• Developed standard cells, PCells, and automation scripts (TCL/SVRF), improving verification accuracy and reducing turnaround time.

• Executed full-custom physical design with comprehensive verification: DRC/LVS/ERC/ PERC/OPC/Smart-Fill, IR-drop, EM, antenna, and sign-off.

• Managed circuit-level design, simulation and validation flows for DRAM and SRAM, analog, and mixed-signal ICs using industry-standard EDA tools.

• Led multimillion-euro APAC semiconductor sales programs, securing Tier-1 accounts in Korea, Japan, China, Taiwan, and Singapore.

• Recognized with **SK Hynix** Key Talent Award (Sep. 2002), Outstanding Achievement Award (Dec. 2002), Best Product Award (Feb. 2001), and **GF** Supporting Award (Dec. 2014).

• Authored multiple patents in memory circuits and the real design (2 U.S., 12 Korean).

CORE PROFESSIONAL COMPETENCIES

IC Design (DRAM and SRAM) • Analog/Mixed-Signal Simulation • Physical Design & Sign-off • Calibre Verification • ESD • Parasitic Modeling • Timing Closure • PDK Development • Design Automation & Programming Scripting • DFM/Yield Improvement • OPC/RET & Mask Data Prep-Kerf • Foundry Collaboration • Manufacturability • Multi-Die/2.5D–3DIC Packaging • Customer Success Leadership • Enterprise Sales & Negotiation

TECHNICAL EXPERTISE & EDA CAD TOOLS

Deep expertise in Siemens/Mentor Calibre: PERC (ESD/Latch-Up), DFM/Yield Enhancer, Smart-Fill/ECO-Fill, OPC/RET checks, SVRF/TVF programming, 3DSTACK/3DIC, DRC/LVS/ERC, CMP analysis, pattern matching, FastXOR, antenna assessments, debug, and 2.5D–3D chiplet analysis. Also proficient in DESIGNrev, curvilinear layout verification, auto-waivers, mPower, and HPC/MTFLEX grid environments (1K+ CPUs, cloud-enabled).

Hands-on experience with IC manufacturing flows: lithography simulation, SRAF/RET evaluation, OPC/MEBES, JobDeck preparation, multi-patterning, and full mask data pipelines (nmModelFlow & litho modeling). Familiar with SiGe BiCMOS process.
Worked extensively with major foundry nodes:
TSMC (N45/N28/N16/N7/N3E) | GF (N45/N28/N22) | ST (N45/N40/N28)
Intel (i1278/i1276/i1226/i1222) | Samsung (S16N/S14N FinFET).

Highly proficient across the semiconductor design and manufacturing toolchain, including circuit simulation (HSPICE, FastSpice, HSIM, NanoSim), timing analysis (PrimeTime), and extensive automation scripting (Python, TCL, Perl, awk, C++, shell, bash/csh). Experienced with Linux/Unix workflows, Git/GitLab, Bitbucket, Salesforce, SAP, Siemens Teamcenter, KLayout, and enterprise collaboration environments.

Cadence Physical Verification System:

- Virtuoso XL Schematic/Layout, Assura DRC/LVS | SKILL, PCells, Analog/Mixed-Signal Circuit simulation (HSPICE) | Pegasus Design Review, photomask compose, sign-off | Digital implementation: standard-cell Place & Route (LEF/DEF), Innovus

Synopsys ICV

- Hercules DRC/LVS, digital design IC Compiler (ICC2) P&R | StarRCXT extraction, power and IR-drop analysis | Circuit Timing sign-off using PrimeTime (STA)

WORK HISTORY

Expert Design-to-Mask Preparation

Robert Bosch Semiconductor Manufacturing, Dresden, Germany | 2025.04 – 2025.10

• Led full tape-out and photomask preparation (OPC, frame generation), and data integrity validation. Released complete mask datasets ensuring manufacturability compliance.

• Adapted TI and TSMC process technologies to Bosch's automated 300mm production environment. Created reticle alignment targets to ensure manufacturability. Revision CTR.

• Designed Kerf(scribe-line) structures, alignment/CD overlay markers, metrology patterns, process control monitor circuits, and mask job data using Pegasus and Mask Compose.

Senior Customer Application Engineer – Calibre

Siemens EDA (Mentor Graphics), Munich, Germany | 2014.06 – 2025.03

• Delivered detailed evaluations, benchmarks, and pre-sales support for Calibre solutions across DRC, LVS, PEX, PERC, DFM, 3DSTACK, SmartFill, and OPC / RET enabling major European semiconductor customers to optimize verification and manufacturability.

• Collaborated with Infineon, Intel, GlobalFoundries, ST, and Apple on PDK and ASIC development, SoC integration, and manufacturability enhancements.

• Built automation scripts that streamlined verification workflows and significantly mitigated customer tape-out bottlenecks; authored eq-DRC checks specifically targeting photonics layouts and complex curvilinear shapes.

• Provided advanced product training (PERC-ESD, SmartFILL, eq-DRC, OPC) and hands-on engineering support, ensuring successful deployment of Calibre products portfolio.

• Strong proficiency in OPC/ILT simulation, OPC-Verify, and SRAF/ModelFlow/multi-patterning pipelines, including Lithography optimization, Workbench, MPC environments.

• Experienced in producing manufacturable layouts that enhance lithography robustness, process development, yield performance down to TSMC's FinFET 10nm/5nm/3nm nodes.

Consultant Sales Engineer (Asia Market)

DSP-Weuffen GmbH, Amtzell, Germany | 2013.02 – 2013.11

• Led technical sales for ADAS, multi-cameras, MCU, DSP platforms in China and Korea.

• Developed key accounts including Delphi, Mando, Hyundai Mobis, and Desay.

• Delivered system-level demos (SW/HW surround-view tech), and customer evaluations.

Consultant – IC Package / PDK Engineer

Infineon Technologies AG, Munich, Germany | 2012.12 – 2013.09

• Developed Calibre-based DRC rule decks for wire-bond BGA, TSSOP, MQFP LF packages.

• Created test cases and validated rule decks for production readiness, documentation.

• Coordinated OSAT alignment with Amkor Technology and ASE.

Senior Sales Representative Asia (Asia Market)

ELMOS Semiconductor SE, Dortmund, Germany | 2010.01 – 2012.09

• Managed sales operations/distributors across Korea, China, Japan, Taiwan, and Singapore.

• Generated €15M in revenue for ultrasonic parking sensor ICs at ELMOS through OEM/ Tier-1 customer engagement.

• Negotiated major contracts and price with Hyundai Mobis, Panasonic, Delphi, and Alpine.

• Delivered complete technical and commercial design-in support for ASIC projects, covering 3D-gesture sensors, ultrasonic parking sensors, power supplies, IGBT drivers, pressure sensors, airbag squib drivers, BLDC/stepper motor, CAN, LIN-SBC, and FlexRay.

Senior IC Physical Designer – DRAM DDR memory & mixed-signal

Qimonda / Infineon Technologies, Munich, Germany | 2004.09 – 2009.07

• Led full-custom DDR memory and mixed-signal layout efforts, covering LVS/DRC sign-off.

• Executed Analog & mixed-signal, Power layout across 90nm → 45nm CMOS technologies, ensuring manufacturability, yield, and device matching precision. tape-out–ready silicon.

• Performed ICC2 P&R, parasitic extraction, IR-drop/EM optimization, and antenna checks.

• Reduced design cycle time by integrating digital blocks through PCells and Virtuoso XL.

• Authored technical guidelines and contributed to global analog layout methodology.

Senior IC Design Engineer

Integrated Silicon Solution Inc. (ISSI), Hsinchu, Taiwan | 2004.01 – 2004.07

• Developed DRC/LVS rule decks and automation flows using EDA tools: Dracula/Hercules.

• Completed mask revisions and layout optimization for 256Mb LP-SDRAM, RTL-GDS.

• Supported manufacturability enhancements and sign-off quality aligned with TSMC PRRM.

Senior IC Design Engineer – DRAM Circuit & Physical Design

SK-Hynix Semiconductor, Icheon, South Korea | 1996.02 – 2003.12

• Designed DRAM and SRAM circuits (PLLs, vref-bandgap, High speed clock-800MHz, sense amps, regulators, power-up, decoders, refresh, I/O drivers, address, bank array, logic state-machine), Defined chip architecture, full-chip simulation, timing and JEDEC specification.

• Executed HSPICE/HSIM simulation, first silicon debug, failure analysis, and timing closure.

• Coordinated Physical design team, chip floor-planning, tape-out, and sign-off execution.

• Designed and verified key layout blocks—including I/O pads, ESD and latch-up protection, core arrays, power routing, sense amps, decoders, address buffers, and A/D converters—along with split-power domain evaluation, RC extraction, IR-drop analysis, and DRC/LVS/ ERC/OPC sign-off. Implemented dummy-fill and CMP-aware optimization to enhance wafer yield and pattern fidelity.

• Developed CAD automation flows, P & R, authored Hercules, and Assura decks. StarRCXT.

• Filed 2 U.S. & 12 Korean patents in DRAM design; received multiple innovation awards.

Education

Bachelor of Science, Electronics Engineering
University of Ulsan, South Korea (1989.03 – 1996.02)
Completed 29 months of mandatory **military service** with the Republic of Korea Army Infantry while pursuing degree studies (1991.01 – 1993.06).

German Language Training (Professional Integration Track)
Completed a series of certified German language programs supporting professional integration, technical communication, and customer-facing responsibilities in Germany:

- **B2** Level (2013.12–2014.05), CBZ München **| Berlitz Level 4** (2010.11–2011.04), Berlitz Dortmund **| B1** Level (2009.08–2009.12), Münchener Volkshochschule

Japanese Language Course in Dortmund (02.2010~ 05.2011), in KOR(03.1996~ 08.1996)
Microcontroller with infrared optical sensor at ELMOS in Karlsruhe (06.2010 & 09.2011)
IC-Compiler, Place and Route at Synopsis in Munich (03.2018)
Semiconductor processes at university of Bundeswehr München (10.2004)
SKILL-codes, parameterized cells training at Cadence in Seoul (04.2000)
Programming SVRF at Mentor Graphics-Calibre, and Synopsys-Hercules in Seoul (03.2000)
Semiconductor design and processes at university of KAIST in Daejeon (08.1996)

Interests

Machine Learning/AI, cloud-based EDA innovation, and European historical studies.

Hobbies

Long-distance running, hiking, cycling to support a balanced and healthy daily routine.