Frontend Design

• Supported European semiconductor programs using Calibre DRC/LVS/PERC, reliability checks, parasitic analysis, and advanced-node physical implementation.

• Delivered technical guidance across FinFET design, multi-die integration, and SoC workflows with TSMC, Intel, GF, ST, and Apple.

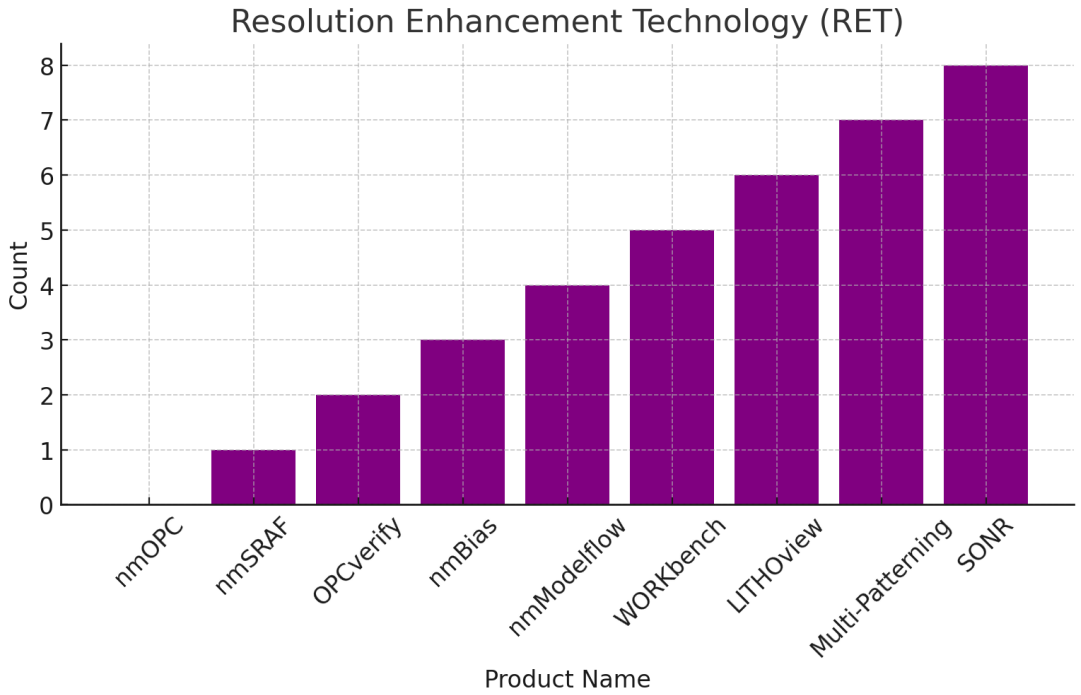
• Improved customer flows by creating automation scripts (TCL/Python) to shorten sign-off cycles and reduce tape-out delays.

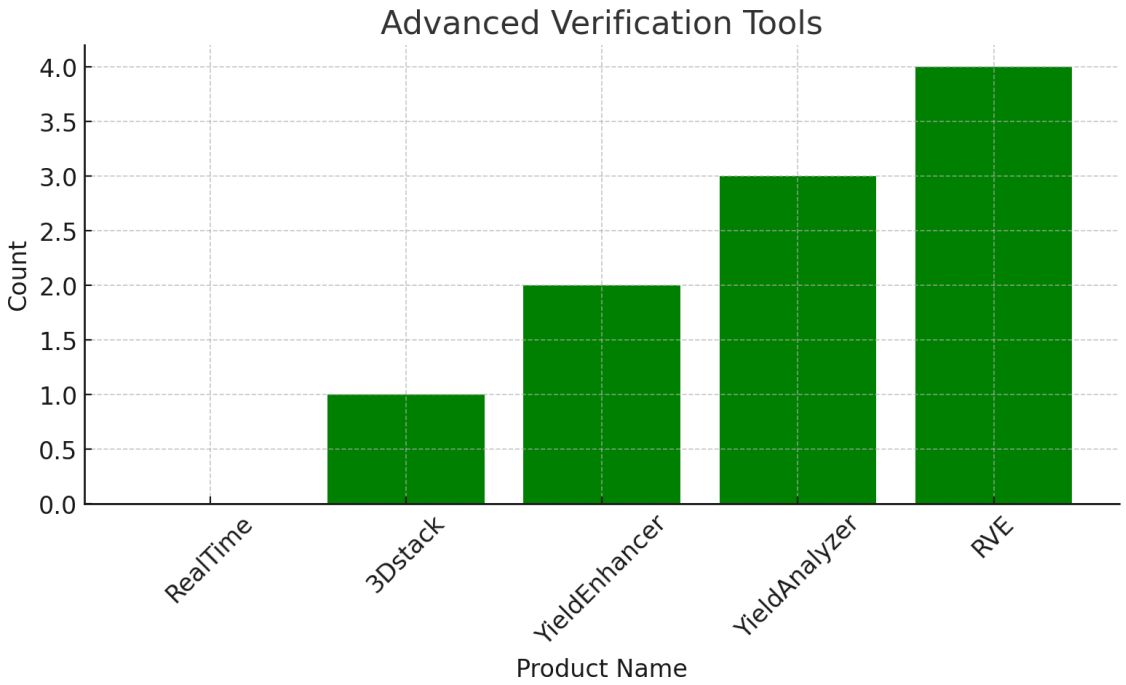
• Enabled rule-deck quality by debugging PDK logic and collaborating with R&D on feature enhancements.

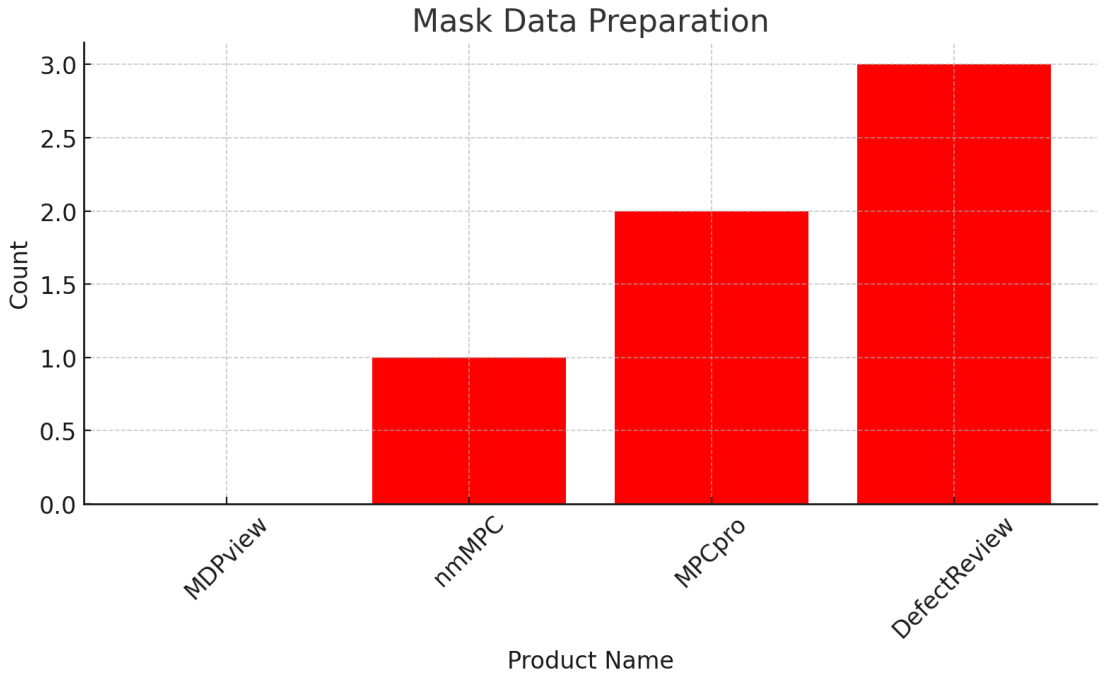
• Trained engineering groups in SmartFill/ECO-Fill, PERC, ESD/LUP, and advanced verification methodologies.

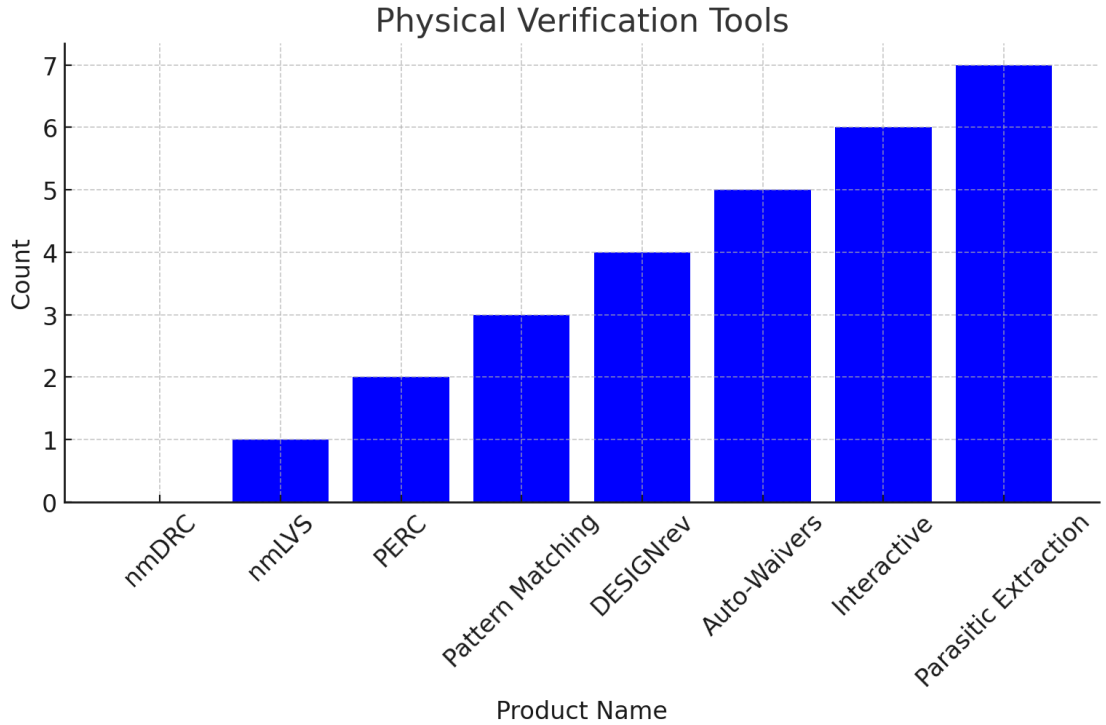
• Provided evaluations, benchmarks, and pre-sales support for new Calibre capabilities.

Calibre Products Portfolio
Frontend Design & Backend manufacturing

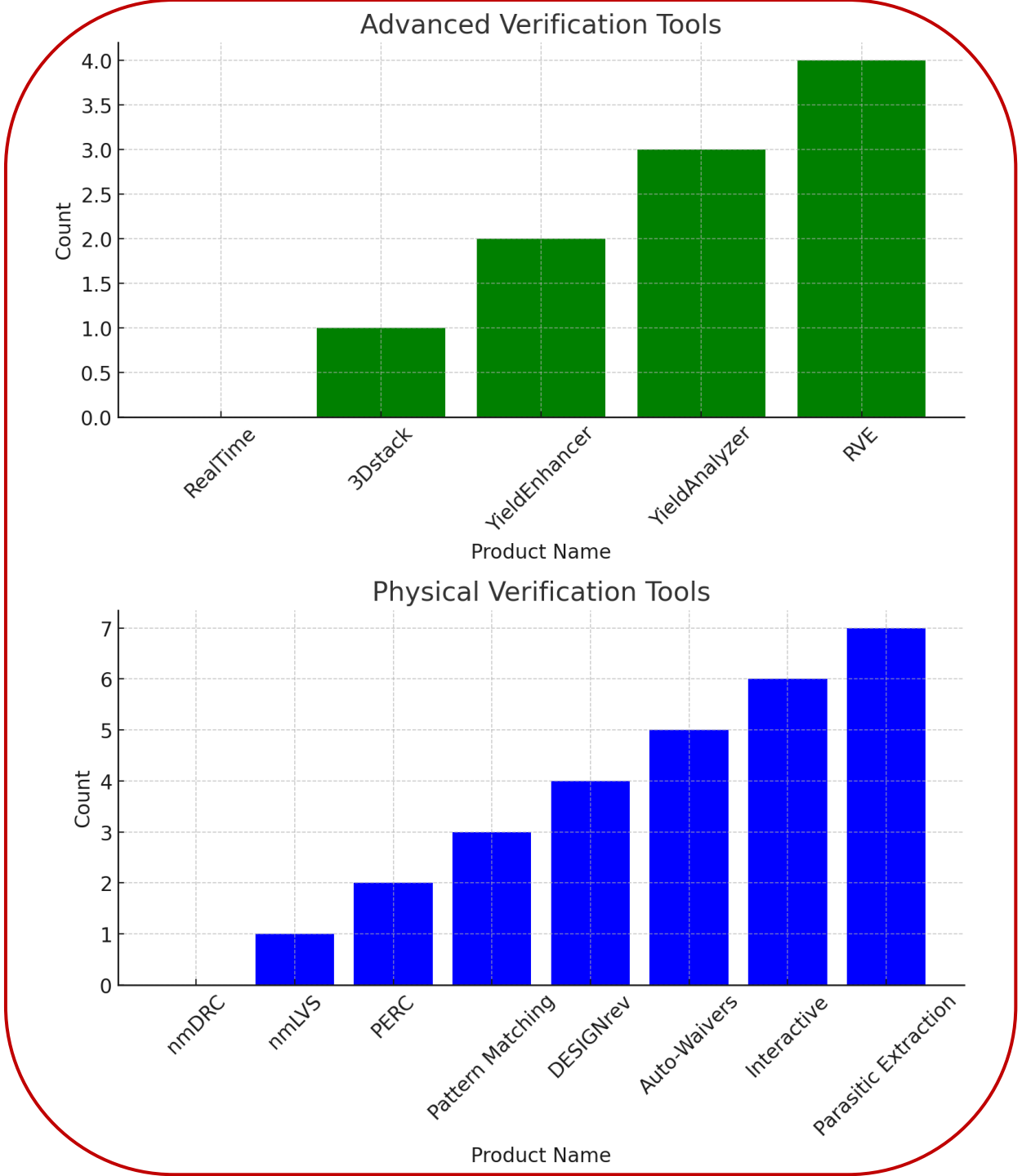




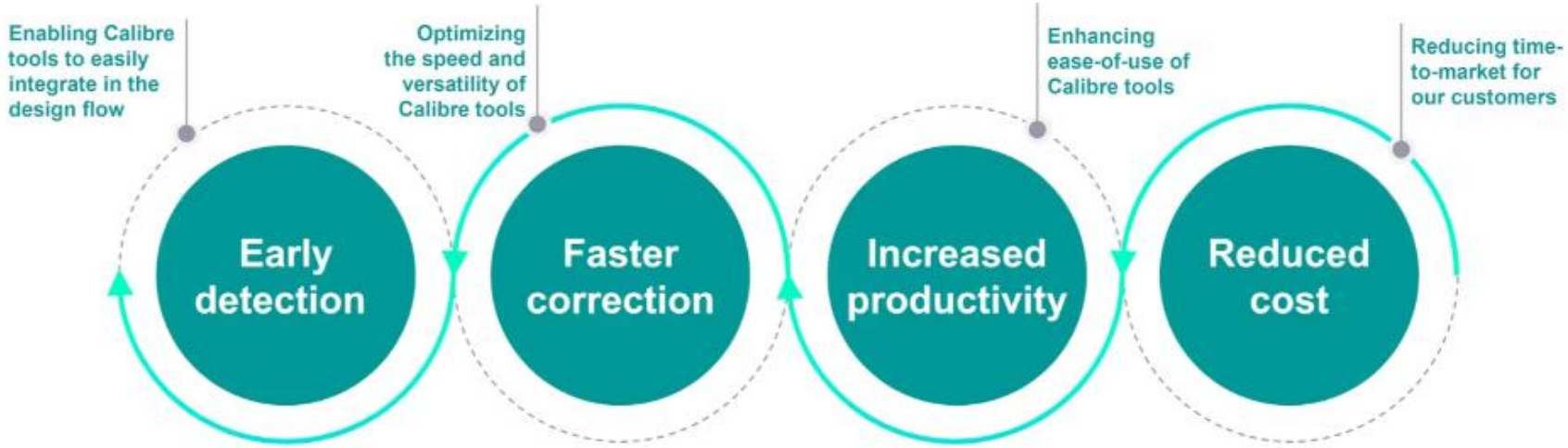




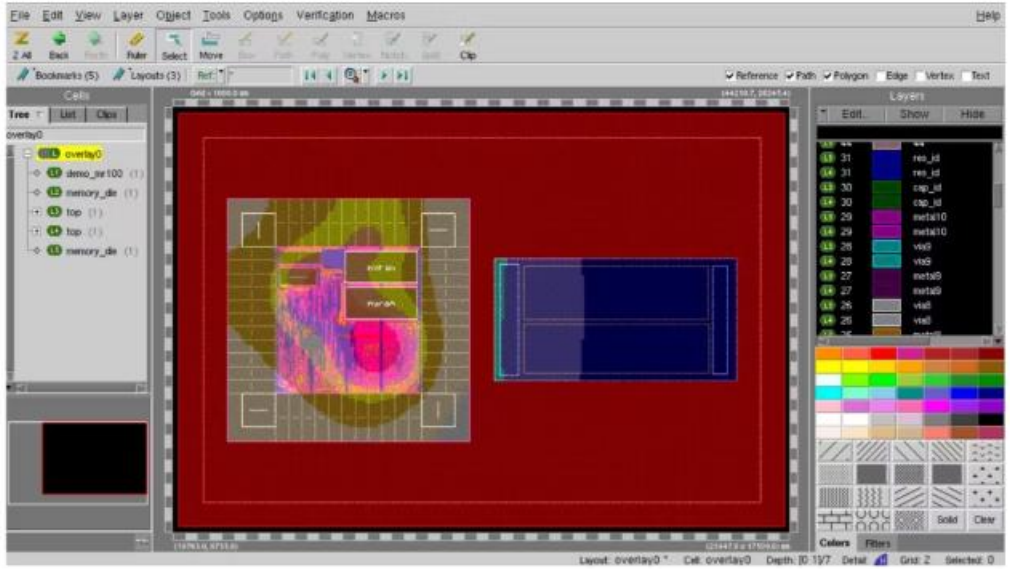
Calibre Products Portfolio
Frontend Design



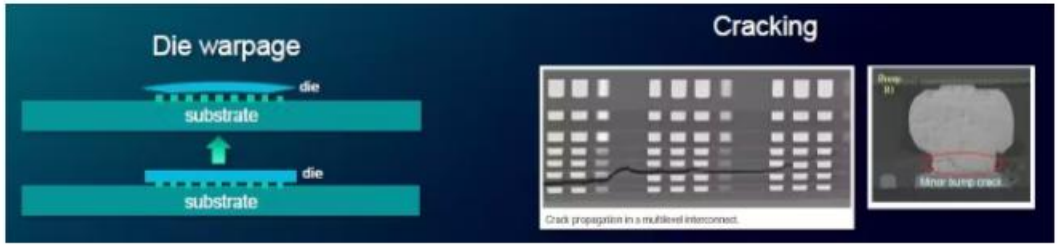
Shift-left Solutions



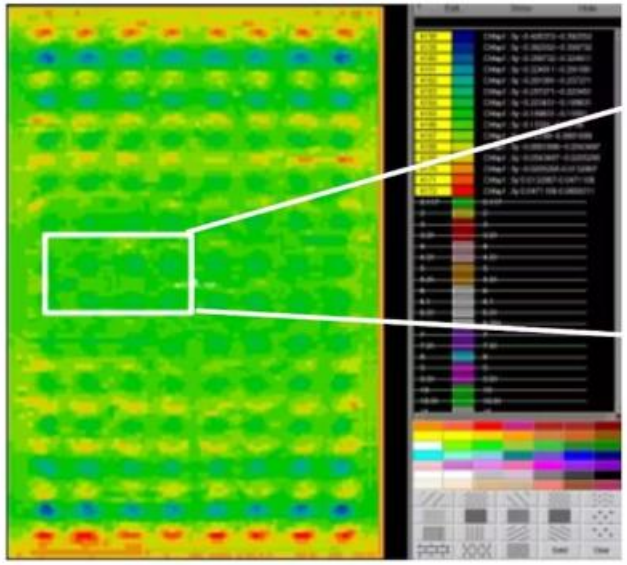
Calibre shift-left solutions continuously pursue innovative strategies and enhancements to provide design companies with the greatest value.

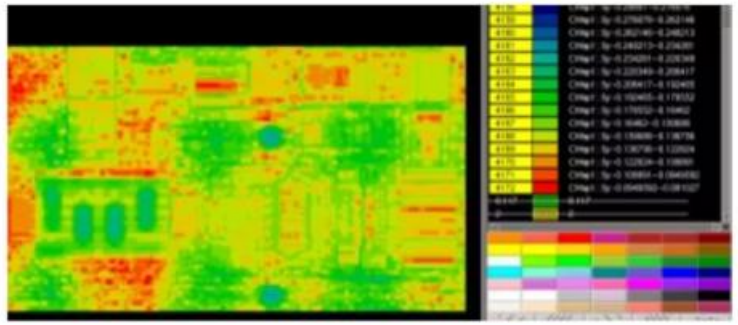


A screenshot of a Calibre **3D Thermal**, the Siemens EDA 3D IC thermal analysis tool. Thermal gradients are shown overlaid on the physical layout



Mechanical stress can be caused by IC architecture and packaging

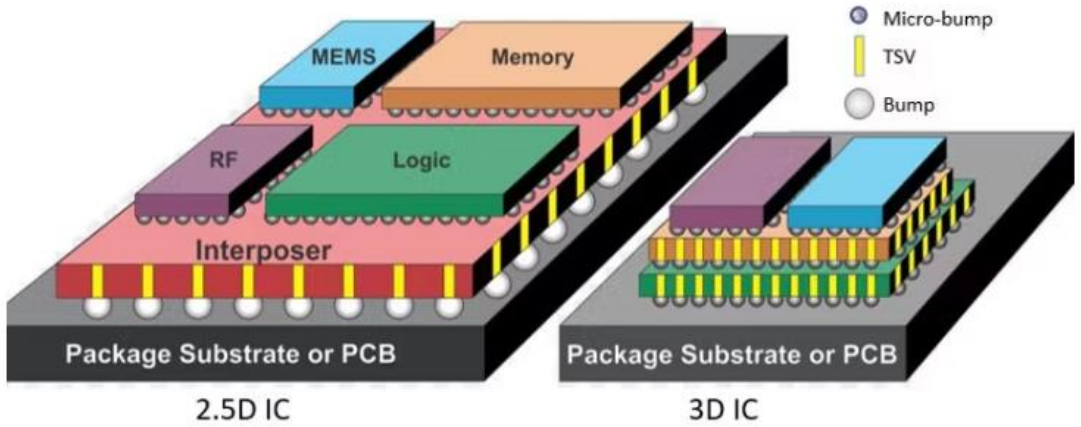




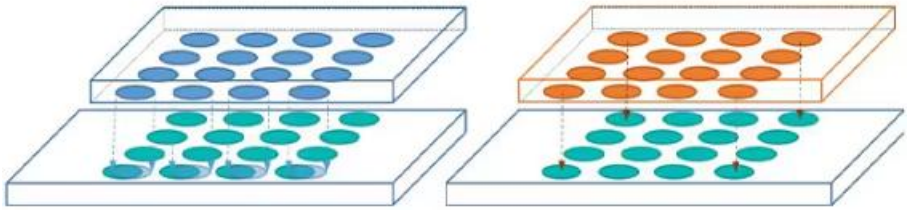
Stress analysis for 3D ICs

Calibre 3D IC

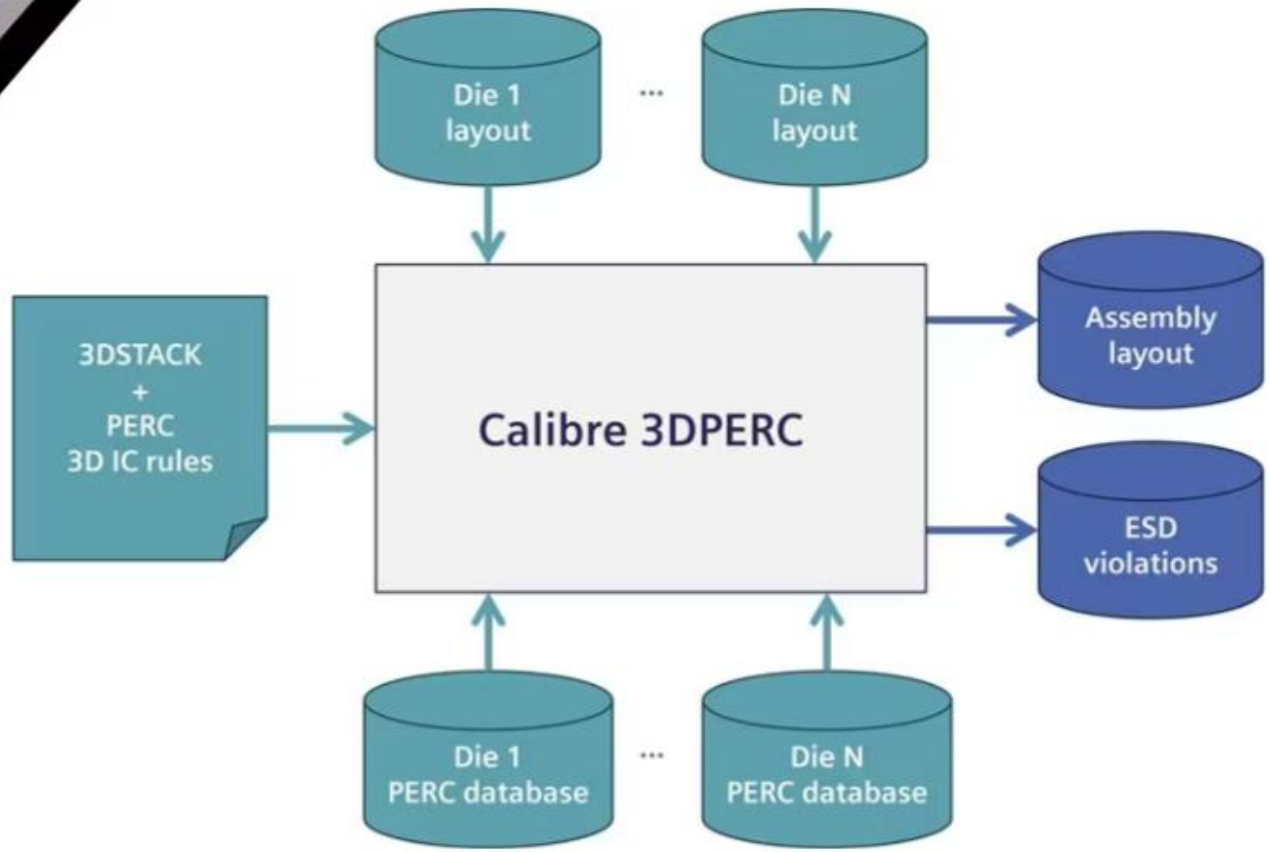
Accurate 3D circuit analysis



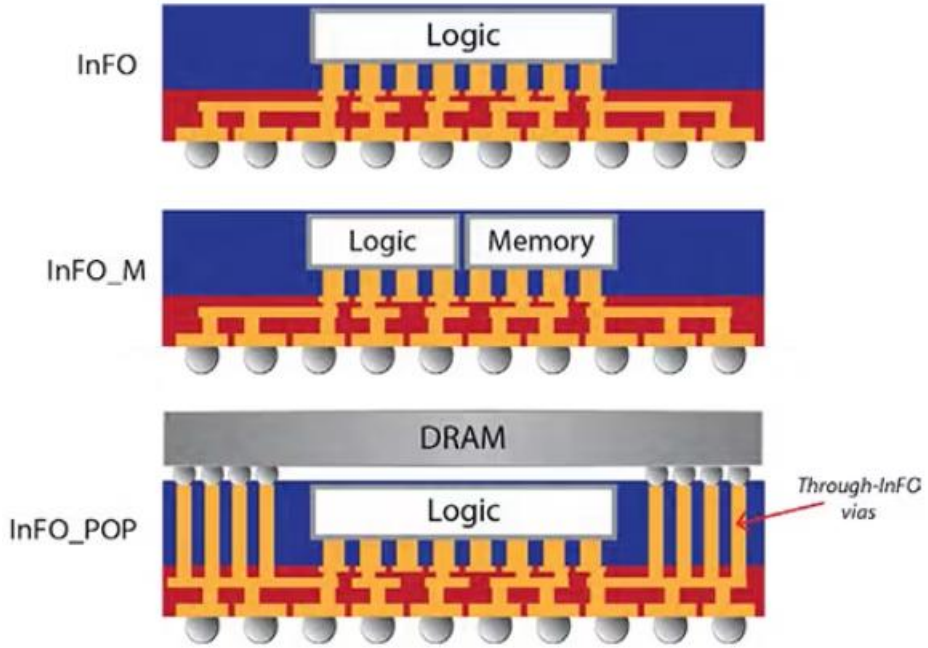
2.5D and 3D IC designs



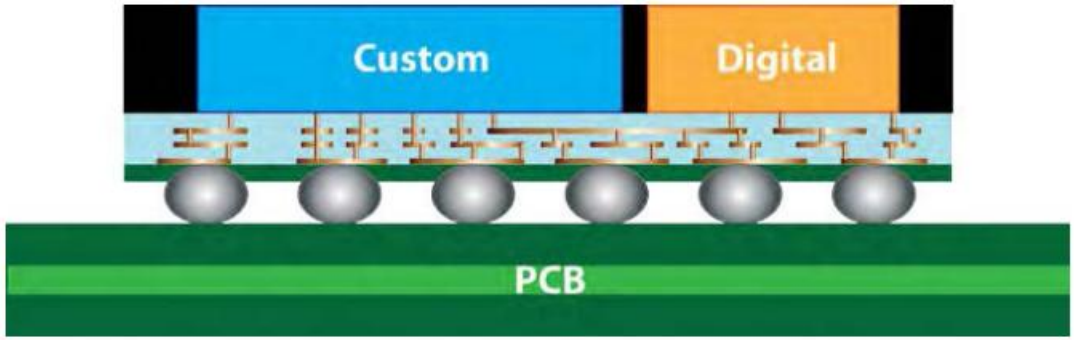
Designers working on multi-die, multi-chiplet stacked configurations in 2.5/3D IC designs can use Calibre **3DStack** physical verification checks to verify die alignments for proper connectivity and electrical behavior



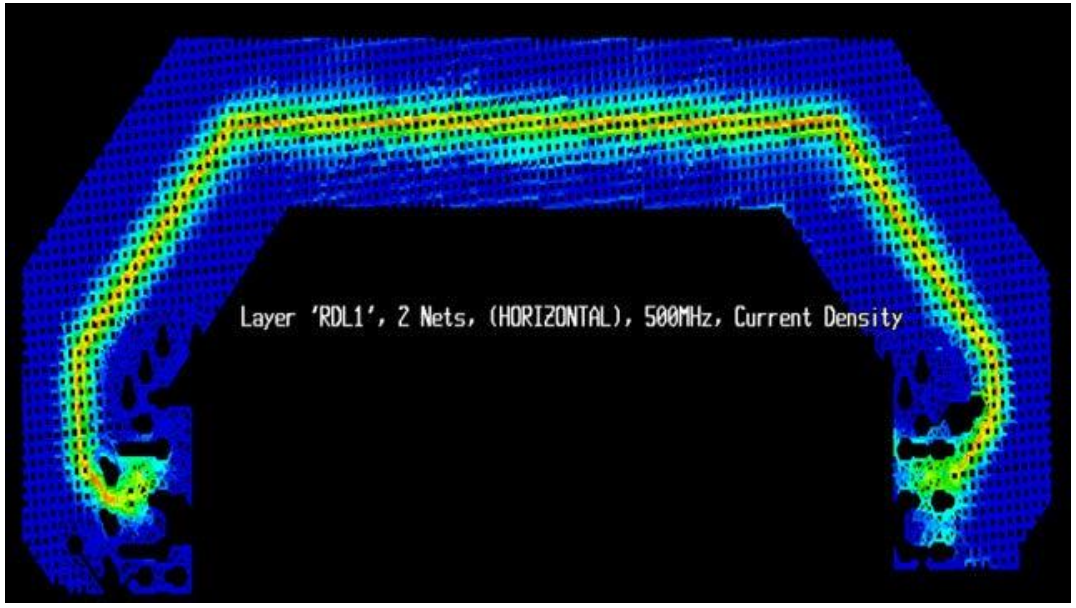
Inputs and outputs of Calibre 3DPERC ESD verification



Implementing Fan-Out Wafer-Level Packaging (FOWLP) with the HDAP Flow



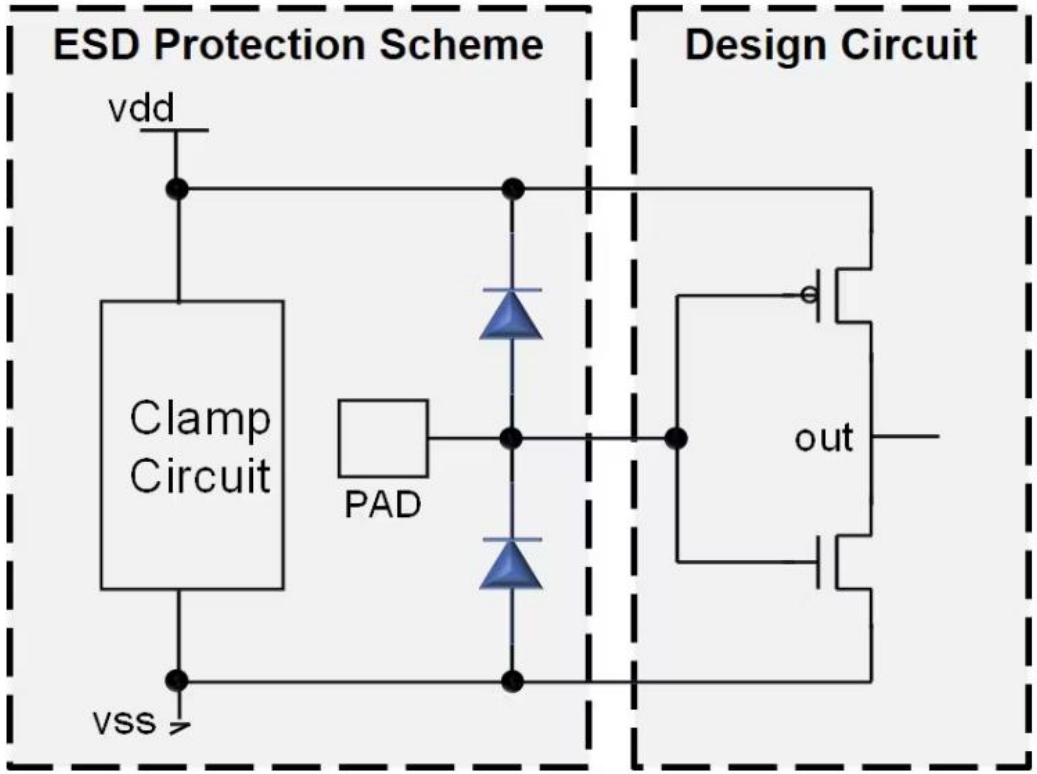
FOWLP can significantly reduce the package footprint



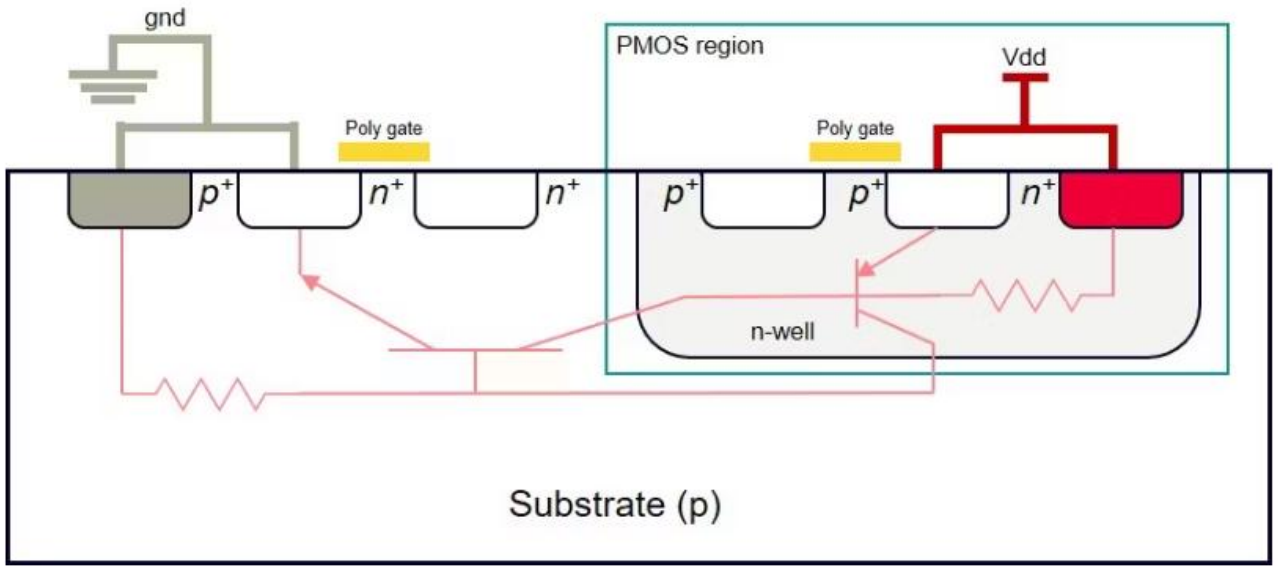
Achieving OSAT and foundry fabrication rules for package substrate outgassing, metal-filled areas and power planes

Calibre 3D IC

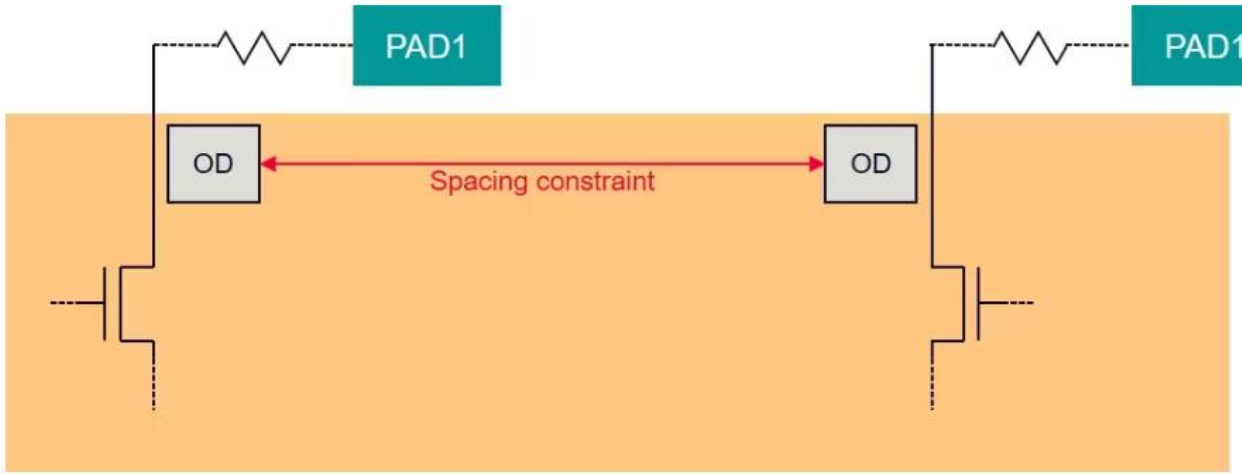
ESD Latch-UP



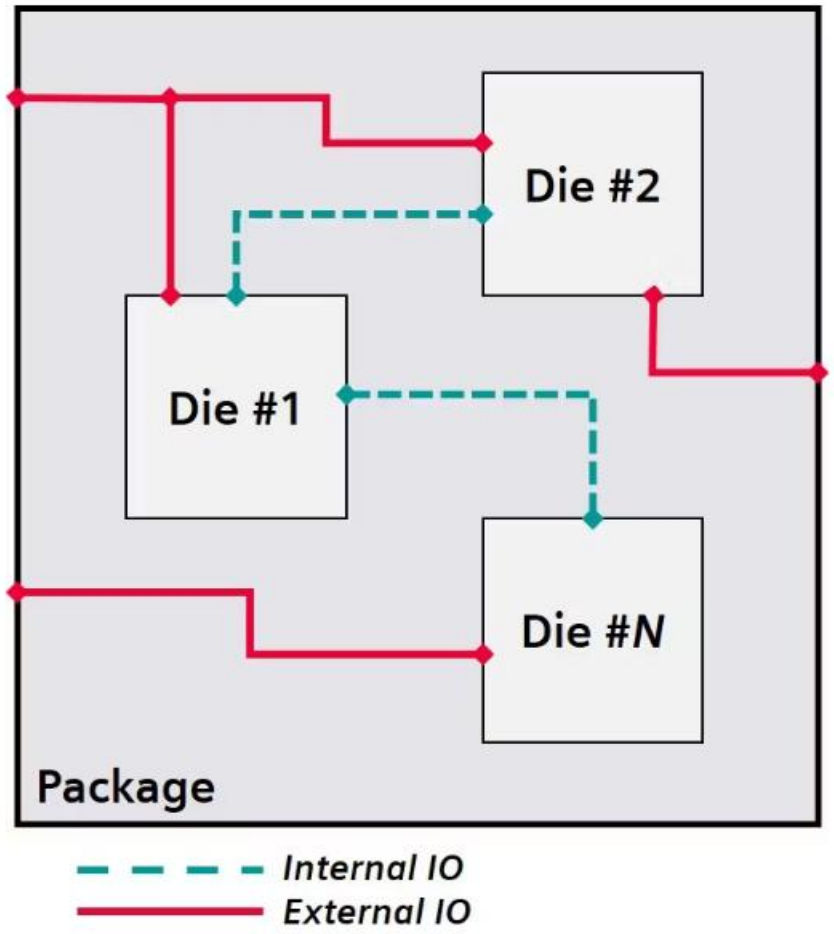
Typical ESD protection scheme



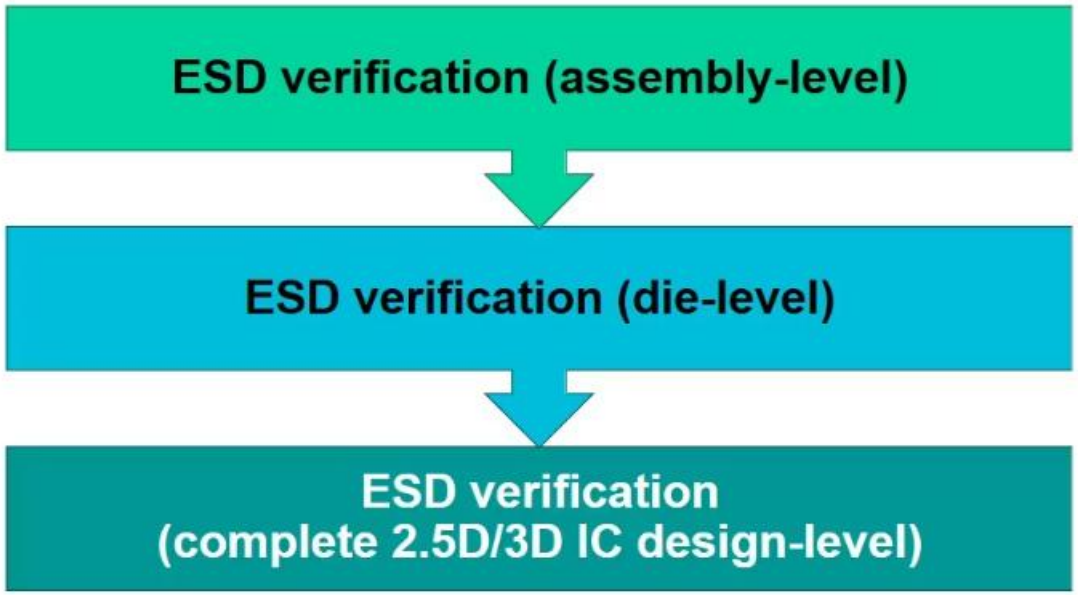
Latch-up formation



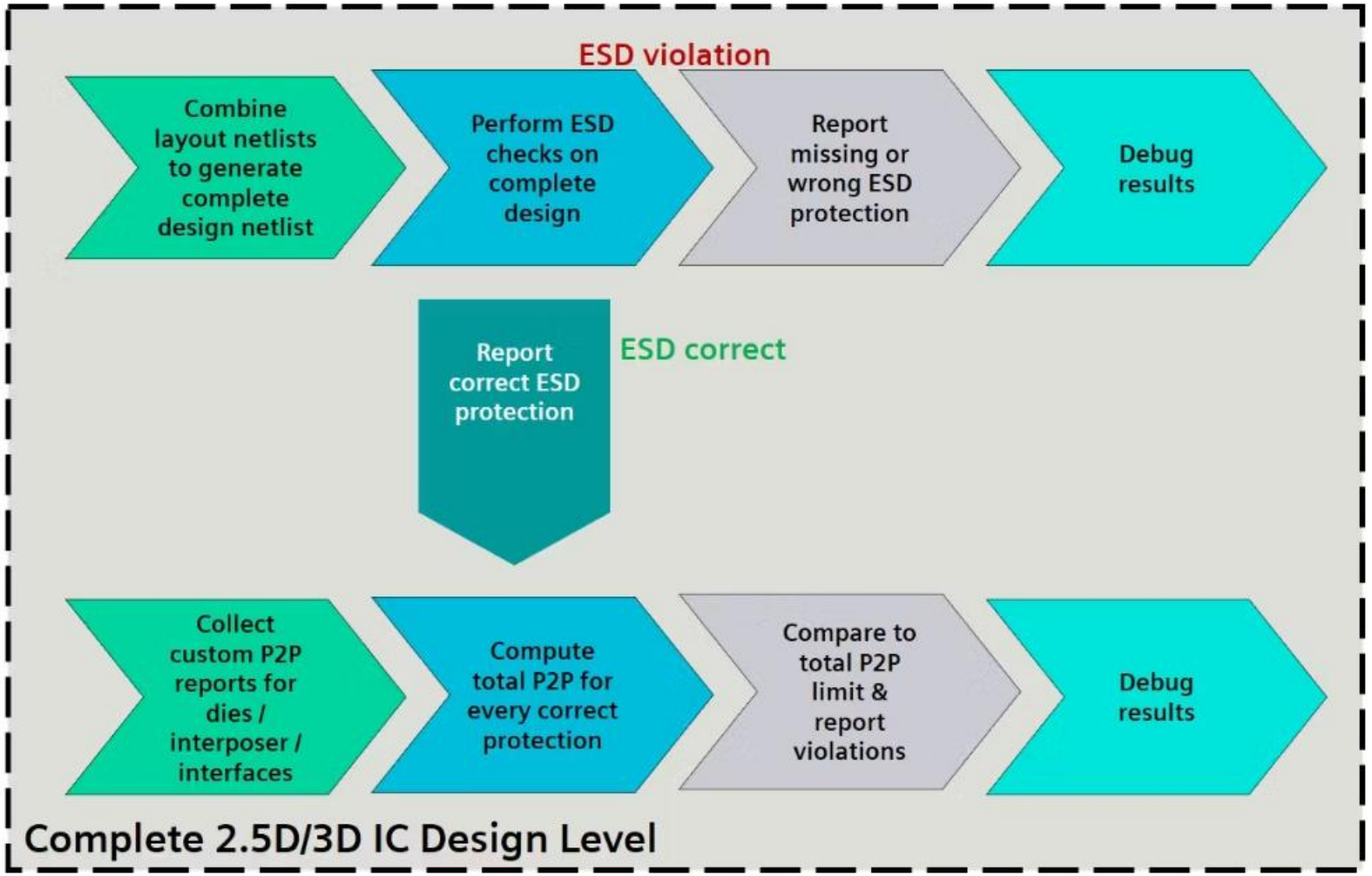
Candidate hot junction detection



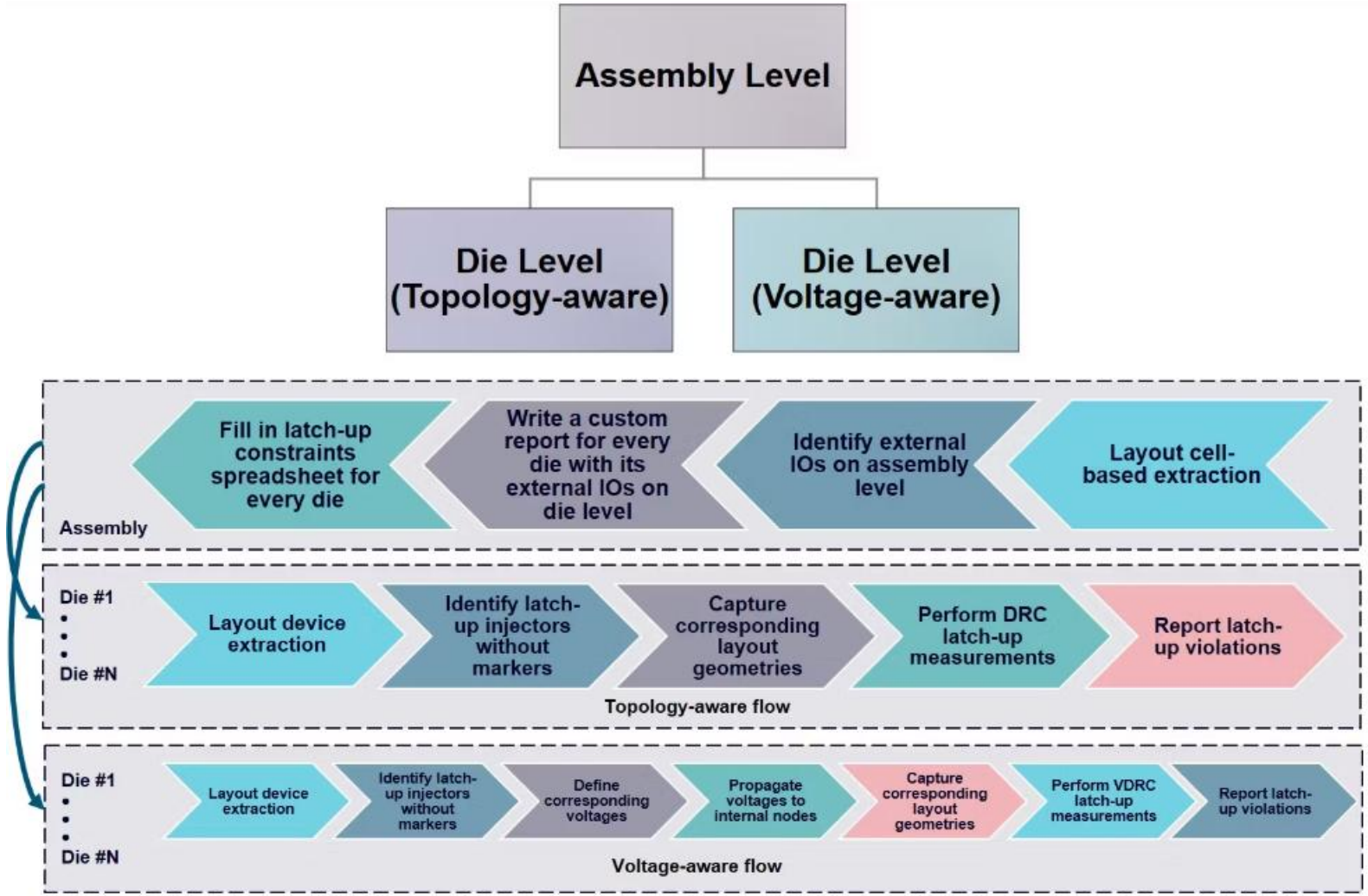
External IOs vs. internal IOs



2.5D/3D IC ESD verification methodology flow

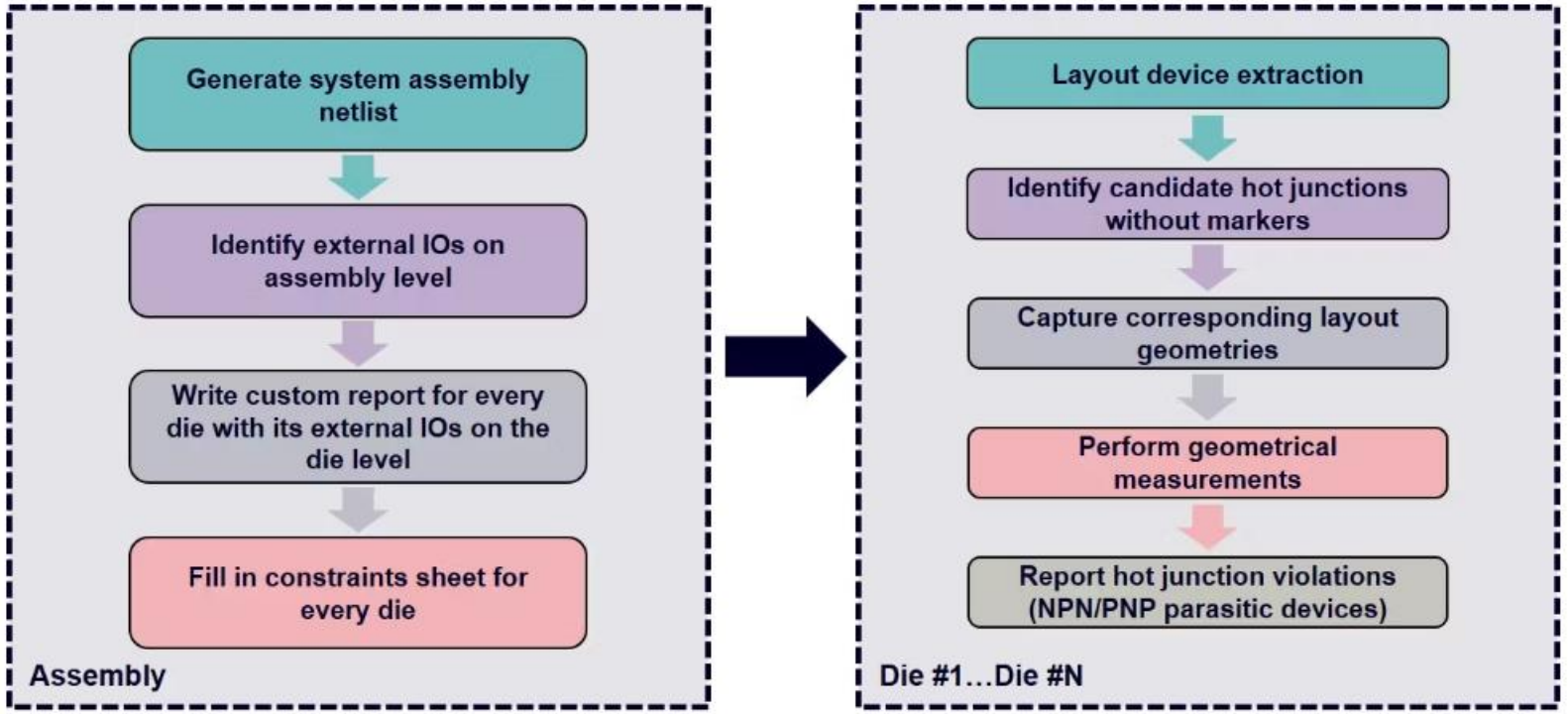


ESD design-level verification (complete 2.5D/3D IC)



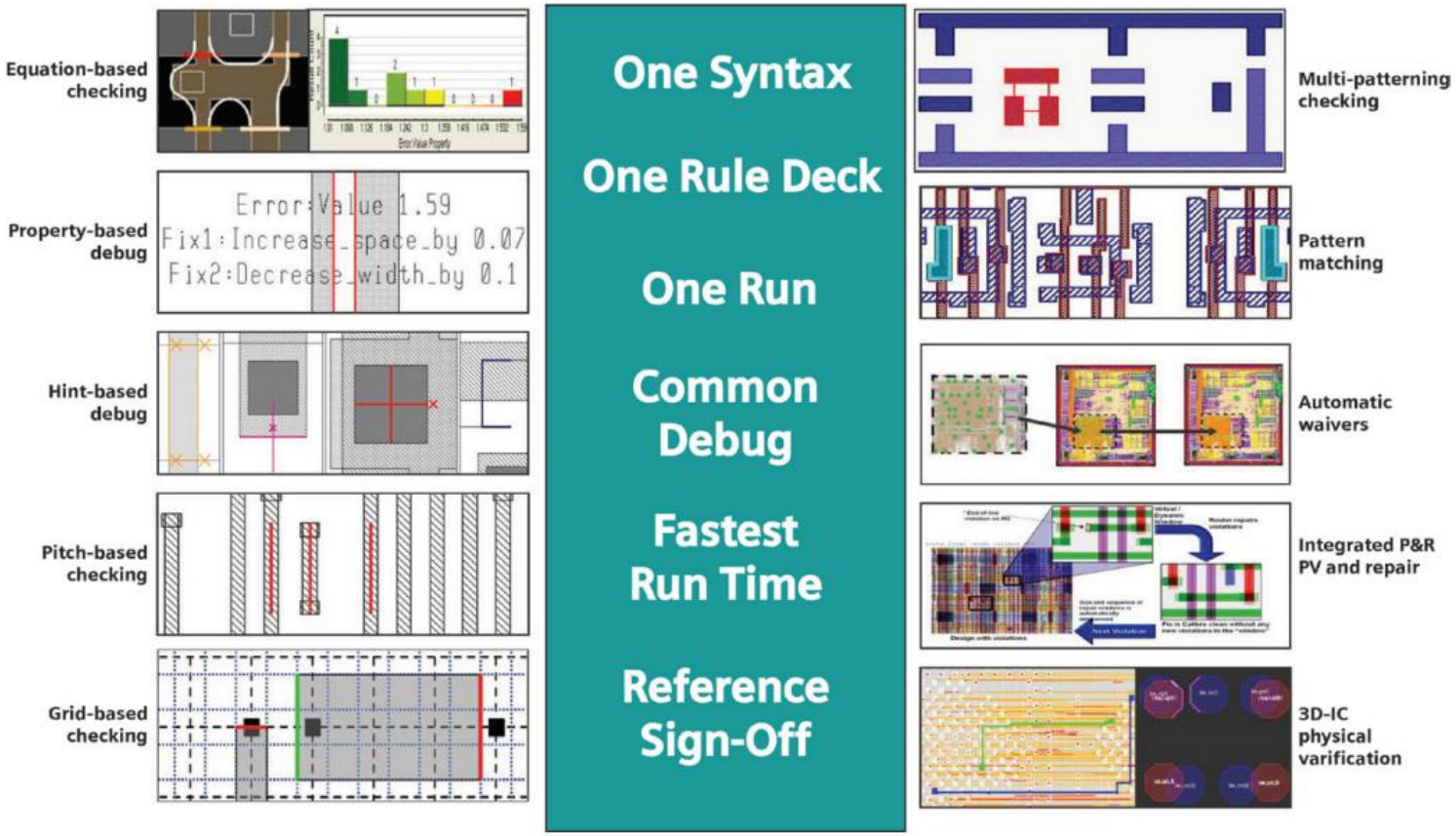
Latch-up design rule checking methodology and flows

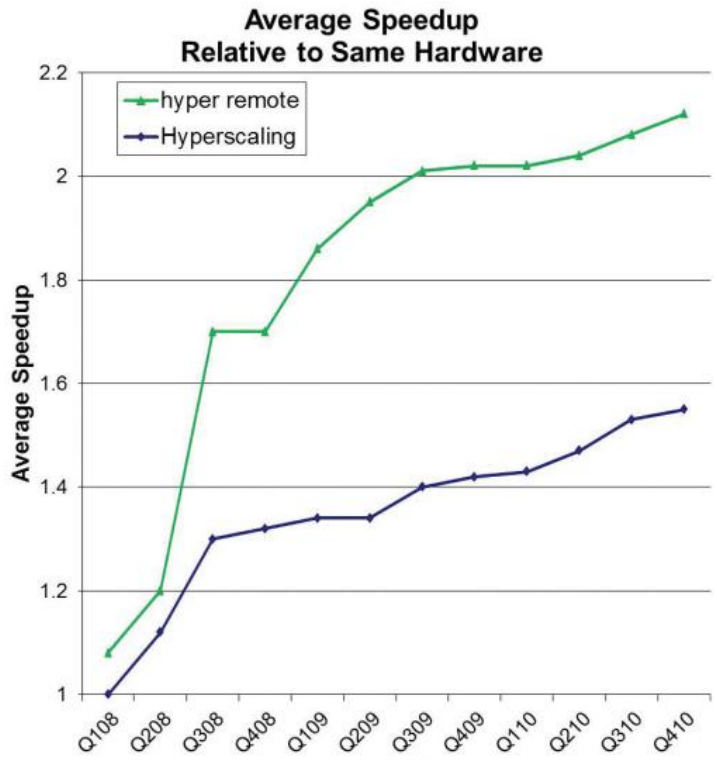
Calibre 3D IC
hot junction detection



Candidate hot junction detection methodology

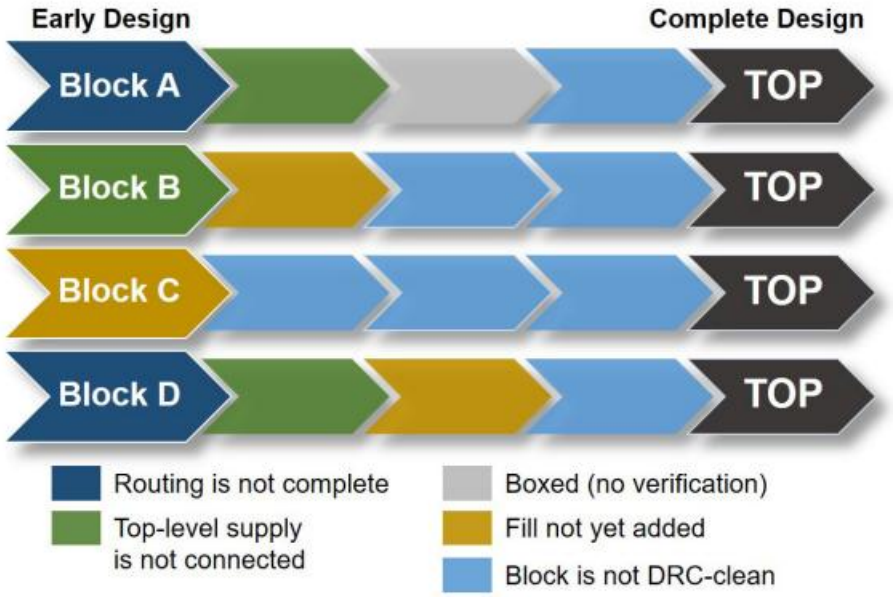
Physical Verification

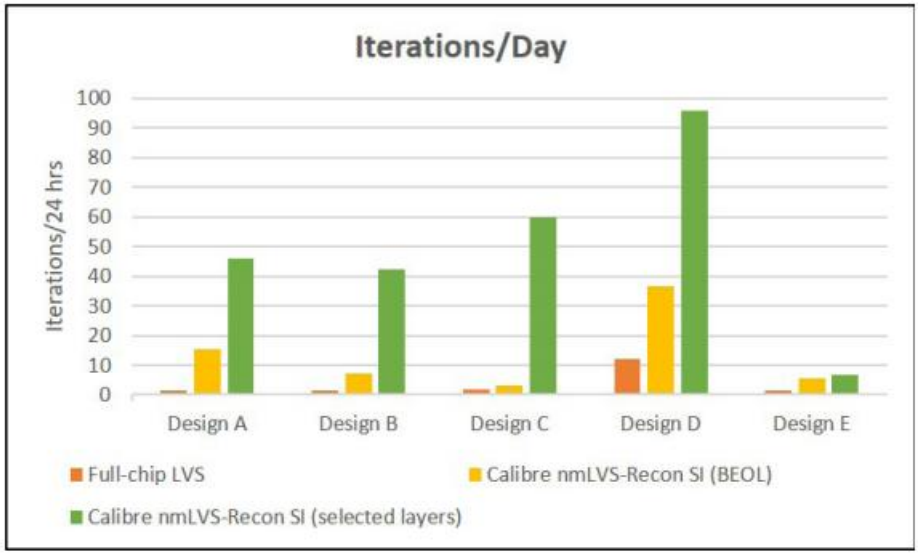




DRC provides fast, sophisticated, and proven technology that enables the fastest and most accurate physical verification of the most challenging designs at any node

Physical Verification
Early design circuit verification
LVS Recon SI

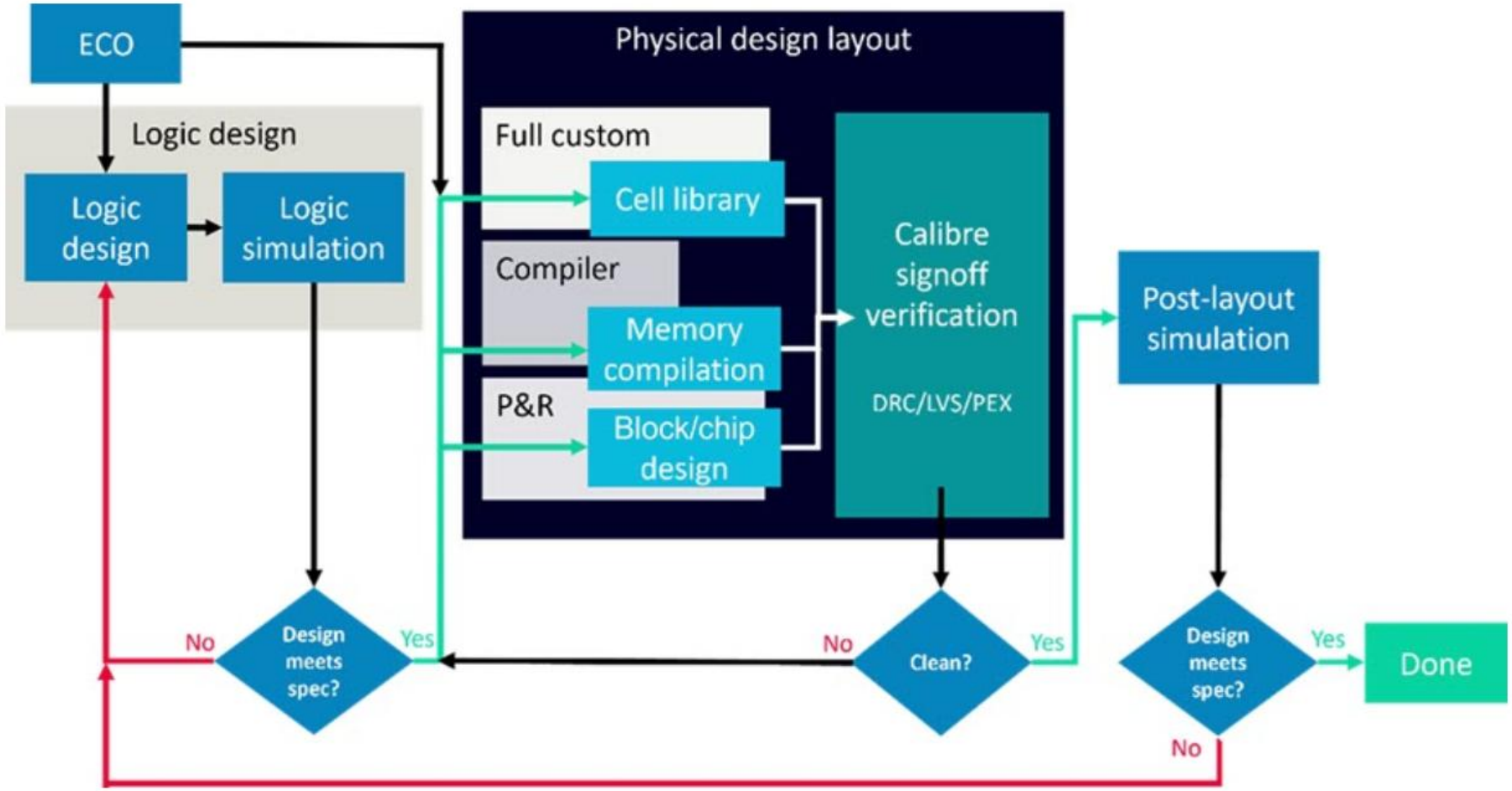




LVS Recon runs selected circuit verification early in the design flow, enabling designers to accelerate debug cycles and reduce the number of full-chip verification iterations

Selective connectivity extraction / Short isolation / Layer-aware short isolation / Net-aware short isolation / Custom short isolation / Fast, integrated debugging / Design process optimization

Calibre Physical Verification

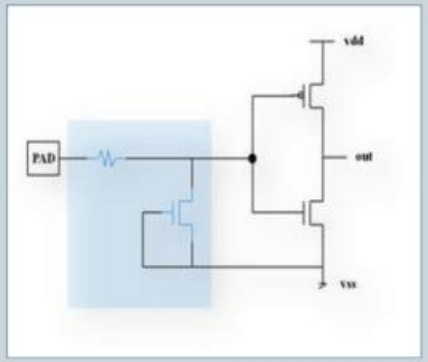


ACCURACY AND INNOVATION Preferred Foundry Sign-Off Tool

SVRF / Tcl Verification Format (TVF)/ Equation-based design rule checking / Optical grid and pitch checking / Pattern matching / Double patterning / Automated waiver management / Fast XOR / 3D-IC Physical Verification / Direct Database Access / HTML batch reports / RealTime / Dummy SmartFill DFM / Recon DRC

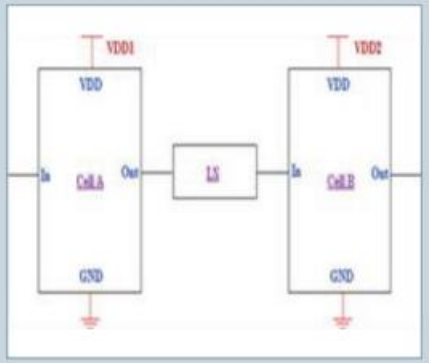
Calibre Physical Verification PERC
Advanced reliability verification

Custom



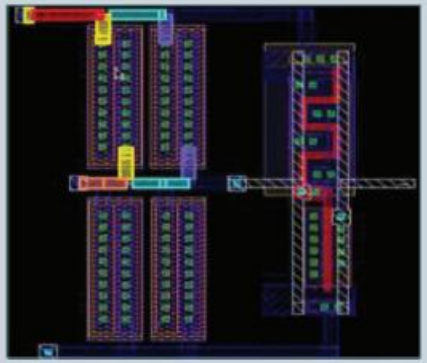
- Electrostatic discharge (ESD) checking
- Electrical overstress (EOS) checking

Digital



- Cross-power domain checking
- Low power verification

Post-layout



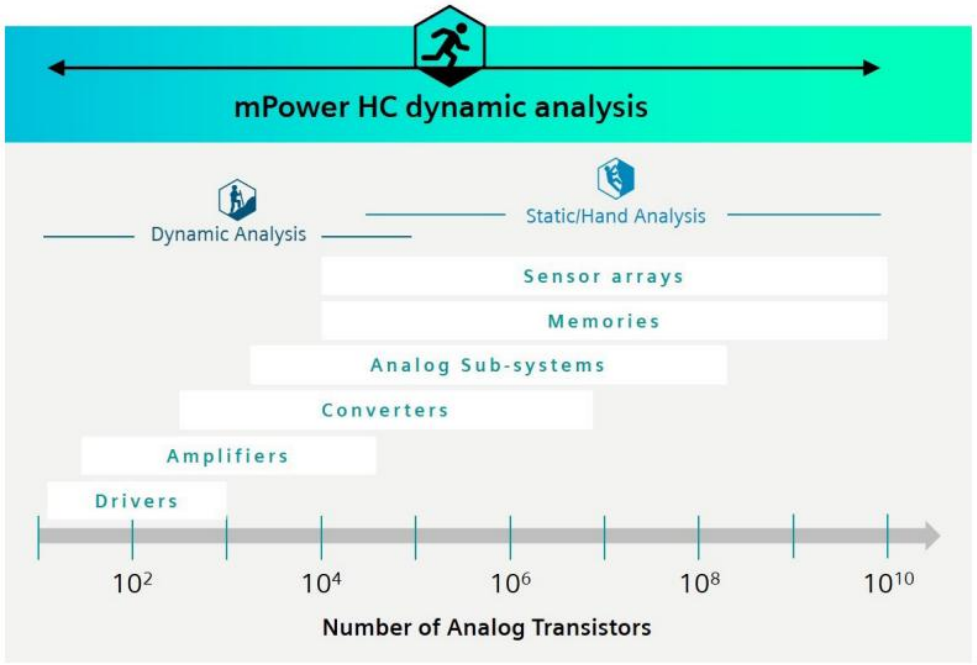
- Point-to-point resistance
- Current density
- Voltage-dependent DRC

PERC enables a wide range of complex electrical and geometrical verification requirements to ensure product reliability and performance

Circuit reliability verification /Electrical overstress / Electrostatic discharge / Multiple power domains / Post-layout verification :

- Point-to-Point resistance (P2P)
- Current Density (CD)
- Voltage-Dependent DRC
- Hot gate/diffusion identification
- Layer extension/coverage
- Device matching

Physical Verification mPOWER
Power integrity solution



The synchronized quad-view **mPower GUI** simplifies and streamlines debugging and analysis

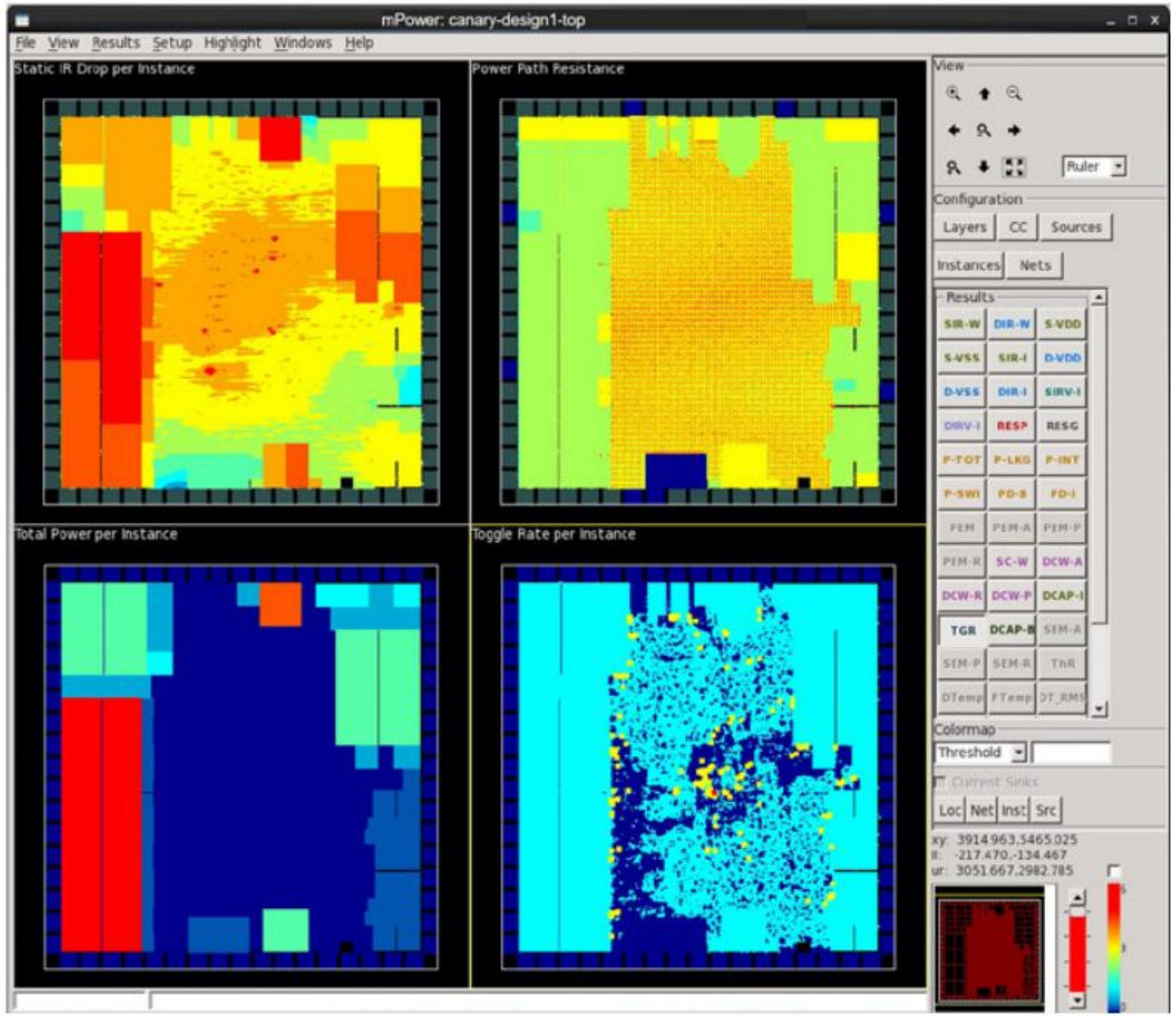
The **mPower power integrity solution** enables design teams to provide complete, high-confidence power coverage for all designs at any scale within their existing design and verification flows.

mPower Analog:

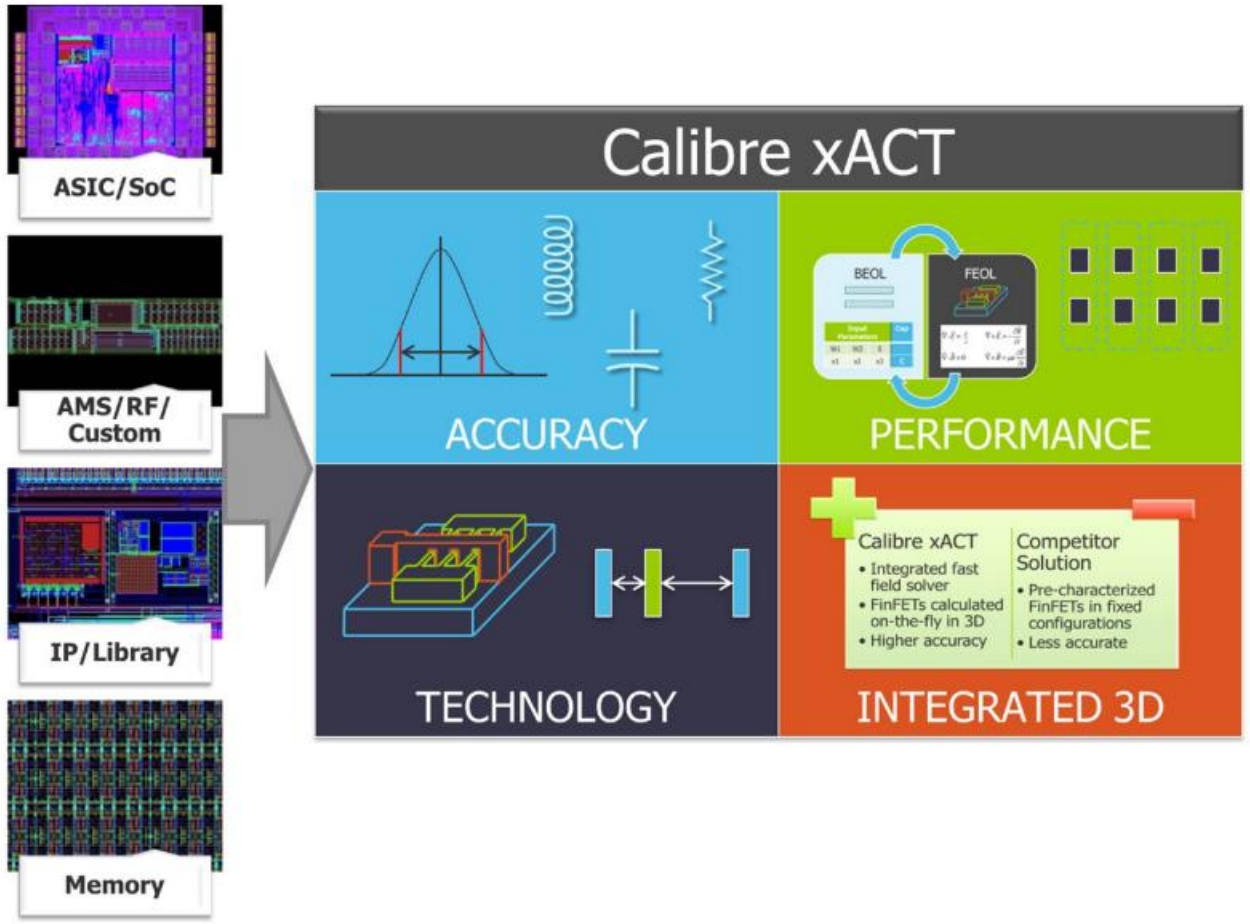
- Simulation-based, high-capacity dynamic **EM/IR** drop analysis
- Schematic and post-layout simulation waveforms

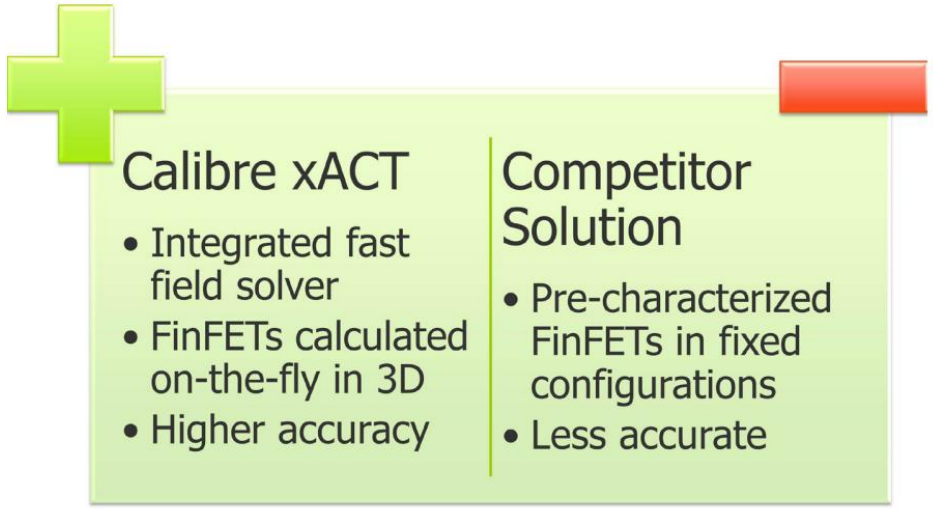
mPower Digital:

- Chip power modeling and packaging flows
- Vectored and vectorless analysis



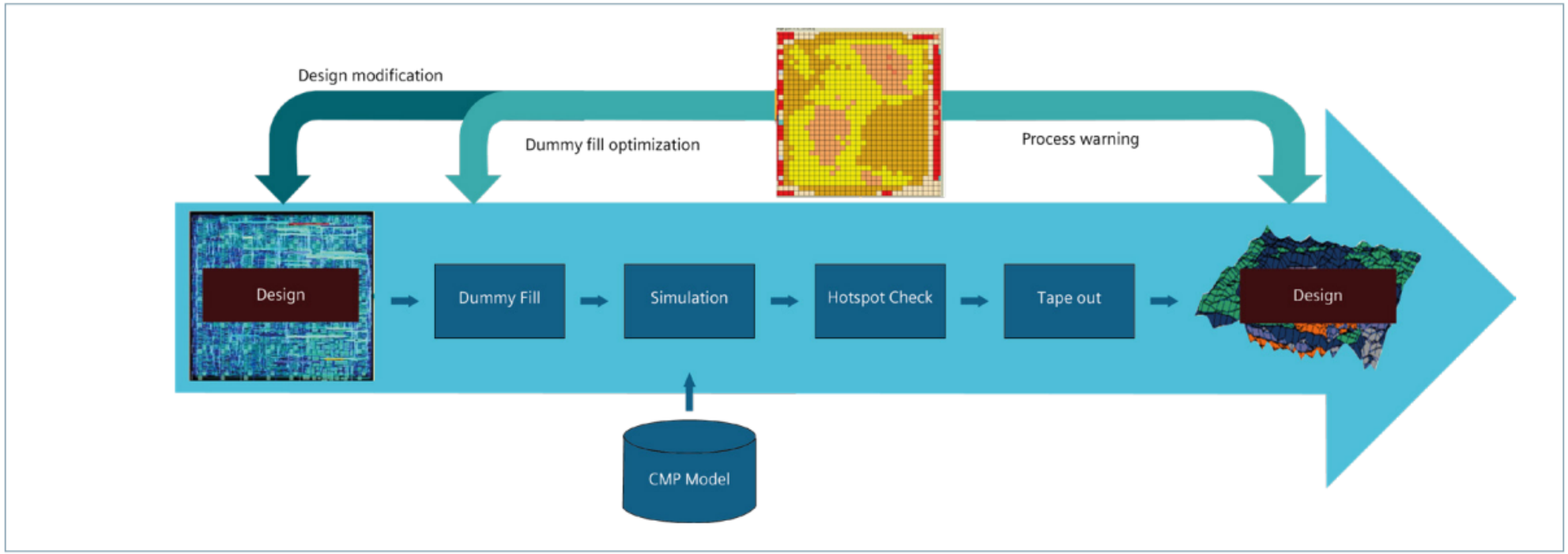
High coverage vectorless analysis
RTL profiling and vectored analysis

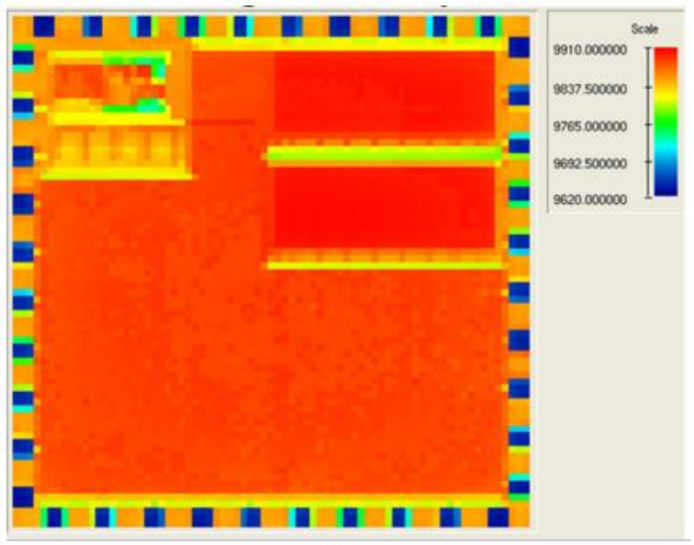


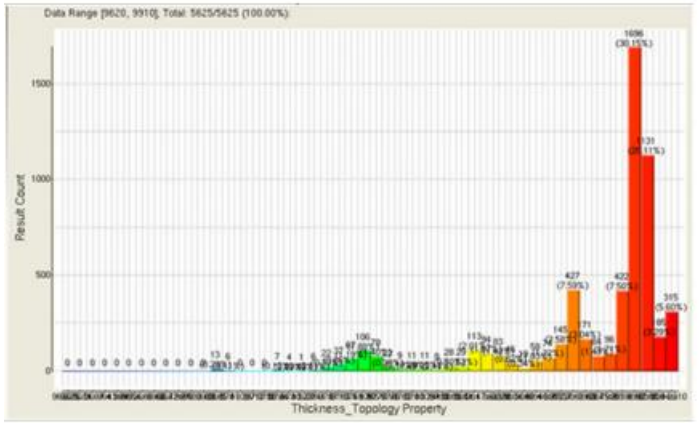


xACT platform quickly and accurately, **extracts parasitic capacitance, resistance and inductance** for a variety of IC design styles, from digital to custom analog and RF.

Physical Verification
CMP Analyzer simulations



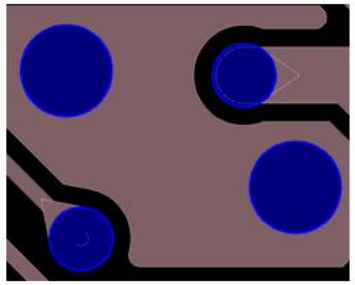
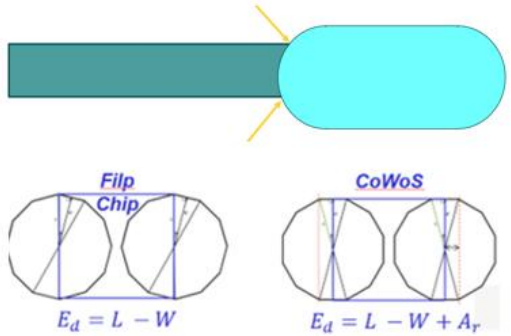
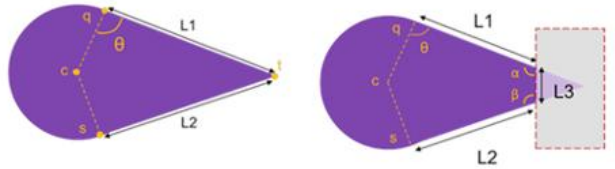
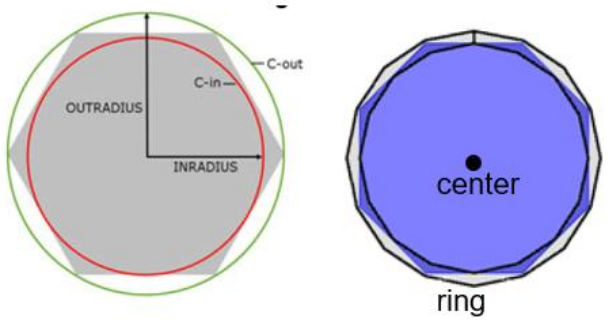
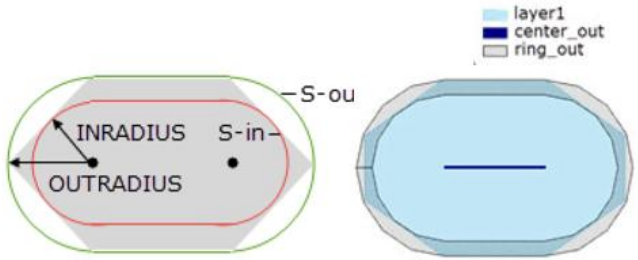
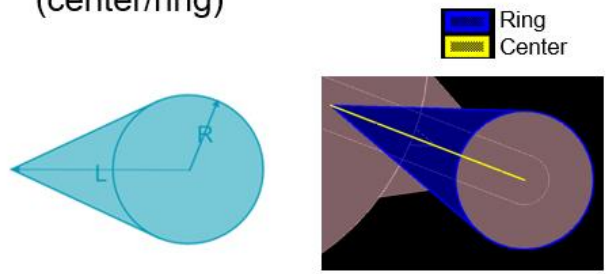




Surface planarity improvement by **dummy fill** optimization for M1 layer of a design with 5 layers

Calibre Capabilities to Simplify Irregular Shape Checking

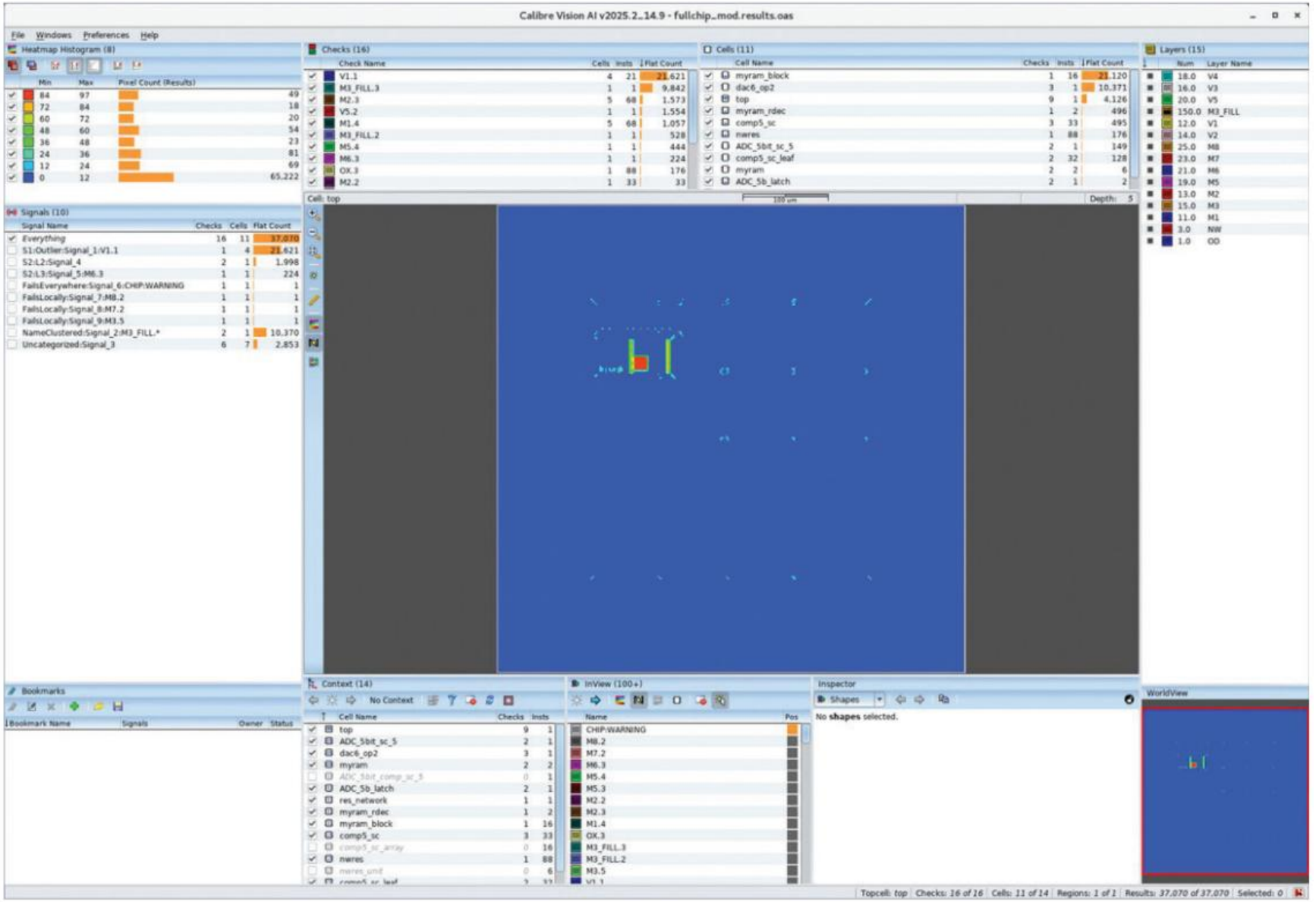
Photonics, through-silicon via, & packaging checks

	Circle	Stadium	Teardrop
Recognize & separate	• INSIDE CELL [NOT] CIRCLE 	• INSIDE CELL [NOT] STADIUM 	• INSIDE CELL [NOT] TEARDROP 
Check Dimension & Ref Output	• DFM CIRCLE ANALYZE • DFM CIRCLE ANALYZE (center/ring) 	• DFM STADIUM ANALYZE • DFM STADIUM ANALYZE (center/ring) 	• DFM TEARDROP ANALYZE • DFM TEARDROP ANALYZE (center/ring) 

Calibre Vison AI

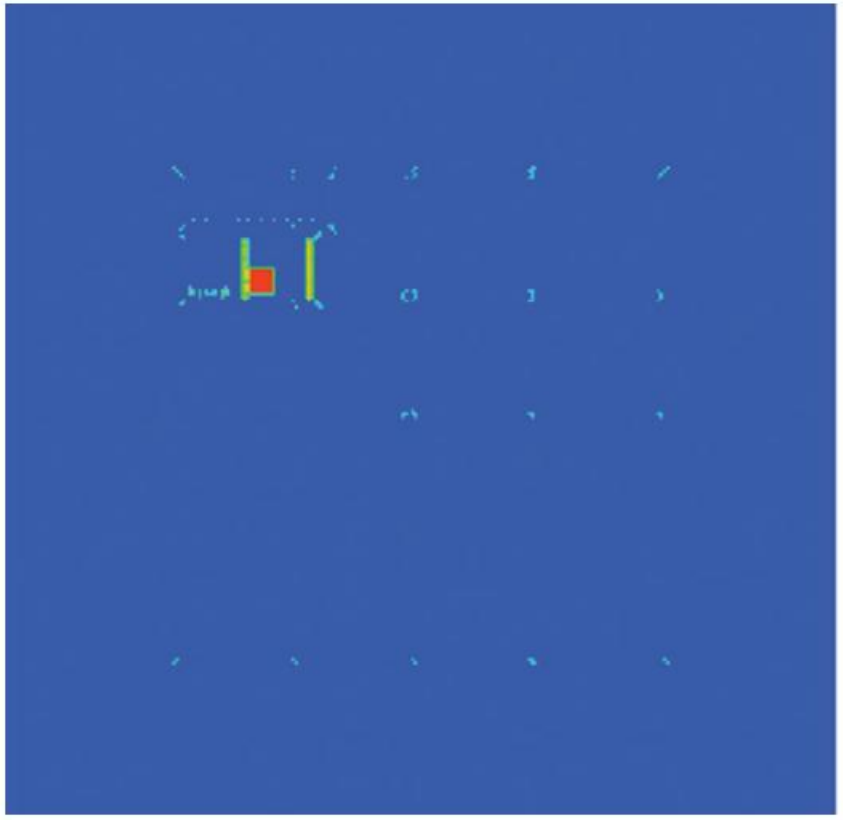
Features

- High-speed processing of massive violation databases
- Full-chip visualization with intelligent violation density heatmap
- AI-powered “Signals” for automatic violation clustering
- Dynamic analysis panels with real-time updates
- Hierarchical debug capabilities for precise violation isolation
- Seamless integration with industry standard design tools
- Shareable debug states and analysis context

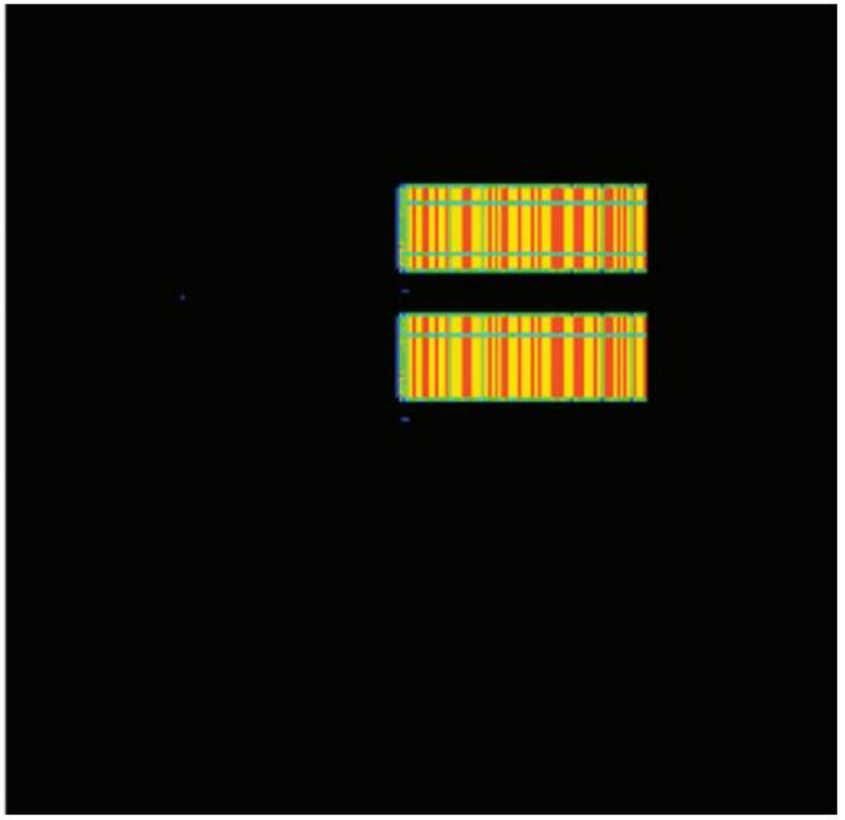


Multi-view debug environment showing synchronized views of violation density heatmap, detailed layout and analysis panels

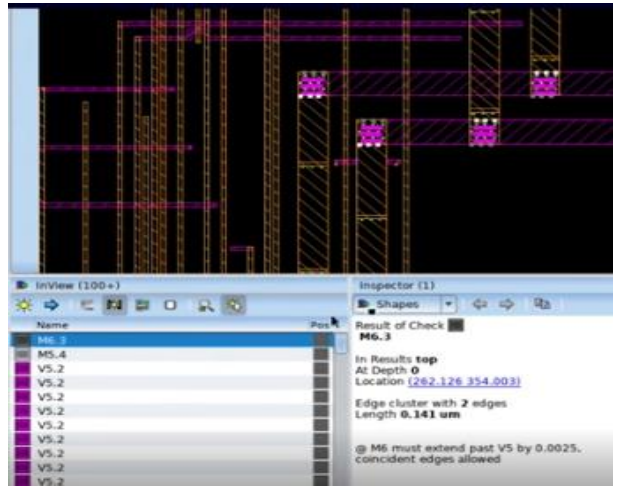
Calibre Vision AI
Advanced **DRC debug** and analysis



Left image shows the heatmap for all checks



Rright side image shows the heatmap from a selected Signal group



- **AI/ML-powered DRC analysis and intelligent clustering**
- **Full-chip visualization and interactive analysis**
- **Integration, interoperability and collaboration with P&R tool**

cadence

Cadence Tool Experience

Tools Used:

PVS / Pegasus – Physical Verification System & signoff (+ MDP Photomask preparation)

Assura – writing DRC/LVS rule decks and performing layout verification at block level

- Virtuoso Schematic Editor & Virtuoso Layout Suite
- SKILL Language Programming of Parameterized Cells(Pcells)

Quantus QRC – Parasitic extraction

Voltus / EMIR – Power, Electromigration models simulation, IR drop analysis

- EMX simulator GUI / EMX Planar 3D Solver & Voltus InsightAI
- Voltus IC Power Integrity Solution
  - *Fast incremental analysis*
  - *IR drop diagnostics*
  - *Multi-method fixing*
  - *Seamless integration*

Strengths & Achievements

Key Achievements:

Reduced signoff runtime by 30% using optimized PVS multi-thread flow

Customized DRC/LVS runsets aligned with foundry standards (i.e. TSMC 28nm, 7nm)

Collaborated with DFM/Mask teams for tape-out verification

Experienced in both **frontend** (Physical Verification) and **backend** (mask preparation, data verification)

Cadence® Pegasus Design Review Environment

The Pegasus Design Review Environment rapidly loads large layouts (GDSII, OASIS®, LEF/DEF, MEBES, and other industry- standard formats) providing a rich set of debugging and inspection features, including measurement, dynamic visualization, multi-database overlay, net connectivity tracing, cross-section viewing, and GDSII/OASIS editing.

Pegasus Layout Pattern Analyzer

Improve systematic and parametric yield and meet foundry DFM signoff requirements

Pegasus CMP Predictor

Predict and reduce systematic and parametric variability at chip- and wafer-level due to CMP-induced topography and layer thickness variations

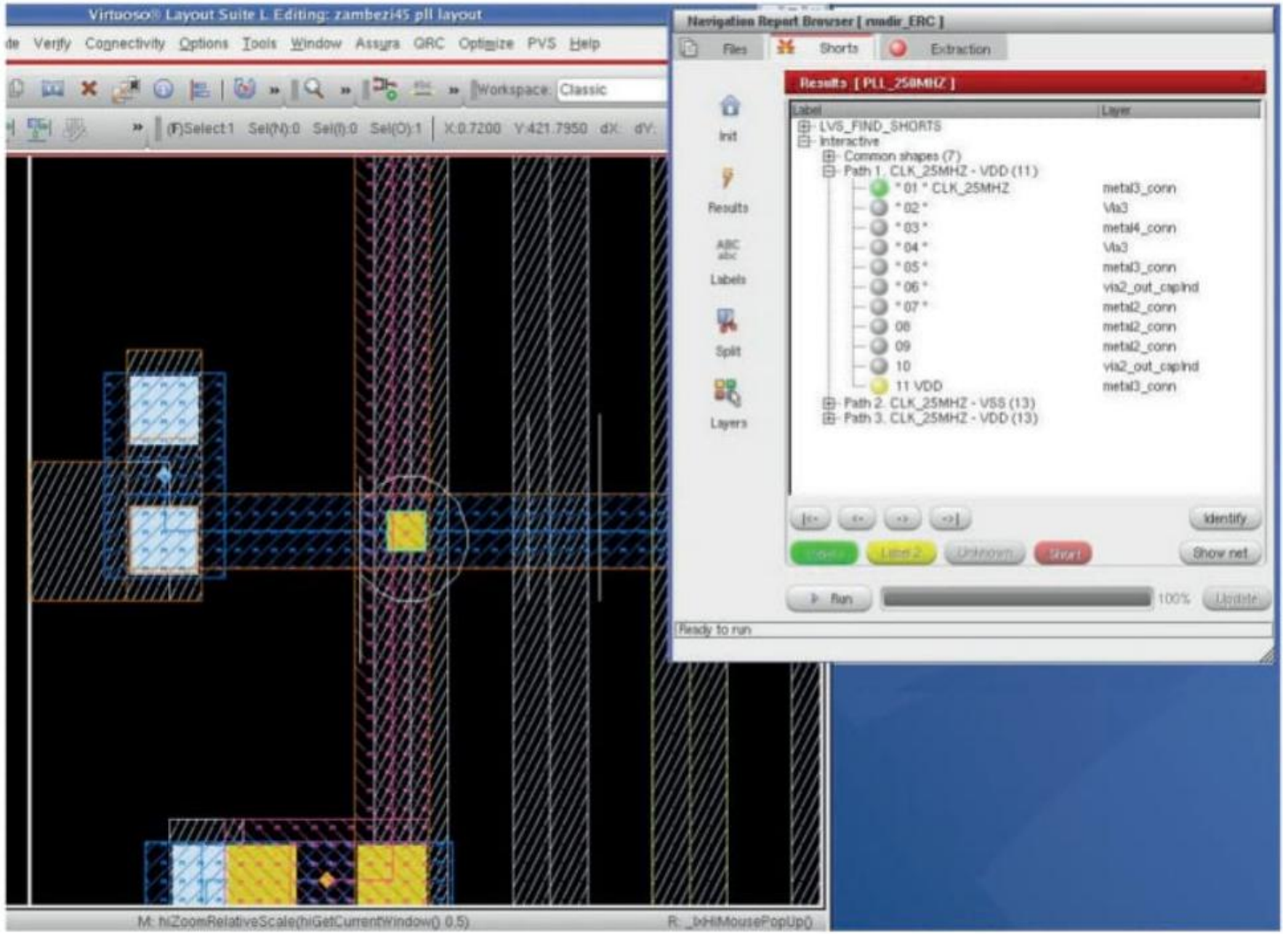
Pegasus Computational Pattern Analytics

High-performance production-proven layout processing

Pegasus Critical Area Analyzer

Estimate random yield loss and assess layout robustness against random defects

The Interactive Short Locator running within the Virtuoso Layout Editor



DRC Runtime in seconds with Virtuoso PVS

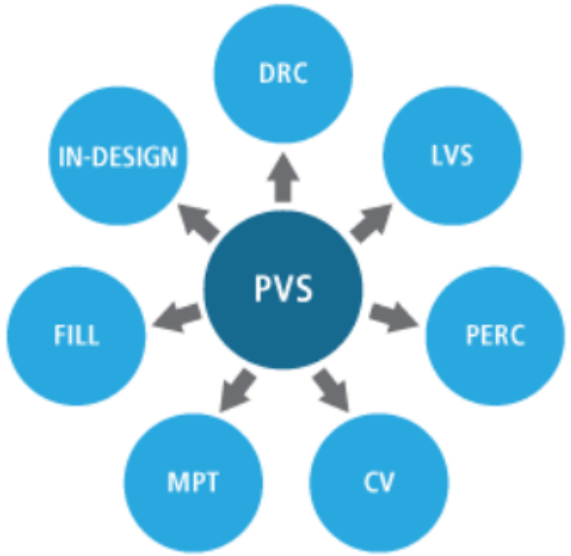
DRC Runtime in Seconds with Virtuoso® Integrated Physical Verification System (IPVS)

Innovus™/PVS DRC

Automated DRC Fixing

Track-Based Fill

ECO, Timing-Aware Metal Fill



3D Devices/FinFET, 3D-IC/TSV

Voltage-Dependent Rules

Multi-Pattern Decomposition

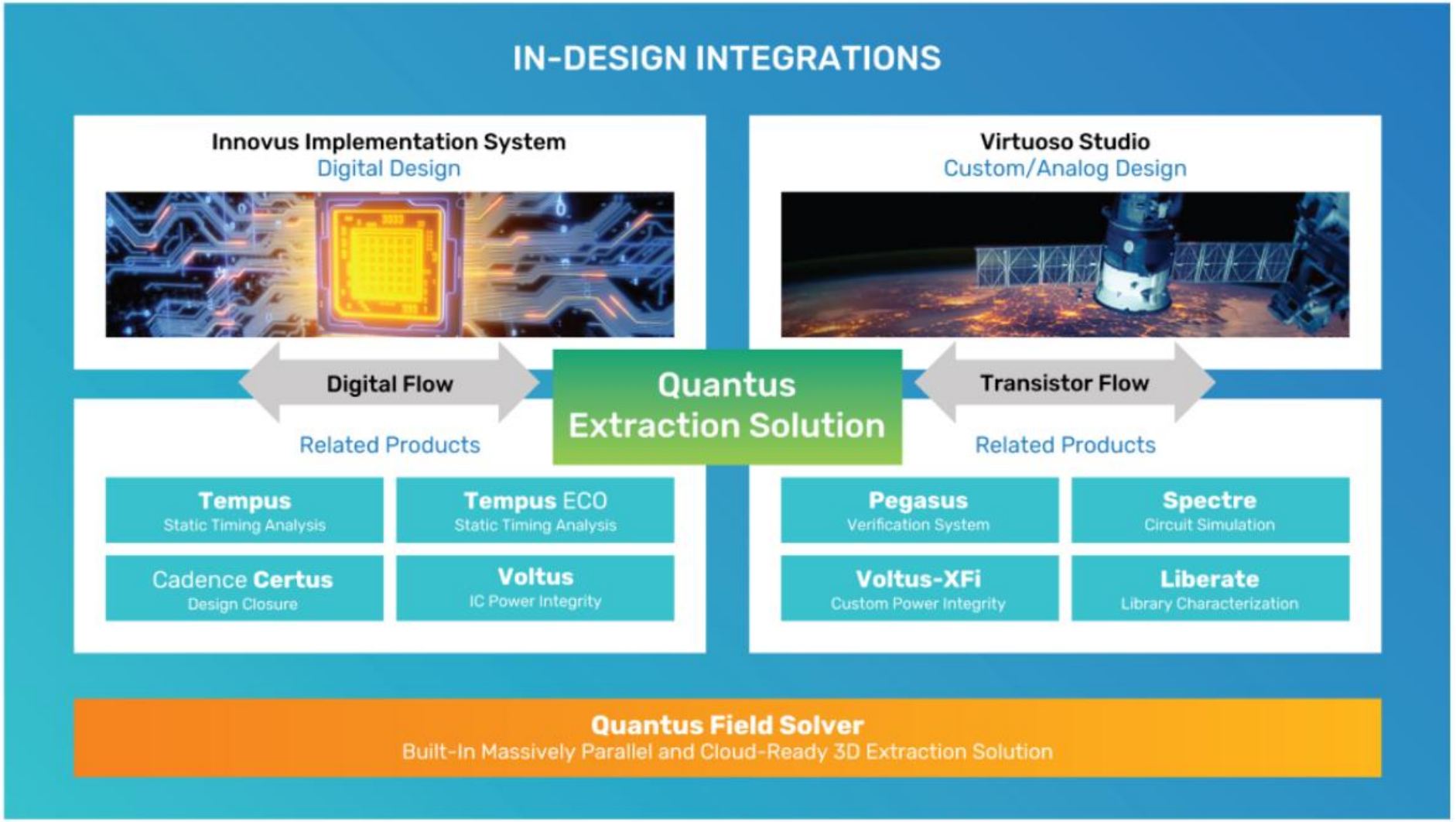
Programmable ERC (PERC)

Full-Chip Review/Finishing

Mixed-Signal Constraint Validation

With PVS, the flow supports double patterning, triple patterning, quadruple patterning, 3D-IC and FinFET rules, advanced device extraction, and extends physical verification technology into design reliability checking and constraint validation

IN-DESIGN INTEGRATIONS

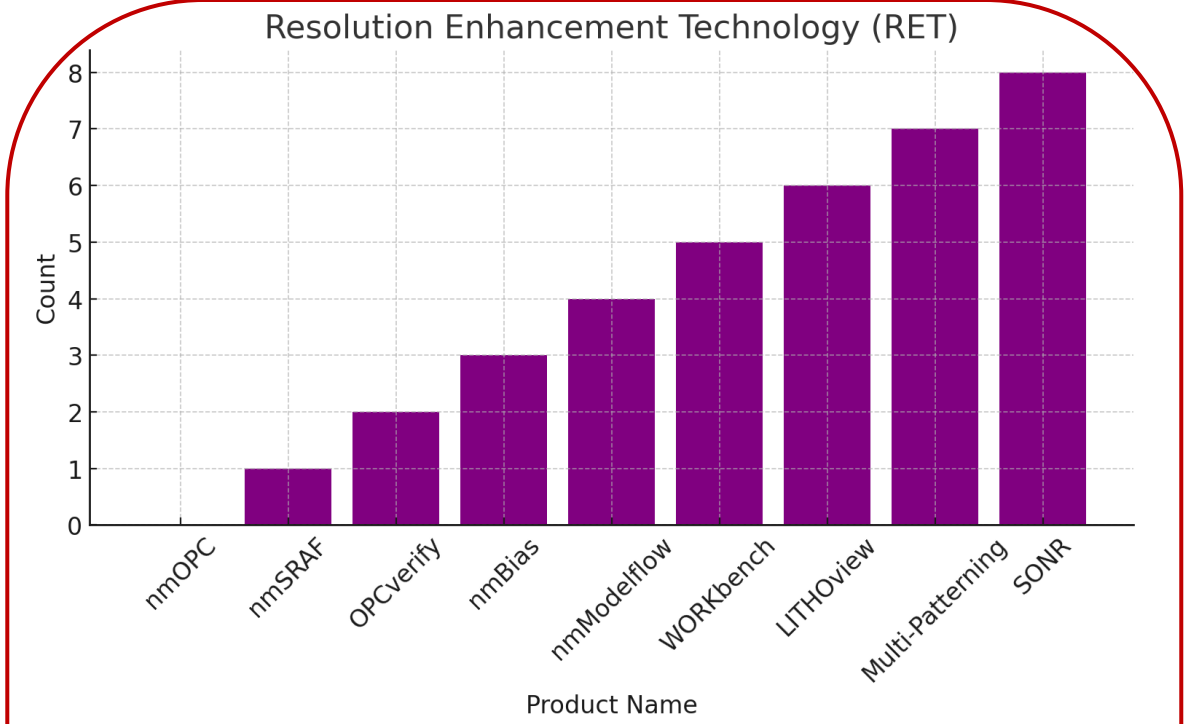


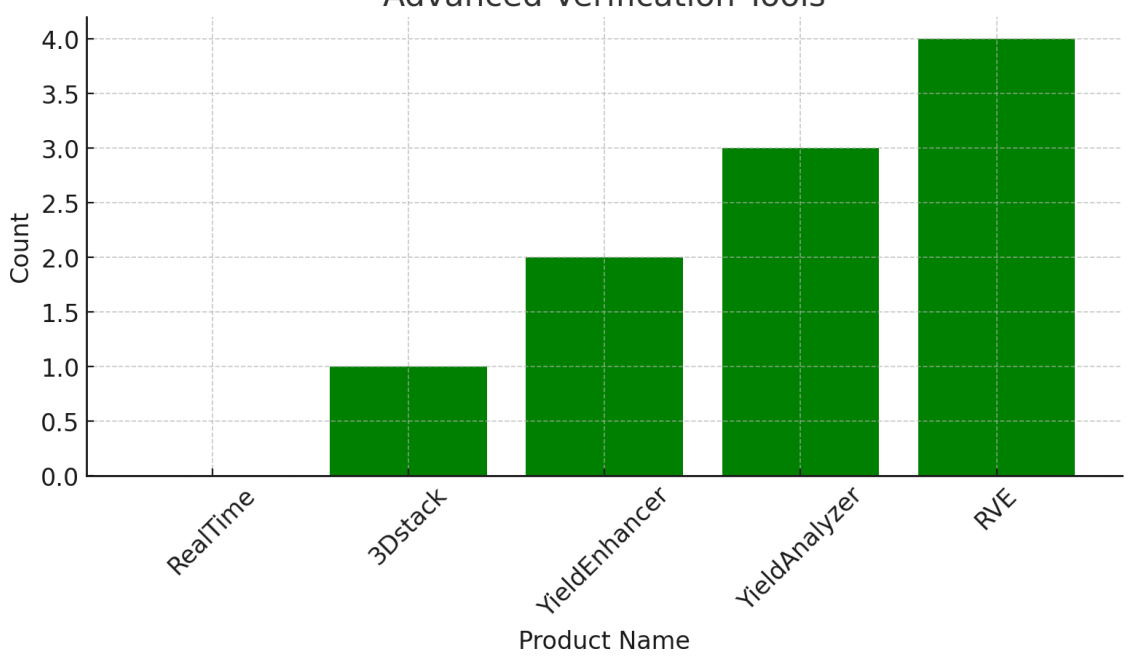
The **Quantus Extraction Solution** is tightly integrated with the Innovus Implementation System for digital designs and Virtuoso Studio for custom /analog designs. Quantus also offers **Quantus Field Solver**, a cloud-ready extraction tool delivering unmatched accuracy.

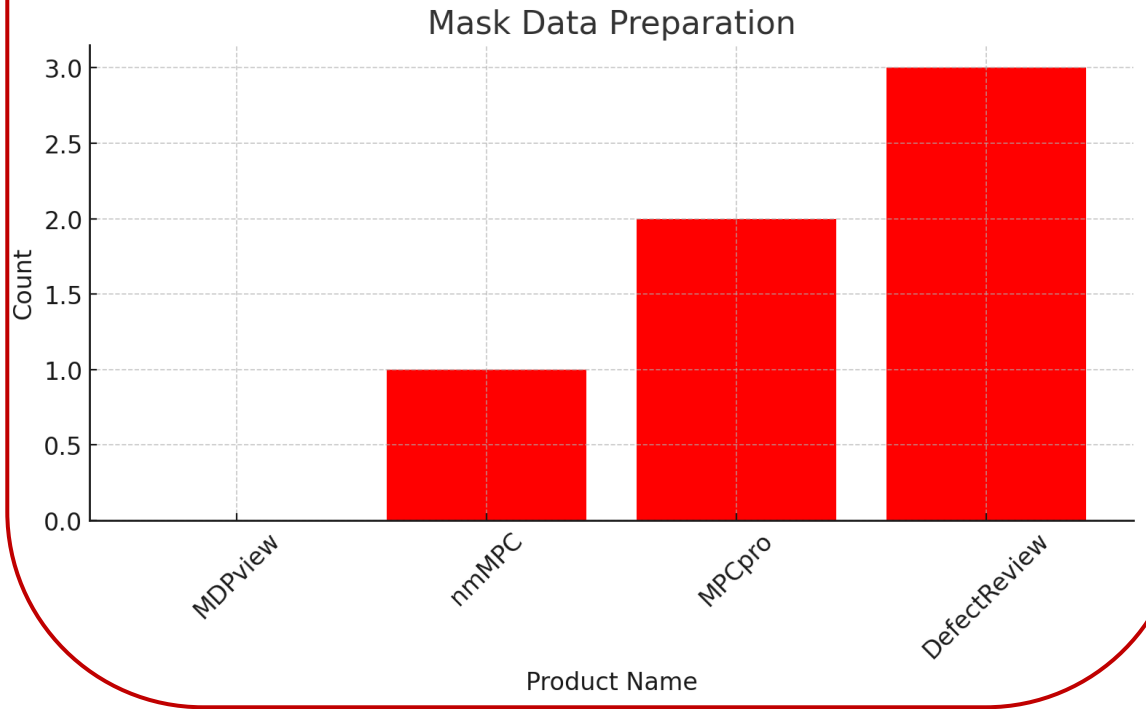
Backend manufacturing

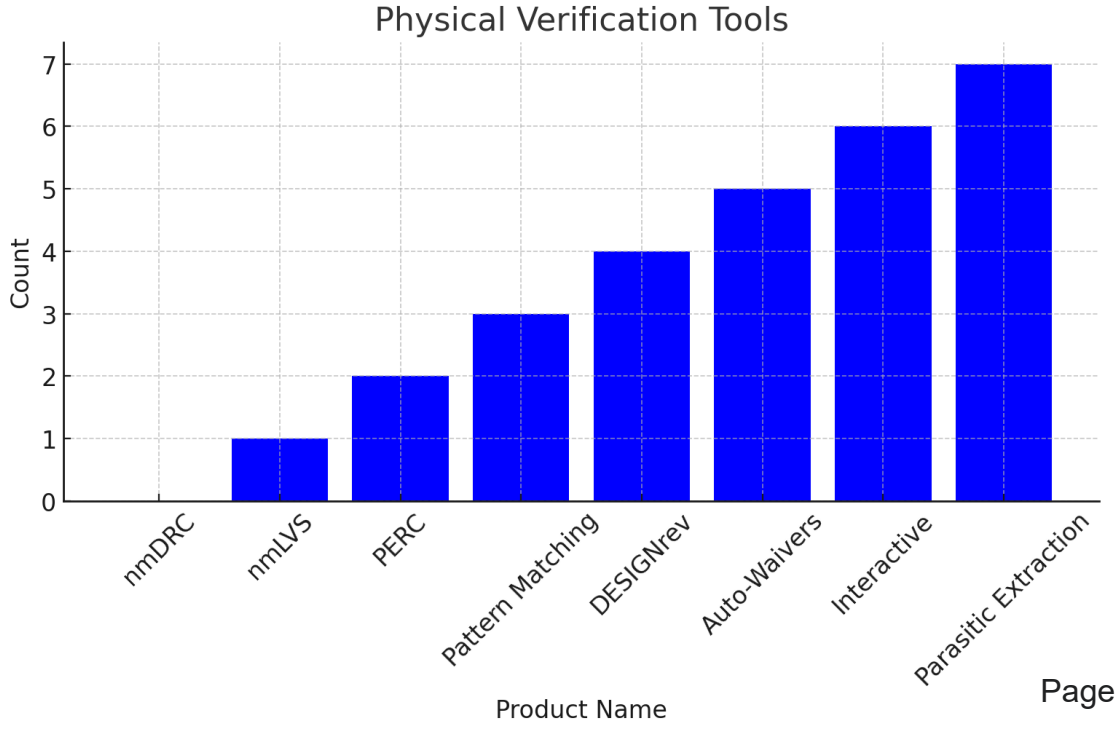
- Focused on manufacturing-oriented engineering using Calibre RET/OPC and lithography workflows for top European foundries.
- Executed ILT/OPC simulation, OPC-Verify checks, multi-patterning analysis, and SRAF optimization for next-generation nodes.
- Built manufacturable layout strategies and improved wafer pattern fidelity through lithography modeling and process-aware tuning.
- Developed and validated MDP/JobDeck structures, including MPC, ModelFlow, LithoView, and Workbench integrations.
- Supported GlobalFoundries, STMicroelectronics, Infineon, and Intel via on-site guidance, remote troubleshooting, and lithography engineering collaboration.

Calibre Products Portfolio
Backend manufacturing

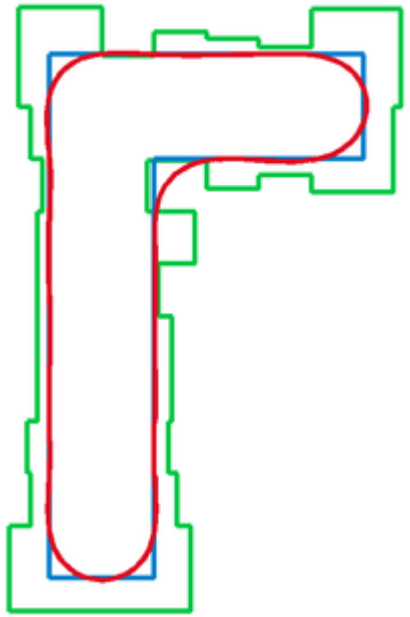








Calibre OPC - Inverse Lithography Technology



A conventional optical proximity correction. The blue Γ-like shape is what chip designers would like print on the wafer, in green is the shape after applying optical proximity correction(OPC), and the red contour is how the shape is actually printed.

In semiconductor device fabrication,
The **inverse lithography technology** (**ILT**) is an approach to photomask design.

An approach to solve an inverse imaging problem: to calculate the shapes of the openings in a **photomask ("source")** so that the passing light produces a good approximation of the **desired pattern ("target")** on the illuminated material, typically a **photoresist.**

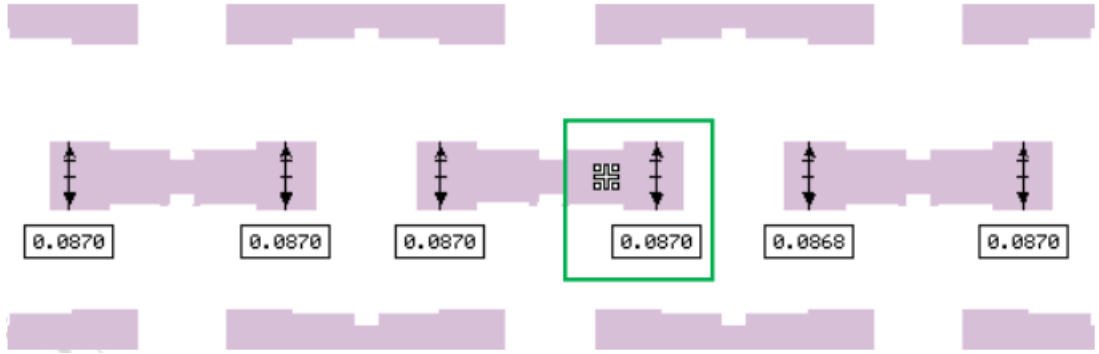
As such, it is treated as a mathematical optimization problem of a special kind, because usually an analytical solution does not exist.

In conventional approaches known as the optical proximity correction (OPC) a "target" shape is augmented with carefully tuned rectangles to produce a "Manhattan shape" for the "source", as shown in the illustration.

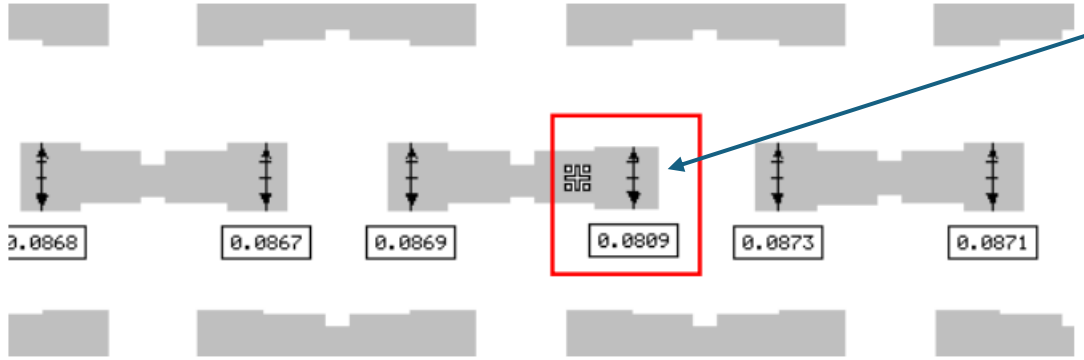
The ILT approach generates curvilinear shapes for the "source", which deliver better approximations for the "target".

Calibre OPC outcome – Inconsistency

OPC -1x1mm^2 widow clip

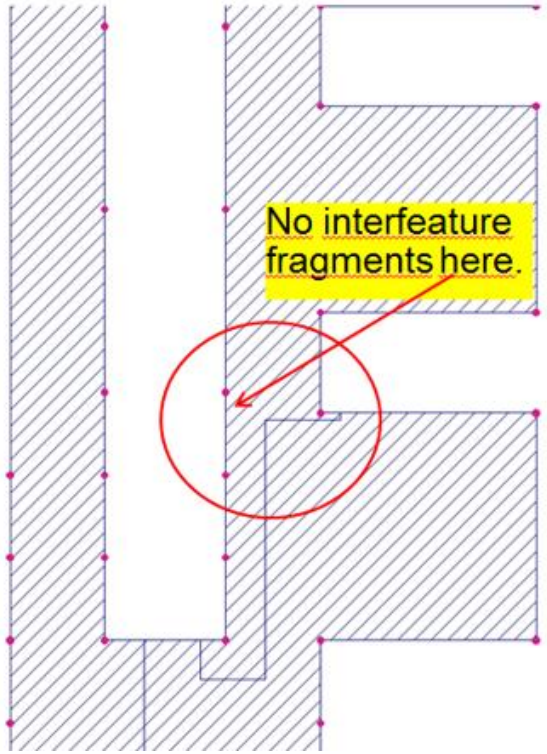


2x2mm^2 window clip error

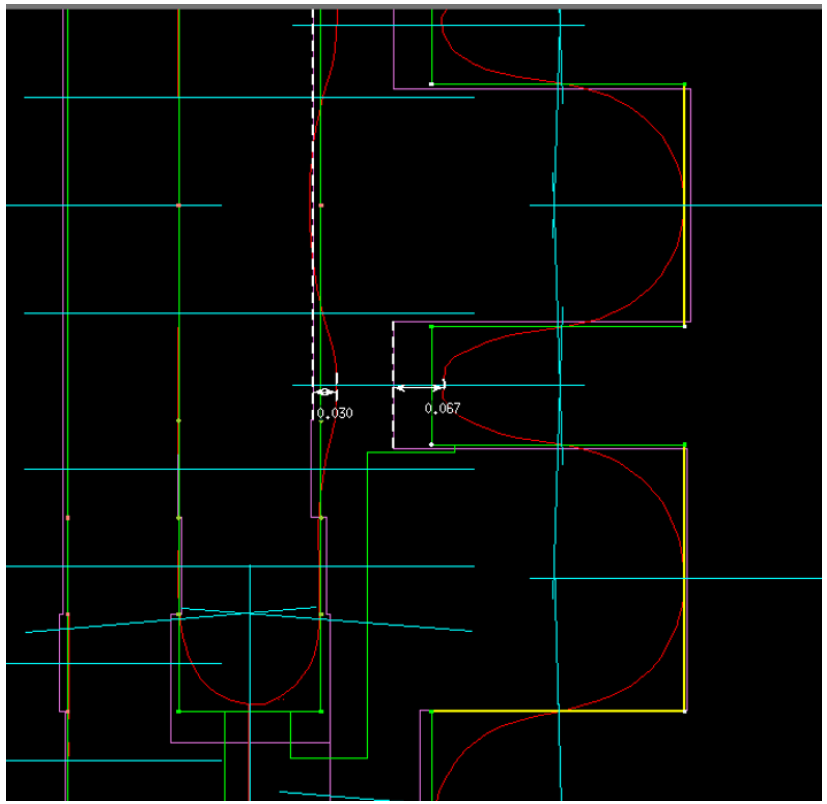


"The edge **post-OPC** feature appears to be undersized. The CUT layer analysis indicates post-OPC mask errors, as expected. The observed CD (~81 nm) deviates significantly from the target CD (~87 nm),
with no apparent justification for the observed asymmetric shape."

Calibre OPC – No ripple generation observed due to the absence of inter-feature fragments



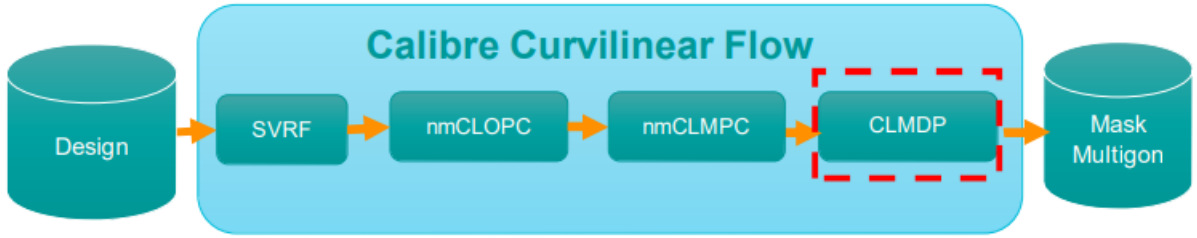
OPC simulation



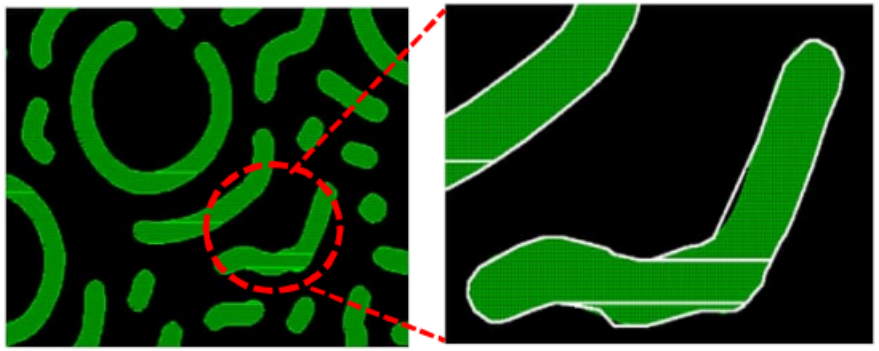
A conventional optical proximity correction. The green Γ-like shape is what chip designers would like printed on the wafer, in purple is the shape after applying optical proximity correction(OPC), and the red contour is how the shape is actually printed.

Calibre Curvilinear MDP Support New Fracture Formats for Multigons

- The Calibre Curvilinear MDP solution enables the support of new Multibeam formats in the fracture and verification flows.



- Calibre Fracture commands are updated to support the new Multibeam fracture formats.
  - `FRACTURE NUFLARE_MBF` now supports version 2.1.
  - `FRACUTER OASIS_MBW` now supports version 3.0.

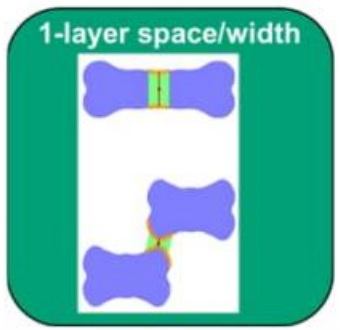


MBW 3.0 fracture output **Zoomed-in**

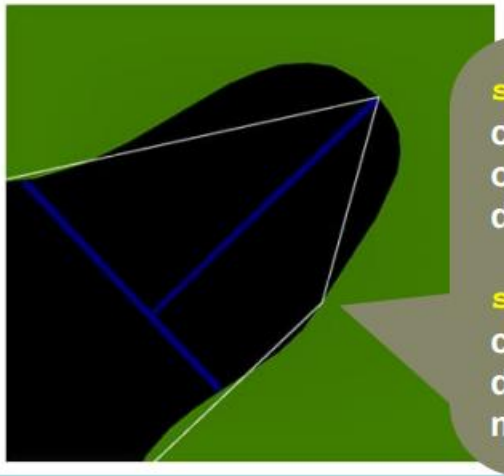
Calibre OPCverify Curvilinear Verification for Multigons

- Calibre OPCverify is updated to address the challenges of curvilinear verification for multigons.
- In 2024.4 release, four spline-based checks are production released to support post-OPC verification on multigon layers.

Distance checks on a multigon layer using `spline_distance` command.



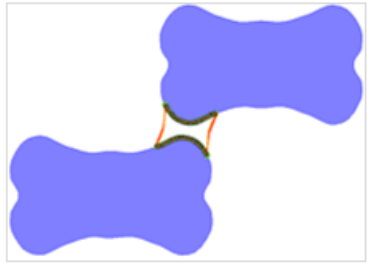
Angle check on a multigon layer using `spline_angle` command.



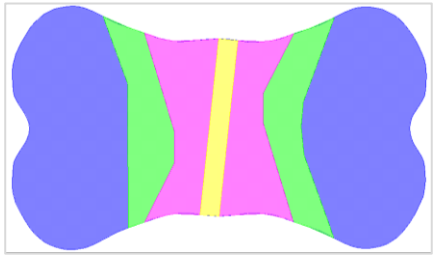
`spline_depth_width` checks minimum width of a multigon using its depth as a constraint.

`spline_dw_ratio` checks the maximum depth-to-width ratio for multigons on a layer.

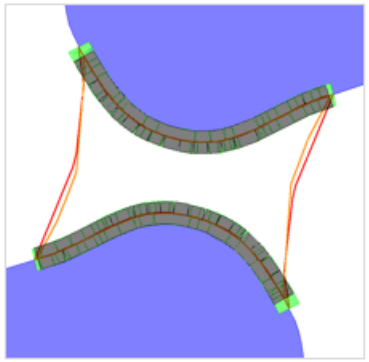
Calibre OPCverify Multigon Support - spline_distance check



Red—SD, non-Manhattan region
Green—SD, non-Manhattan edge
Orange—MD, non-Manhattan region
Black—MD, non-Manhattan edge



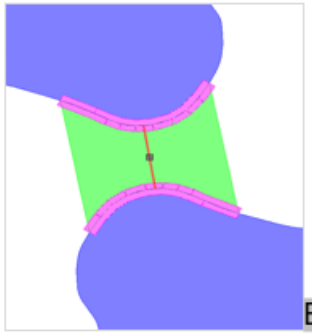
Green — separation=90nm
Pink — separation_factor=3.0
Yellow — separation_factor=3.4



Spline distance

Measure distance

- An example of Spline distance(SD) check performed on MULTIGON.
  - In comparison, Measure distance(MD) is performed on PWL(converted from Multigon with dev=1dbu).

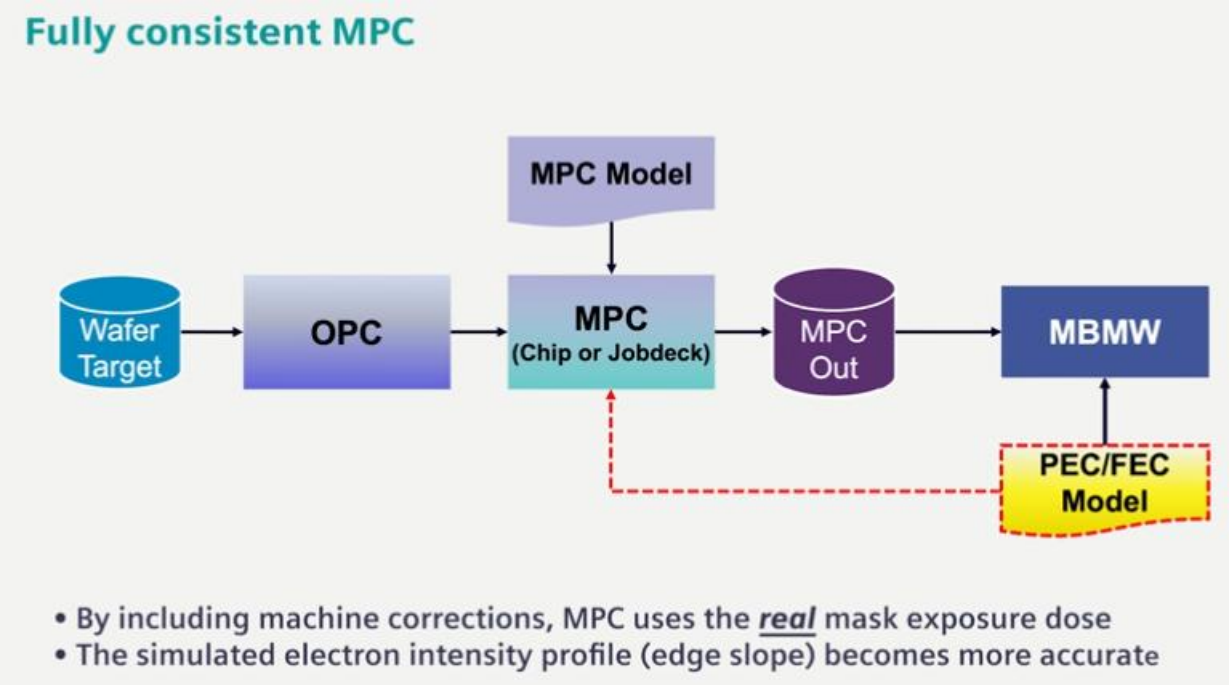


Pink—non-Manhattan edge
Green—non-Manhattan region
Red—pinpoint gauges
Black—pinpoint markers

Error marker

Calibre Mask Process Correction(MPC)

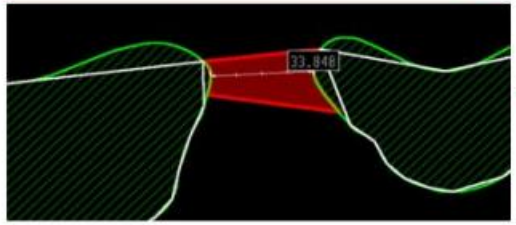
The Calibre Mask Process Correction family of **rule and model-based products** is used in advanced photomask manufacturing to correct for **systematic mask lithography** and **process error sources** to ensure that the mask critical dimension signature is within specification



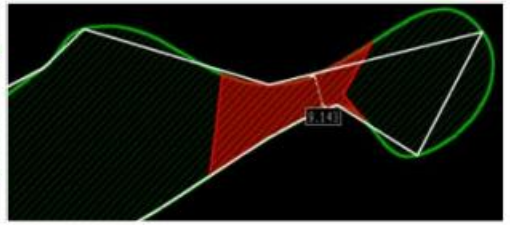
Calibre Standalone Curvilinear Mask Rule Checks (MRC) for Multigons

- Calibre provides new curvilinear MRC methodologies to support the requirements of leading-edge mask manufacturing through key innovations in native curvilinear data handling and representation techniques.
- New standalone SVRF commands are available for curvilinear MRC checks on multigons.
  - `RET SPLINE_ANGLE` checks the angle of splines on a multigon layer.
  - `RET SPLINE_DEPTH_WIDTH` checks the minimum width of a multigon shape.
  - `RET SPLINE_DISTANCE` measures the distance between spline sections on multigon layers.
  - `RET SPLINE_DW_RATIO` computes the depth-to-width ratio for multigon shapes.

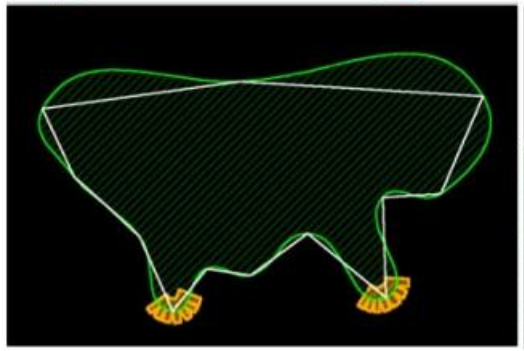
External Distance Check Example



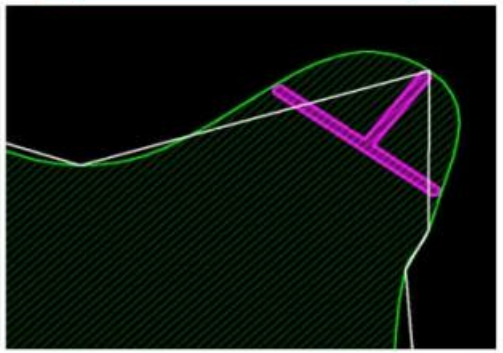
Internal Distance Check Example



Spike Detection Example

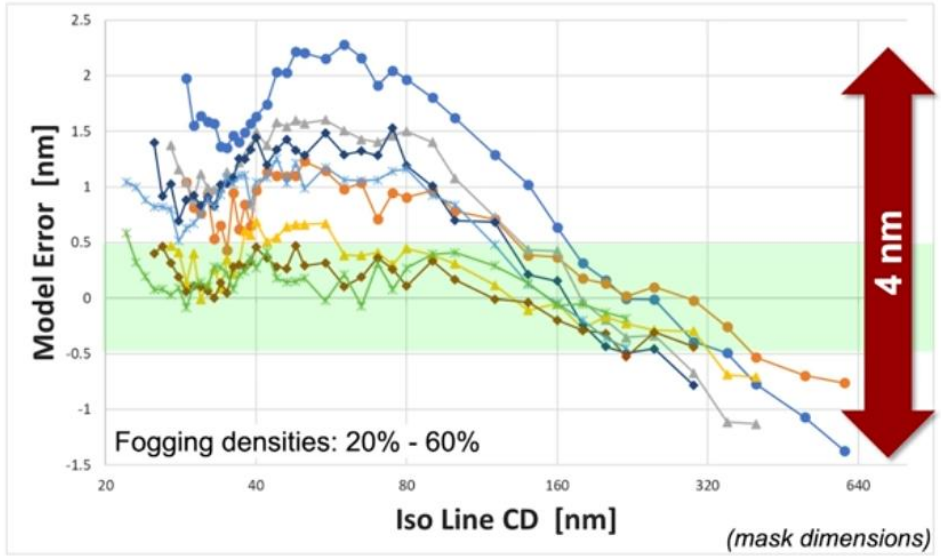


Depth-Width Check Example

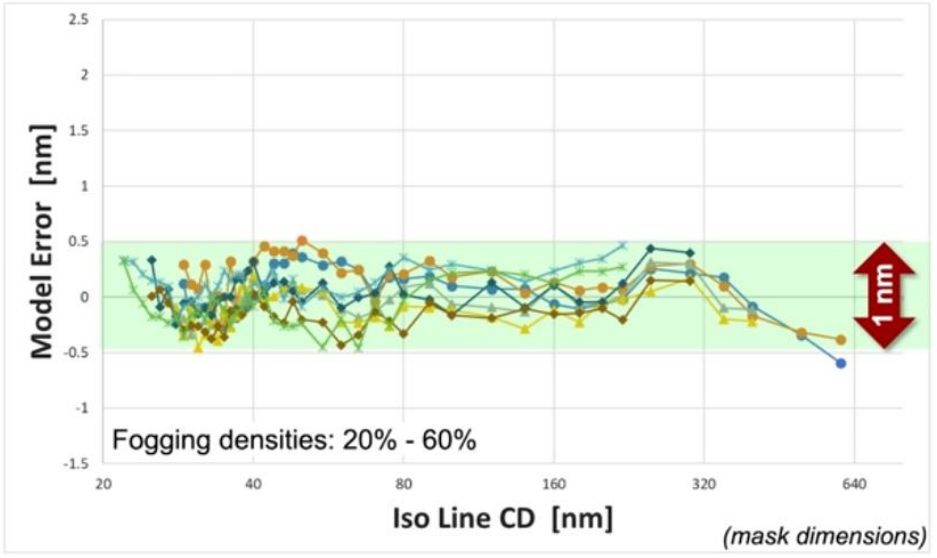


Calibre Mask Process Correction(MPC) – Reduces the CD model error

IsoLn CD model error when ignoring e-beam writer corrections for Fogging

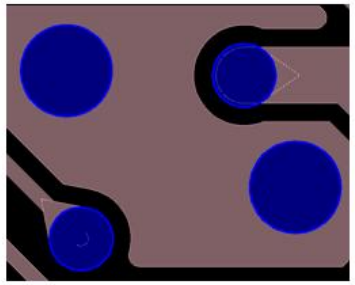
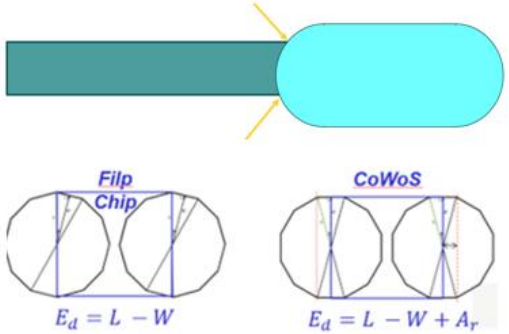
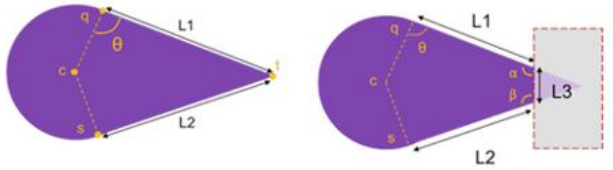
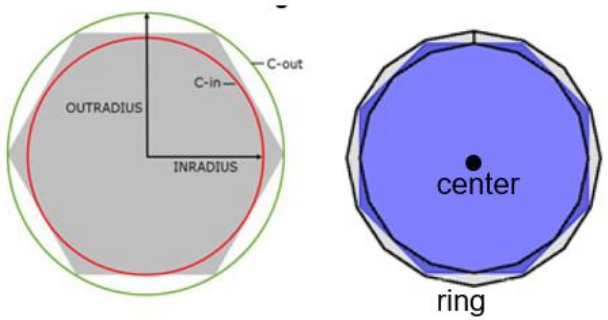
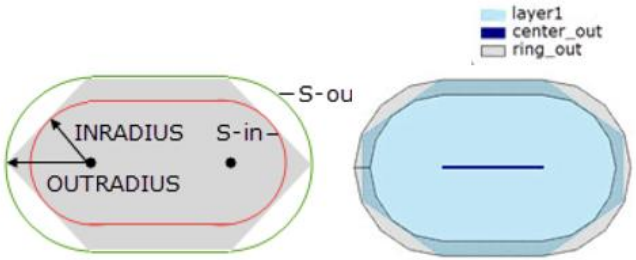
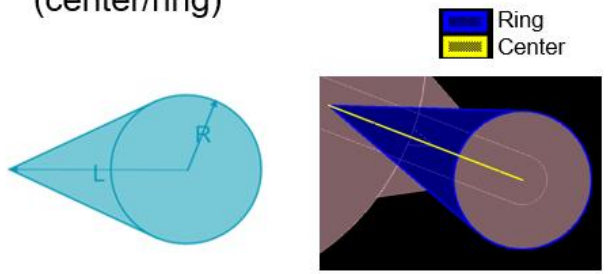


IsoLn CD model error reduced from over ± 2 nm to ± 0.5 nm when including e-beam writer corrections for Fogging



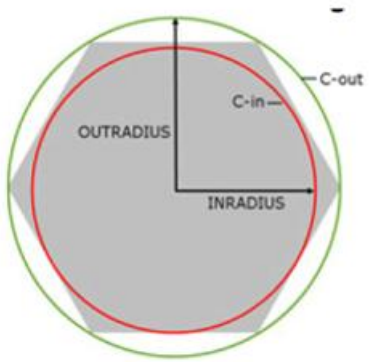
Calibre Capabilities to Simplify Irregular Shape Checking

Photonics, through-silicon via, & packaging checks

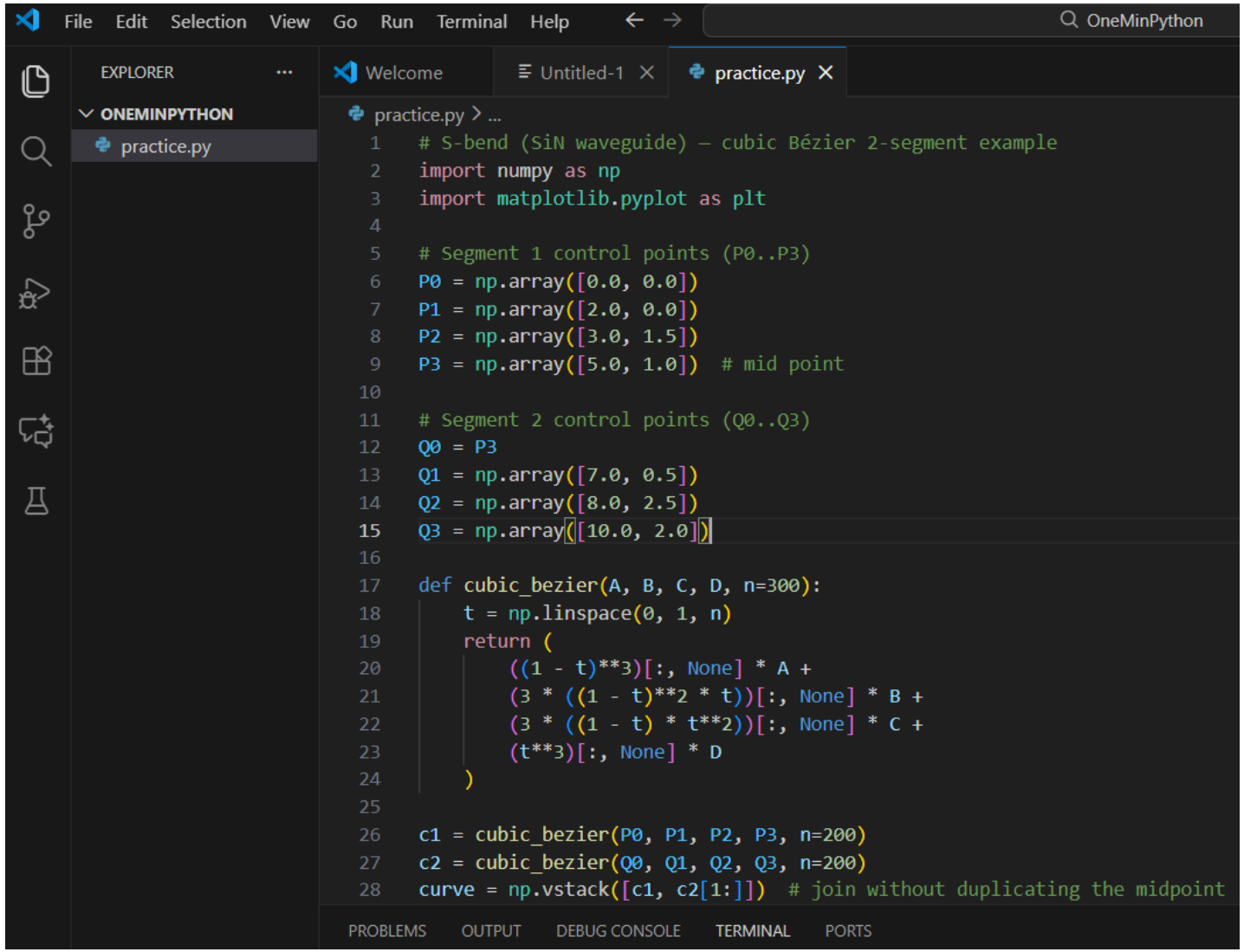
	Circle	Stadium	Teardrop
Recognize & separate	• INSIDE CELL [NOT] CIRCLE 	• INSIDE CELL [NOT] STADIUM 	• INSIDE CELL [NOT] TEARDROP 
Check Dimension & Ref Output	• DFM CIRCLE ANALYZE • DFM CIRCLE ANALYZE (center/ring) 	• DFM STADIUM ANALYZE • DFM STADIUM ANALYZE (center/ring) 	• DFM TEARDROP ANALYZE • DFM TEARDROP ANALYZE (center/ring) 

Calibre Capabilities to Simplify Irregular Shape Design Rule Check
DFM Circle Analyze

```
VARIABLE minimum_radius 1.0
VARIABLE maximum_radius 2.0
VARIABLE minimum_curvature_width 0.1
VARIABLE maximum_curvature_width 0.2

LAYER M1  54 350

// To obtain a Circle with a width of 0.14um (>=0.14)
circle_props = DFM CIRCLE ANALYZE M1
circle_ringL14 = DFM PROPERTY circle_props
        [inrad   = PROPERTY(circle_props, INRADIUS)]
        [outrad  = PROPERTY(circle_props, OUTRADIUS)]
        [annulus_in = PROPERTY(circle_props, ANNULUS_INRADIUS)]
        [ratio   = PROPERTY_REF(inrad)/PROPERTY_REF(outrad)] > 0.9
        [enclosing_width = 2*(PROPERTY(circle_props, OUTRADIUS))]
        [width   = (PROPERTY_REF(annulus_in)!=0) ? (PROPERTY_REF(inrad)+PROPERTY_REF(outrad))/2 –
PROPERTY_REF(annulus_in): PROPERTY_REF(inrad)+PROPERTY_REF(outrad)] >= minimum_curvature_width <=
maximum_curvature_width
        [radius  = (PROPERTY_REF(annulus_in)!=0) ? (PROPERTY_REF(width))+PROPERTY_REF(annulus_in):
(PROPERTY_REF(inrad)+PROPERTY_REF(outrad))/2] >= minimum_radius <= maximum_radius

DFM_out { DFM RDB circle_ringL14 "dfm.rdb"  ALL CELLS CHECKNAME "%_l_“ }
```



Python Code and its output: S-bend for SiN waveguide (Cubic Bezier segments)

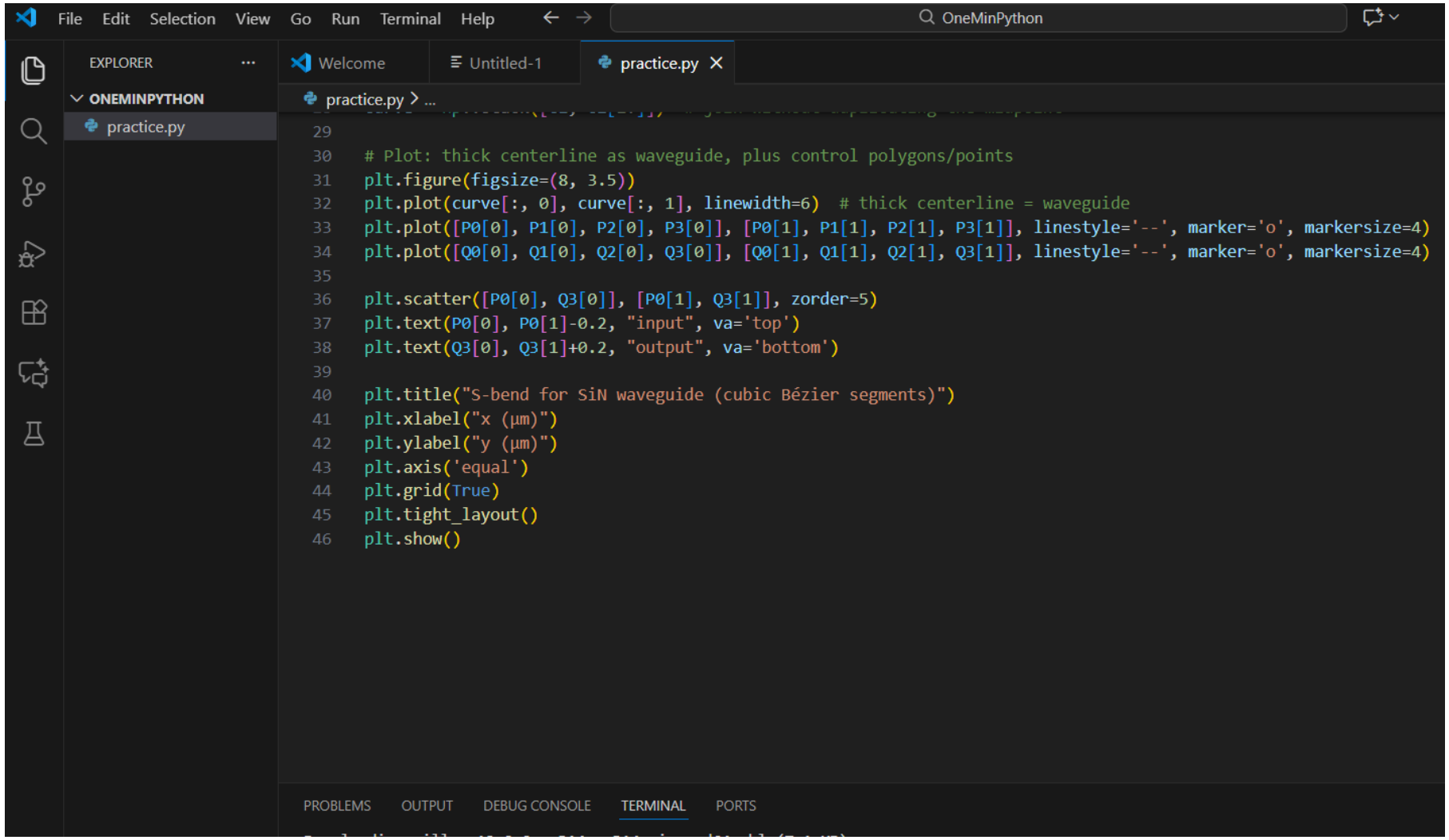


(Code continued)

Cubic Bezier curve in mathematics

$B(t) = (1-t)3P0 + 3t(1-t)2P1 + 3t2(1-t)P2 + t3P3,\ 0 \le t \le 1$

Python Code and its output: S-bend for SiN waveguide (Cubic Bezier segments)



(Code output)

Python Code and its output: S-bend for SiN waveguide (Cubic Bezier segments)