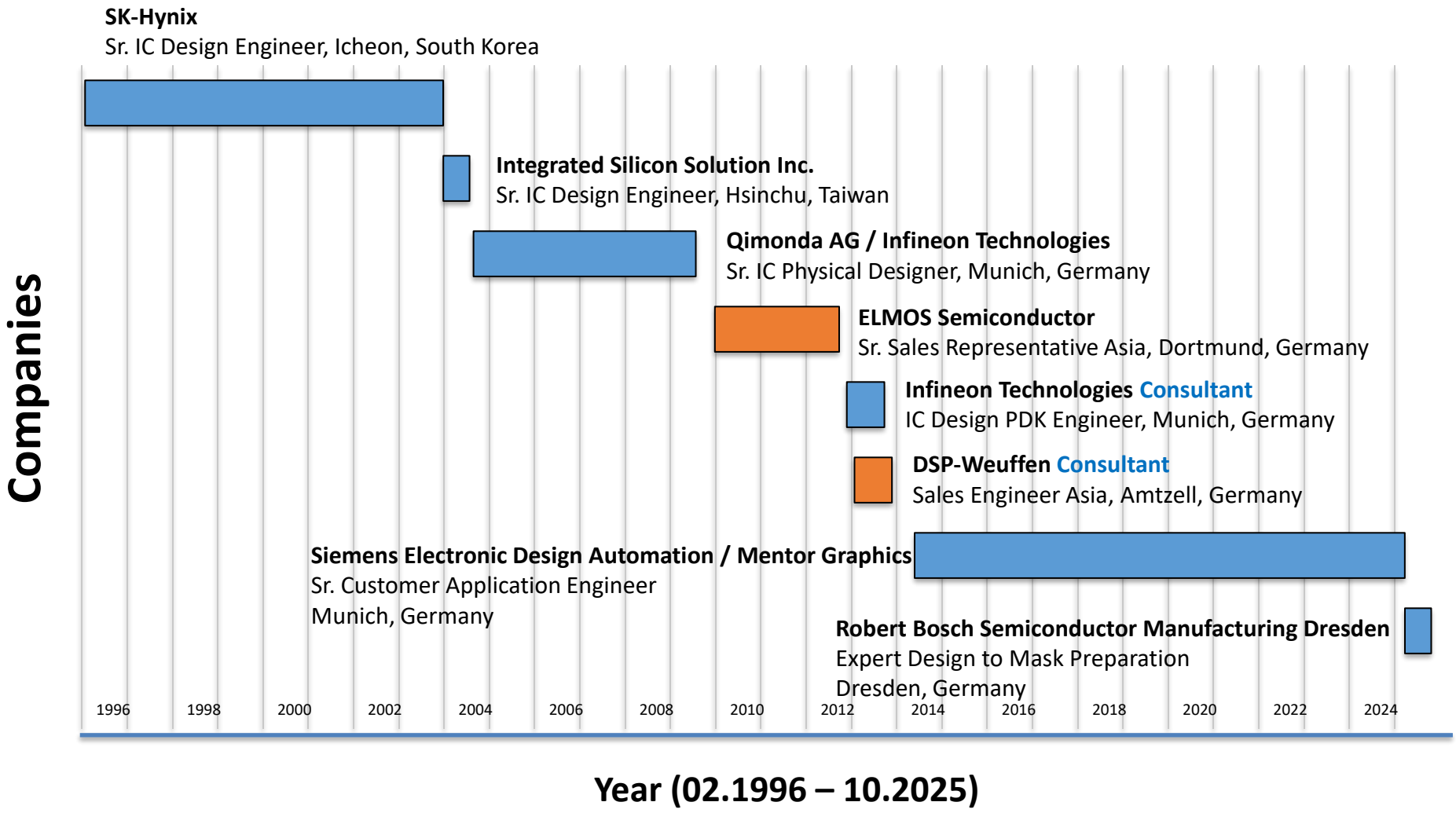
Be Joyful always pray continually
Give thanks in all circumstance

Career Timeline



CAREER SNAPSHOT

Kyung Wook Park — Senior Semiconductor Expert

Nearly 3 decades — Tape-Out • EDA • Sales • Physical Design • Verification • IC Design

Munich, Germany

DAUERAUFENTHALT–EU

TECHNICAL EXPERTISE

- Design-to-Mask & Tape-Out: OPC/RET, MDP, mask assembly, Manufacturing, 300mm fab integration (Bosch)
- Physical Verification (Calibre): DRC | LVS | PERC | OPC RET | SmartFILL | Pattern Matching
- Memory & Mixed-Signal: DDR1/DDR2, arrays, decoders, I/O, Sense Amps, ESD/LUP
- Advanced Processes: TSMC N3E/N7/N16/N28 | GF 45/28/22 | Intel i1277/i1226 | Samsung 14nm
- EDA & Automation: Siemens Calibre, Cadence, Pegasus, SKILL, Synopsys, ICC2, Python, and TCL

CUSTOMER & BUSINESS IMPACT

- Siemens EDA (Calibre CAE): customer support, training, adoption (Intel, GF, Infineon, Apple, and ST)
- ELMOS: Senior Sales Manager Asia, €15M revenue ownership
- DSP-Weuffen: China/Korea market development for ADAS SoCs
- Cross-functional leadership across Sales, Product, Design, QA, Finance, and Legal teams
- Secured key accounts and led successful annual price negotiations, maintaining and growing revenue stream

ACHIEVEMENTS & RECOGNITION

- Patents: 2 US + 12 Korean (DRAM & design automation)
- Awards: Key Talent Award (€20,000), Outstanding Achievement, Best Product
- Recognized expert in Memory, CAD EDA, DFM, SmartFILL, OPC, and DRC

GLOBAL EXPERIENCE & CORE STRENGTHS

- Germany, Korea, Taiwan, China, Japan, Singapore — EMEA/APAC engagements
- Languages: English (C2), Korean (native), German (B2)
- Core strengths: End-to-End lifecycle, Automation, and Problem-solving

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SENIOR SEMICONDUCTOR TECHNICAL LEADER | Kyung Wook Park

Design → Mask → Manufacturing | Sign-off Customer-Facing Technical Leadership

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PROFESSIONAL PROFILE

Highly experienced semiconductor technologist with nearly three decades of experience and senior technical leadership spanning **IC design, EDA sign-off, and manufacturing**.

Operates at **the intersection of technology strategy, global foundry ecosystems**, and commercial execution, enabling automotive and high-reliability silicon from concept through high-volume manufacturing.

Demonstrated ability to **translate complex technical risk** into clear, actionable decision frameworks, accelerate time-to-tape-out, and drive sustained, multi-region revenue growth.

CORE LEADERSHIP THEMES

- End-to-end accountability from **design intent to manufacturing sign-off**
- Risk governance for **automotive, safety-critical, and long-lifecycle silicon**
- Senior-level interface across **customers, foundries**, and internal organizations
- Scalable enablement across **EMEA and APAC**

TECHNICAL & STRATEGIC IMPACT

- De-risked complex tape-outs across advanced and legacy nodes by aligning design, verification, mask, and **foundry constraints early in the lifecycle**
- Enabled manufacturing-ready sign-off for **automotive and safety-critical products** under stringent reliability, yield, and longevity requirements
- Served as a trusted technical authority supporting **customer adoption, investment, roadmap, and sourcing decisions** through hands-on enablement and escalation support
- Drove sustained revenue growth by combining **sign-off–level technical credibility** with enterprise-level customer engagement

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IC DESIGN & EDA GOVERNANCE

Provide **strategic oversight** for IC design and EDA verification programs across memory, analog, and mixed-signal domains. **Own governance of full-chip sign-off** including DRC, LVS, DFM, and **OPC lithography** through GDSII tape-out, ensuring alignment between design intent, manufacturing feasibility, and business timelines.

Act as **escalation point for high-risk design and manufacturability issues** impacting schedule, yield, or customer commitments.

MANUFACTURING & DESIGN-TO-MASK OWNERSHIP

Own and execute end-to-end tape-out execution and photomask preparation for automotive and high-reliability semiconductor programs. **Ensure data integrity, manufacturability validation**, and predictable handoff between design teams, mask shops, and foundries.

Drive continuous improvement in **yield learning, defect reduction, and sign-off efficiency** across multi-project portfolios.

FOUNDRY & ECOSYSTEM LEADERSHIP

Act as the primary technical interface to global foundries, enabling technology transfer, yield ramp, and process optimization across **planar and FinFET nodes**. Influence foundry-facing decisions through deep understanding of silicon physics, customer product requirements, and manufacturing constraints, balancing performance, cost, risk, and long-term supply assurance.

Foundry Experience: TSMC | Samsung Foundry | Intel Foundry | GlobalFoundries | STMicroelectronics

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COMMERCIAL & ENTERPRISE LEADERSHIP

Combine **sign-off-level technical credibility** with commercial leadership to support enterprise sales, strategic accounts, and long-term customer partnerships. Enable multi-million-euro **engagements by aligning executive stakeholders**, engineering teams, and foundry partners around clear technical and business outcomes.

Trusted advisor to Tier-1 customers and senior leadership across **EMEA and APAC**.

DOMAINS & INDUSTRIES of Expertise:

- Automotive Semiconductors
- Engineering and Sales of High-Reliability & Safety-Critical ICs
- Electronic Design Automation (EDA) Software

TECHNICAL FOUNDATIONS

Design & Verification: IC Design, EDA Sign-off, Design-to-Mask

Manufacturing: Foundry Enablement, Yield Optimization, Tape-out Governance

Automation & Scripting: Python, TCL, SKILL, Shell
