Lab3 Report

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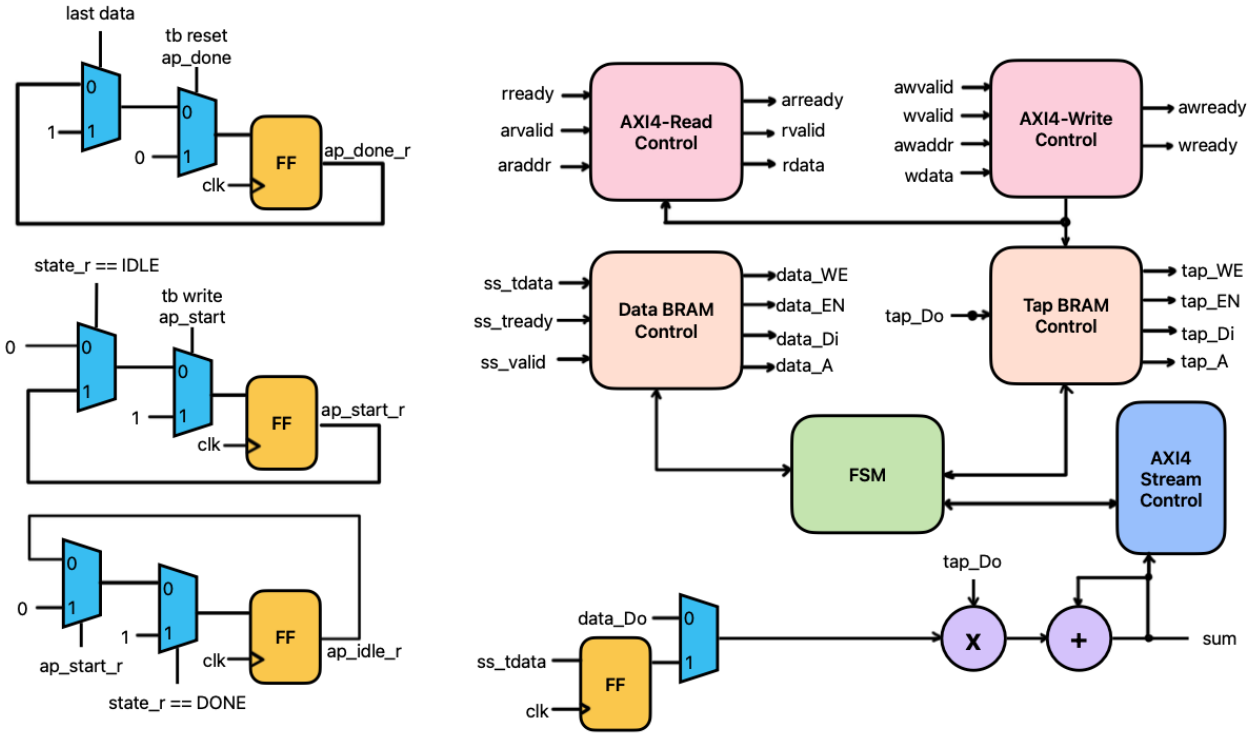
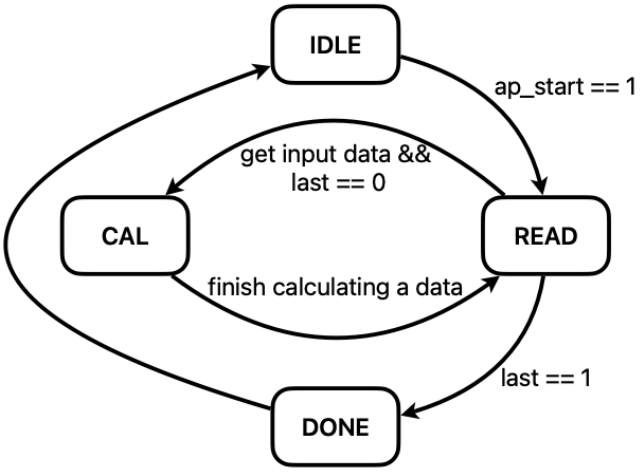
Block Diagram

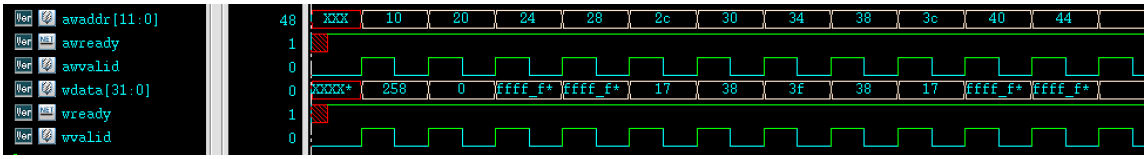


Finite State Machine

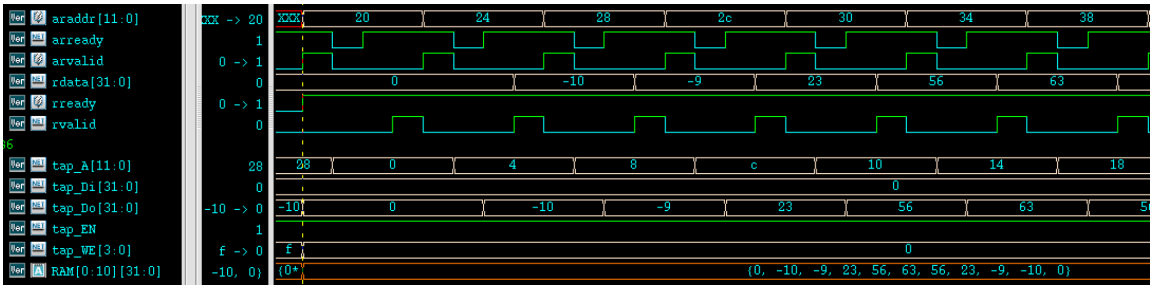


Operation

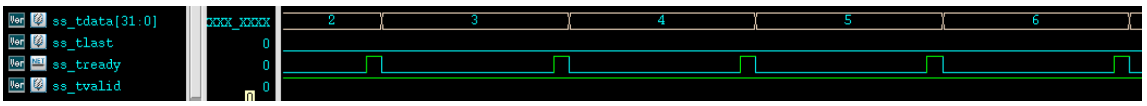
- AXI4-Lite Write
  - If address == 0, FIR immediately changes ap_idle, ap_done, ap_start
  - if address == 1, FIR immediately changes data_length
  - if other addresses, meaning that coefficients are inputted, write the data into tap_bram



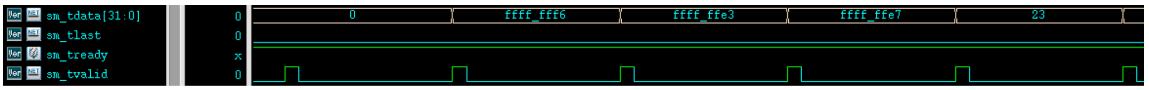
- AXI4-Lite Read
  - If address == 0, FIR immediately output {ap_idle, ap_done, ap_start}
  - if address == 1, FIR immediately output data_length
  - if other addresses, meaning that tb wants to read coefficients, then read the corresponding coefficients from tap_bram and then output
    - The reading process takes 3 cycles, one for asking tap_bram for data, one for tap_bram to read, one for outputting the data
    - Because the reading process can be pipelined, “arready” will be pulled down to 0 only for 1 cycle



- AXI4-Stream Read
  - FIR pulls “ss_tready” to 1 for 1 cycle if FIR needs data



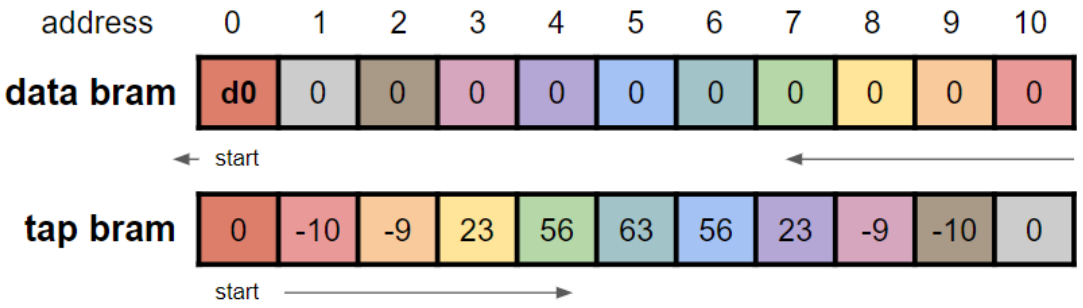
- AXI4-Stream Write
    - When FIR finishes calculating one answer, FIR pulls “sm_tvalid” to 1 for 1 cycle and sets “sm_tdata” to the output answer at the same time



- At The Very Start
    - Before tb starts to input coefficients, tb first checks whether FIR is idle. If ap_idle == 1, then tb starts to input coefficients.
    - After FIR receives all coefficients, tb will start reading coefficients
    - If all coefficients are correct, then tb write ap_start 1, and FIR start calculating
- BRAM access during calculation
    - Before any calculation is conducted, I write 0 to every address except address 0 in tap_bram, because the first n answers are calculated using the first n data only
    - Input data from AXI4-Stream is stored in data_bram sequentially, and it replaces the oldest data if data_bram is full. That is, the i^{th} data is stored in address (i % 12) in data_bram
    - The figure below shows the calculation of the first data
        - Data with the same color in data_bram and tap_bram will multiply.
        - Since there is only one multiplier, each data pair is multiplied in 1 cycle. The product is added to a register called sum.
        - The first data read from data_bram is address 0, after that, read address in decreasing order.
        - The first data read from tap_bram is address 0, after that, read address in increasing order.

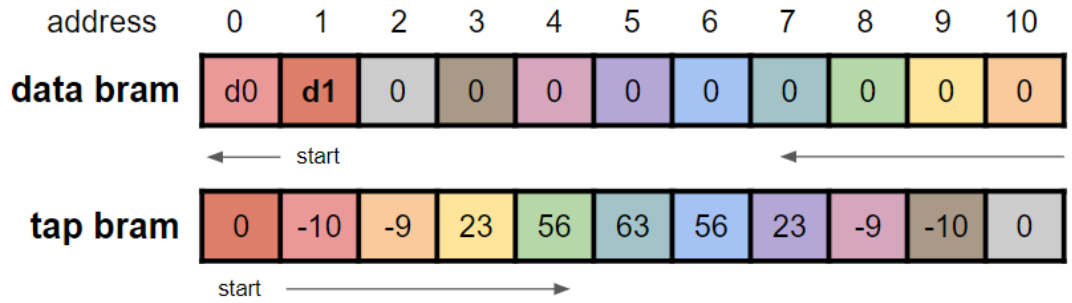
- After 11 cycles of calculation, the sum will be outputted to “sm_tdata” and pull “sm_tvalid” to 1 simultaneously for 1 cycle

First data



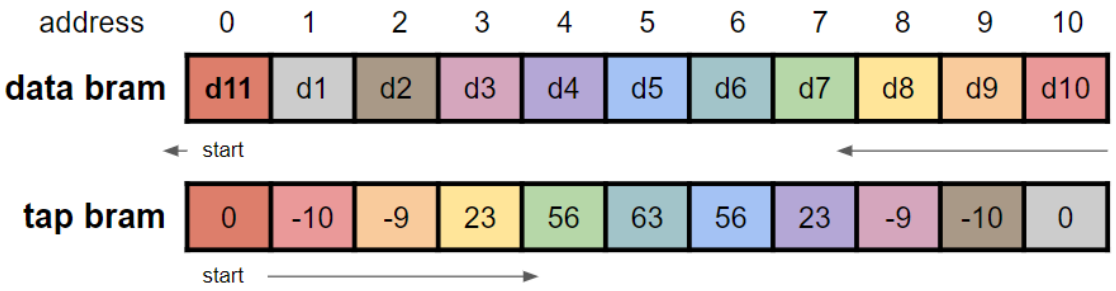
- The figure below shows the calculation of the second data
  - The first data read from data_bram is address 1, after that, read address in decreasing order.
  - The first data read from tap_bram is address 0, after that, read address in increasing order.

Second data



- The figure below shows the calculation of the 12th data
  - d11 replace the original d0 in data_bram
  - The first data read from data_bram is address 0, after that, read address in decreasing order.
  - The first data read from tap_bram is address 0, after that, read address in increasing order.

12th data



- How ap_done is generated
  - When FIR gets stream data with “ss_tlast” high, then FIR will calculate the last data, and after the calculation, FIR will pull ap_done to 1
  - After the last data is successfully sent to tb, FIR will pull ap_idle to 1

Resource Usage

Component

```
Detailed RTL Component Info :
+---Adders :
           2 Input   32 Bit       Adders := 1
           2 Input   12 Bit       Adders := 3
           2 Input    4 Bit       Adders := 1
           2 Input    3 Bit       Adders := 2
+---Registers :
                     32 Bit    Registers := 6
                     16 Bit    Registers := 1
                     12 Bit    Registers := 3
                      4 Bit    Registers := 3
                      3 Bit    Registers := 1
                      1 Bit    Registers := 15
+---Multipliers :
                    32x32  Multipliers := 1
+---Muxes :
           2 Input   32 Bit        Muxes := 9
           4 Input   32 Bit        Muxes := 1
           2 Input   12 Bit        Muxes := 6
           4 Input   12 Bit        Muxes := 2
           2 Input    8 Bit        Muxes := 3
           2 Input    4 Bit        Muxes := 4
           4 Input    4 Bit        Muxes := 3
           2 Input    3 Bit        Muxes := 1
           4 Input    3 Bit        Muxes := 1
           2 Input    2 Bit        Muxes := 1
           2 Input    1 Bit        Muxes := 52
           3 Input    1 Bit        Muxes := 3
           4 Input    1 Bit        Muxes := 15
```

LUT & FF & BRAM

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP
synth_1	constrs_1	synth_design Complete!												261	260	0	0	3

Register

```
1.1 Summary of Registers by Type
--------------------------------


+-------+--------------+-------------+--------------+
| Total | Clock Enable | Synchronous | Asynchronous |
+-------+--------------+-------------+--------------+
| 0     |            _ |           - |            - |
| 0     |            _ |           - |          Set |
| 0     |            _ |           - |        Reset |
| 0     |            _ |         Set |            - |
| 0     |            _ |       Reset |            - |
| 0     |          Yes |           - |            - |
| 1     |          Yes |           - |          Set |
| 259   |          Yes |           - |        Reset |
| 0     |          Yes |         Set |            - |
| 0     |          Yes |       Reset |            - |
+-------+--------------+-------------+--------------+
```

DSP

```
DSP Final Report (the ' indicates corresponding REG is set)
+------------+--------------+--------+--------+--------+--------+--------+------+------+------+------+-------+------+------+
|Module Name | DSP Mapping  | A Size | B Size | C Size | D Size | P Size | AREG | BREG | CREG | DREG | ADREG | MREG | PREG |
+------------+--------------+--------+--------+--------+--------+--------+------+------+------+------+-------+------+------+
|fir         | A*B          | 17     | 15     | -      | -      | 48     | 0    | 0    | -    | -    | -     | 0    | 0    |
|fir         | A*B          | 17     | 17     | -      | -      | 48     | 0    | 0    | -    | -    | -     | 0    | 0    |
|fir         | PCIN>>17+A*B | 17     | 15     | -      | -      | 48     | 0    | 0    | -    | -    | -     | 0    | 0    |
+------------+--------------+--------+--------+--------+--------+--------+------+------+------+------+-------+------+------+
```

Timing Report

Max Delay Paths

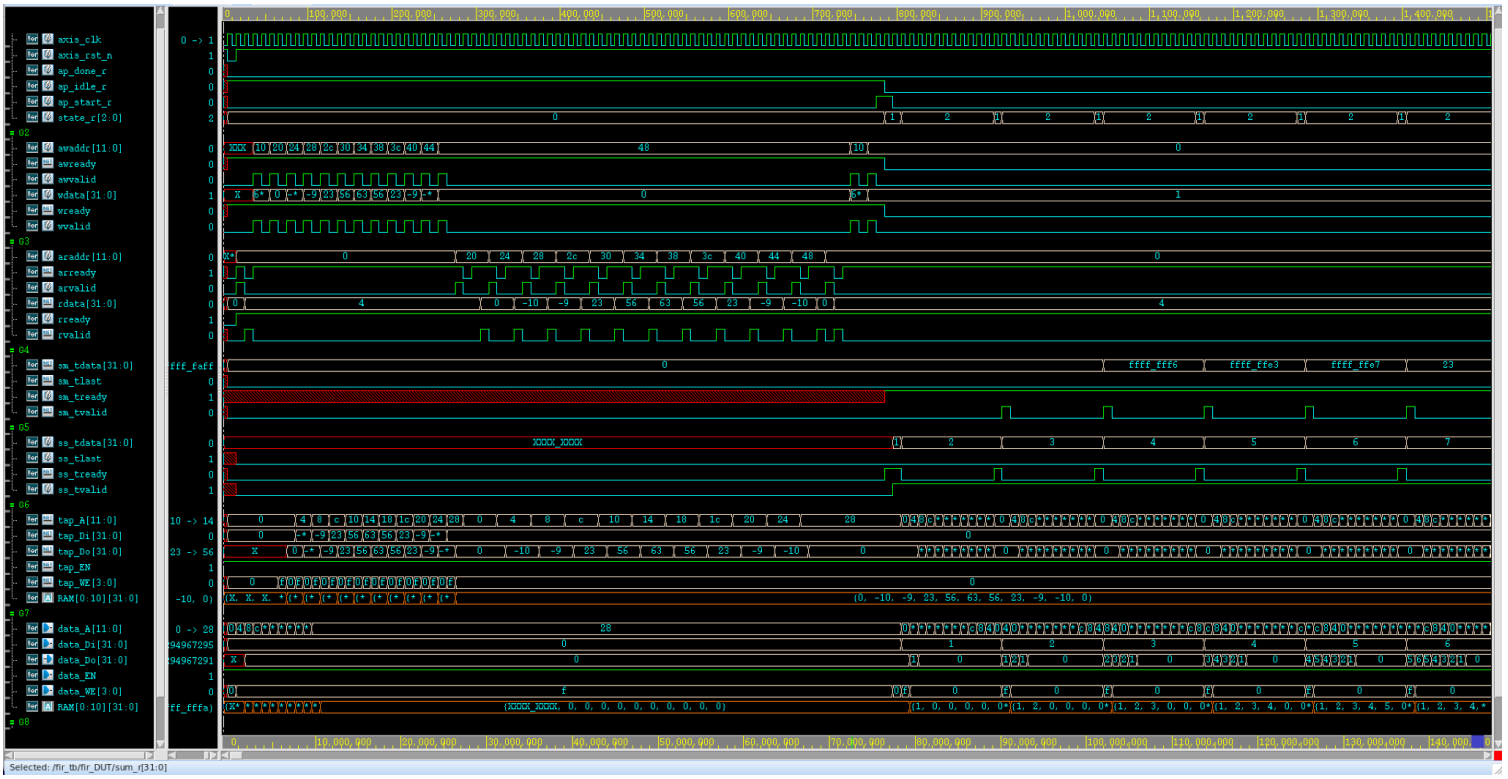
```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             1.767ns  (required time - arrival time)
  Source:                 tap_A_r_reg[5]/C
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@7.500ns period=15.000ns})
  Destination:            sum_r_reg[31]/D
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@7.500ns period=15.000ns})
  Path Group:             axis_clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            15.000ns  (axis_clk rise@15.000ns - axis_clk rise@0.000ns)
  Data Path Delay:        13.096ns  (logic 8.684ns (66.308%)  route 4.412ns (33.692%))
  Logic Levels:           12  (CARRY4=5 DSP48E1=2 LUT2=3 LUT3=1 LUT6=1)
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 17.128 - 15.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
```

Location	Delay type	Incr(ns)	Path(ns)		Netlist Resource(s)
	(clock axis_clk rise edge)				
		0.000	0.000	r	
		0.000	0.000	r	axis_clk (IN)
	net (fo=0)	0.000	0.000		axis_clk
				r	axis_clk_IBUF_inst/I
	IBUF (Prop_ibuf_I_O)	0.972	0.972	r	axis_clk_IBUF_inst/O
	net (fo=1, unplaced)	0.800	1.771		axis_clk_IBUF
				r	axis_clk_IBUF_BUFG_inst/I
	BUFG (Prop_bufg_I_O)	0.101	1.872	r	axis_clk_IBUF_BUFG_inst/O
	net (fo=260, unplaced)	0.584	2.456		axis_clk_IBUF_BUFG
	FDCE			r	tap_A_r_reg[5]/C

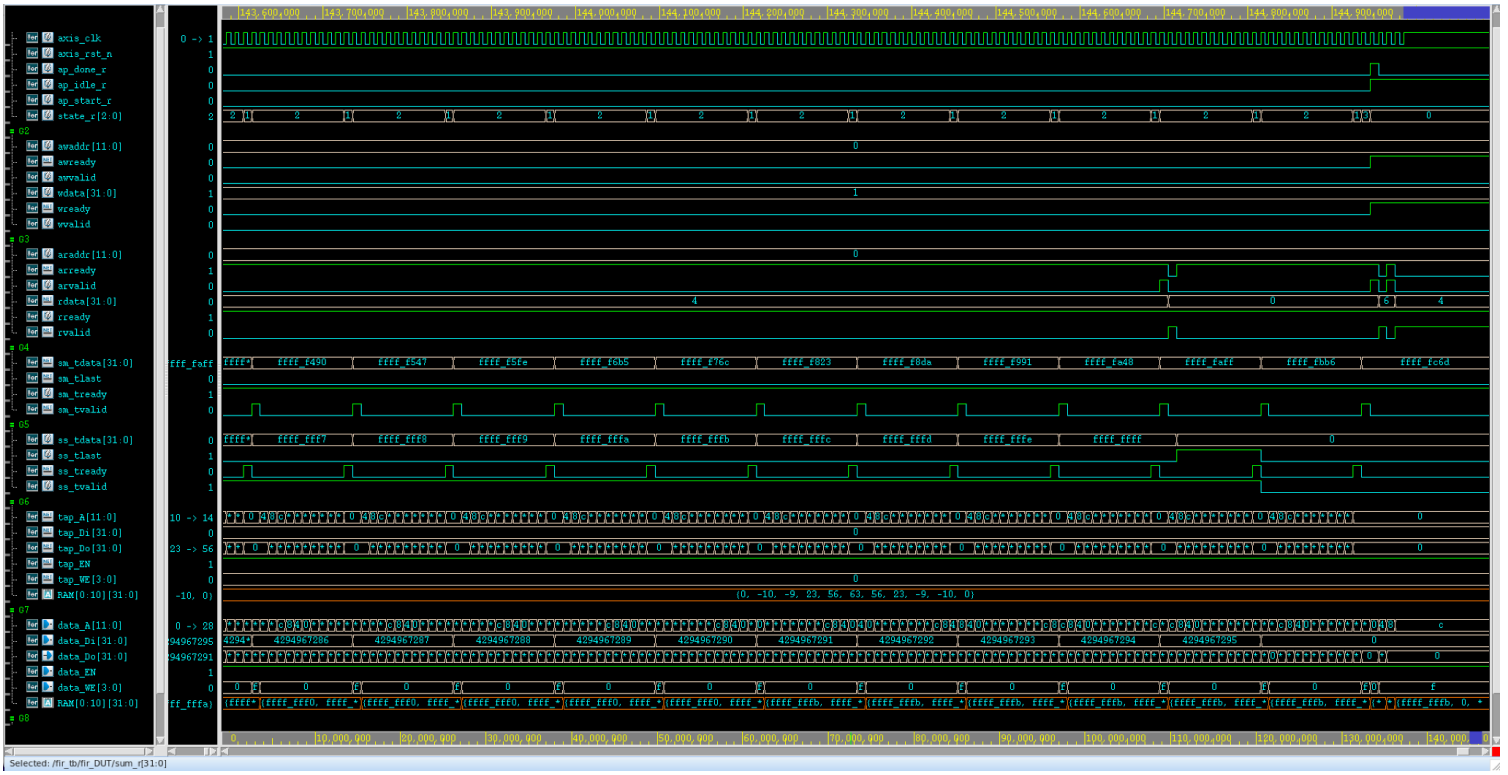
```
-------------------------------------------------------------------    -------------------
                         FDCE (Prop_fdce_C_Q)         0.478     2.934 r  tap_A_r_reg[5]/Q
                         net (fo=5, unplaced)         0.993     3.927    tap_A_OBUF[5]
                                                                      r  sum_w1_i_18/I0
                         LUT6 (Prop_lut6_I0_O)        0.295     4.222 r  sum_w1_i_18/O
                         net (fo=32, unplaced)        0.520     4.742    sum_w1_i_18_n_0
                                                                      r  sum_w1_i_1/I1
                         LUT3 (Prop_lut3_I1_O)        0.124     4.866 r  sum_w1_i_1/O
                         net (fo=2, unplaced)         0.800     5.666    sum_w1_i_1_n_0
                                                                      r  sum_w1__0/B[16]
                         DSP48E1 (Prop_dsp48e1_B[16]_PCOUT[47])
                                                      3.851     9.517 r  sum_w1__0/PCOUT[47]
                         net (fo=1, unplaced)         0.055     9.572    sum_w1__0_n_106
                                                                      r  sum_w1__1/PCIN[47]
                         DSP48E1 (Prop_dsp48e1_PCIN[47]_P[0])
                                                      1.518    11.090 r  sum_w1__1/P[0]
                         net (fo=2, unplaced)         0.800    11.890    sum_w1__1_n_105
                                                                      r  sum_r[19]_i_10/I0
                         LUT2 (Prop_lut2_I0_O)        0.124    12.014 r  sum_r[19]_i_10/O
                         net (fo=1, unplaced)         0.000    12.014    sum_r[19]_i_10_n_0
                                                                      r  sum_r_reg[19]_i_7/S[1]
                         CARRY4 (Prop_carry4_S[1]_CO[3])
                                                      0.533    12.547 r  sum_r_reg[19]_i_7/CO[3]
                         net (fo=1, unplaced)         0.009    12.556    sum_r_reg[19]_i_7_n_0
                                                                      r  sum_r_reg[23]_i_7/CI
                         CARRY4 (Prop_carry4_CI_CO[3])
                                                      0.117    12.673 r  sum_r_reg[23]_i_7/CO[3]
                         net (fo=1, unplaced)         0.000    12.673    sum_r_reg[23]_i_7_n_0
                                                                      r  sum_r_reg[27]_i_7/CI
                         CARRY4 (Prop_carry4_CI_O[3])
                                                      0.331    13.004 r  sum_r_reg[27]_i_7/O[3]
                         net (fo=1, unplaced)         0.618    13.622    sum_r_reg[27]_i_7_n_4
                                                                      r  sum_r[27]_i_3/I1
                         LUT2 (Prop_lut2_I1_O)        0.307    13.929 r  sum_r[27]_i_3/O
                         net (fo=1, unplaced)         0.000    13.929    sum_r[27]_i_3_n_0
                                                                      r  sum_r_reg[27]_i_2/S[3]
                         CARRY4 (Prop_carry4_S[3]_CO[3])
                                                      0.376    14.305 r  sum_r_reg[27]_i_2/CO[3]
                         net (fo=1, unplaced)         0.000    14.305    sum_r_reg[27]_i_2_n_0
                                                                      r  sum_r_reg[31]_i_3/CI
                         CARRY4 (Prop_carry4_CI_O[3])
                                                      0.331    14.636 r  sum_r_reg[31]_i_3/O[3]
                         net (fo=1, unplaced)         0.618    15.254    sum_r_reg[31]_i_3_n_4
                                                                      r  sum_r[31]_i_2/I0
                         LUT2 (Prop_lut2_I0_O)        0.299    15.553 r  sum_r[31]_i_2/O
                         net (fo=1, unplaced)         0.000    15.553    sum_w[31]
                         FDCE                                         r  sum_r_reg[31]/D
-------------------------------------------------------------------    -------------------

                         (clock axis_clk rise edge)
                                                     15.000    15.000 r
                                                      0.000    15.000 r  axis_clk (IN)
                         net (fo=0)                   0.000    15.000    axis_clk
                                                                      r  axis_clk_IBUF_inst/I
                         IBUF (Prop_ibuf_I_O)         0.838    15.838 r  axis_clk_IBUF_inst/O
                         net (fo=1, unplaced)         0.760    16.598    axis_clk_IBUF
                                                                      r  axis_clk_IBUF_BUFG_inst/I
                         BUFG (Prop_bufg_I_O)         0.091    16.689 r  axis_clk_IBUF_BUFG_inst/O
                         net (fo=260, unplaced)       0.439    17.128    axis_clk_IBUF_BUFG
                         FDCE                                         r  sum_r_reg[31]/C
                         clock pessimism              0.184    17.311
                         clock uncertainty           -0.035    17.276
                         FDCE (Setup_fdce_C_D)        0.044    17.320    sum_r_reg[31]
-------------------------------------------------------------------
                         required time                         17.320
                         arrival time                         -15.553
-------------------------------------------------------------------
                         slack                                  1.767
```

Simulation Waveform

At the begin



At the end


axis_clk
axis_rst_n
ap_done_r
ap_idle_r
ap_start_r
state_r[2:0]
awaddr[11:0]
awready
awvalid
wdata[31:0]
wready
wvalid
araddr[11:0]
arready
arvalid
rdata[31:0]
rready
rvalid
sm_tdata[31:0]
sm_tlast
sm_tready
sm_tvalid
ss_tdata[31:0]
ss_tlast
ss_tready
ss_tvalid
tap_A[11:0]
tap_Di[31:0]
tap_Do[31:0]
tap_EN
tap_WE[3:0]
RAM[0:10][31:0]
data_A[11:0]
data_Di[31:0]
data_Do[31:0]
data_EN
data_WE[3:0]
RAM[0:10][31:0]
(0, -10, -9, 23, 56, 63, 56, 23, -9, -10, 0)
Selected: /fir_tb/fir_DUT/sum_r[31:0]