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2013 J. Micromech. Microeng. 23 097001

(http://iopscience.iop.org/0960-1317/23/9/097001)

IOP PUBLISHING JOURNAL OF MICROMECHANICS AND MICROENGINEERING

J. Micromech. Microeng. **23** (2013) 097001 (7pp) doi:10.1088/0960-1317/23/9/097001

TECHNICAL NOTE

Fabrication of multi-electrode array platforms for neuronal interfacing with bi-layer lift-off resist sputter deposition

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Received 4 April 2013, in final form 11 June 2013
Published 6 August 2013
Online at stacks.iop.org/JMM/23/097001

Abstract

We report a bi-layer lift-off resist (LOR) technique in combination with sputter deposition of silicon dioxide (SiO_2) as a new passivation method in the fabrication of a multi-electrode array (MEA). Using the photo-insensitive LOR as a sacrificial bottom layer and the negative photoresist as a patterning top layer, and performing low-temperature sputter deposition of SiO_2 followed by lift-off, we could successfully fabricate damage-free indium-tin oxide (ITO) and Au MEA. The bi-layer LOR sputter deposition processed Au MEA showed an impedance value of 6×10^5 Ω (at 1 kHz), with good consistency over 60 electrodes. The passivation performance of the bi-layer LOR sputter-deposited SiO_2 was tested by electrodepositing Au nanoparticles (NPs) on the Au electrode, resulting in the well-confined and uniformly coated Au NPs. The bi-layer LOR sputter deposition processed ITO, Au, and Au NP-modified MEAs were evaluated and found to have a neuronal spike recording capability at a single unit level, confirming the validity of the bi-layer LOR sputter deposition as an effective passivation technique in fabrication of a MEA. These results suggest that the damage-free Au MEA fabricated with bi-layer LOR sputter deposition would be a viable platform for screening surface modification techniques that are available in neuronal interfacing.

S Online supplementary data available from stacks.iop.org/JMM/23/097001/mmedia

(Some figures may appear in colour only in the online journal)

1. Introduction

A multi-electrode array (MEA) can be defined as a two-dimensional arrangement of multiple electrodes. It has been widely used in long-term extracellular recording of electrophysiological activity from neuronal networks and slice tissues, and has served as a test platform for screening drugs (Morin *et al* 2005, Berdondini *et al* 2006, Wheeler and Brewer 2010, Xiang *et al* 2007). Even though MEAs based on a flexible substrate and polymeric insulation layer have received interest, most commercially available MEAs are fabricated from a glass substrate, due to its robustness, transparency, and durability. Dielectric passivation is an essential step for protecting electrodes and insulating interconnection lines in the fabrication of a MEA. Although various polymers, such as SU-8, polydimethylsiloxane, silicon-based positive photoresist (PR) and polyimide have been used as dielectric materials for passivation (Seker *et al* 2010, Guo *et al* 2010, Suzuki *et al* 2004, Lin *et al* 2008), silicon dioxide (SiO_2) and silicon nitride are still favored because they provide robust and secure passivation. In particular, SiO_2 is advantageous because it is easy to chemically modify the neuronal cell to have an attractive surface. Currently, plasma-enhanced chemical vapor deposition and reactive ion etching (RIE) have

been most widely adopted for the deposition of SiO_2 and for active electrode opening, respectively. Since RIE is a top-down approach, it requires a highly uniform dielectric layer and tight control of the dielectric layer thickness, to get uniformly etched profiles, and reproducible results. Frequently, extended RIE is performed when the thickness profile of the dielectric layer is not uniform. When the electrode underneath the dielectric layer has poor etch selectivity, the extended RIE may induce morphological damages to the electrode. For example, Au does not have poor etch selectivity for almost all gas mixtures involved in the RIE of SiO_2 (Ranade *et al* 1993), so that damaging of Au surface is unavoidable while RIE is employed. The introduction of a relatively thick Cr or Ti adhesion layer as a protecting layer on top of the Au layer (van Pelt *et al* 2004), and etching away with wet etchant preceded by RIE, would be an alternative solution in obtaining an intact Au electrode. A combined RIE and wet etching of dielectric layer (Frey *et al* 2011) could also be another candidate.

Au has long been used as an electrode material for extracellular recordings using MEAs (Mohr *et al* 1996, Jaber *et al* 2009, Guo *et al* 2010), and is particularly advantageous, in that it can easily be modified with nanostructures via electro-deposition to have lower electrical impedance. In this work, in order to protect Au electrode from damage, the challenge was to use a bi-layer lift-off resist (LOR) process in combination with RF sputter deposition of dielectric, instead of RIE. The bi-layer LOR process uses both a conventional PR top layer for pattern transfer from the photomask, and a sacrificial bottom layer which is not photosensitive. The bi-layer LOR process has already been employed for metal patterning in the fabrication of a MEA (Berdondini *et al* 2006), a perforated complementary metal–oxide–semiconductor microchip (Greve *et al* 2007) and a biosensor (Frey *et al* 2011), and we have extended the process to dielectric lift-off for the purpose of passivation. We have confirmed the effectiveness of the bi-layer dielectric LOR process in terms of impedance and by checking the neuronal spike recording capability.

2. Dielectric bi-layer lift-off process

As shown schematically in figure 1, dielectric bi-layer lift-off is almost the same as that commonly adopted for metal bi-layer lift-off (Chen *et al* 2004, Ouattara *et al* 2010), except that dielectric is sputter-deposited instead of through physical metal deposition. For dielectric bi-layer lift-off, polydimethylglutarimide (PMGI) 15B (MicroChem) was first spin-coated on the indium-tin oxide (ITO) substrate, and baked on a hot plate at 180 °C for 10 min, forming a bottom layer 2 μm thick. Then, negative PR (AZ nLOF 2070, Clairant) was spin-coated and baked on a hot plate at 110 °C for 90 s, forming a top layer 5 μm thick. After ultra violet (UV) exposure for 5 s with an intensity of 45 mW cm^{-2} at 365 nm, and a post-exposure-baking at 110 °C for 90 s, developing and undercut formation were performed with 2.38 wt% tetramethyl ammonium hydroxide containing developer (AZ 300 MIF, Clairant) in the same bath without refreshing the developer, followed by rinsing with deionized water (DIW) and drying

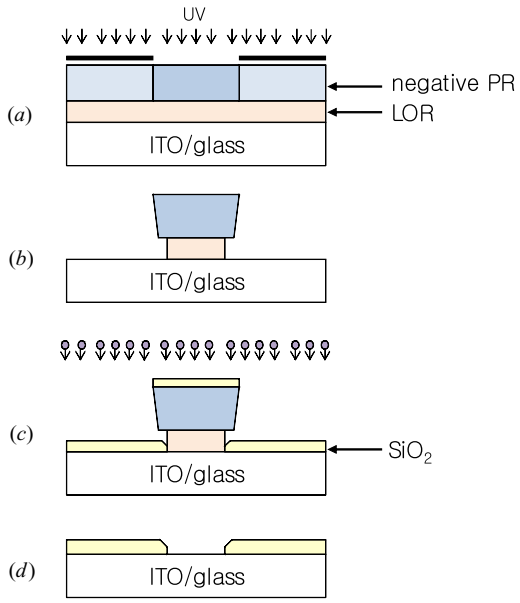
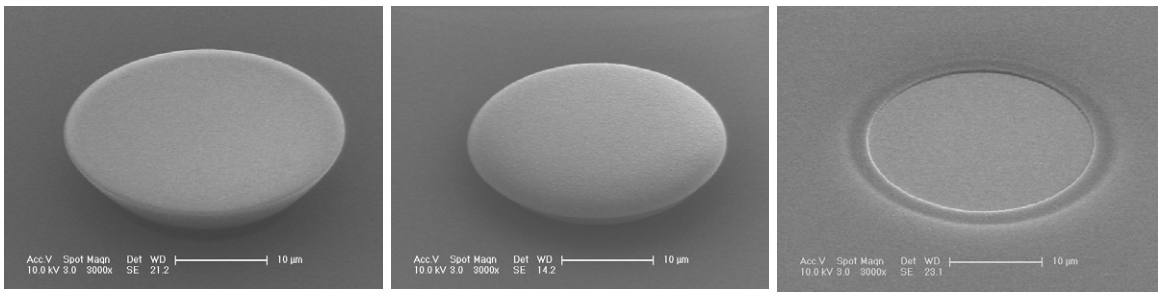


Figure 1. Schematic representation of the dielectric bi-layer lift-off process: (*a*) bi-layer formation and photo-patterning, (*b*) undercut formation via develop, (*c*) dielectric sputter-deposition, and (*d*) bi-layer lift-off.

with nitrogen gas. Although the undercut size is influenced by the baking temperature, time and developing time, the baking temperature and time were fixed, and only the developing time was varied.

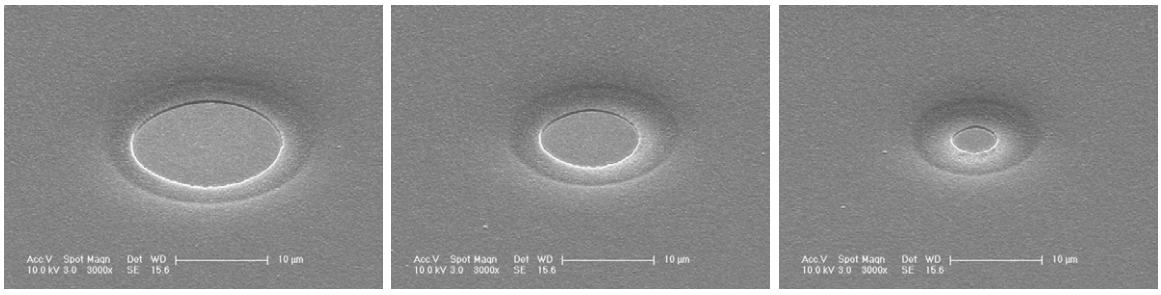
Then, SiO_2 was sputter-deposited on a bi-layer LOR-patterned structure, and the sputtering conditions were: working pressure of 4 mTorr, 150 W RF power, argon and oxygen gas flow rate of 40 sccm and 1 sccm, respectively, target-to-substrate distance of 40 mm, no sample rotation, and the 'sputter down' configuration. The high purity 4 inch silicon oxide (99.9999%, Kojundo Chem Lab) was used as a target. Substrates were cooled with cooling water. The thickness of the sputtered SiO_2 layer was fixed to approximately 1 μm for all samples reported in this paper. Finally, the lift-off of sputtered SiO_2 was done in LOR remover solution (Remover PG, MicroChem), maintained at 60 °C with sonication for 30 min, followed by rinsing with DIW and drying with nitrogen gas.

Figure 2 shows typical field-emission scanning electron microscope (FESEM) images taken from samples processed with semi-optimal conditions. Figure 2(*a*) shows that the developed bi-layer LOR has an overhang structure, even though the bottom layer is not seen in the figure, with a conventional negative slope of the top layer. Figure 2(*b*) shows that the top layer almost keeps its shape throughout the sputtering process, while the edge is slightly bent downward. Figure 2(*c*) shows a bi-layer lift-off processed feature of electrode. We can find from the figure 2(*c*) that the diameter of the active electrode (approximately 25 μm) is smaller than the designed value of 30 μm. The scattering nature of plasma, and surface mobile nature of the sputtered atoms (Rossnagel *et al* 1982, Murty *et al* 1998), would contribute to the decreased electrode diameter. In the bi-layer LOR Au metallization process, the size of metal pattern is independent of the degree of the undercut size.



(*a*) (*b*) (*c*)

Figure 2. Typical FESEM images of (*a*) a bi-layer overhang structure, (*b*) a SiO_2 sputter-deposited bi-layer overhang structure, and (*c*) a lift-off processed feature.



(*a*) (*b*) (*c*)

Figure 3. FESEM image of lift-off processed features with different feature size (D) and designed pattern size (D_p): (*a*) $D/D_p = 16\ \mu m/20\ \mu m$, (*b*) $D/D_p = 10.5\ \mu m/15\ \mu m$, and (*c*) $D/D_p = 4.6\ \mu m/10\ \mu m$.

Since the decrease in electrode diameter is related to the undercut size, we have investigated the effect of the develop time on the bi-layer LOR processed electrode feature. As can be seen in figure S1 (available from stacks.iop.org/JMM/23/097001/mmedia), the diameter of the active electrode decreased with respect to the develop time. When the developing time is shorter than 3 min 45 s, the electrode is surrounded by a dielectric wall which is irregular in shape and not controllable. But, the electrode can achieve clear round features when the developing time is over 3 min 45 s. Compromising the decrease in electrode diameter and reproducibility, we have determined 4 min as the optimal develop time.

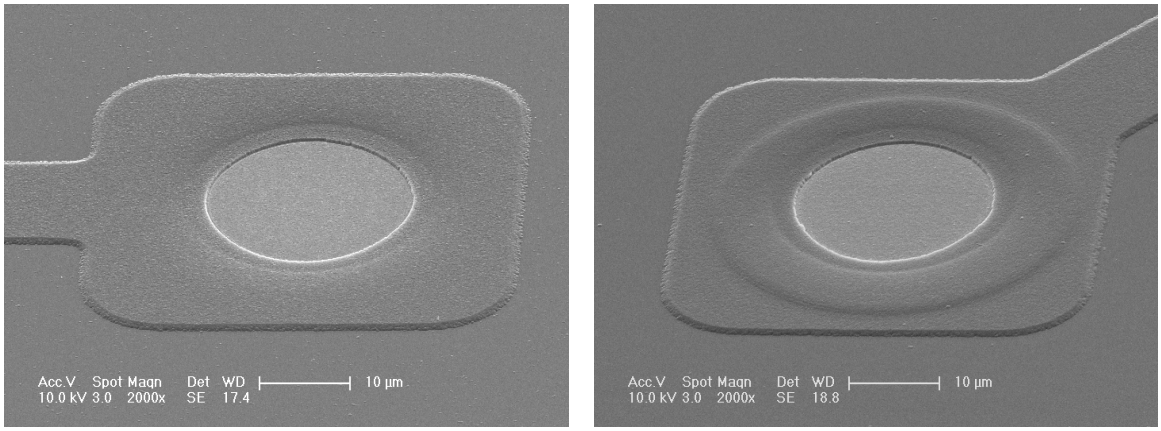
Normally, the substrate temperature increases with respect to radio frequency (RF) sputtering power, due to the conversion of kinetic energy of plasma to heat. For example, it has been reported that the silicon wafer temperature increases slightly above 150 °C without forced heating or cooling, for RF power of 150 W at a 5 mTorr working pressure, with a target-to-substrate distance of 45 mm (Bhatt and Chandra 2007). When forced cooling was not performed, as shown in figure S2(*a*) (available from stacks.iop.org/JMM/23/097001/mmedia), traces of LOR remained on the electrode surface even after the twice LOR stripping processes, indicating that the substrate temperature may exceed the glass transition temperature of PMGI SF15 (approximately 190 °C). However, when forced cooling was applied, by supplying cooling water maintained at a temperature below 20 °C to the substrate holder, a clear electrode surface was obtained figure 2S(*b*) and (*c*) (available from stacks.iop.org/JMM/23/097001/mmedia).

In order to check the minimum feature size obtainable, we have applied variety of designed diameters ranged from 20 to 5 μm. As shown in figure 3, the minimum feature size obtained is approximately 4.6 μm when the designed diameter is 10 μm. In this study we have used 2 μm thick LOR as a lift-off bottom layer and 5 μm thick negative PR as a patterning top layer. The use of thinner LORs and negative PRs with vertical profile would result in a smaller minimum feature size.

3. Design and fabrication of a MEA with LOR sputter deposition of SiO_2

The electrode and pin layout was designed to fit a commercially available MEA 1060 amplifier (Multi Channel Systems). The MEA had dimensions of 50 mm × 50 mm × 0.7 mm. The electrode layout was an 8 × 8 configuration, with 59 active electrodes, 4 blank electrodes and a single ground electrode. Each electrode was designed to have a diameter of 30 μm, and the electrodes were separated 200 μm apart from each other.

Non-alkali glass (Eagle 2000 EXG) sputter-coated with a 300 ± 1.8 nm thick ITO layer, with a sheet resistance of 4.5 ± 0.27Ω/□, was supplied by AMG and used as a starting substrate. First the substrate was cleaned in cleaning solution (SC88-500, Fischer Scientific) with sonication for 10 min, and subsequently rinsed with de-ionized water, acetone and methanol, followed by drying with nitrogen gas. Standard photolithography and ITO wet etching were employed to fabricate ITO electrode arrays, pads, and interconnect lines connecting the electrodes and pads. After spin-coating of positive PR (AZ GXR 601 46CP, Clairant) the substrate was pre-baked on a hot plate at 100 °C for 70 s. The substrate was



(*a*) (*b*)

Figure 4. Representative FESEM image of the bi-layer LOR sputter deposition processed (*a*) ITO and (*b*) Au electrode.

then placed underneath the chromium photomask, and exposed to UV light for 4 s with an intensity of 45 mW cm^{-2} at 365 nm, using a mask aligner. Prior to developing, the exposed sample was post-exposure-baked on a hot plate at 110 °C for 70 s. The exposed PR was developed by using AZ 300 MIF for 45 s, followed by rinsing with running de-ionized water, and drying with nitrogen gas. Prior to etching, the sample was hard-baked on a hot plate at 120 °C for 10 min. ITO etching was performed by immersing the sample into ITO etchant (LCE-12, Cyantek) maintained at 30 °C, followed by rinsing with DIW, and drying with nitrogen gas. After etching, the remaining PR was stripped twice with acetone, under sonication for 10 min.

For the fabrication of Au MEA, the same bi-layer LOR process was applied, except that 0.7 μm thick LOR 7B (MicroChem) and 2 μm thick AZ nLOF 2020 (Clairant) was employed as a sacrificial bottom layer and as a patterning top layer, respectively. 20 nm thick Cr and 200 nm thick Au layer was subsequently deposited by thermal evaporation. Au lift-off was performed in Remover PG maintained at 60 °C with sonication for 30 min, followed by rinsing with DIW and drying with nitrogen gas. After ITO and gold patterning, the bi-layer LOR sputter deposition and lift-off process described in detail in previous section was applied.

Figure 4 shows typical FESEM images of the bi-layer LOR sputter deposition processed (*a*) ITO and (*b*) Au electrode, respectively. The images clearly show the round electrodes fabricated on the transparent ITO pad for active electrode. The round electrode and the ring pattern covered with SiO_2, as shown in figure 4(*b*), belong to the same Au layer. The distinct advantage of the bi-layer LOR sputter deposition is that it is not influenced by thickness uniformity of a dielectric layer. In case of RIE, it requires tighter film thickness uniformity, particularly when etch selectivity is poor. The disadvantage of the dielectric lift-off process is that the size of an opened electrode is smaller than that of the designed mask pattern size, however, we can compensate for the disadvantage, by reflecting the difference in designing the mask pattern. We were actually able to control the size of the electrode within 1 μm tolerance by controlling the temperature of a developer solution with 0.1 °C precision.

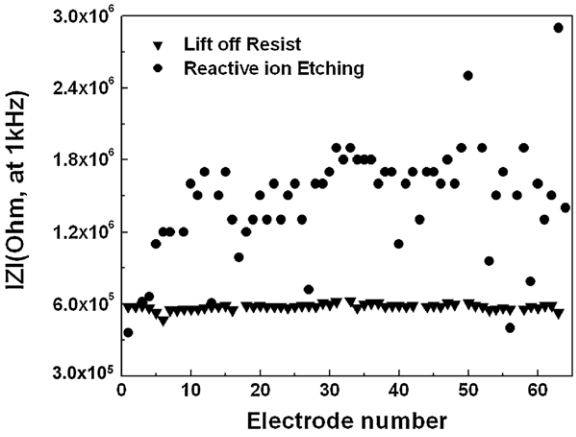
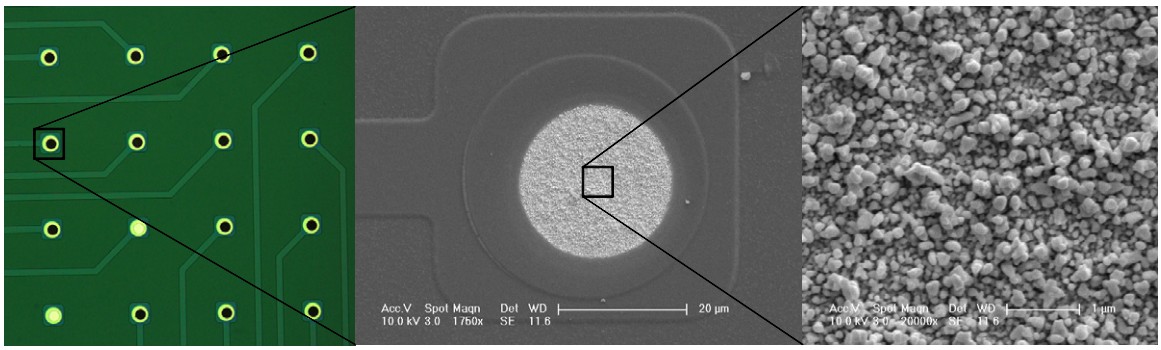


Figure 5. Electrical impedance of lift-off processed (▼) and RIE processed MEAs (●), according to the number of electrodes.

4. Impedance measurement and analysis

To check the uniformity of the electrode surface, electrochemical impedance spectroscopic (EIS) measurements were carried out using the ModuLab system (Solartron Analytical) with a three-electrode configuration: a fabricated MEA as a working electrode, a platinum plate as a counter electrode, and Ag/AgCl (sat'd KCl) as a reference electrode. The EIS measurements were carried out in the range between 100 kHz and 0.1 Hz in 0.1 M KCl solution containing 2.5 mM 1:1 $K_4Fe(CN)_6/K_3Fe(CN)_6$. The working electrode was connected to the analyzer using a home-built pin-block which can be connected to each 60 channel electrode through contact pads.

To compare the electrical impedance of both bi-layer lift-off and RIE processed MEAs, they were measured in the frequency domain over the range of 0.1 Hz–100 kHz. Figure 5 shows EIS results (at 1 kHz) from microelectrode sites of both bi-layer lift-off and RIE processed MEA. The impedance values for bi-layer lift-off processed electrodes are about 6×10^5 Ω (at 1 kHz) with excellent consistency over 60 electrodes. However, the impedance values for the RIE processed electrodes show broader values in the range



(*a*) (*b*) (*c*)

Figure 6. (*a*) Optical microscope image of Au NP-modified gold electrodes (an electrode was intentionally not modified for use as a reference), (*b*) FESEM image of an Au NP-modified gold electrode and (*c*) magnified FESEM image of Au NPs.

of 1×10^5–3×10^6. The consistency of the impedance value over electrode number supports that the bi-layer lift-off processed MEA can save effort in the systematic investigation of the surface modification in terms of impedance. The damage-free Au electrode should be useful in quantitative characterization of surface modification of MEA for enhancing neuronal adhesion in terms of impedance (Lin *et al* 2008) since impedance is sensitive to the surface area.

5. Electrochemical deposition of Au nanoparticles

To secure the passivation performance of the sputter-deposited SiO_2 layer, we have carried out electrochemical deposition of Au nanoparticles (NPs) on the Au electrodes. Electrochemical deposition of Au NPs on Au electrodes was carried out in a conventional three electrode system. The Au electrode of the MEA was employed as a working electrode. The counter and reference electrodes were platinum plate and Ag|AgCl in saturated KCl solution, respectively. Electrochemical deposition of Au NPs on an Au electrode was performed in 0.5 M H_2SO_4 solution containing 2 mM $HAuCl_4$ by potentiostatic method. An applied potential was at −0.5 V.

As shown in figures 6(*a*) and (*b*) Au NPs are electrochemically deposited and confined on the Au electrode area indicating that the sputter-deposited SiO_2 layer has a reasonable passivation performance. The Au NP-modified electrodes yield an impedance value of $2.1 \pm 0.2 \times 10^5\ \Omega$ (averaged for 14 electrodes shown in figure 6(*a*)), which is roughly four times lower than that of the Au electrode. The small deviation in impedance value with respect to the electrode may reflect the rather uniform surface area of the Au NP-modified electrodes, demonstrating the application potential of sputter deposition bi-layer LOR fabricated MEAs as a platform for surface modifications.

6. Primary neuronal cell culture and neuronal signal recording

To evaluate the neuronal signal recording performance of the sputter deposition bi-layer lift-off processed MEAs, we have performed recording of signals from primarily cultured neuronal cells. Prior to culture, a glass ring (internal diameter 21 mm, height 5 mm) was positioned at the center of the MEA, and glued with Sylgard 184 (Dow Corning). The MEA was exposed to oxygen plasma at 30 W RF power for 5 min, followed by overnight immersion into a 0.1 g L^{-1} poly-D-lysine (PDL) phosphate buffer solution (pH 8.0) at 4 °C. After PDL coating, the surface was rinsed with running DIW, and washed with 0.01 M tris buffer at pH 7.5 and 0.1 M NaCl. Finally, the surface was once again rinsed thoroughly with running DIW.

Primary neuronal cell cultures were done with explants from the embryonic day 17 Sprague–Dawley rat, and the detailed procedures are described in our previous report (Baek *et al* 2011). The neuronal activities were recorded using a MEA 1060 (Multi Channel System) controlled through MC Rack software. Signals were sampled at 20 kHz with 1200 amplification and bandwidth of 10–3000 Hz.

Figure 7 shows the spike signals recorded using the fabricated (*a*) ITO, (*b*) Au, and (*c*) Au NP-modified MEA, respectively; proving that the bi-layer LOR sputter deposition processed MEAs can record neuronal activity at a single unit level. In this study signals were analyzed in terms of noise level V_{rms} which is defined $V_{\mathrm{rms}} = (\Sigma y_k/\mathrm{K})^{\frac{1}{2}}$, where y_k ($k = 1{\sim}\mathrm{K}$) is sampled from the $K = 3000$ (∼1.5 s) period in the signal. The ITO MEA exhibited a noise level of ∼14.8 μV_{rms}, which is slightly larger than that of Au MEA (∼12 μV_{rms}), and is attributed to the increased interface resistance due to the PDL layer and contact resistance between ITO and pin probe. However, ITO MEA is advantageous in that the detailed neuronal network structure can be observed even through the recording electrode, making it suitable for optical recording and imaging purposes. As shown in figure 6(*c*), Au NP-modified MEA shows the lowest noise level (∼7.1 μV_{rms}), even though it is not yet optimized, among the MEAs fabricated in this study. The reduced electrical impedance of an electrode would enable us to achieve higher signal-to-noise ratio values, thus long-term recording, since the noise level is proportional to the electrical impedance. We are optimizing the conditions for electro-deposition of Au NPs in terms of impedance, and will report the results elsewhere.

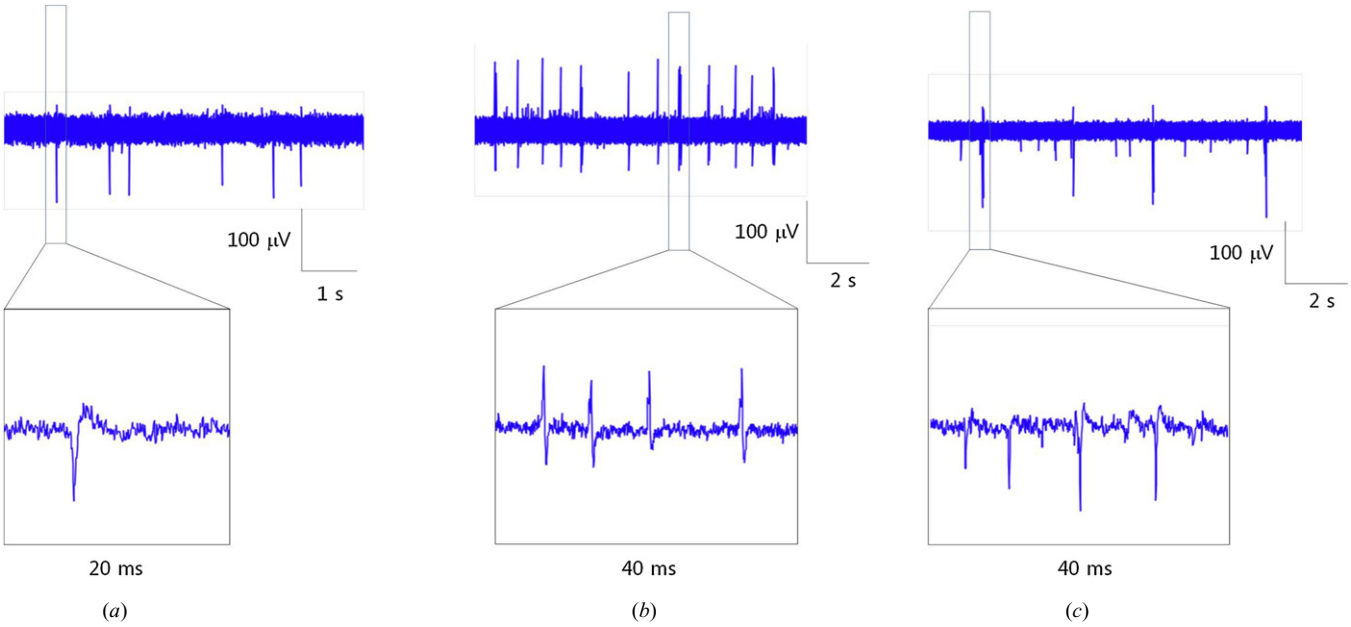


Figure 7. Neuronal activities recorded using the bi-layer LOR processed (*a*) ITO, (*b*) Au, and (*c*) Au NP-modified MEA. The signals were filtered using digital filtering and shown with a magnified time scale.

7. Conclusions

We have challenged the lift-off of sputter-deposited SiO_2 by applying the bi-layer LOR technique, to achieve the damage-free passivation of a microelectrode. Using the 2 μm thick photo-insensitive LOR as a sacrificial bottom layer and the 5 μm thick negative PR as a patterning top layer and performing low-temperature sputter deposition of SiO_2 followed by lift-off, we could successfully fabricate damage-free ITO and Au MEAs. We have also demonstrated the minimum feature size of 4.6 μm using the same bi-layer LOR condition. The detailed shape of microelectrode and fabrication reproducibility was found to be critically influenced by the undercut length, which is defined by develop time, and forced cooling of the substrate during sputter deposition. The bi-layer LOR sputter deposition processed Au MEA showed an impedance value of 6×10^5 Ω (at 1 kHz), with good consistency over 60 electrodes. Passivation performance of the bi-layer LOR sputter-deposited SiO_2 was tested by electrodepositing Au NPs on the Au electrode, resulting in the well-confined and uniformly coated Au NPs. The bi-layer LOR sputter deposition processed ITO, Au, and Au NP-modified MEAs were evaluated to have a neuronal spike recording capability, confirming the validity of the bi-layer LOR sputter deposition as an effective passivation technique for the fabrication of MEA.

The bi-layer LOR sputter deposition is not limited to SiO_2 but can be extended other dielectrics such as silicon nitride and metal oxides, and also expandable to the passivation of titanium nitride (Egert *et al* 1998) and iridium oxide that are currently used as an electrode material for MEAs. Furthermore we may extend this technique to a variety of substrate materials, such as silicon wafers used in fabrication of implantable neural electrodes, since there are no technical hurdles.

Acknowledgments

This study was supported by the Happy Tech. Program and Global Research Laboratory Program through the National Research Foundation of Korea funded by the Ministry of Education, Science and Technology.

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